

DS90UB953/954 I2S Evaluation

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1 Introduction

Texas Instruments (TI) is a world leader in supplying automotive and industrial video distribution solutions. TI's FPD-Link technology is used extensively in the automotive industry, providing for the transfer of video, audio, and other signaling over a simple serialized interface.

The DS90UB953-Q1 serializer represents the next generation in FPD-Link III serializers and is designed to support high-speed raw data sensors including 2MP imagers at 60-fps and as well as 4MP, 30-fps cameras, satellite RADAR, LIDAR, and Time-of-Flight (ToF) sensors. The chip delivers a 4.16-Gbps forward channel and an ultra-low latency, 50-Mbps bidirectional control channel and supports power over a single coax (PoC) or STP cable. The DS90UB953-Q1 features advanced data protection and diagnostic features to support ADAS and autonomous driving. Together with a companion deserializer such as the DS90UB954-Q1 (single port) or DS90UB960-Q1 (multi-port), the DS90UB953-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

While similar to prior generations of FPD-Link devices in providing the aggregation of several interfaces common to camera systems (e.g., I2C, GPIO, other) over a single link; the DS90UB953 family does diverge in some areas, particularly the direct support for the commonly used I2S audio format. This divergence was intentional; and a result of the nature of I2S (constantly running clock) not necessarily meshing well with that of the CSI-2 video interface the DS90UB953 includes.

However, the DS90UB953 (and receiving DS90UB954/960) device(s) can reliably support I2S signaling within some nominal bounds; thereby enabling real-time transmission of audio while concurrently supporting video and I2C interfaces. It should be noted that none of the limits or specifications defined in this document supersede nor contradict any of the specifications documented in the device datasheet, and that document still serves as the final authority on device operations. The following document simply outlines the 'box' for support of I2S using the DS90UB953 device and was developed and tested on actual hardware to prove out functionality.

2 I2S Overview

The I2S standard is used extensively in the digital audio world; and provides a simple interface for serialized audio data. It minimally consists of three digital lines, comprised of a serial clock, a data line of two channels, and a word clock that selects between the two channels. In the simplest implementation, the digital interface looks like the following.

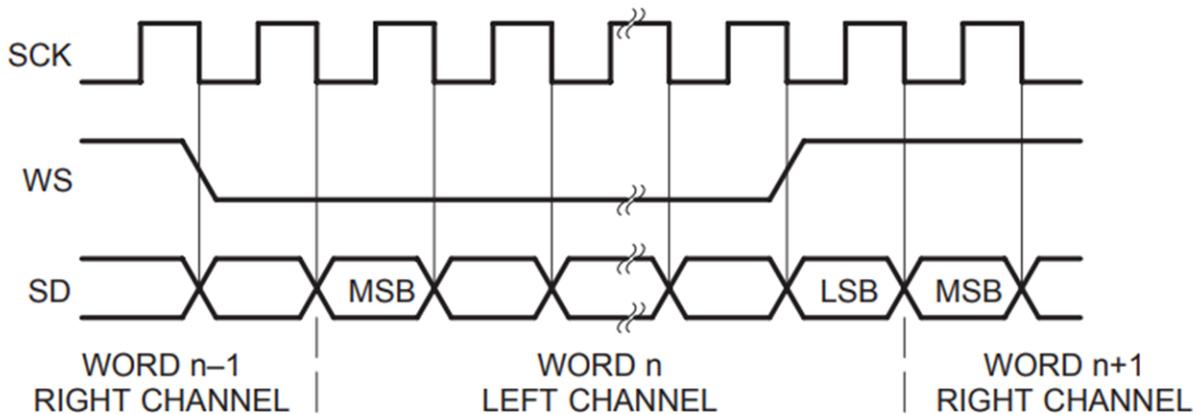


Figure 1. I2S Timing

Because the transmitter and receiver have the same clock signal for data transmission, one of the two sides of the interface must generate the SCK and WS signals while the other side accepts these as inputs. The generating side is referred to as the master; and the other side is referred to as the slave. Note however that this designation is independent of the SD data direction. That is, a master may be a receiver or a transmitter of serialized data; likewise a slave may assume the same positions as well. This is one of the things that makes the I2S format so popular, but can also lead to confusion.

2.1 I2S System Architecture

There are many manufacturers of integrated circuits (ICs) that have adopted the I2S format; and over time, some of the signals have modified names; however the underlying signaling has remained the same. In this document, the WS signal shown in Figure 1 shall be referred to as the LRCLK, which is commonly used in the industry to more accurately define this signal as the L (left, when low) R (right, when high) channel select. The SD line is identified as SDATAIN or SDATAOUT in this document to more accurately define the direction of the signal relative to the IC being discussed. By way of example, consider a typical I2S system as shown in Figure 2.

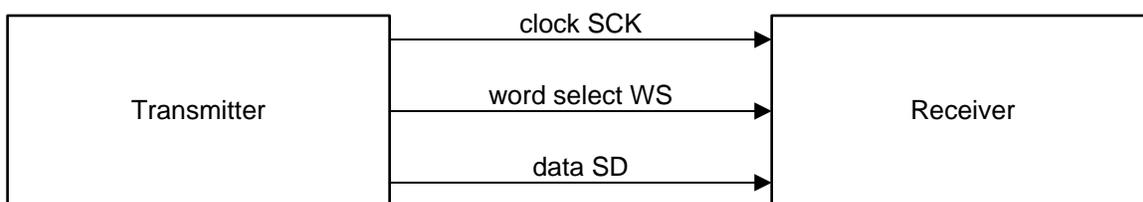


Figure 2. I2S System

For this document, the same system would be defined as Figure 3.

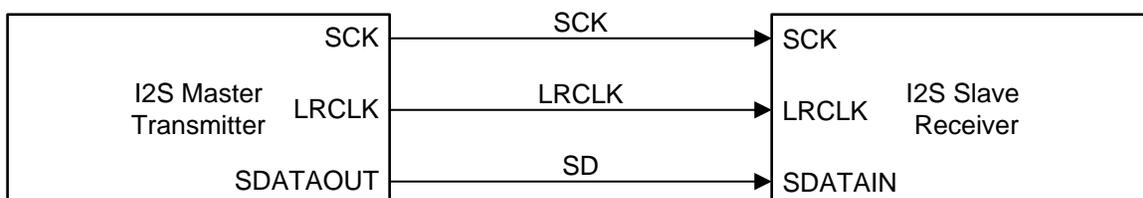


Figure 3. I2S System - Refined

The I2S interface itself is comprised only of the [Figure 3](#) signals, however, the reader should be aware that often several other ‘sideband’ signals are sometimes present in digital audio interfaces. A master clock is often provided, which is normally a high speed multiple of the WS (usually 256x to 512x); which allows lower jitter synchronization of the two ends of the interface. The signal is not required as the serialized data and clock are sufficient to extract the audio stream; however can be useful for synchronizing streams from multiple devices at the receiving end. Optionally, a second SD line in the opposite direction to facilitate bidirectional audio is often provided (e.g. a codec IC has both audio outputs; line or speaker, and inputs; line or microphone). And then to further complicate things, some ICs have multiple SD lines in possibly both directions to facilitate greater number of audio channels that share the same clocking. For example, 8 channels of audio can be serviced by 4 SD lines; as each SD line supports left and right time multiplexed data.

Due to the flexibility of the I2S interface and the optional signals that may also exist, [Figure 2](#) and [Figure 3](#) represent only one possible system implementation. Because of the nature of the application space where the DS90UB953/954/960 are applicable; it will be the architecture largely discussed here.

2.2 Remote Camera Application

The DS90UB953 is ideally suited for a remote camera application; wherein an image sensor, local control or possibly even minimal processing exists on one end of the data link; while more elaborate processing, storage, and possibly aggregation of multiple channels of similarly formatted data exists on the other end. In such systems, while audio could exist in both directions, the most common applications will involve audio being sourced from the camera (e.g., an integrated camera plus microphone); and such a system is discussed in this paper. While the addition of audio in the opposite direction is not precluded, there are certain limitations relative to FPD-Link channel bandwidth that may limit the usefulness of such an implementation. These will be discussed shortly in this document; but for the purposes of this discussion, the following system architecture was evaluated.

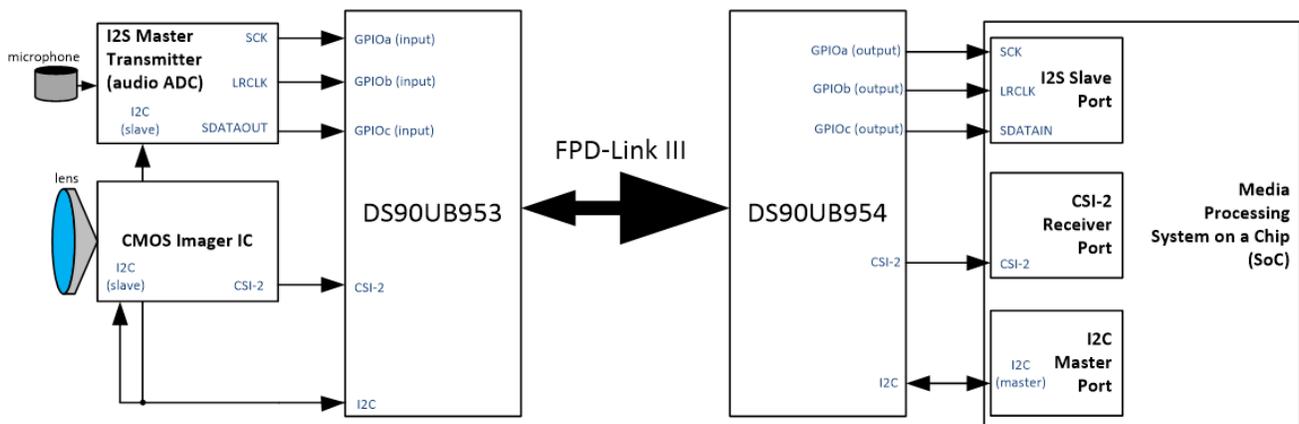


Figure 4. Remote Camera System

[Figure 4](#) illustrates two key elements of the I2S interface, which quickly help to define the ‘box’ in which I2S can be supported in such a system. However, to fully understand the nature of the system, it is necessary to first understand a few key elements of the FPD-Link III interface.

2.3 FPD-Link III Channels

FPD-Link III by nature is comprised of a set of high-speed serializers and deserializer. Note that both are required to facilitate bi-directional communication, as is required for interfaces such as I2C; plus some other synchronization features that devices such as the DS90UB953 can support. Data that is in the same direction as the video data, that is, from DS90UB953 to DS90UB954, is termed the forward channel; while data in the opposite direction, from the DS90UB954 to DS90UB953 is termed the back-channel. Because the primary function of the FPD-Link interface is the described topology is to transport video data; ancillary

forward and back-channel bandwidth is allocated highly asymmetrically. That is, forward channel data has significantly higher bandwidth than back-channel data. Note that in the most common systems, this is perfectly fine, as GPIO and I2C data is significantly lower bandwidth than the video data. As we consider the I2S interface however, it is important to understand these limits, because ultimately these will dictate what variances of the interface can be supported.

2.3.1 DS90UB95x GPIOs

The DS90UB953/DS90UB954 each support 4 generic GPIO signals; each of which may be designated as either an input or an output, which inherently allocates them to either the aforementioned forward or back-channel. That is, an input to the DS90UB953 would map to an output of the DS90UB954, and this would then require bandwidth on the FPD-Link III forward channel; because this direction is in the same direction as the video data. Likewise an output of the DS90UB953 would be input from the DS90UB954; and would require back-channel bandwidth. To support I2S audio; the DS90UB953/954 GPIO signals are used and the bandwidths for each signals must be evaluated.

Per the device datasheet, forward channel GPIO timing looks like [Table 1](#).

Table 1. DS90UB95x GPIO Forward Channel Timing

Number of Linked Forward Channel GPIOs	Sampling Frequency (MHz) at FPD-Link III Rate = 4Gbps	Maximum Recommended Forward Channel GPIO Frequency (MHz)	Typical Jitter (ns)
1	100	25	12
2	50	12.5	24
4	20	5	60

Reverse channel GPIO timing has one additional complication in that the DS90UB953 supports two different clocking modes. Normally, the forward channel and more specifically the video channel is clocked at a higher speed than the video data rate; which is recovered from the FPD-Link III bidirectional control channel. This is the most common configuration, because it allows the camera end, e.g. the DS90UB953, to operate without a local oscillator, and is called Synchronous Mode. If however a local oscillator is used with the DS90UB953, then it must be synchronized to the FPD-Link III serializers ultimately, and as a result the back-channel data rate is further reduced. This is termed non-synchronous CLK-IN mode, and its effect on the back-channel data rate is shown in [Table 2](#).

Table 2. DS90UB95x GPIO Forward Channel Timing

DS90UB953 Clocking Mode	Back Channel Rate (Mbps)	GPIO Sampling Frequency (kHz)	Maximum Recommended Back Channel GPIO Frequency (kHz)	Typical Latency (us)	Typical Jitter (us)
Synchronous Mode	50	1670	416	0.750	0.6
Non-Synchronous CLK_IN Mode	10	334	83.5	3.2	3

[Table 1](#) and [Table 2](#) show the forward channel GPIOs have significantly higher bandwidth and less jitter than the back channel GPIOs. Because of this, when transporting I2S audio, the designer must carefully consider the system requirements. In the block diagram shown in [Figure 4](#), note that the 3 GPIOs chosen have all been allocated to the forward channel, and this is generally the most useful configuration to consider. This generically implies that from an I2S perspective, the master will be on the camera side, and the I2S slave will be on the receiving side. It is worth noting that while this is not absolutely necessary; for the I2S sides to be flipped would natively limit the fastest signal, the I2S SCK, to the back-channel limit of 416kHz. When this is further divided by 2 channels of audio data and a minimum sample size of say 16 bits; a resulting 13kHz sample rate for the audio data more or less limits the designer to voice-only quality (8KSPS nominally). However, this is certainly supportable.

2.4 I2S Data Rates Supported

In the more common case as shown in the system block diagram on [Figure 4](#) however, we have far more options. In addition to the significant bandwidth offered by the forward channel, its exceptionally low jitter lends itself well to a synchronous interface such as I2S. Note that in the I2S protocol, data is launched from the falling edge of the SCK, with the intended sampling of the signal on the rising edge of SCK by the receiving end. This inherently provides $\frac{1}{2}$ clock cycle of setup and hold times. SCK rates of 2-3MHz for example provide such times of 100ns or more; which is well in excess of any modern IC setup/hold time requirement. As such, even the small amounts of jitter and latency introduced by the FPD-Link III interface have any effect on the robustness of an I2S interface. By way of paper design, one could easily surmise that an SCK rate of up to 5MHz can be supported, and as such the SD and LRCLK lines are by definition slower and thus easily supported. Digital audio is generally constrained to some more typical sample rates; as an example CD-quality audio is typically 44.1KHz sampling rate. So to look at the resulting 'box' of supportable I2S rates in the architecture of [Figure 4](#) one would expect the following.

Table 3. I2S Rates Supported

I2S Datum Size (bits)	Sample Rate (SPS)	Resulting SCK Rate (MHz)	Supportable?
16	32000	1.024	Yes
24	32000	1.536	Yes
32	32000	2.048	Yes
16	44100	1.411	Yes
24	44100	2.116	Yes
32	44100	2.822	Yes
16	48000	1.536	Yes
24	48000	2.304	Yes
32	48000	3.072	Yes

Obviously there are other formats that could be supported; [Table 3](#) covers most of the foreseeable space that the DS90UB953 device would be targeted for use.

3 IS2 Test Platform

As a means of verifying the supportable I2S rates outline in [Table 3](#), the author constructed a test platform as shown in [Figure 5](#).

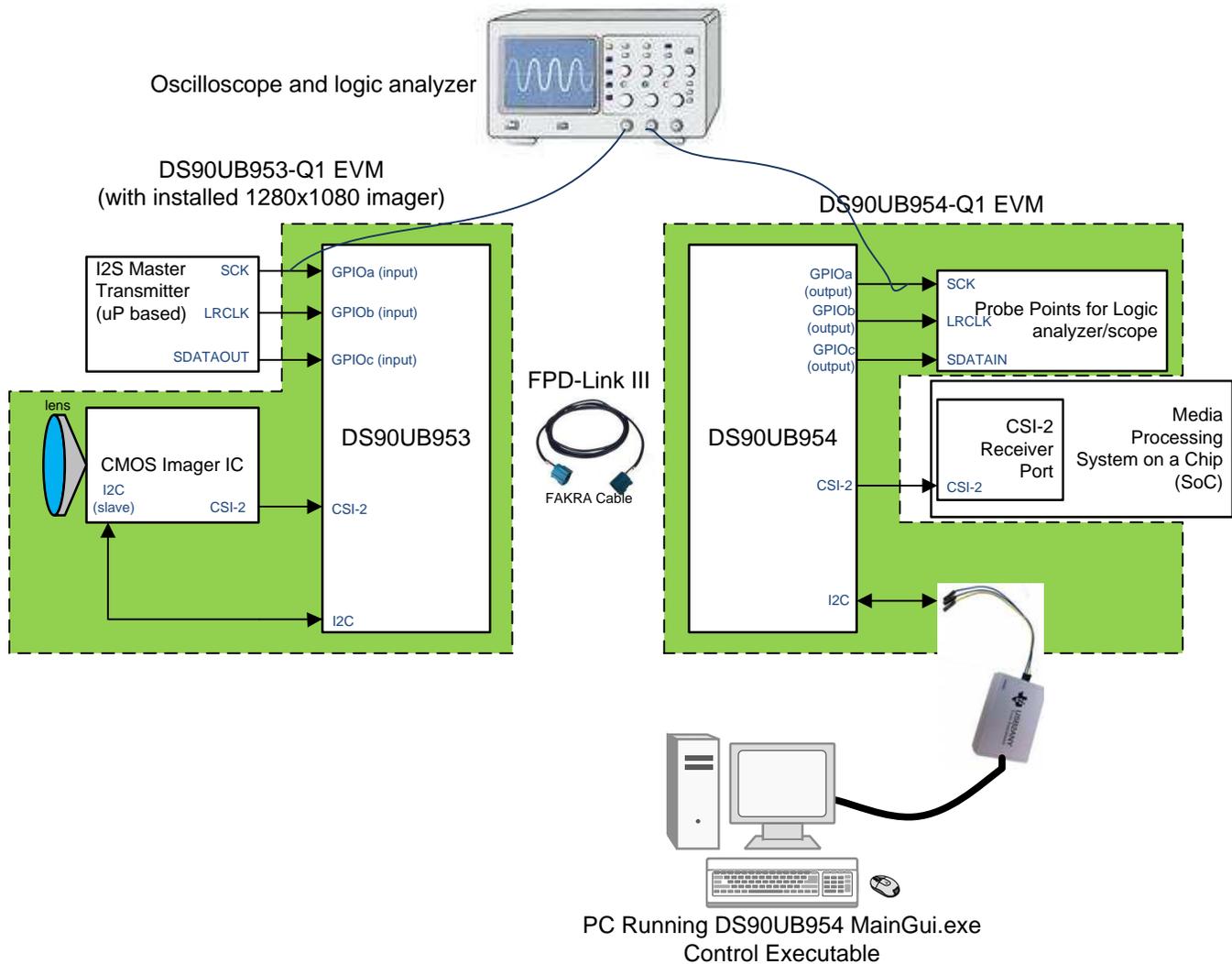


Figure 5. I2S Test Platform

The setup shown in [Figure 5](#) lends itself to several key flexibilities. First, all control of the FPD-Link system is handled directly by the DS90UB954 EVM GUI tool as described in the DS90UB954-Q1 EVM User’s Guide. Emulation of the I2S master with a small microprocessor allowed the data rates and formats to be quickly changed and debugged. The oscilloscope and logic analyzer connections were taken directly from test points on the associated EVMs, which allowed both fine grain timing measurements of jitter and latency; as well as long term stability tests wherein over 20 minutes of continuous data was captured and analyzed for bit errors.

3.1 Test Platform Modifications

There was a slight modification made to the default EVM setup. Key among these was the configuration of the data link. The CMOS imager that was available was a 1280x1080 imager running at 30 frames per second (fps). While this is actually very high resolution; the DS90UB953 device can accept even faster rates; up to 1920x1080 @ 60fps; or some 4MP imagers at 30fps. To accommodate this in the testing; the FPD-Link III rate was run at the maximum rate of 4.16Gbps; which is easily adjustable in the DS90UB954-Q1 EVM GUI. Additionally, the DS90UB953-Q1 is a 1.8V digital device; so level translation was applied using a small translator board.

Lastly, the EVM natively supports only two of the 3 required GPIOs to be easily accessible. This was addressed by removing the low-power capability of the imager for the purposes of conducting the test; which freed up an extra GPIO.

3.2 Test Results

While 32KSPS, 44KSPS, and 48KSPS were all tested; because of the nature of the GPIO usage to support the interface; only the 48KSPS was extensively measured for bit errors and jitter measurements, because all slower rates would be supported by nature of supporting 48KSPS. The following results were obtained.

3.2.1 Timing Validation

In Figure 6, Channels 1 and 2 are the sourcing I2S SCK and SD lines; Channels 3 and 4 show the received versions of these signals after transmission and reception over the FPD-Link III interface. There are a couple of features worth noting; firstly that on this particular capture; the sourcing side has provided 163ns of setup time (CH1-CH2 measurement) from the SCK to the SD line. This is basically the ideal for a 3.072MHz SCK. On the receive side; this is reduced to 149ns; which is due to the jitter introduced on the sampled GPIO signals across the link. Secondly, also note that while this 12ns reduction exists, the resulting 149ns is well in excess of the setup/hold times of any I2S interface; which are normally on the order of 10-20ns worst case.

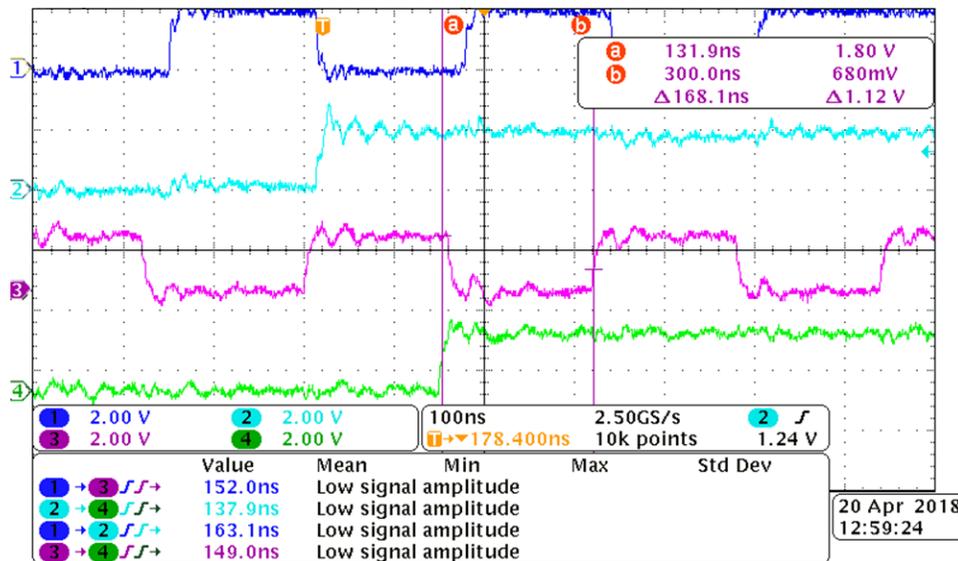


Figure 6. I2S Captured Timing (Raw)

To get an idea how this varies over time, the same plot was then taken using infinite persistence mode to establish a jitter minimum setup/hold time on the received signals. Notice again the setup times on the 1-2 and 3-4 pairs are still at the nominal levels; but the absolute delay on each signals (channel 1-3 delay and channel 2-3 delay) is degraded by 9ns or so. This happens because as the input timing walks with respect to the DS90UB953-Q1 internal clock; GPIO inputs get sampled at later times with respect to the packetization process, and in some cases ‘just miss’ the window and have to wait for the next FPD-Link III available packet. This is normal; but as can be seen, makes no difference to the overall setup/hold times received over the link.

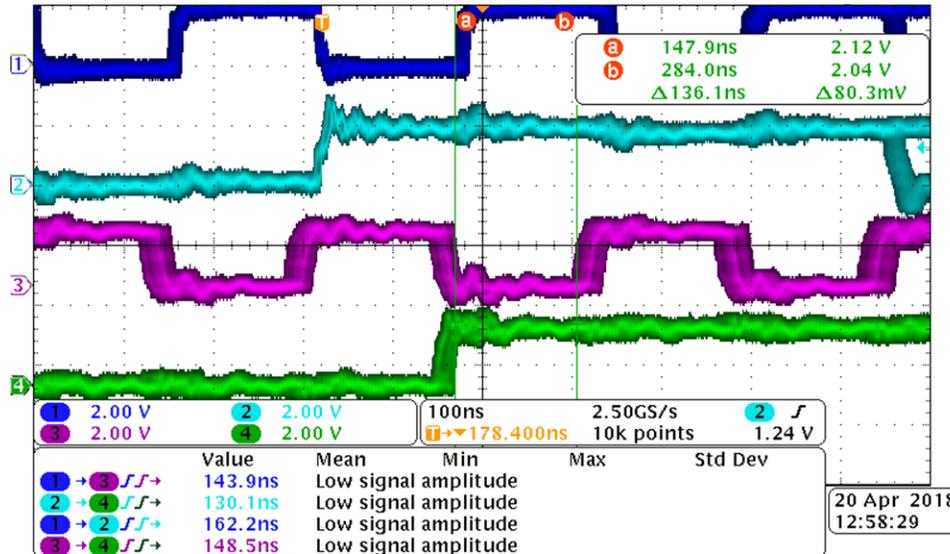


Figure 7. I2S Timing Captured (Infinite Persistence)

3.2.2 Data Verification

To establish the robustness of the link, data verification was additionally performed. This test was run in a temperature chamber with the temperature varying from -20 °C to 85°C; with the note that the DS90UB953/954 are in fact rated for -40 – 105 °C operation. The lower limit was imposed by the temperature chamber itself; the upper limit was imposed because the test fixture, chiefly the I2S source and the USB2ANY adapter for controlling the DS90UB954-Q1 EVM were not rated for temperatures past 85 °C.

The test was run with 10 minute ‘wells’ at each temperature as the temperature was stepped in 10 °C increments with a ramp rate of approximately 5 °C/minute. That is to say, each step accommodated approximately 8 minutes of soak, and then 2 minutes of update to the new temperature; this was mostly a function of the chamber controls. Data was generated randomly and captured and decoded on both ends using a logic analyzer. The results were then exported to a file for comparison and any bit error would be flagged.

As shown in Table 4, no bit errors were observed across this test.

Table 4. Bit Error Test Results

Time (s)	Temperature °C	# Bit Errors
0	-19.8	0
480	-19.7	0
600	-10.2	0
1080	-9.9	0
1200	-0.1	0
1680	0	0
1800	9.9	0

Table 4. Bit Error Test Results (continued)

Time (s)	Temperature °C	# Bit Errors
2280	10.1	0
2400	19.9	0
2880	20	0
3000	30	0
3480	30.1	0
3600	39.9	0
4080	40	0
4200	50	0
4680	50.1	0
4800	59.9	0
5280	60	0
5400	69.9	0
5880	70	0
6000	80	0
6480	80.1	0
6600	85	0
7080	85.1	0
EndOfTest	Total Errors	0

4 Summary

In summary, the DS90UB953-Q1 is an excellent device for creating a remote camera interface. Audio can be supported using I2S; and across a wide range of use cases that meet the following criteria.

- Sourcing I2S device on DS90UB953-Q1 is the master of the I2S interface (e.g. drives SCK, LRCLK, and SD)
- SD bit rate is less than 5MHz

Alternative solutions for DS90UB953-Q1 side slave audio can be supported for voice-only quality within the device back-channel bandwidth limits (nominally 2 channels, 16bits/channel, 8KSPS).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2019) to A Revision	Page
• Added units throughout document.	1

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