CLC018,LMH0001,LMH0002,LMH0024,LMH0026, LMH0034,LMH0036,LMH0040,LMH0044,LMH0046, LMH0051,LMH0056,LMH0070,LMH0071,LMH0074, LMH0202,LMH0302,LMH0303,LMH0307,LMH0340, LMH0341,LMH0344,LMH0346,LMH0356,LMH0384, LMH0387,LMH0394,LMH0395,LMH1981,LMH1982, LMH1983

Broadcast Video Owner's Manual

Broadcast Video Owner's Manual

1st Edition, Spring 2004

National Semiconductor, The Premier Analog Company

National Semiconductor
The Sight & Sound of Information

Broadcast Video Owner's Manual

Spring 2004
1st Edition

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Semiconductor
The Sight & Sound of Information

National Semiconductor's SDV Group

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1.1 Introduction

The production of television and film has been transformed through the use of digital production techniques. Improvements in digital imaging have spurred worldwide adoption of digital video transmission and processing. Many advantages accompany this change: lossless archiving and transmission, improved editing and special effects, greater picture definition, improved audio processing and quality, to mention but a few.

The digital transition has not been without accompanying problems for the TV system and equipment design engineer. The new digital signal realm that he or she must contend with extends into portions of the electro-magnetic spectrum considered as microwave but a few years ago. And the semiconductor devices that process these signals present a new array of design problems and challenges.

National Semiconductor's Broadcast Video Owner's Manual addresses components and their application in digital video circuits and systems. It is intended as a guide to best practices and proven design techniques that will assist the video engineer in the design task. Many areas are covered including: signals and data coding, mechanical and electrical components, power supply systems, signal transmission systems, testing and device-specific issues. Also included are guides to other resources that will assist and inform the designer.

1.2 Standards organizations

The specific requirements for digital television video are administered by several standards organizations:

The Society of Motion Picture and Television Engineers (SMPTE) is the worldwide standards body for television and film production. Its standards, engineering guidelines and recommended practices address almost every aspect of signals, and data used in digital video.

The International Telecommunications Union (ITU) is the standards body for Europe and much of the world other than the United States. Its standards embody or parallel those of SMPTE.

The Digital Video Broadcast Consortium (DVB) is the standards body for European satellite and terrestrial broadcasting of video and other data that may contain compressed video originating as one of the above standards.

A list of relevant standards is provided in the bibliography.

1.3 Digital video signals

Digital video data signals may be transmitted and processed in parallel or serial format. Parallel data transmission formats are usually found inside equipment or between pieces of equipment where the transmission system length is relatively short, usually a few meters maximum, although certain standards allow links up to 50m. Transmission systems are usually differential between equipment. Cabling of these links is commonly multi-pair, shielded, or twisted pair. Single-ended transmission may be found within equipment and on printed circuit assemblies; however, differential transmission is also common, particularly for the higher data rates. Parallel format data coding is normally non-return to zero (NRZ). Data words may be 8- or 10-bits depending upon the originating equipment and overall data standard requirement. Parallel data is the form most convenient for manipulation such as editing, addition of other data or special effects.

Serial data transmission is the preferred method of signaling between equipment over longer distances, usually greater than 10m to about 300m. Transmission distance depends upon several factors such as data rate, type of cable and the receive system's capability to overcome or mitigate transmission system losses. Serial transmission is commonly single-ended using precision 75Ω coaxial cable for lowest signal loss.

Serial links using fiber optics and twisted pair are also found. The data signal format is polynomial encoded non-return to zero inverse (NRZI) and is polarity insensitive. Both the signal and its inverted polarity form represent the same data. Serial video data is transmitted in a continuous stream and is not packetized. The data is transmitted uncompressed within the television plant. This is termed "baseband data transmission."

1.4 Digital video data structures

Digital video data may originate as the digitized representation of analog video data or may be created directly from a digital data source such as computer-generated animation. In either case, the basic elements comprising the data are similar. Data derived from a video source, where all of the picture information including video and synchronizing signals is multiplexed in a single signal like NTSC, PAL or SECAM, is termed a composite digital video representation. Data from a source where the individual color components are represented by separate signals, like RGB or $YC_R'C_B'$, is termed a component digital video representation. When converted into digital representation, both have a common structure. The video signal is transmitted in the form of one luminance (Y) and two color-difference components, scaled versions of R_Y and B_Y.

Digital video data may be represented as either 8- or 10-bit words or samples. Composite video usually uses 8-bit representations and component 10-bit. Regardless, transport and processing involve similar processes. Since equipment exists that support both 8- and 10-bit representations, all synchronizing signals (EAV, SAV, and ANC) are detected by reference only to the eight most significant bits. The composite video signal is carried at the 4 fsc representation as prescribed in SMPTE 244M at 14.32 MHz. Sampling is also at four times the color subcarrier frequency.

The component video signal is transmitted at the 4:2:2 family level of ITU-R BT.601 (SMPTE 125M), with a nominal luminance sampling frequency of 13.5 MHz. The interface allows the transmission of appropriate ancillary signals that may be multiplexed into the data stream during video blanking intervals.

Introduction to broadcast video
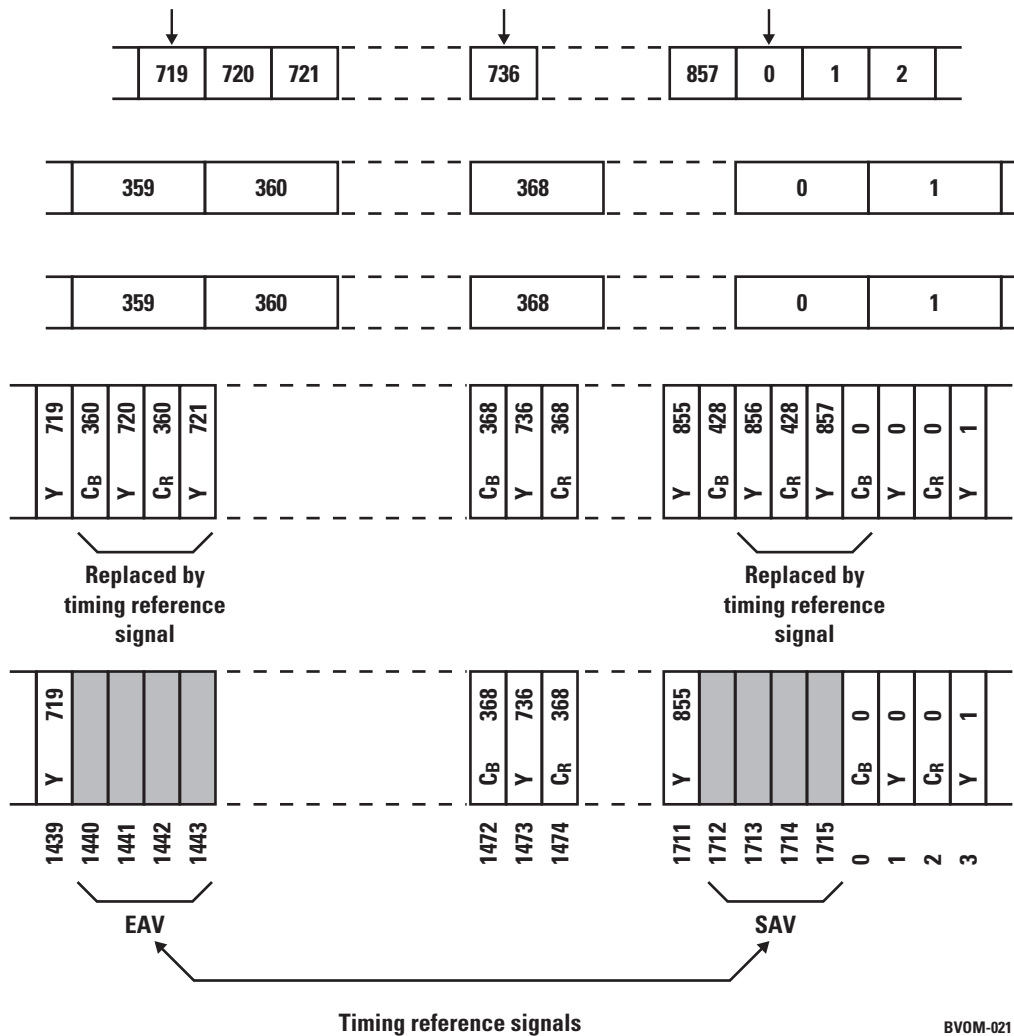
Figure 1.1. Example of multiplex data structure

Data originating from parallel sources may be manipulated easily and is the preferred format for editing, mixing and other special effects operations. The bits of the digital code words comprising the video signal are transmitted in a parallel arrangement using ten balanced conductor pairs. Each pair carries a multiplexed stream of bits of the same order or significance of each of the component signals. The bit-rate used in each pair for standard-definition formats may be 14.3 Mbps, 17.7 Mbps, 27 Mbps or 36 Mbps, depending on the particular picture format. An 11th conductor pair carries a clock signal at a frequency corresponding to the respective data rate in MHz. The signals may be transmitted point-to-point using balanced conductor pairs for a distance up to 50m without equalization and up to 300m with appropriate equalization.

However, transport of parallel data presents difficulties, especially over long distances, because of timing skew and other signal distorting conditions. Parameters of the signal format were selected to facilitate conversion to and from a serial digital interface format. When data is to be moved long distances, it is converted into serial representation. Data is converted from 8-bit to 10-bit representation before serialization.

1.4.1 Timing reference signals (TRS)

Synchronization words are inserted into the data to serve a similar function to the synchronizing pulses in analog video. In composite data there is only one TRS: the sequence 3FFh, 000h, 000h, 000h. The position in the line data corresponds to the leading edge of analog sync. In component data the TRS sequence is more informative of the type of data present in the line. The sequence is 3FFh, 000h, 000h, XYZh. The XYZh sequence is replaced by protection state bits identifying such things as the beginning and ending of line data, the field being transmitted and position of lines in certain places in the raster.

1.4.2 Serial data representation — standard-definition

Serial data is transmitted over single-ended coaxial interfaces at a data rate ten times that of the corresponding parallel data. Data is transmitted most significant bit (MSB) first. Both 4:2:2 component and 4 fsc composite sampled data may be converted to serial format. NTSC 525/60 and PAL 625/50 at both 4:3 and 16:9 raster aspect ratios can be handled by the existing standard-definition serial standard. The corresponding data rates are 270 Mbps (4:3 raster at 13.5 MHz sampling) and 360 Mbps (16:9 raster at 18 MHz sampling).
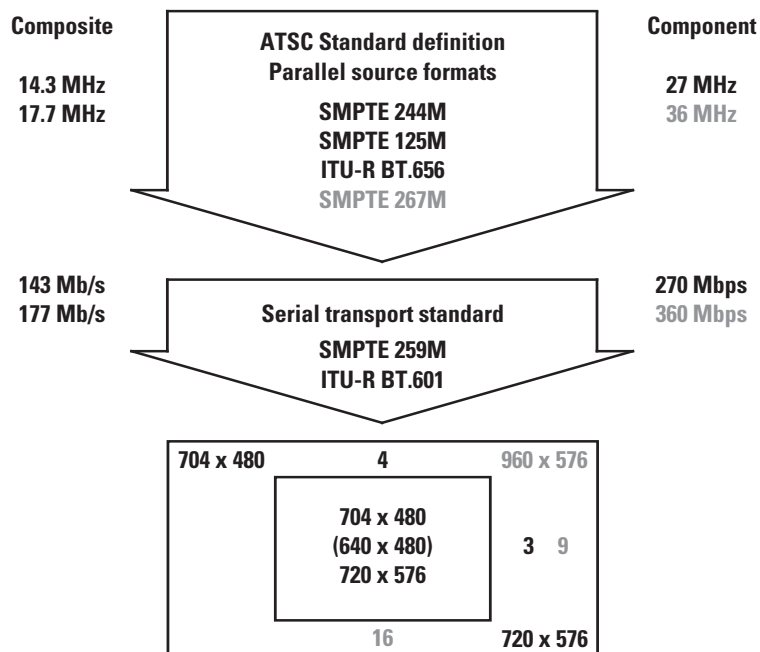
Figure 1.2. Relationship of SD parallel and serial formats to resulting raster

Serialization requires that the data be encoded using a polynomial scrambling technique which attempts to eliminate long runs of 1's or 0's in the resulting serial data and achieve better DC balance. The self-synchronized pseudo-random scrambling technique is used to improve the data transmission characteristics while maintaining the bandwidth. This technique is used in both standard- and high-definition data. After scrambling, the data is fed through a bi-stable which reduces the number of transitions and hence the effective frequency. The data is thus converted into NRZI representation. NRZI is similar to bi-phase mark or bi-phase space coding. This type of coding also makes the data polarity insensitive whereby both polarities represent the same data. This composite encoding is therefore given as G (x) = (x^9 + x^4 + 1) (x + 1). Naturally, the receiving system must perform the reverse operation in order to recover the unencoded data.

Introduction to broadcast video

1.4.3 Serial data representation — high-definition

Serial data in high-definition systems may be carried over either coaxial cable or fiber optic cable. The two principal serial data rates are 1.485 Gbps and 1.483 Gbps. These correspond to parallel data and sampling rates of 74.25 MHz and 74.176 MHz (74.25/1.001).

Component

74.25 MHz
74.176 MHz

**ATSC HDTV
Parallel source formats**

**SMPTE 274M
SMPTE 296M
ITU-R BT.709
SMPTE 260M**

1.485 Gbps
1.485 Gbps

Serial transport standard

**SMPTE 292M
ITU-R BT.1120**

**1920 x 1080
I & P**

**1280 x 720
P**

9

16

BVOM-002
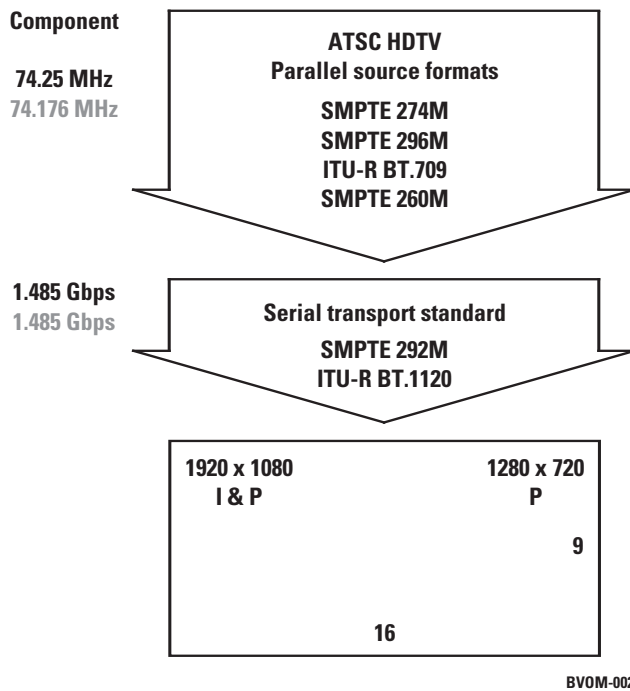
Figure 1.3. Relationship of HD parallel and serial formats to resulting raster

Encoding of SMPTE 292M data is similar to that of SMPTE 259M data in most respects. The main difference lies in the way in which the chrominance and luminance data are first interleaved from two or three simultaneous parallel, 10-bit data streams. The 20-bit system, where the color difference and luminance data are carried in separate 10-bit sample streams, is the most common interface. HDTV picture formats are also specified in both progressive scan (P) and interlaced (I) scan modes. All HD picture formats are 16:9 aspect ratio. HD data uses a line-by-line CRC method of reporting data errors. Individual video lines also include a line number after the EAV-TRS.

1.4.4 Pathological data sequences

Data encoding schemes used for serial data communication systems generally attempt to maximize the density of data transitions and equalize the numbers of 1's and 0's. Despite the attempt to avoid long periods without transitions in the serial data, the scrambling and encoding process is not perfect in accomplishing this. The algorithm fails about 0.2% of possible times. It has been found that certain repeated parallel data sequences will produce extended periods with reduced transitions in the serial data. When repeated over significant portions of a video line, the result can be extended repeating runs of intervals of up to 20-bit times without transition. These originating data sequences are called pathological or stressing data conditions. Pathological data conditions can also occur during the ancillary data portion of the line and the TRS but are not considered as stressing conditions. In standard-definition data this interval can extend for 44-bit intervals and in high-definition data, 59-bit intervals. These are sometimes referred to as "super-pathological conditions."

It should be appreciated that the special data sequences used to produce pathological data conditions do not usually originate from cameras or other natural image sources. The instances of these pathological data conditions in these sources are infrequent or short-termed. There is usually enough naturally occurring noise in the signal to prevent serious situations from occurring. Pathological conditions are more likely to occur with synthetic image sources such as matte generators or graphics generators.

Pathological conditions in the serial data can produce corruption of the video data when received and decoded. If the receiving system is not designed to cope with these conditions, poor picture quality can result from the lost or incorrectly decoded data. In particular, two main types of pathological conditions are to be guarded against:

- The conditions affecting the cable equalizer
- Those affecting the receiving system PLL and data recovery system

Pathological conditions in serial digital video systems are explained in SMPTE EG 34. Test data suitable for pathological testing is defined in SMPTE RP 178 for standard-definition and RP 198 for high-definition systems. Stressing the automatic cable equalizer is done with a data pattern having long sequences of 1's or 0's and infrequent single-bit transitions of the opposite polarity. The bit ratio is 19:1 and occurs for both data polarities. This stressing condition with very high (or low) duty cycle also tests whether the AC coupling network has sufficient low-frequency response. In cases where LF response is lacking, the baseline DC level of the data is shifted up or down. Pulse width distortion will occur which can prevent proper data recovery. High-definition standard SMPTE 292M specifies the maximum DC shift in a line period for coaxial systems. SMPTE 259M (standard-definition) does not specify this parameter.

The receiver PLL is stressed using a data sequence having maximum low-frequency content or maximum time between transitions. The bit ratio is 20:20 and occurs for both data polarities.

Pathological data conditions can be avoided in synthetic image generation and sources by adding a small amount of noise in the form of dithering to the least significant bit of the digital video words. The noise breaks up the repetitive nature of the data feeding the scrambler and thus the repeated output that results.

Introduction to broadcast video

1.5 Serial digital interface electrical parameters[1]

Table 1.1. Serial digital interface electrical properties

Parameter	SMPTE 259M	SMPTE 292M
Serial system impedance	75Ω	75Ω
Serial signal amplitude	800 mV ±10% p-p	800 mV ±10% p-p
DC offset	0.0 ±0.5V	0.0 ±0.5V
Rise/fall time, 20% to 80%	0.4 to 1.5 ns	<270 ps
Rise/fall time difference	0.5 ns	100 ps
Amplitude overshoot	10%	10%
Return loss at I/P or O/P connector, 5 MHz to clock	15 dB	15 dB

1.6 Serial digital interface mechanical parameters

Table 1.2. Serial digital interface connector properties

Serial connector	SMPTE 259M	SMPTE 292M
Type	BNC	BNC
Impedance	50Ω or 75Ω	50Ω or 75Ω
Return loss	Not specified	15 dB @ 1.5 GHz
Useable frequency range	850 MHz	2.4 GHz
Mechanical specification	IEC 60169-8 (IEC 169-8)	IEC 60169-8 (IEC 169-8)

[1]Quoted from SMPTE 125M-1995: Component video signal 4:2:2 – Bit-parallel digital interface

Chapter 2
System design elements

2.1 Power systems

2.1.1 Power and grounds

Most problems in controlling device-generated noise in Serial Digital Video (SDV) systems have their origins in the thinking pictured in Figure 2.1. More often than not, the power supply, and particularly the ground system, is given little attention, is left until last or simply forgotten until problems occur. The active devices are somehow magically powered from an ideal, unknown and invisible source. This is a sure recipe for trouble. The power supply system should be the most thought-about portion of the SDV system, even ahead of the analog or digital signal-carrying circuitry. A well-designed power and ground system prevents most other types of problems from happening and provides the best foundation for device and system performance from the prototype to the final product.
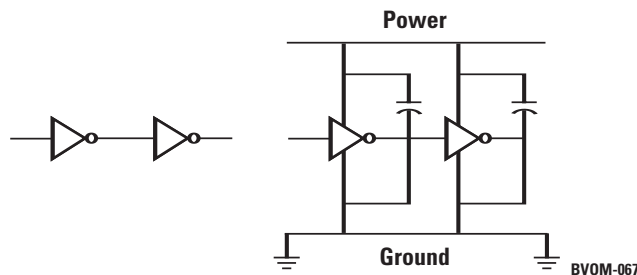
Figure 2.1. Keeping well grounded

2.1.1.1 Power system bypass recommendations

Digital video circuits process signals with a wide frequency range. The signal components include a substantial low-frequency component as well as the high-frequency components of single bits and fast edges. This means that bypassing needs to cover the entire frequency range from low kHz to upper GHz in most cases. To cover this range, both RF and LF bypass capacitors are needed.

- Each active device should have at least one RF bypass capacitor, more if the device power requirement is large, the device has many power and ground pins or the manufacturer recommends additional capacitors. Check the individual IC datasheets for the recommended bypassing.

- External bypass capacitors should include both RF ceramic and tantalum electrolytic types. All capacitors are not created equal. Insist on manufacturer's impedance and reliability data before incorporating them in your design.

- RF capacitor values may be in the range 0.01 µF to 0.1 µF. Choose the best size for the operating frequency or data rate being handled by the affected device or circuit. The value may be a compromise.

- Tantalum capacitors may be in the range 2.2 µF to 10 µF. The voltage rating for tantalum capacitors should be at least five to seven times the power supply voltage being used. This is needed to prevent destruction of the capacitors due to internal low-resistance heating effects.

- Use the capacitance of the power-ground system for extra RF bypassing by using thin dielectrics between the power and ground planes.

- Bypass power feed points on PCBs with RF and LF capacitors.

- Bypass on-card regulators following the device manufacturer's recommendations.

• All discrete bypassing is ineffective above 30 MHz to 50 MHz in power plane-based distribution systems. Above this frequency range, the intrinsic capacitance of the power-ground system can be used to provide additional RF bypassing.
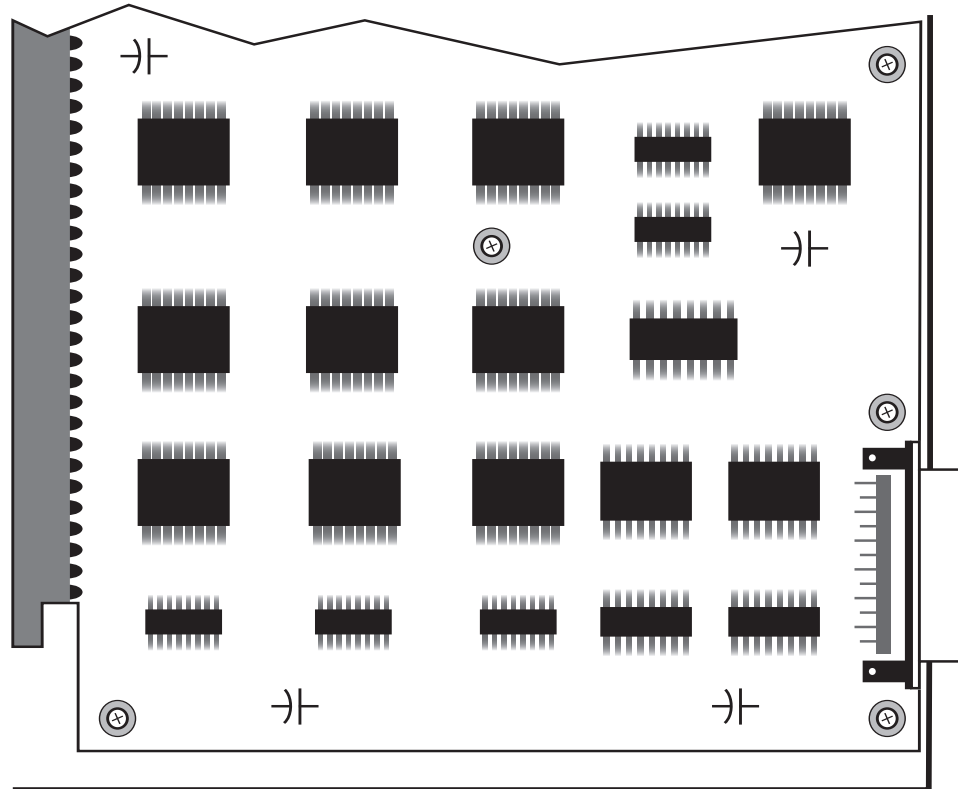
BVOM-003

Figure 2.2. Insufficient bypassing

System design elements

BVOM-004
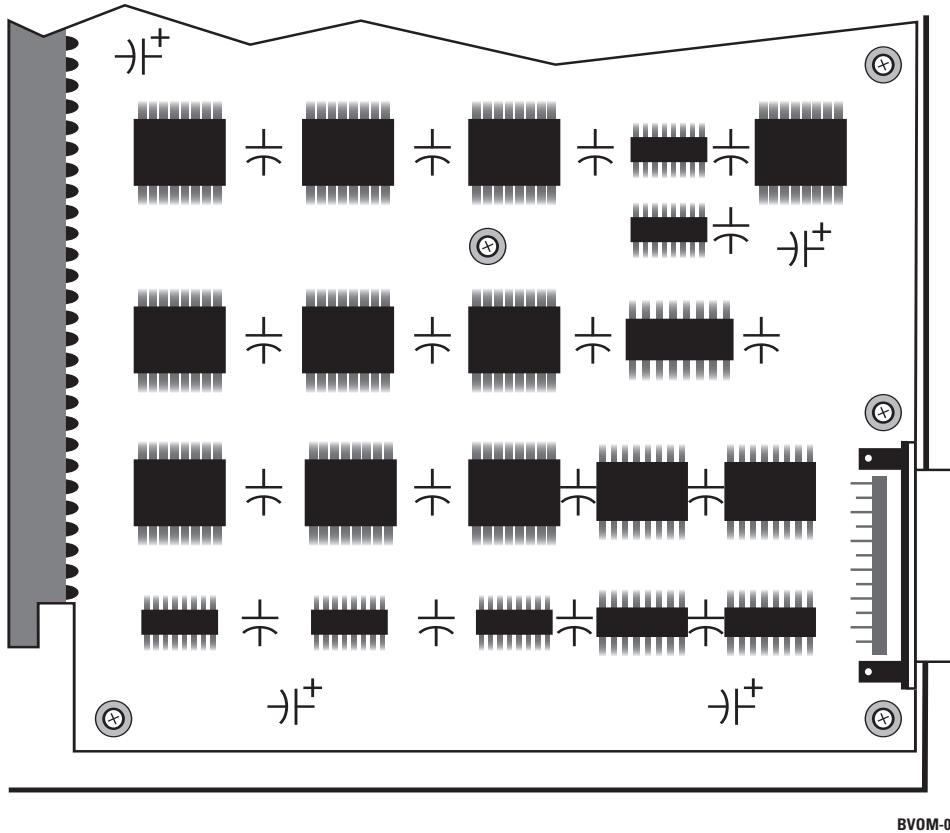
Figure 2.3. The result of adequate bypassing

2.1.2 PCB layout for serial digital video systems

2.1.2.1 Common PCB layout mistakes to avoid:

- Uncritical use of automatic placement and routing
- Poor functional or ergonomic board organization
- Poor or insufficient grounding
- Poor placement of bypassing components
- Unconnected connector shells or ground pins
- Improperly paired differential lines
- Poor network organization and routing
- Image grounds not extending under all traces

2.1.2.2 PCB organization and device grouping

Performance of different signal realms that coexist on a PCB benefits from good organization. Some engineers like to think of these organizations as "signal islands" whether or not they share a common power system. In some cases, isolation may be effectively used to control device-generated noise. Some general guidelines to organization by signal type are:

- Isolate or group analog and sensitive signals away from higher level or faster signals.

- Group similar fast, high-level logic signals such as ACMOS together.

- Group I/O circuits or bus-interface circuits according to functionality. Locate active devices near the I/O connectors with which they are associated. Usually these are located near card edges.

- Locate circuits with higher current demands near power-feed points or the on-card regulators serving them.

- Avoid narrow cards that force large concentrations of connectors and signals along the short edge.

Bus driver island

Digital circuit

Analog island

I/O island
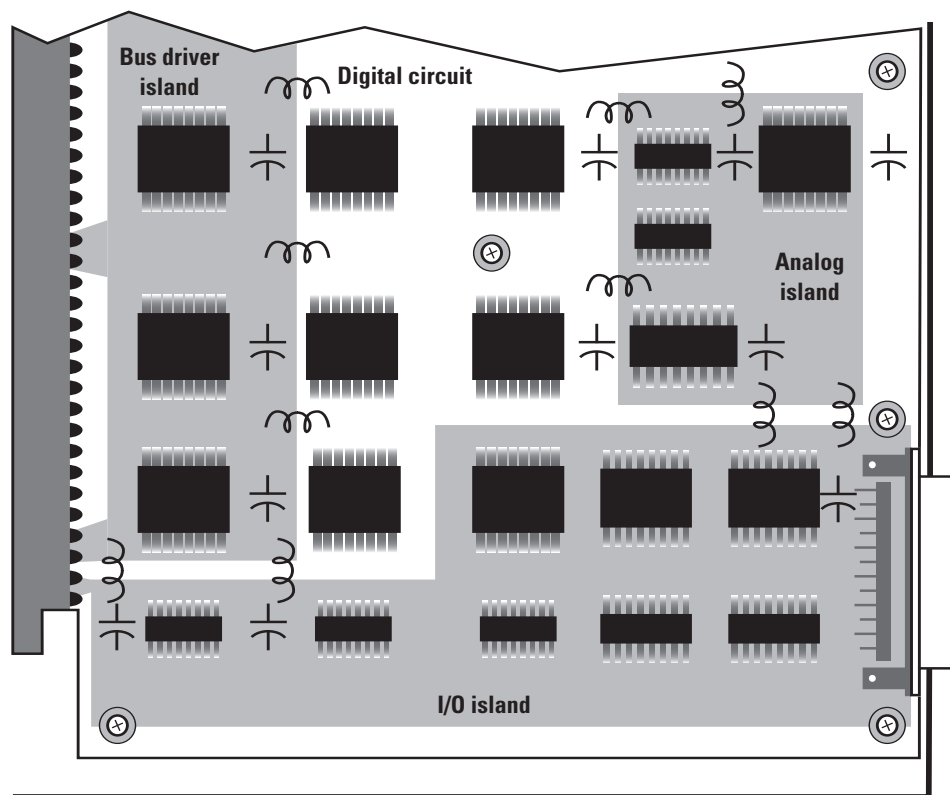
BVOM-005

Figure 2.4. PCB organization and partitioning

System design elements

2.1.2.3 Controlling device-generated noise

BVOM-006
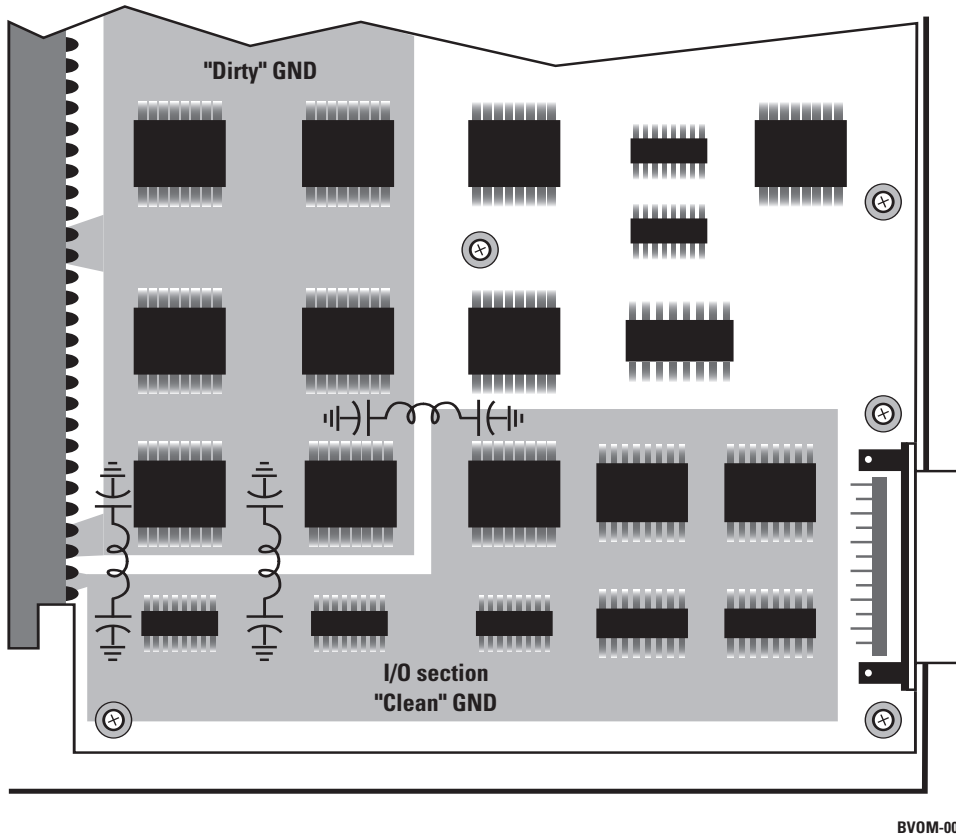
Figure 2.5. Isolate noisy components

Another primary means of controlling device-generated noise is to keep it isolated. Here are some suggestions.

- Keep noisy devices grouped together. Take special care in the powering and bypassing of these devices. In extreme cases, the entire power supply system for these devices might need to be separated and fed independently from the primary power source.

- Care should be taken to make sure that circuit reference potentials, both power and ground, are preserved. A good way to do this is to couple power sub-nets together with adequately sized chokes, frequently spaced and well bypassed at both ends. In Figure 2.5, the sub-nets are connected using Pi-section filter networks.

- Use only one common feed point for powering and grounding (common supply voltage). The feed point should be at a power supply output that is well bypassed. Noise is killed by the low impedance at the common feed point. This prevents noise from reaching and affecting sensitive portions of the PCB or system.

2.1.2.4 PCB layout recommendations

Circuit board layouts and stackups for the digital video devices should be designed to provide noise-free power to the device. Here are some rules for achieving better performance from your designs.

- Multi-layer stackups are mandatory, especially for HD designs. At least four layers are needed for most designs: SDV signals, power plane, ground plane and signals other than SDV. Dedicated power and ground planes are typical of good HF design practice. The solid planes provide a controlled, low-impedance transmission system for the power supplies. These planes also serve as the image conductor paths for currents in the transmission line systems on the adjacent layers.

- Keep power and ground planes in adjacent layers. Power system performance may be greatly improved by using thin dielectrics (four to ten mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system that improves power supply RF filtering and makes the value and placement of external bypass capacitors less critical. This excellent RF bypassing costs next to nothing.

- Isolate fast-edge rate, high-frequency or high-level signals like CMOS and TTL from low-level SDV signals, especially sensitive inputs such as adaptive cable equalizer inputs. Keep the ECL-level, SDV circuits isolated from TTL, CMOS and other high-level signals. True ECL outputs and pseudo-ECL (open-collector) outputs pass 50% to 100% of V_{CC} noise directly on to the following input. It is good practice to put signals associated with the low-level digital video devices on a separate layer or the opposite side of the PCB from high-level signals. This will minimize unwanted stray noise pickup, feedback and interference. Signals having large dv/dt or di/dt should be placed nearest a ground plane.

- Separate cable equalizers, especially their input circuits, from other devices such as cable drivers. Isolate equalizer input networks and connectors to prevent unwanted signal pickup and EMI. Place guard rings or ground floods around equalizer inputs and networks for shielding. Provide closely spaced ground vias in the rings or floods to reduce RF impedance and improve isolation.

- Locate equalizers, cable drivers and associated input or output network components close to PCB edges to minimize transmission system lengths on the PCB.
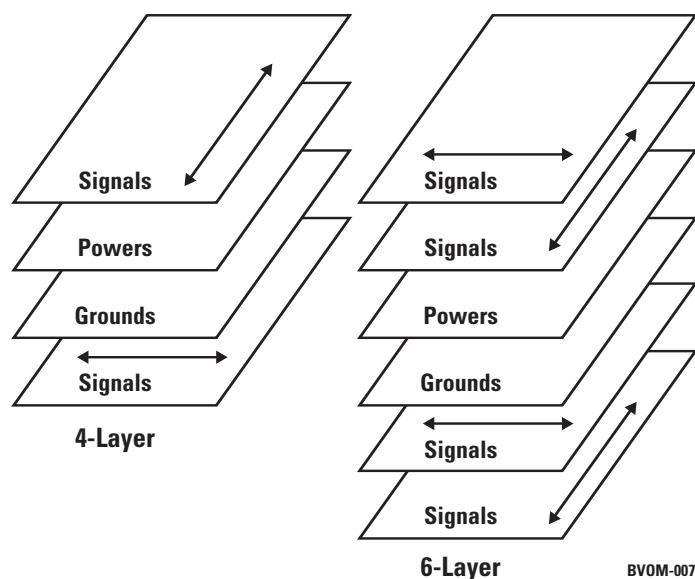
Figure 2.6. PCB stackups and signal orientations

System design elements

2.1.2.5 Organizing power and ground layers

Many digital video systems today require multiple supply voltages in the system as well as on individual PCBs. When the number of components requiring a particular operating voltage is large or the devices are widely dispersed on the PCBs, separate voltage planes for each supply may be the most economical choice. The expense comes with the additional number of layers in the stackup.

When the number of devices requiring a particular supply voltage is few or confined to a small area, the power and/or ground planes can be split into two or more sub-planes. Splitting within the plane may result in reduced cost to manufacture but can cause voltage distribution and noise problems if not done correctly.

If only two voltages are needed in an exclusively CMOS or TTL logic system, then only the positive power layer need be separated since these logic types share the ground as the common voltage reference node.

However, as is the usual case in digital video systems where ECL, analog or other circuitry is used on the same PCB, then both the power and ground planes must be separated. The portions of the split planes should be joined only at the main power feed point of the PCB. If the separate portions of the planes exhibit excessive differential voltage between the sub-planes, inductors may be used to join the sub-planes at frequent intervals to equalize the voltage difference.
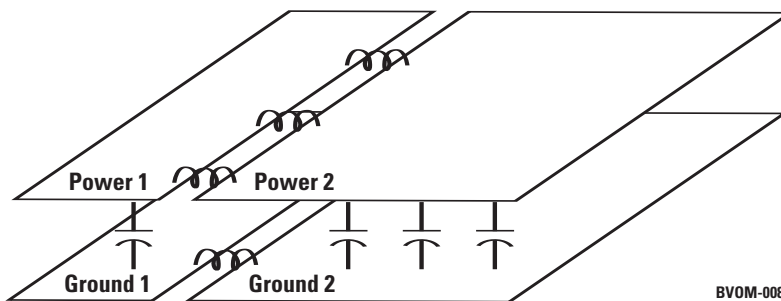
Figure 2.7. The correct way to split planes confines noise

The cardinal rule to observe when separating both planes is: Split both planes along the same boundaries. As shown in Figure 2.8, if the planes are allowed to overlap, the inter-layer capacitance will couple noise from one supply system to the other. This can be disastrous in cases where a CMOS logic power system couples to an ECL or analog power system. The noise thus coupled from the logic can badly degrade the operation of the analog or ECL portion.
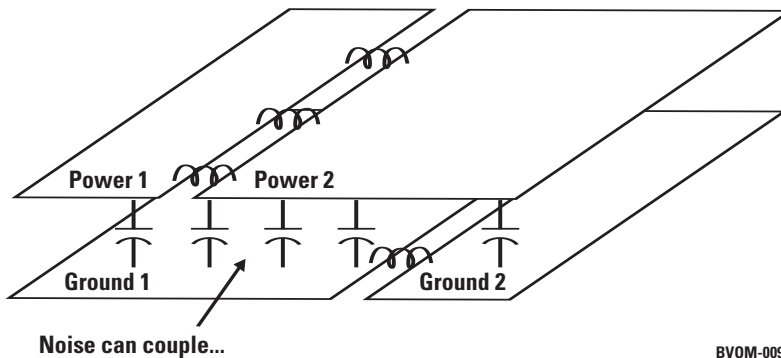
Figure 2.8. The wrong way to split planes couples noise

2.1.3 Voltage regulators and local supply regulation

Analog and mixed-signal devices like many of National's digital video products, particularly adaptive cable equalizers and the PLL-based products, work best when powered from linear regulators. The output of linear regulators is generally cleaner with less noise than switching regulators. Output filtering and power system frequency compensation are generally simpler and more effective with linear regulators. Low dropout linear regulators are available which can usually operate from lower input voltages such as logic power supplies, thereby reducing regulator power dissipation. Cascading of low dropout regulators should not be done since this places the entire supply current load of both load systems on the first regulator in the cascade and increases its loading and thermal output.

On-card voltage regulators operating from a common higher voltage supply are a good way of supplying multiple voltages to devices and PCBs. This is most effective when the amount of power supplied by the regulators is not so large that sizeable amounts of heatsinking or cooling is needed. Unless the enclosure's mechanical design promotes adequate and proper airflow for cooling, it is best to limit on-card regulation to low power applications. Also, location of on-card regulators should consider airflow and cooling relative to other devices.

2.1.3.1 Copper thickness vs. frequency range

High-frequency currents flow within a certain depth below the conductor's outer surface, the so-called skin depth. With digital video systems, it is not enough to think only about the really high frequency signals and their components. Most of the signal frequencies are relatively low such as power supply switching frequencies, control signals, and frequencies inherent in pathological data patterns. These frequencies call for thicker conductors so that there is adequate skin depth. Insufficient skin depth raises conductor impedance at lower frequencies thereby promoting increased noise production and radiation.

Good RF design practice dictates that at least three skin depths of copper must be maintained in power and ground planes to deal with critical frequencies.

- 2 oz. is good down to 7.5 MHz.
- 1 oz. is good down to 30 MHz.
- ½ oz. is good down to 120 MHz.

2.1.4 Planes, pads, and vias

It is recommended practice to use two vias at each power pin of the digital video devices as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance to the IC. When dual vias are used to couple bypassing components to power planes, the effective frequency range of the bypass components is extended.

System design elements
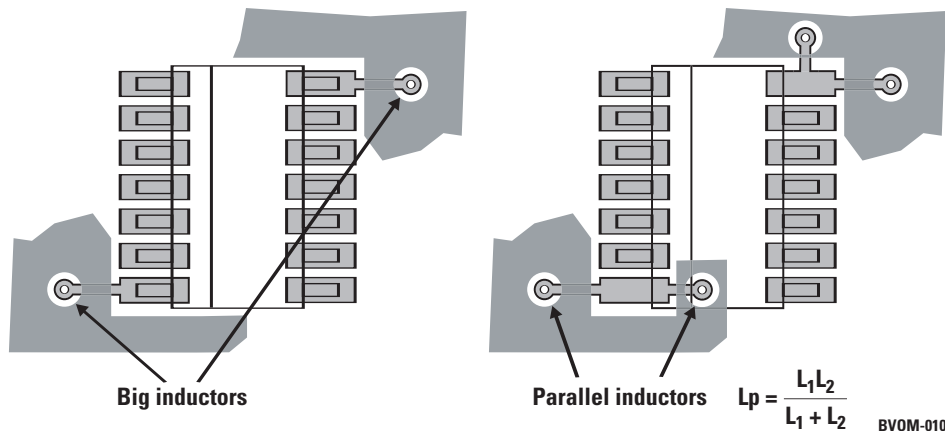
Figure 2.9. Reducing inductance in IC power connections

$$Lp = \frac{L_1 L_2}{L_1 + L_2}$$

Labels on figure: **Big inductors**, **Parallel inductors**, BVOM-010

2.1.4.1 PCB floods

The outer layers of the PCB may be flooded with additional V_{SS} (ground) plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the V_{SS} power supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents that reduce signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) – whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

2.1.4.2 Extra filtering

In especially noisy power supply environments, such as is often the case when using switching power supplies, separate filtering may be used for the different power supply feeds for sections such as the digital logic, PLL or VCO, and output driver power pins. Supply filtering may take the form of L-section or pi-section, or L-C filters in series with these V_{CC} inputs. Such filters are available in a single package from several manufacturers. Despite being independent feeds, all device power supplies should be applied simultaneously as from a common source.

2.2 Transmission line systems

2.2.1 Network topologies

Printed circuit board transmission lines for SDV data paths are generally differential and point-to-point. This is one of the simpler types of transmission line systems and is generally easy to design and have work correctly. The Serial Digital Video & Interface RAPIDESIGNER© slide rule (Lit# 633202-001) can simplify the design of this and other types of PCB transmission line systems (to obtain a slide rule visit www.national.com to find the local support center). Some guidelines to good transmission system design are given below. Less demanding data path applications such as lower frequency parallel data networks can use single-ended microstrip or stripline. Single-ended networks are covered extensively in the transmission line literature. The Transmission Line RAPIDESIGNER slide rule (English units Lit# 633201-001 or metric units Lit# 633200-001) simplify the calculations for these types of lines.

Edge-coupled microstrip, edge-coupled stripline, or broad-side striplines all work well for differential lines.

The differential pair traces for SDV signals should be closely coupled and are best designed for 100Ω differential impedance. The base impedance of the individual lines can be 75Ω. This gives a choice of two simple terminations:

1. Each line can be terminated in 75Ω to V_{CC} or ground (check the device data sheet for recommended load connections). Devices like the CLC014 equalizer and others with open collector outputs are terminated to V_{CC} or similar positive voltage rail when used in PECL power systems. They are loaded to ground which is the positive supply rail when the supply is standard (negative) ECL.

2. The differential line system can be parallel terminated between the lines with 100Ω.

More complex termination schemes can be used, but the simpler terminations generally work quite satis-factorily.

Edge-coupled microstrip lines offer the advantage that a higher differential Z_O is possible (100Ω to 15Ω). Also, it may be possible to route from a connector pad to the device pad without layer changes or any vias. This provides a cleaner interconnect with less chance of a significant impedance discontinuity. A limitation of microstrip lines is that they can be routed only on the two outside layers of the PCB. This is usually not a problem in SDV PCB designs.

Striplines may be either edge-coupled or broad-side coupled pairs. Since they are embedded in the board stack and sandwiched between ground planes, striplines provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect input or output pads to them. Striplines have both lower intrinsic impedance and, therefore, lower differential impedance than microstrip lines of comparable geometries.

Transmission lines and terminations are discussed in more detail in subsequent paragraphs.

System design elements
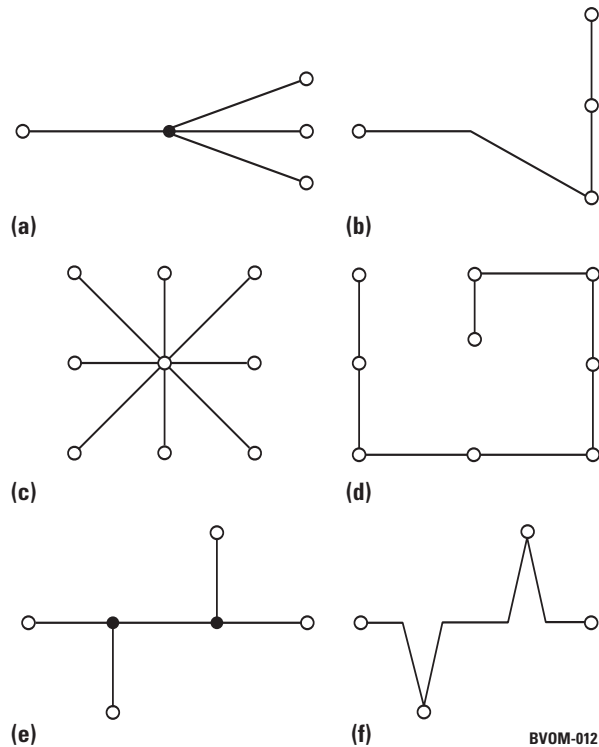
Figure 2.10. Transmission system network topologies

Although SDV networks could be made using any of these configurations, those in Figure 2.10 (a), (c), and (e) should be avoided. They cannot be made to produce quality signals due to multiple reflections and resulting complex impedances. Those in 2.10 (b), (d), and (f), offer superior transmission-line performance. Those network topologies recommended for use in SDV systems, point-to-point and series or "daisy chain", are characterized by simplicity and signal quality.

2.2.2 Differential lines

- Use controlled impedance PCB traces that match the differential impedance of your transmission medium (e.g., cable) and termination resistor. Route the differential pair traces as closely together as possible and as soon as they leave the IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. Signals, which are 1 mm apart, radiate far less noise than traces 3 mm apart, since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the differential receiver.

Microstrip   Stripline   BVOM-013
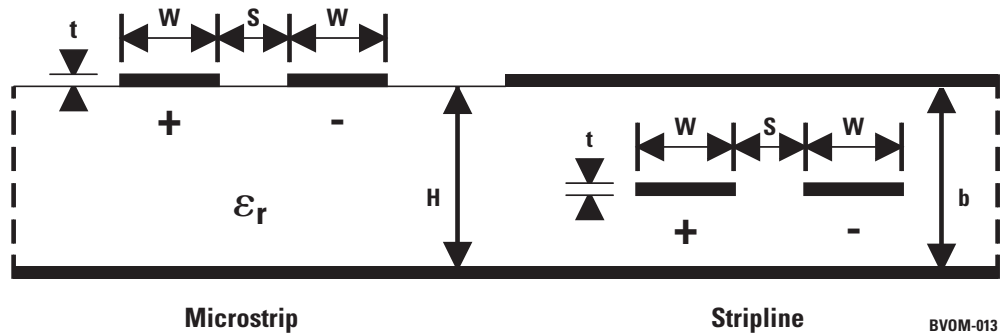
Figure 2.11. Microstrip and stripline

When designing for a specific differential Z_O (Z_{DIFF}) for edge-coupled lines, it is recommended that you adjust trace width "W" to alter Z_{DIFF}. It is recommended not to adjust "S" which should be the minimum spacing specified by your PCB vendor for line-to-line spacing. You can use National's Transmission Line RAPIDESIGNER slide rule (Lit# 633200-001 metric or Lit# 633201-001 English units) and application note AN-905, Lit# 100905-002) to calculate Z_O and Z_{DIFF}, or you can use the equations below for edge-coupled differential lines:

Microstrip   **Stripline**

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.48 e^{-0.96 \frac{S}{b}} \right) \Omega$$ $$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.374 e^{-0.29 \frac{S}{b}} \right) \Omega$$

Microstrip   **Stripline**

$$Z_0 = \frac{60}{\sqrt{0.457 \varepsilon_r + 0.67}} \ell n \left(\frac{4h}{0.67 \left(0.8W + t \right)} \right) \Omega$$ $$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ell n \left(\frac{4b}{0.67 \pi \left(0.8W + t \right)} \right) \Omega$$

Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary. Please refer to AN-905 for accuracy information and ranges supported.

Broadside coupled-line structures can also be used. The dimensions for this type of line are shown in Figure 2.12. Broadside-coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector-pin field. There is no closed-form equation for calculating the impedance of broadside-coupled stripline. Instead, a field solver must be used.

System design elements

Broadside stripline

BVOM-014
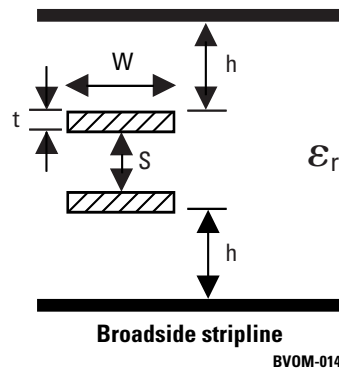
Figure 2.12. Broadside coupled striplines

Always use consistent dimensions (e.g., all dimensions in mils, cm or mm) for S, h, W, and t when making calculations.

Common values of dielectric constant (ε_r) for various printed circuit board (PCB) materials are given in Table 2.1. Consult your PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most SDV applications, the widely used FR-4 PCB material is acceptable. GETEK (also known as FR408) is about 1.5 times as expensive as FR-4, but can be considered for designs over 1000 MHz. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

Table 2.1. Dielectric material properties

PCB material	Dielectric constant (ε_r)	Loss tangent
Air	1.0	0
PTFE (teflon)	2.1 to 2.5	0.0002 to 0.002
BT resin	2.9 to 3.9	0.003 to 0.012
Polyimide	2.8 to 3.5	0.004 to 0.02
Silica (quartz)	3.8 to 4.2	0.0006 to 0.005
Polyimide/glass	3.8 to 4.5	0.003 to 0.01
Epoxy/glass (FR-4)	4.1 to 5.3	0.002 to 0.02
GETEK	3.8 to 3.9	0.010 to 0.015 (1 MHz)
ROGERS4350 core	3.48 ± 0.05	0.004 @ 10G, 23°C
ROGERS4403 prepreg	3.17 ± 0.05	0.005 @ 10G, 23°C

- Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/\varepsilon_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in./ps). A general rule is to match lengths of the pair to within 100 mils.

- Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.

- Minimize the number of vias and other discontinuities on the line.

- Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.

- Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

2.2.2.1 Trace corners and intersections
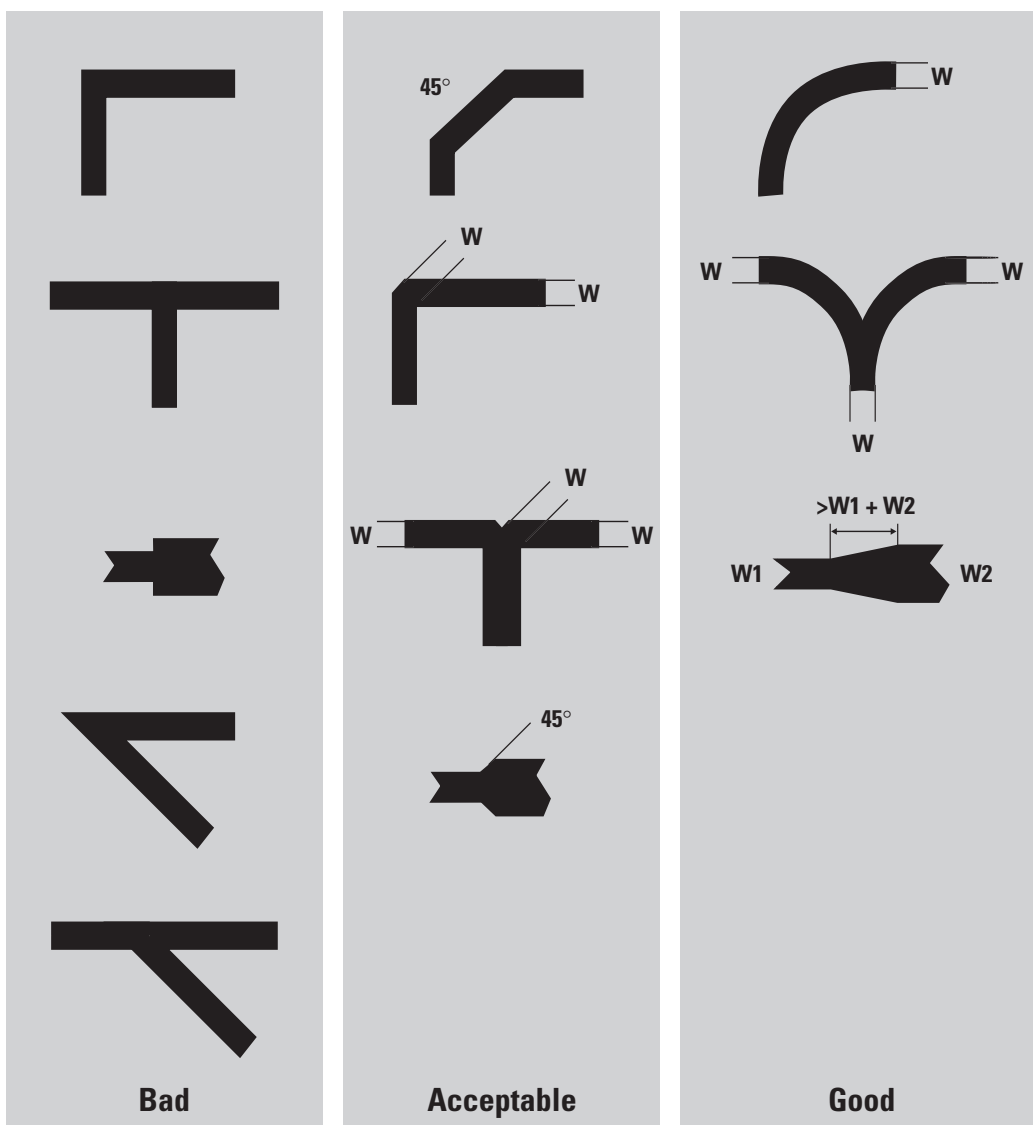
BVOM-015

Figure 2.13. Good, bad and acceptable trace intersections

System design elements

Figure 2.13 illustrates several types of trace intersections in transmission lines. In the left-hand column are intersections that range from bad to worse. Right-angled corners, T-intersections and abrupt changes in line width are to be avoided in SDV transmission lines. Acute intersections are also to be avoided.

In the center column, mitered trace corners and t-intersections where impedance integrity is maintained may be used. Though not preserving of impedance, mitering steps in transmission line width reduces the disturbance. If the difference in widths is small, acceptable signal integrity can usually be obtained.

In the right column, better ways of transitioning and cornering in transmission lines are shown. These methods preserve impedance integrity except in the case of changing line widths. In the case of changing line widths, unless the trace to image plane spacing is also appropriately altered, the impedance will change with the width.

2.2.2.2 Trace and differential pair spacing
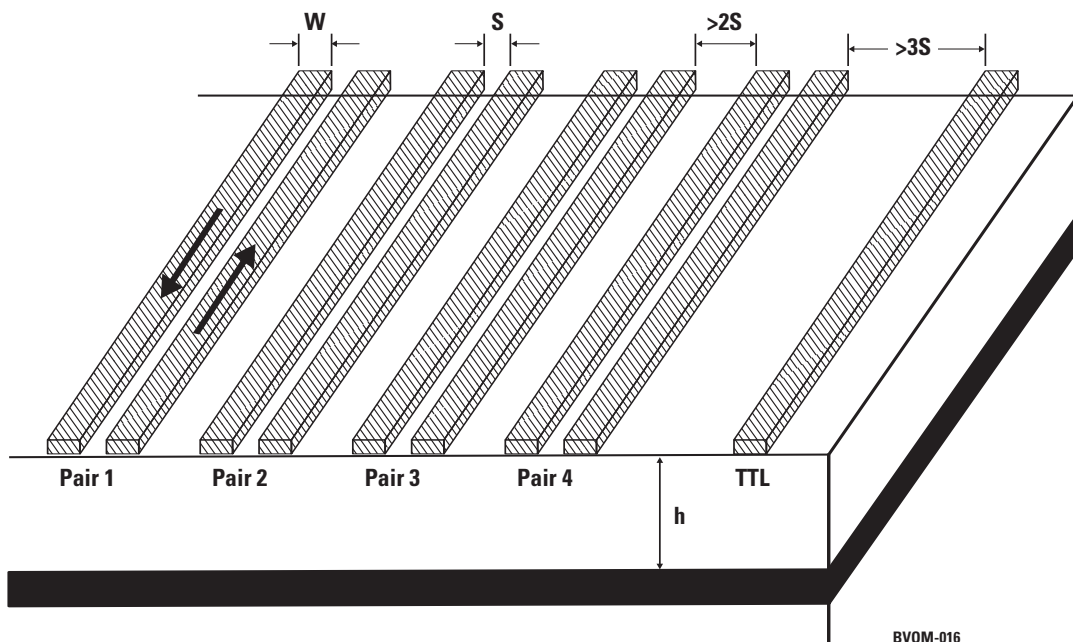
Figure 2.14. Differential line spacing

Following from Figure 2.14 and using the edge-to-edge "S" distance between the traces of a pair, transmission line separation rules can be defined:

- The distance between two pairs should be >2S.
- The distance between an SDV pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane or on the opposite side of the PCB from the SDV signals.
- If a guard ground trace or ground fill is used, it should be >2S away.

2.2.2.3 Crosstalk problems in SDV circuits

Inductive and capacitive coupling between transmission lines causes crosstalk. The magnitude of the crosstalk voltage is proportional to the reciprocal of the square of the spacing between the conductors (strictly speaking, the ratio of line spacing to the distance separating the line from its image plane is s/t). The greater the spacing (or smaller distance to the image plane), the less possibility there is for crosstalk.

The duration of a crosstalk signal is proportional to the length over which the lines are coupled together. Longer coupled lengths produce longer duration crosstalk signals. Crosstalk resulting from reverse coupling, or backward crosstalk, is considered the most disruptive since its amplitude is greater than that of forward crosstalk. For forward crosstalk to be a factor, the network's electrical length must be much longer than the period of the pulses since the amplitude increases slowly with the distance traveled.

Crosstalk can be reduced through some simple steps:

- Space individual transmission lines, or groups of differential transmission line pairs, apart by at least twice the width of the widest conductor. See Figure 2.14.
- Place a shield line or guard trace between or around conductors that are sensitive to interference such as those used in inputs to adaptive cable equalizers. Frequent ties to ground along the shield or guard trace are required.
- Separate clock or other high-frequency signals away from other circuits and surround by ground floods or guard traces.
- Use stripline for especially sensitive signal conditions.

2.2.3 Termination

2.2.3.1 Single-ended termination

There are numerous termination schemes that may be used: series, parallel, AC parallel, and Thevenin termi-nations. AC parallel and series terminations are useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations can have relatively high DC power consumption.

2.2.3.2 No termination

Transmission line systems used for the high data rates in SDV video data transmission must be terminated to preserve pulse and signal characteristics. The no termination situation is not used as it produces the worst possible signal distortion. Sometimes in non-critical, low speed TTL or CMOS logic networks, it can be used but line lengths must be kept short. The one-way propagation delay should not exceed about ½ of the signal risetime for the logic being used.

System design elements

a. No termination

c. Parallel termination

b. Series termination

d. AC parallel termination

V+

e. Thevenin termination
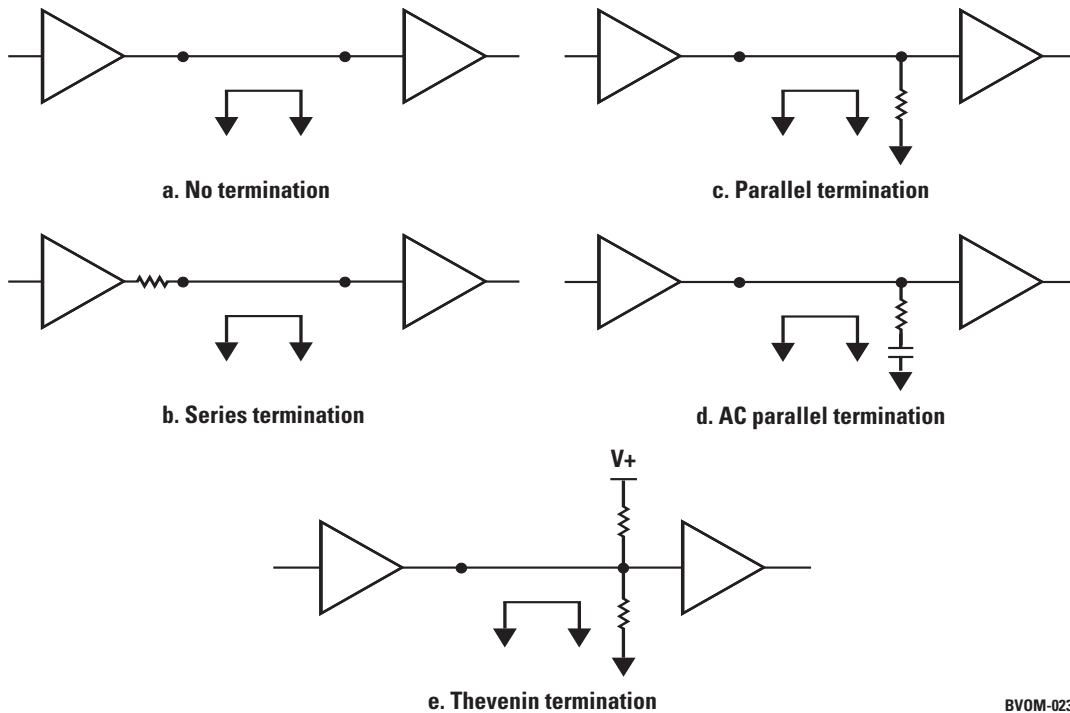
BVOM-023

Figure 2.15. Single-ended termination

2.2.3.3 Series termination

Series terminations, Figure 2.15 (b), may be used in high-speed applications such as SDV systems where the load is located at the far end of the line. This situation is typically found in the coaxial transmission systems using cable drivers having so-called back-matched terminations. Generally, SDV networks have terminated load ends.

When used for networks with loads located between the driver and the unterminated receiving end of the line, the intermediate loads will receive a two-step waveform. The first step will be the incident wave, V_I. The amplitude is determined by the output equivalent generator resistance of the driver, the value of the series resistor, and the impedance of the line according to the formula:

$$V_I = \frac{V_{OUT}\,Z_0}{Z_0 + R_S + R_{GEN}}$$

The amplitude will be one-half the voltage swing if series resistance, R_S, plus the driver output equivalent generator resistance, R_{GEN}, is equal to the line impedance. R_{GEN} for the cable drivers is about 5Ω.

In the case of an unterminated load end, the second step of the waveform is the reflection from the destination end of the line. It will have an amplitude and polarity equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing after a time equal to the round-trip delay of the line.

2.2.3.4 Parallel termination

Parallel terminations, Figure 2.15 (c), are commonly found in SDV circuits, both on PCBs and coaxial transmission systems. The resistor value is most commonly the value of the transmission line Z_0. These terminations are not generally recommended for TTL or CMOS circuits because of their power consumption. Sometimes this can exceed the power consumption of the logic itself. Output circuit overloading is quite common if the resistor is not correctly sized. Power consumption of parallel terminations is a function of the resistor value and the signal duty cycle. Generally, the resistor cannot be made equal to the transmission line impedance because of this overloading. In addition, parallel termination affects the output bias of the driver towards either the positive supply or ground depending on to which it is returned. While this characteristic is not desirable when driving CMOS inputs, it can be useful when driving TTL inputs.

2.2.3.5 AC parallel termination

AC parallel terminations, Figure 2.15 (d), work well in networks where delays caused by series terminations are unacceptable. The effectiveness of AC parallel terminations is similar to that of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption. The capacitor is generally sized to be effective during the transitions.

2.2.3.6 Thevenin termination

Thevenin terminations, Figure 2.15 (e), are common in SDV circuits. The principal drawback to their use is their power consumption that is typically 11 times that of a comparable parallel termination (in ECL circuits). Like the parallel termination, a DC path across the power supply exists due to the series connected terminating resistors. The power consumption of a Thevenin termination is not strictly a function of signal duty cycle. Thevenin terminations are often used in CMOS applications because they do not bias the output levels as do parallel terminations.

2.2.3.7 Differential termination

Differential lines are most commonly terminated using a single resistor of a value equal to the characteristic differential impedance of the line. The main issue with differential terminations is where to locate the resistor. The principal concern is the stub created when connecting the load to the line.
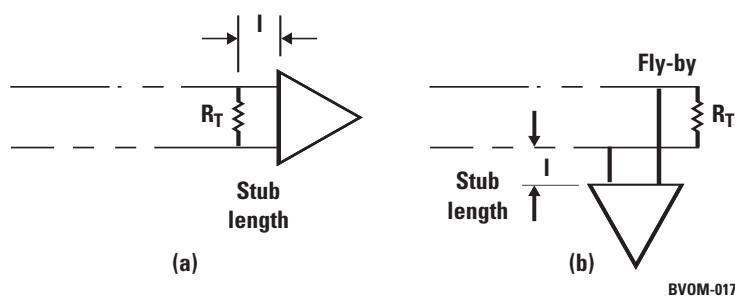
Figure 2.16. Differential termination location

By way of illustrating the tradeoff, Figure 2.16 shows two conditions. In Figure 2.16 (a) the termination is located immediately ahead of the receiver input. The stub exists in the excess line connecting the termination to the receiver and the lead frame and bond wire inside the package. If long enough, this stub can cause ripples or overshoot in the transitioning edges of the signal. This is particularly troublesome in HDTV serial data links where the risetime is <270 ps. When using this configuration in lower data rate SDTV systems, the stub length should be as short as possible.

System design elements

The "fly-by" termination is shown in Figure 2.16 (b). This form is particularly useful where the transmission line is connected to the input in "daisy-chain" fashion: i.e. the line first connects to the mounting pads of the IC and from there continues to the termination. Only the lead frame and bond wire inside the package forms the stub in such cases. This greatly reduces the possibility of signal distortion.

2.2.4 System-to-system transmission

Digital video employs both parallel and serial transmission line systems for communicating between system elements. In general, common design rules, such as those governing terminations, apply to both cases. Parallel cabling systems generally employ multi-pair, shielded, or twisted pair cables of about 110Ω impedance. Serial cabling systems use coaxial cable, precision 75Ω cable having the lowest possible losses being the norm. Various types of coaxial cable can be used provided that the frequency response approximates the $\sqrt{f}$ characteristic outlined in the serial standards. Yet no matter how good the coaxial cable is, significant attenuation of the SDV signal is a fact of life as Figure 2.17 attests. The expected operational distance for standard-definition systems is approximately 300m and about 100m for high-definition systems.
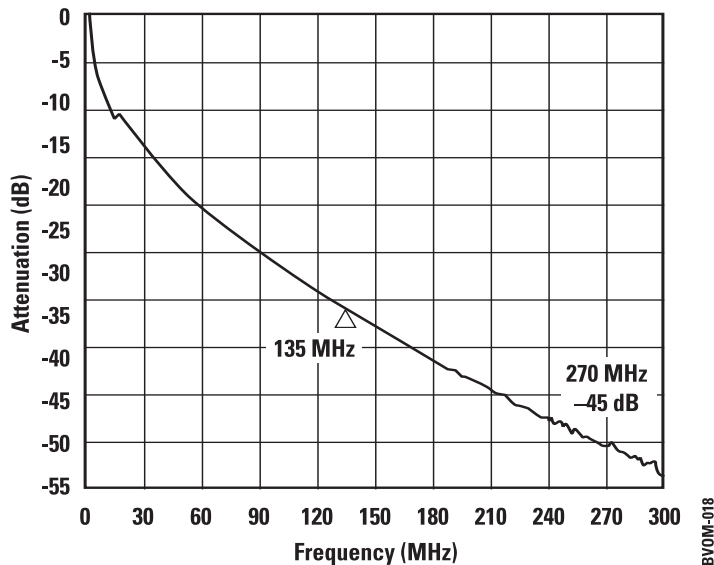
Figure 2.17. Coaxial cable attenuation vs. frequency

Parallel digital video communications use uni-polar, NRZ signaling codes at data rates from 14.3 Mbps to 74.25 Mbps depending on the particular parallel source format and standard. The handling of such links and their signal integrity issues has been well covered in the literature. National's application notes AN-806, AN-807, and AN-808 are some of the most comprehensive discussions of transmission line signaling available anywhere.

Serial digital video communications employ bi-polar, Non-Return to Zero Invert-on-ones (NRZI), as shown in Figure 2.18. This coding is relatively simple to generate but falls short of the desirable features for pulse codes employed for low-jitter, extended distance communications over cable, namely:

- Compress the overall bandwidth normally required to adequately transmit the signal yet still ensure recovery of the binary data.

- Eliminate the need for a DC response in the transmission medium. (The elimination of a DC characteristic of the pulse code also allows AC coupling of amplifier circuits).

- Provide a clocking scheme within the signal so that no separate clock channel is required for synchronization.

- Provide built-in error detection.

The NRZI coding does have a pronounced DC component, is not self-clocking nor does it have error detection features. AC (capacitor) coupling is required for digital video serial links. However, transformer coupling could be used except for operational problems involving the IC adaptive cable equalizers. (The equalizers are specifically designed for capacitive coupling). And, the fact that this coding is not self-clocking requires the use of phase-locked loops of other means to generate a transport clock with which to fully recover the data at the receiver.
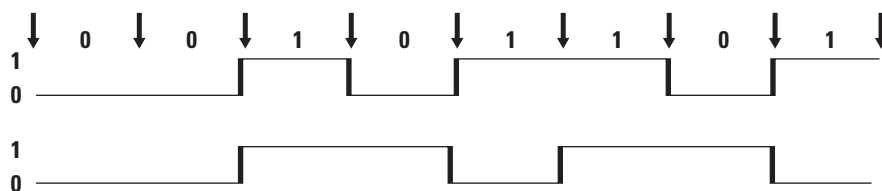
BVOM-019

Figure 2.18. Example of NRZI coding

It should be appreciated that all codes including NRZI suffer from the effects of DC-bias shift during transmission. This is a major contributor to jitter production and signal timing distortion at the receiver. In order for the transmission not to suffer greater distortion, additional requirements must be met such as:

- Driver output swings and rise or fall times should be symmetrical.

- Terminations should match the transmission system impedance.

- And differential timing delays in the receiver channel should be avoided.

System design elements

2.2.4.1 Connectors for coaxial systems

Serial digital transmission systems employ BNC connectors, which have been used in analog video systems for many years. The BNC connector, though widely used and fairly rugged, is not ideal for use in broadband digital signaling. Chief among its less desirable attributes is its non-precision impedance characteristic. Digital video standards are generous in allowing both the original 50Ω and newer 75Ω versions through a fairly wide return loss (impedance) specification of ±15 dB (a reflection coefficient of ±18%). In terms of a 75Ω system impedance, this translates into a 52Ω to 107Ω range. This loose characteristic did not present large problems for signals with classical ECL risetimes, 500 ps to 1.5 ns. However, with the advent of high-definition serial links having risetimes <270 ps, the limitations of the BNC became more pronounced. Connector manufacturers now produce a 75Ω version of the BNC having good return loss characteristics at frequencies above 2 GHz. An example of one such connector for PCB applications is shown in Figure 2.19.

BVOM-020
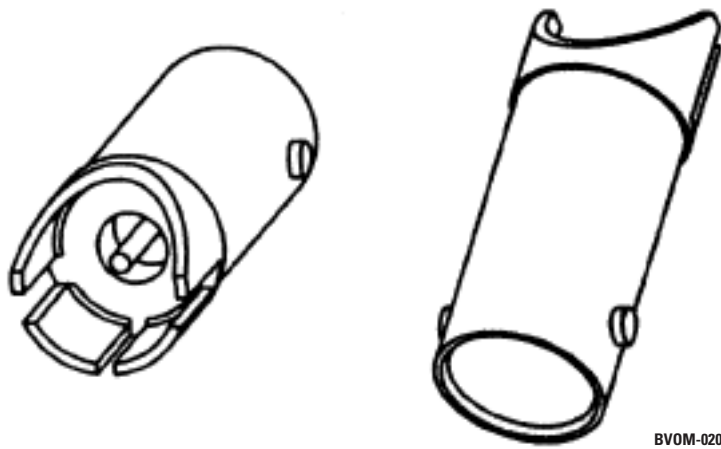
Figure 2.19. 75Ω PCB mount BNC connector

Certain configurations of a BNC connector present problems in serial digital systems. One such example is shown in Figure 2.20. The close proximity of the center conductor "pig tails" allows signal coupling to occur. If one of these lines were connected to an adaptive cable equalizer and the other to a cable driver, the result would be faulty operation of the equalizer. Since the equalizer has very high gain, especially when connected to long cables or when its input is unconnected (open circuit), it will pick up the signal from the cable driver and produce nonsensical output signals.

BVOM-022
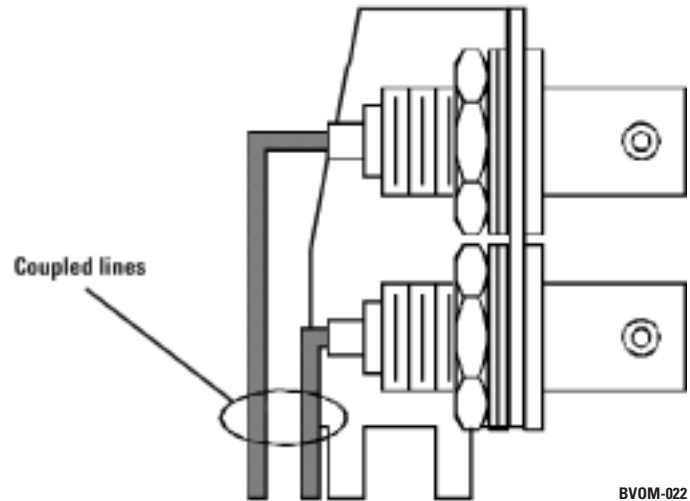
Figure 2.20. Dual BNC connector

System design elements

2.2.4.2 Source and load termination summary
Table 2.2. Source and load conditions

Configuration name (if any)	(Driver) source resistance	(Receiver) load resistance	Signal characteristics	Optimum receiver threshold	Line receivers allowed at other than load end of line?	Comments
Unterminated	$< R_0$	$> R_0$	Ringing pronounced.	$0.5\ V_{SS}$	Yes	Undershoot may cause errors.
Parallel terminated	$< R_0$	$= R_0$	Excellent fidelity.	$0.5\ V_{SS}$	Yes	Load resistor consumes power. $$P_L = \frac{V_{SS}^{2}}{R_L}$$
	$< R_0$	$< R_0$	Awful to different signals at each point on the line.	NA	No	Not generally useful.
Series terminated or backmatched driver	$= R_0$	$> R_0$	Load signal excellent.	$0.5\ V_{SS}$	No	Reduced power consumption over parallel termination.
Fully matched	$= R_0$	$= R_0$	Excellent fidelity	$0.25\ V_{SS}$	Yes	Greater tolerances on resistors allowed for same fidelity as parallel termination.
	$= R_0$	$< R_0$	Load signal like a one shot.	NA	NA	Not generally useful for data, is useful as pulse generator.
	$> R_0$	$> R_0$	Exponential like signal waveforms.	$0.5\ V_{SS}$	Yes	Low power consumption. Increased delay due to signal "rise" times.
	$> R_0$	$= R_0$	Small signal amplitude and excellent fidelity.	$0.5\ V_{SS}$	Yes	Produces only small signal voltages compared with other methods.
	$> R_0$	$< R_0$	Very small signal amplitudes, also ringing.	NA	NA	Not generally useful.

2.2.4.3 Termination summary — the advantageous combinations

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in Table 2.2. Those combinations generally used in voltage mode communications circuits are as follows:

- Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced "ringing" effects. The ringing can be reduced by controlling signal rise/fall time vs. time delay of the line, or by clamping (with diodes, for example) to limit load signal excursions. This case is representative of TTL/CMOS circuits and thus, is widely employed.

- The parallel-terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires specific line driver devices such as the CLC006 or CLC007 or other devices having cable drive outputs.

- The series terminated or back-matched driver case ($R_S = R_0$, $R_L \gg R_0$) provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular bridging points. Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these constraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time contributing a significant savings in steady state power consumption.

- The fully matched case ($R_S = R_0$, $R_L = R_0$) not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel-terminated case. Additionally, the power consumption is somewhat less than the parallel-termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

System design elements

2.3 Signal path inputs and outputs

2.3.1 Network component and layout guidelines

This section includes a discussion of the specifics of particular signal path inputs and outputs. It is important to understand the layout of these networks. The networks generally serve relatively low-impedance 75Ω systems, where the individual properties of the components and their method of mounting can dramatically affect the integrity of the SDV data signal. The main guidelines are listed below:

1. Group input and output network components compactly to avoid excessive interconnect lengths. Coupling can occur between the bodies of components that can add unwanted parasitics to the network and affect impedances or signal waveforms. Therefore, maintain appropriate spacing between components to reduce this unwanted coupling. Generally, a spacing of at least twice the thickness (or height) of the component body is sufficient.

2. Use components of minimum physical size, but be sure that these have adequate power and voltage ratings.

3. When attempting to maintain the characteristic impedance and reduce parasitic effects, voids or clearance areas in the image power and ground planes directly under the affected components may be used. The void areas in the copper planes should be larger than the area of the components. The cleared area should include additional clearance (or "shrink-back" as it is often termed) all around of at least twice the thickness of the dielectric layer under the components. This will minimize stray capacitance to pads and lines.

4. The layout of differential inputs and outputs should be symmetrical or mirror-image. This equalizes the effect of parasitic elements and stray pickup effects on either inputs or outputs.

5. Surround sensitive inputs with ground rings or ground floods on the outer PCB layers to prevent pickup of EMI. This applies especially to the inputs of adaptive cable equalizers. Also, do not locate high-level outputs or other high-level signals adjacent to the inputs and input networks of these devices.

6. SDV serial signals are broadband RF signals. Grounding in networks carrying RF signals requires larger area conductors and more vias than is the case with other types of signals. Grounding considered adequate for audio, common digital and other lower frequency applications is not adequate for baseband SDV serial signals, especially at the HD rates.

7. Use only high quality RF-rated ceramic capacitors for coupling the SDV serial signal. Aluminum and tantalum electrolytic capacitors are not suitable for RF or digital signal coupling. Besides their large physical size which requires large mounting pads that can cause severe signal distortion, these are polarized devices that exhibit non-linear or diode-like effects in the presence of signals with a varying DC component.

2.3.2 Bipolar cable driver inputs — CLC005, CLC006, and CLC007

The CLC005, CLC006 and CLC007 have high-impedance, emitter-follower buffered, differential inputs. These inputs accept both differential and single-ended signals. Either AC or DC coupling as shown in Figure 2.22 or Figure 2.23 may be used. Figure 2.22 shows how Thevenin-equivalent resistor networks are used to provide input termination and biasing. A method of low power biasing is shown in Figure 2.24 that reduces the supply current used by the bias network to about 1 mA. Transmission lines supplying input signals must be properly terminated close to the device. Input coupling network layouts should be kept compact with short interconnecting lines.

The input DC common-mode voltage range of the CLC005, CLC006, and CLC007 is 0.8V to 2.5V below the positive power supply (V_{CC}). Input signals plus bias must be kept within the specified common-mode range. For an 800 mV p-p input signal, typical input bias levels should range from 1.2V to 2.1V below the positive supply.
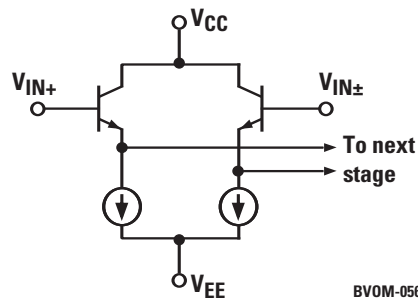
Figure 2.21. CLC005, CLC006 or CLC007 input stage

AC coupling capacitors must be sized for the particular data rate and data coding of the system in which the driver is used. For standard-definition SDV applications operating at 270 Mbps and 360 Mbps, a value of 1 µF is recommended. For applications operating at 143 Mbps and 177 Mbps, either 1 µF or 2.2 µF are recommended. For use at all standard-definition rates, 1 µF is adequate for pathological conditions. For other data codings such as 8B10B and others that are relatively DC balanced, 0.1 µF may be used.
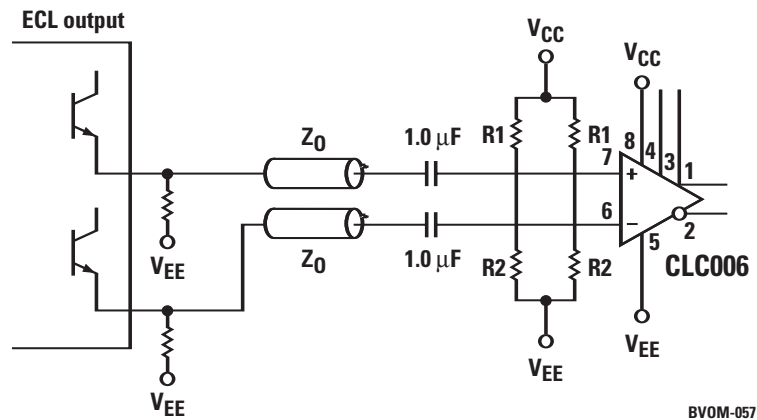
Figure 2.22. AC coupling with Thevenin termination

System design elements

Thevenin terminations are disadvantageous because of the large amount of supply power that they consume, typically as much as 11x that of the equivalent parallel termination. For this reason, lower power bias and termination schemes are preferred such as the one shown in Figure 2.24. Table 2.3 gives resistor values for a variety of common application situations.

Table 2.3. Thevenin terminations

Load type	Resistor to V_{CC} (R1)	Resistor to V_{EE} (R2)
ECL, 50Ω, 5V, V_T = 2V	82.5Ω	124Ω
ECL, 50Ω, 5.2V, V_T = 2V	80.6Ω	133Ω
ECL, 75Ω, 5V, V_T = 2V	124Ω	187Ω
ECL, 75Ω, 5.2V, V_T = 2V	121Ω	196Ω
800 mV p-p, 50Ω, 5V, V_T = 1.6V	75Ω	154Ω
800 mV p-p, 75Ω, 5V, V_T = 1.6V	110Ω	232Ω
800 mV p-p, 2.2kΩ, 5V, V_T = 1.6V	3240Ω	6810Ω

BVOM-058

Figure 2.23. DC coupling with parallel termination

The CLC005, CLC006, and CLC007 may be DC coupled to suitable sources. The source must have a DC output voltage range that meets the CLC005, CLC006, or CLC007 input common mode requirements. The termination may be either Thevenin or parallel according to the designer's choice and the specific needs of the driver output. When the system is PECL, parallel loads should be returned to V_{CC}.
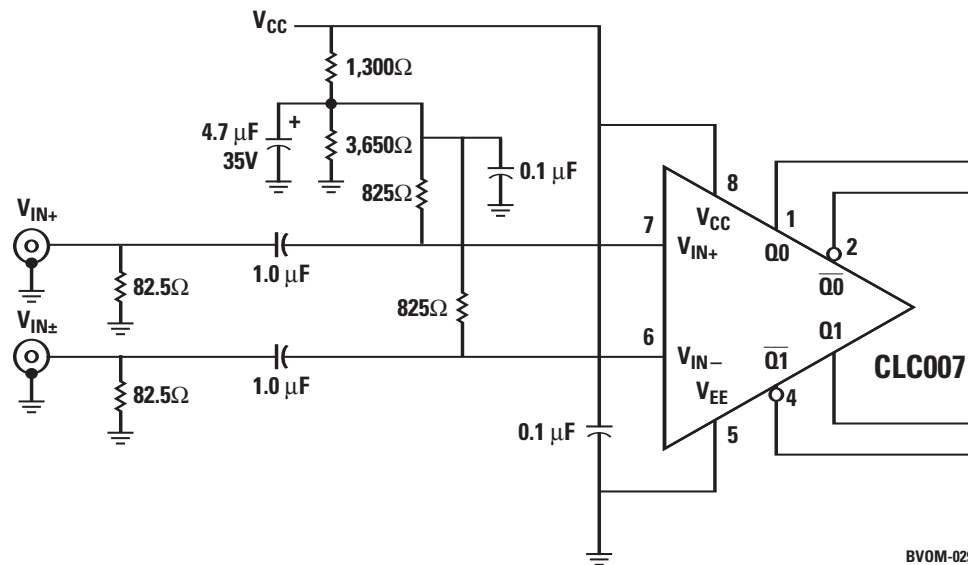
Figure 2.24. AC coupling with low power termination

It is desirable that input bias schemes be designed for low power consumption. Figure 2.24 shows one classical method. The input bias current required by the device is <50 µA per input. Up to 0.1 mA is available from the bias source via the 825Ω resistors. The termination resistance, 75Ω, seen by the source is the parallel combination of the 82.5Ω DC termination and 825Ω AC termination resistors. Many similar schemes are possible including one where the 1300Ω resistor is replaced by a low-current LED such as the HLMP-4700 or similar device. This might provide a power-on indicator virtually for free.

2.3.3 Cable driver outputs — voltage mode
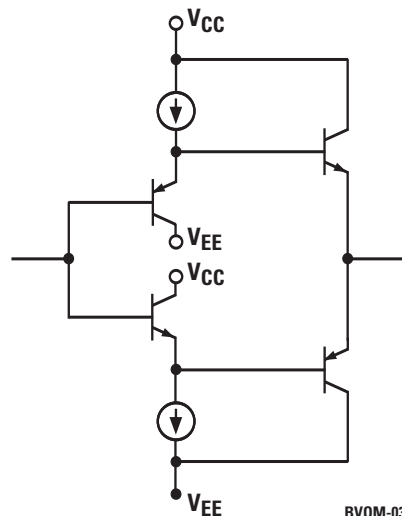
Figure 2.25. Voltage mode cable driver output

System design elements

The output stage of the CLC005, CLC006, and CLC007 is class AB push-pull, shown in Figure 2.25. This design requires no standing current in the output transistors and therefore requires no biasing or pull-down resistors. Advantages of this arrangement are lower power dissipation and fewer external components. The output may be either DC or AC coupled to the load. However, output current limits must be observed, especially in DC drive applications. A bandgap voltage reference sets output voltage levels. These outputs are designed to swing 1.6 V p-p into series terminated load networks, Figure 2.26. The output swing into the cable is 800 mV which is compatible with SDV cable equalizers, F100K and 10K ECL when correctly load-terminated.
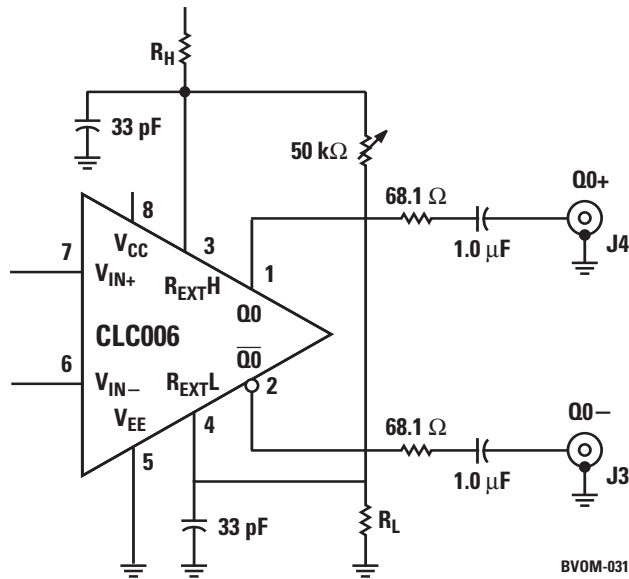
Figure 2.26. Output voltage adjustment

Outputs of the CLC005 and CLC006 are adjustable for swing, high or low level. Figure 2.27 shows the required resistances for output level adjustment. Full details are found in the respective product data sheets.
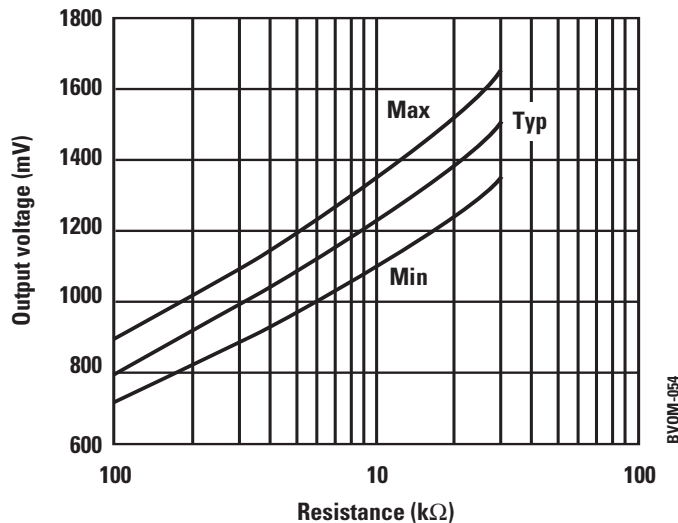
Figure 2.27. Voltage adjustment resistance vs. output voltage

2.3.4 Cable driver outputs — current mode

The CLC020, CLC021, and CLC001 use a CMOS current source cable driver output design. A simplified schematic is shown in Figure 2.28. The nominal output swing is 800 mV for the CLC020 or CLC021 and 1V for the CLC001. The output swing is adjustable over a limited range by adjusting R_{REF}. The output swing is inversely proportional to the value of R_{REF}. The outputs require a DC load, R_S, on both outputs in order to produce the correct output voltage. Both outputs should be loaded equally to maintain signal balance and to reduce noise injection into the device's substrate and the PCB ground. These outputs are designed only for AC coupling to coaxial or twisted pair cables. Receiving-end terminations may be any of the types previously discussed.
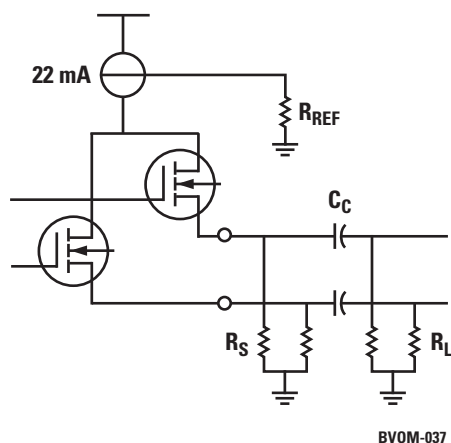
Figure 2.28. CLC020 Current mode output

The CMOS current mode cable driver of the CLC030, Figure 2.29, is pseudo-PECL, being loaded to V_{DD}. It has different risetimes depending on whether it is operating in SD or HD mode. The peak level is adjustable by resistor $R_{REF}LVL$ and the risetime precharge current, used for HD mode, by resistor $R_{REF}PRE$. Automatic operation of the precharge and output level multiplexer is controlled by the rate selected by the PLL. The output swing is equal to the level required by the SMPTE 259M or 292M standard. Both outputs must be equally loaded for balanced output levels and transitions. This output is designed only for AC coupling to 75Ω terminated loads.

System design elements
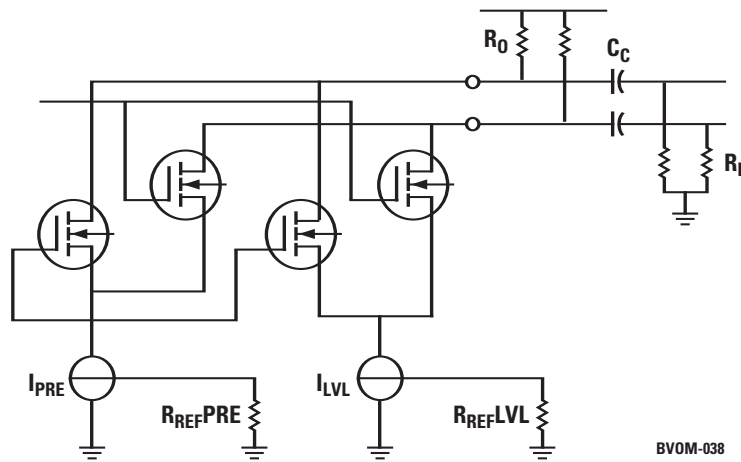
Figure 2.29. CLC030 current-mode output

2.3.5 ECL-compatible inputs

The CLC011, CLC016, and CLC018 have buffered ECL-compatible inputs shown simplified in Figure 2.30. This input has the advantage of being compatible with bipolar and CMOS pseudo-PECL and standard ECL outputs. The input swing can be standard ECL (800 mV) and can swing to the positive rail without input saturation. Therefore, it is not necessary to include a diode drop in pseudo-PECL output loads (bipolar or CMOS) connected to the positive supply rail, as shown in Figure 2.31, when driving these inputs.
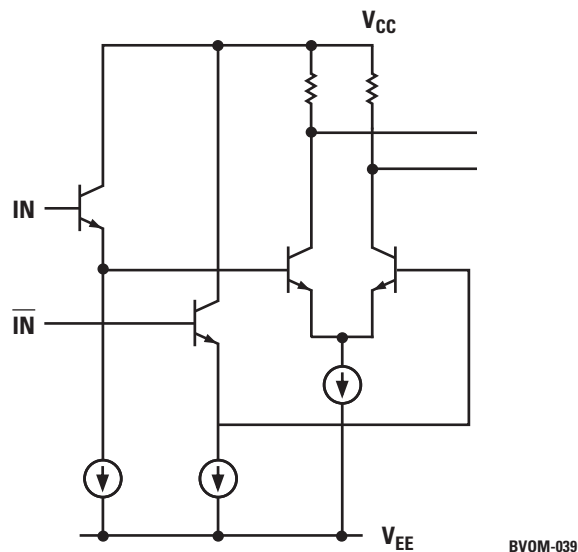
Figure 2.30. Buffered ECL-compatible input

2.3.6 ECL-compatible outputs

The CLC012, CLC014, CLC016, and CLC018 have open-collector, pseudo-ECL outputs (or PECL depending upon the supply scheme used). These are current-sinking outputs that have definite voltage and current boundaries. Output sink current is limited to the maximum given by the relevant product data

sheet. This current therefore determines the maximum voltage swing available under the specification load condition, usually 75Ω. Other load conditions will produce other output voltage swings. There are both upper and lower output voltage swing limits.

Interfacing to standard, unbuffered ECL inputs requires that the voltage supply feeding the output load resistors be lowered by at least one diode drop, about 0.7V. This prevents saturating the input bipolar transistors, which reduces the operating frequency of the device. The minimum supply voltage that may be used to power the outputs is given in the Recommended Operating Conditions table of the product data sheet. In general, the supply voltage minimum that can be applied to the V_{CC} end of the output load resistors is V_{CC}–0.8V. See Figure 2.31.

When interfacing to inputs of the CLC011, CLC016, CLC018 or emitter-follower buffered ECL and pseudo-ECL inputs, the supply dropping diode is optional and not required for signal compatibility. If desired, a 75Ω to 91Ω resistor may be used instead of the diode.
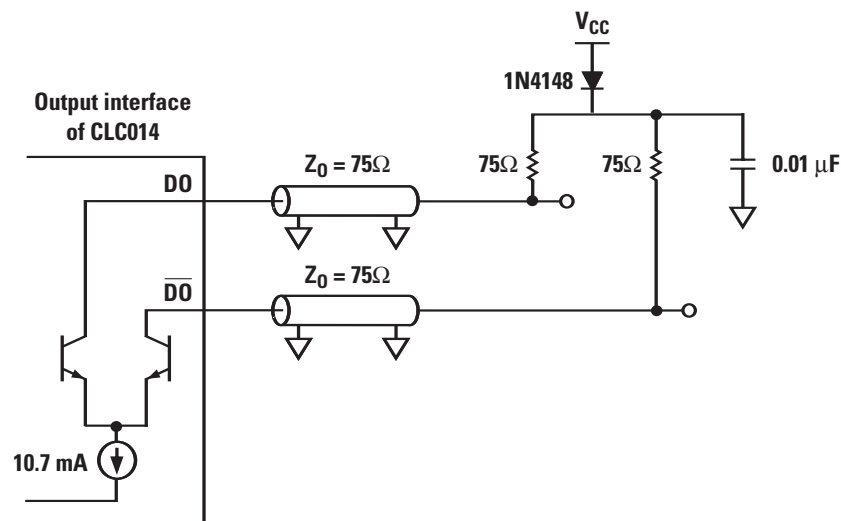
BVOM-040

Figure 2.31. ECL-compatible output
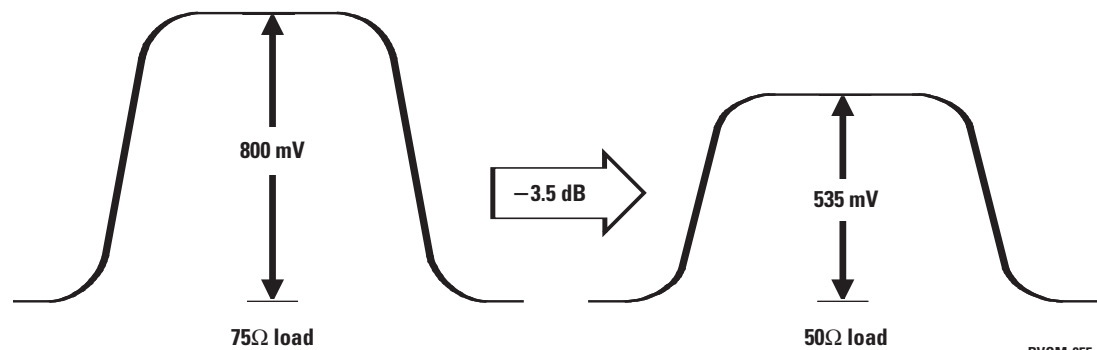
BVOM-055

Figure 2.32. Effect of 50Ω load on output level

System design elements

The ECL-compatible open collector outputs of National's CLC0xx product line are specifically designed to drive 75Ω terminated networks. The fact that these outputs are both current-sinking and voltage-excursion limited means that loading into other than 75Ω will produce output levels differing from the relevant data sheet specification as illustrated by Figure 2.32. As shown, loading these outputs in 50Ω will reduce the swing from a nominal 800 mV to about 535 mV.

2.3.7 CLC011 CMOS outputs

All outputs of the CLC011 are CMOS compatible. They can be programmed to provide appropriate output logic levels to connect to following stages operating from supplies of 3.0V to 5.5V. Output voltages are set by applying the positive supply voltage powering the following stage to V_{DP}, which controls PD0-9, EAV, TRS and NSP, and V_{CP}, which controls P_{CLK}.

BVOM-041
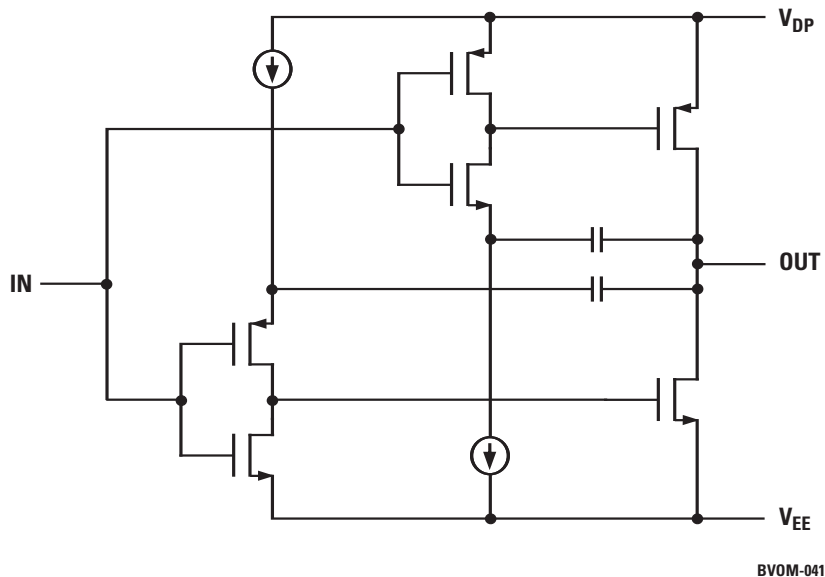
Figure 2.33. CLC011 CMOS output

The CLC011 output driver, shown simplified in Figure 2.33, is designed to maintain a constant, controlled slew rate regardless of load. This design results in lower output switching noise injection via the supply pins and into other circuitry. Even so, it is recommended that the CLC011 and other digital circuitry be separated from analog circuitry and adaptive cable equalizers.

2.3.8 CLC012 and CLC014 Adaptive cable equalizer data inputs

The analog differential data inputs of the CLC012 and CLC014 accept either single-ended or differential input voltages at driver levels specified in their respective data sheets. The inputs are internally self-biased and are designed for capacitor AC coupling to the transmission line. Since these devices compensate for cable losses, input signal levels and other characteristics are specified for the cable driver output signal rather than the equalizer input.
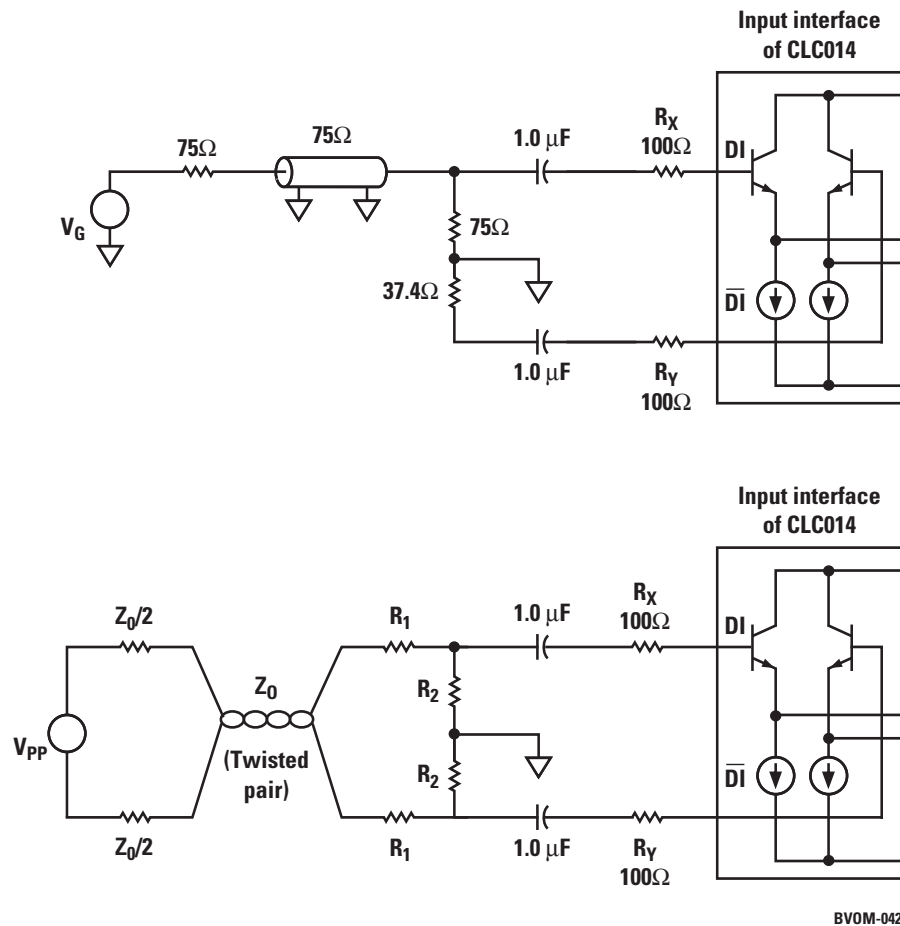
Figure 2.34. Using adaptive cable equalizer data inputs

Balancing unused inputs in single-ended applications helps to lessen the effects noise through the inherent common mode rejection of the input differential amplifier. In a 75Ω system application, use the equivalent 37.4Ω termination to balance the impedance seen by each input. The series 100Ω resistors are recommended for best performance. When interfacing to differential cables, a termination network as shown in Figure 2.34 is usually required. The values of the termination resistors may be determined from the equations that follow. In general, the length of twisted pair cable which can be equalized at a given data rate is about half that of coaxial cable.

$$R_1 = \frac{Z_O}{V_{p-p}}\left(\frac{V_{p-p} - 1.6}{2}\right) \qquad R_2 = \frac{0.8Z_O}{V_{p-p}}$$

Chapter 3
Serial digital video integrated circuits

Figure 3.1 shows the key building blocks used within SDV systems. In this section we will cover the key features of each functional block and present design tips and trade-offs for National's SDV product offerings.
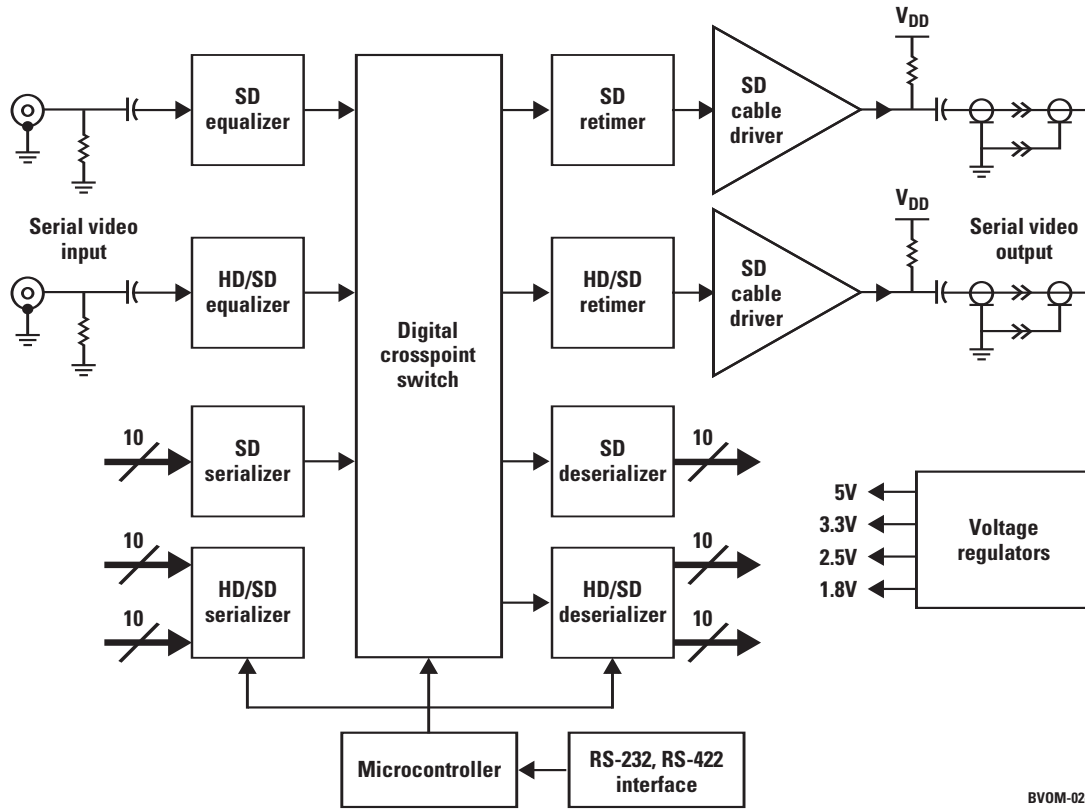
Figure 3.1. The serial digital video system

3.1 Adaptive cable equalizers

Data transmitted over a long length of cable at high data rates must be equalized in order to compensate for cable loss. Adaptive cable equalizers reconstruct serial digital data received from transmission lines such as coaxial cable or twisted pair. They do this by attempting to match the inverse of the cable loss characteristic, and adapting according to cable length. Figure 3.2 shows National's CLC014 adaptive cable equalizer in action.

Before equalization:
300m of Belden 8281 coaxial cable

Equalizer input (200 mV/div)

Data rate: 270 Mbps

Time (1ns/div)

After equalization:
300m of Belden 8281 coaxial cable

Equalizer output (200 mV/div)

Data rate: 270 Mbps

Time (1ns/div)

BV0M-025
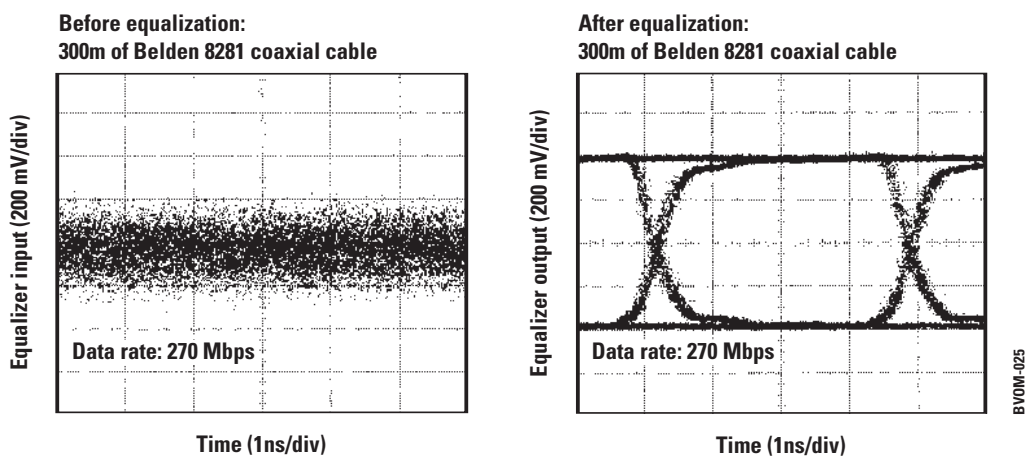
Figure 3.2. CLC014 in operation

3.1.1 Basic operation

Figure 3.3 shows the block diagram for an adaptive cable equalizer (National's CLC014). The equalizer block, consisting of two equalizing stages, receives the serial digital data. The output of this block is sent to the Quantized Feedback Comparator (QFBC), which determines the energy content and amplitude of the signal. The signal is also sent to an Output Eye Monitor (OEM) to view the output directly out of the equalizing filters. The signals before and after the QFBC are sent to the adaptive servo control block to create the control signal for the equalizer block. This sets the bandwidth and gain of the filters. A carrier detect and output mute signal are provided. Carrier detect and mute can be tied together to inhibit the output when no input signal is present.

Serial digital video integrated circuits
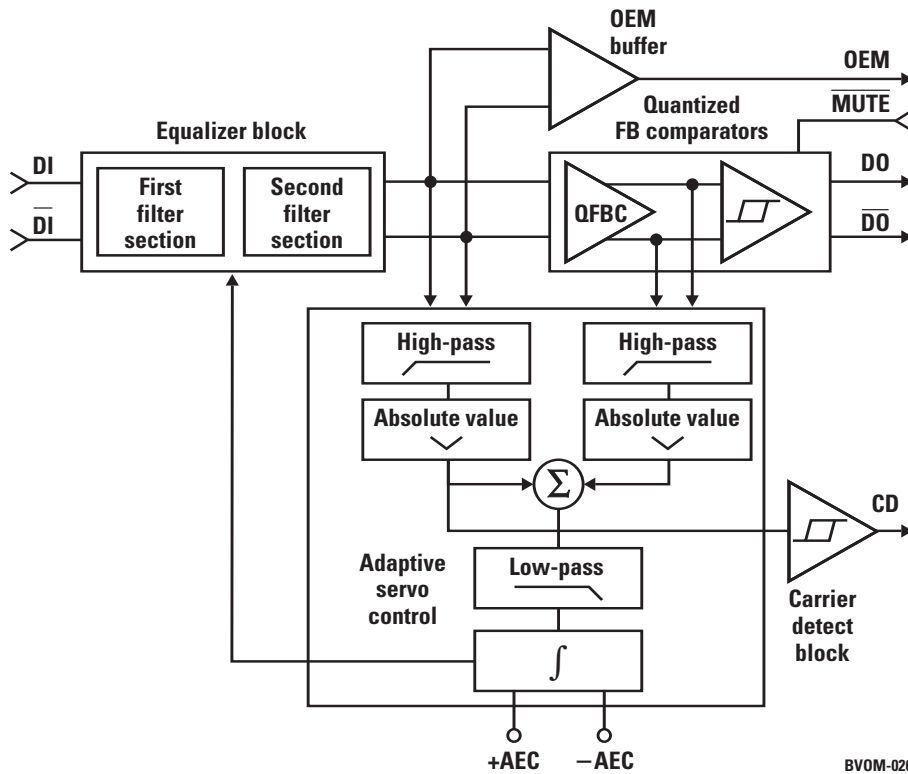
Figure 3.3. Cable equalizer block diagram (CLC014)

Table 3.1. Adaptive cable equalizers

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC014	Adaptive cable equalizer for for SMPTE 259M	5V	50 to 650	Carrier detect
CLC012	Adaptive cable equalizer for ITU-T G.703	5V	50 to 650	Loss of signal

3.1.2 CLC014

The CLC014 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristic). The CLC014 simplifies the task of high-speed data recovery with a single-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from 0m to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300m of Belden 8281 or 120m of CAT5 UTP (unshielded twisted pair).

3.1.3 CLC012

The CLC012 is identical to the CLC014 in every way except for the carrier detect function. The CLC014 is aimed at SMPTE 259M video applications and employs a simple carrier detect which indicates if a signal is present at the input. The CLC012 is intended for ITU-T G.703 telecom applications and employs a Loss-of-Signal (LOS) detection system that operates according to ITU-T G.775.

3.1.4 Typical application

Figure 3.4 shows a typical application circuit for the CLC014. The CLC014 receives the input from the cable. The input requires a 75Ω resistor to ground to terminate the cable. It is AC-coupled by a 1.0 μF capacitor, followed by a series 100Ω resistor. The open collector outputs are pulled up to V_{CC} via 75Ω resistors with an optional diode. Refer to the CLC014 datasheet for full details.
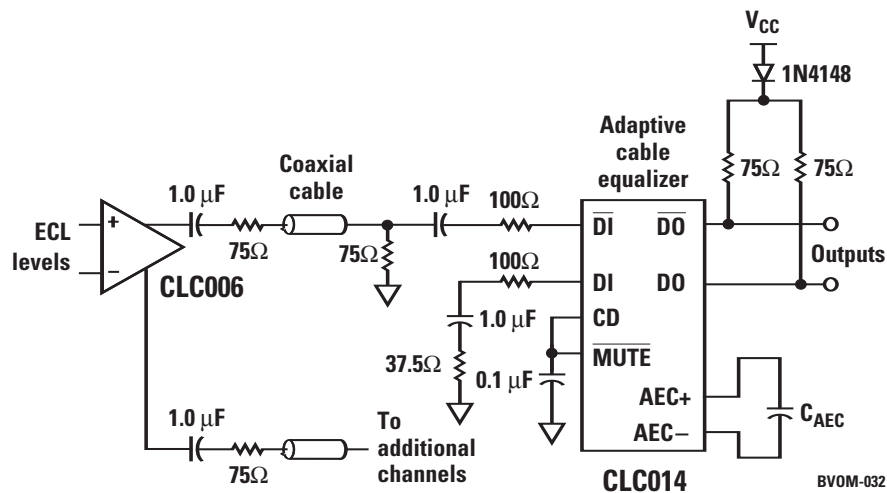
Figure 3.4. CLC014 typical application circuit

- The coupling capacitors must be large enough for the pathological signals. A value of 1 μF or higher is necessary to handle the large DC shifts and transitionless intervals present in serial digital video data.

- Transformer coupling should not be used because it alters the frequency spectrum of the signal. It does not preserve the low frequency energy content and it distorts the high frequency content. This causes the CLC014 to under-equalize, along with other unpredictable effects.

- The unused input requires an R-C network as shown in Figure 3.4. The purpose of the series R-C network in the unused input is to cause the common-mode noise canceling properties of the differential input stage to reject noise and other common-mode signals that may be induced into the input networks. Without equal impedances in both inputs there would be a net differential mode gain resulting from the different currents flowing in the input networks. A single 137Ω resistor may be used in place of the series connected 100Ω and 37.5Ω resistors in the R-C network.

- The CLC014 has open collector outputs that require 75Ω resistors connected to V_{CC} to create an output voltage (see Figure 3.5).

Serial digital video integrated circuits
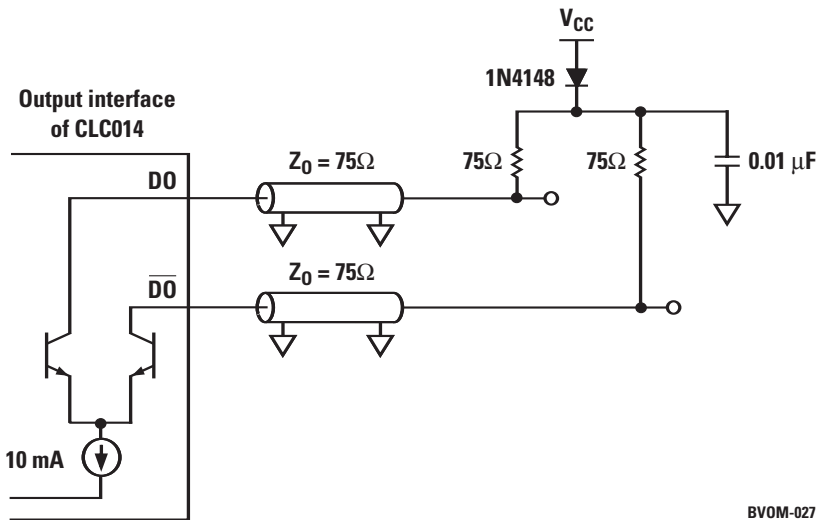
Figure 3.5. CLC014 output loading

- A diode or 75Ω resistor provides a voltage drop from the positive supply to establish proper ECL drive levels. The diode may not be needed if the device being driven has buffered ECL inputs with input levels that extend to V_{CC}. Refer to Table 3.2 for a list of SDV devices and whether they require the diode voltage dropping circuit to interface to the output of the CLC014.

Table 3.2. SDV dropping circuit requirements to interface to open collector outputs

Required	Not required
CLC005	CLC011
CLC006	CLC016
CLC007	CLC031
CLC018	

- The placement of the collector load resistors is important. They should be placed as close to the receiving device inputs as possible, preferably as the last component connected to the transmission line. These resistors serve two functions: 1) they provide collector current which sets the operating point and the voltage swing for the output transistors; and 2) they terminate the transmission lines to prevent signal distortion.

- The minimum supply voltage requirement on the CLC014's outputs is $V_{CC} - 1.6V$. This is necessary because the emitters of the output transistors are clamped at about $V_{CC}/2$, so the output resistors are cut off and will not produce a full output voltage swing if they are operated at a lower DC bias.

3.1.5 Equalizer application tips

3.1.5.1 Equalizer testing

All testing must be done using real coaxial cable. Cable clones should not be used as they can cause errors. The attenuation vs. frequency characteristic of cable clones can differ significantly from that of coaxial cable. Cable clones tend to pass excessive high-frequency energy. Since the CLC014 uses the high frequency portion of the input signal to determine how much equalization to apply, the use of cable clones can cause the CLC014 to under-equalize.

3.1.5.2 Equalizer layout

The CLC014 is a high-gain, wide-band, analog RF AGC (Automatic Gain Control) amplifier. Its successful application requires careful attention to circuit layout and PCB design. If the circuit or PCB design allows even a small amount of noise or crosstalk from other parts of the system or power supply to find its way into the input of the CLC014, then this signal is amplified. The following guidelines will help avoid this.

- Use ground and power planes in the PCB design. Place the main power and ground planes adjacent to each other in the stackup. Use the smallest practical dielectric thickness for this sandwich to produce the maximum possible inter-layer capacitance. This is your best possible RF bypass capacitance for the circuit. It is more effective than discrete RF bypassing because the component interconnect inductance is much less.

- Put a small capacitor, no more than 1 pF or 2 pF, directly across the input terminals of the CLC014. This is a low pass filter and helps eliminate high-frequency noise.

- Cut a ring around the CLC014 circuit in the ground plane, isolating it from adjacent circuitry. Do not make the ring continuous all around the circuit or it will no longer have a good ground connection, but three sides can easily be isolated.

- Put guard stripes (grounded traces) on either side of the input traces to the CLC014. A well-grounded guard ring around the input networks is also effective.

- Do not run other digital signals near the input traces of the CLC014. If this is necessary, make sure they are not parallel to the input traces to the CLC014.

- Arrange the layout so the input and output circuitry of the CLC014 are separated as much as possible. Also, the inputs and outputs should never be routed adjacent to each other.

- Provide a separate via for each power or ground pin of the CLC014. If possible, use two vias for each power or ground for even better RF performance. Never connect multiple power or ground pins together and to the planes using only a single via.

- Decouple each device with a 0.1 µF RF ceramic capacitor placed no more than 3 mm from the power pins. Also, decouple for low frequency with a 4.7 µF to 10 µF, 35V tantalum electrolytic capacitor placed near the ceramic capacitors. Tie the capacitors to the power planes with two vias at each end terminal.

The most common issue with the CLC014 is carrier detect (CD) being active in the absence of an input signal. In the vast majority of cases this is due to noise or coupling on the input caused by poor PCB design and layout. By following these guidelines and good RF and high-speed PCB layout techniques, you will be able to reduce the crosstalk and noise entering the CLC014 and prevent false CD indications.

3.1.5.3 Cable input signal characteristics

In order for the CLC014 to function properly, the input signal driven into the cable must conform to the requirements of SMPTE 259M:

- Amplitude: 800 mV ±10%

- Rise/fall times: 750 ps to 1,500 ps

When the cable input signal differs from this, the equalizer may not function as anticipated.

- **Cable input signal amplitude too large:** When an input signal greater than 800 mV is input to the cable, the cable appears to be shorter than it actually is and the CLC014 will under-equalize the signal.

- **Rise and fall times too fast:** Similarly, when an input signal has fast rise and fall times, the cable appears to be shorter than it actually is and the CLC014 under-equalizes the signal.

- **Cable input signal amplitude too small:** When the cable's input signal amplitude is low, the cable appears to be longer than it actually is and the CLC014 over-equalizes the signal.

- **Rise and fall times too slow:** A similar thing happens when an input signal has slow rise and fall times. Again, the cable appears to be longer than it actually is and the CLC014 over-equalizes the signal.

The output of the CLC014 comes from a comparator, so over- or under-equalization is not immediately apparent on the output. Characteristics that indicate when the equalizer is not properly equalizing are:

- The filter may be under-equalizing when the output of the filter exhibits slow slew rates. This will also cause increased jitter on the output. Duty cycle distortion can also result if there is an offset in the comparator.

- If the CLC014 is over-equalizing, the output of the filter may show double pulses. This is caused by excessive ringing on the output of the filter. Excessive noise on the outputs of the CLC014 can also result.

In the following scope photos, the upper trace is the CLC014 DO output; the lower trace is the CLC014 OEM output which is the output of the filter section before the quantized feedback comparator. In all three cases, the input signal is a 270 Mbps NRZ signal. Cable length is 50m of Belden 8281 coaxial cable.

Figure 3.6 shows the result when the original signal amplitude is 1,200 mV (1.5 nominal). The CLC014 is under-equalizing. Note the low slew rates in the OEM trace. Output jitter is also greater than optimal.

1.25 ns
200 mV

1.25 ns
50 mV

BVOM-033
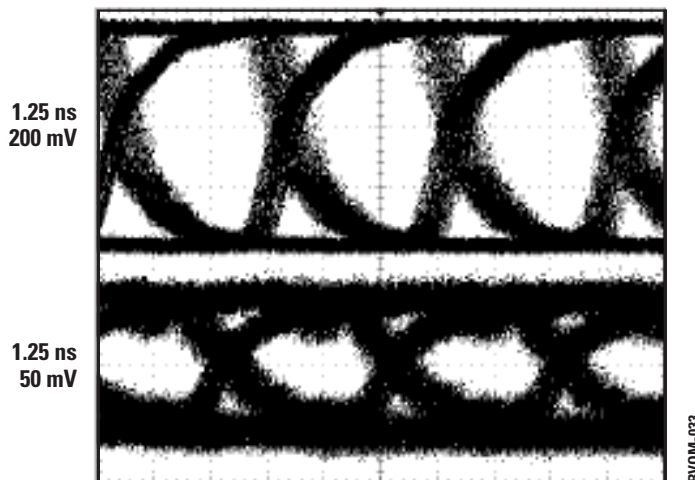
Figure 3.6. Input signal too large, under-equalized result

Figure 3.7 shows the part operating correctly with a cable input amplitude of 800 mV (the nominal level) and standard rise and fall times.

1.25 ns
200 mV

1.25 ns
50 mV

BVOM-064
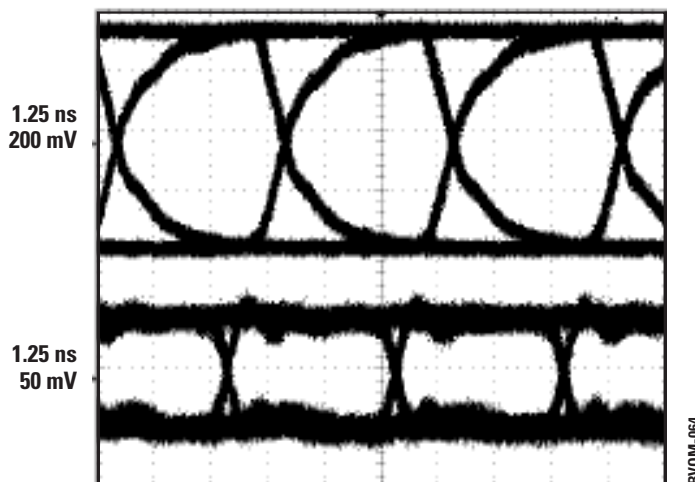
Figure 3.7. Nominal input signal amplitude

In Figure 3.8, the signal input to the cable is 300 mV and the CLC014 is over-equalizing. This causes ringing and overshoot in the OEM signal.

Serial digital video integrated circuits
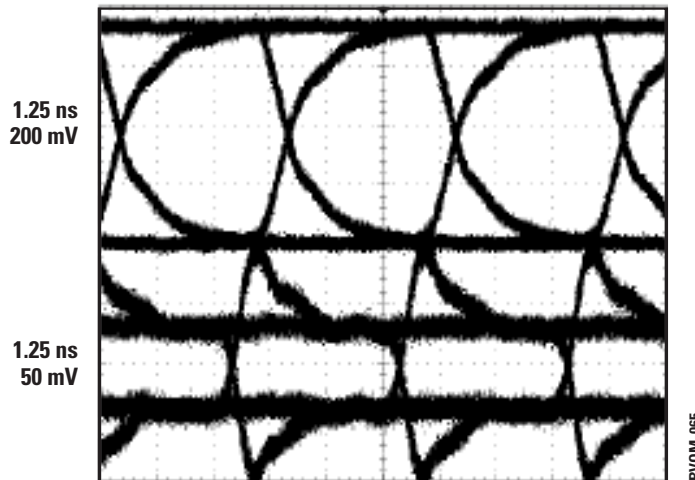
Figure 3.8. Input signal too small resulting in over-equalization

1.25 ns
200 mV

1.25 ns
50 mV

BVOM-065

3.2 Reclockers

Data reclockers/retimers reduce jitter and separate the clock and data in high-speed serial data applications. They re-establish proper bit widths and their correct relationship to the serial clock edges. Figure 3.9 shows National's CLC016 data reclocker in action.

CLC016 input

CLC016 data out

CLC016 clock out

BVOM-043
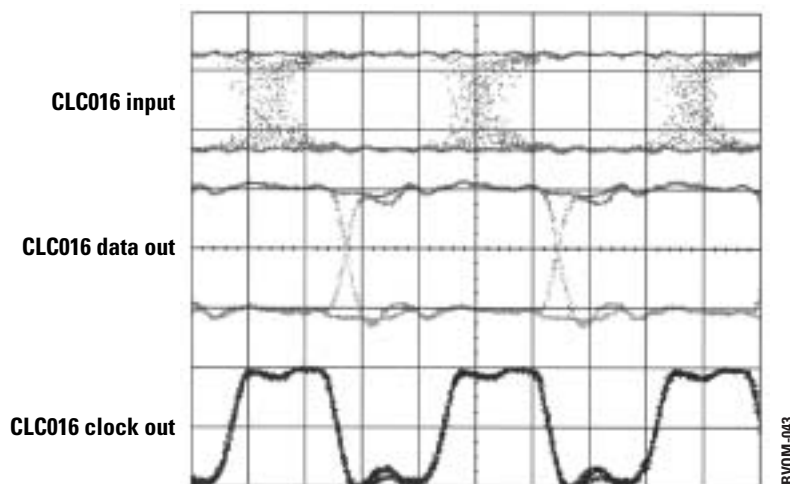
Figure 3.9. CLC016 in operation

3.2.1 Basic operation

Figure 3.10 shows the block diagram for a reclocker (National's CLC016). The frequency detector detects the difference between the input data rate and the VCO frequency and changes the VCO frequency to minimize this difference. As this difference approaches zero, the Phase Lock Loop (PLL) acquires lock, and the frequency detector is no longer active. The PLL, consisting of a VCO, phase detector, and external loop filter, recovers the low jitter clock. Auto Rate Select (ARS) consists of two modes: Auto Rate Mode (ARM) and Manual Rate Mode (MRM). ARM sequences through user-selected data rates until phase lock is reached, while MRM allows the user to select a fixed rate.
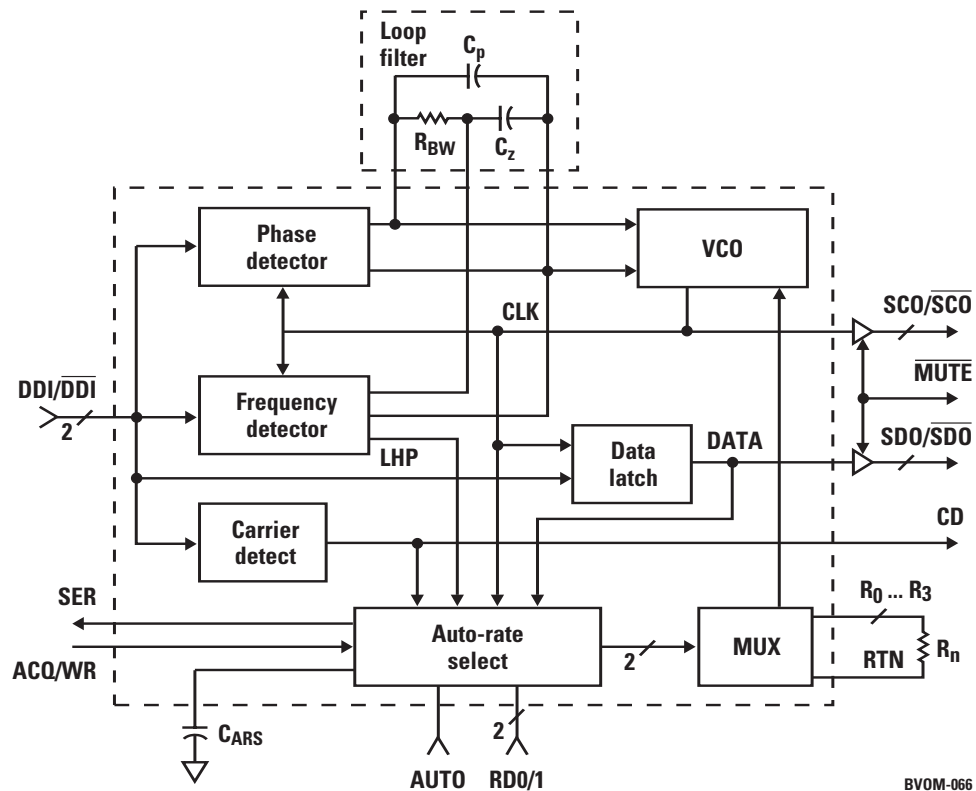
Figure 3.10. Data reclocker block diagram (CLC016)

Table 3.3. Reclocker

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC016	Data retiming PLL	5V	40 to 400	Automatic rate selection

3.2.2 CLC016

National's CLC016 is a cost-effective, monolithic, data retiming phase-locked loop (PLL) designed for high-speed serial clock and data recovery. The CLC016 simplifies high-speed data recovery in multi-rate systems by incorporating auto-rate select (ARS) circuitry on-chip. This function allows the user to configure the CLC016 to recognize up to four different data rates and automatically adjust to provide accurate, low-jitter clock and data recovery. A single resistor is used to set each data rate anywhere between 40 Mbps and 400 Mbps. No potentiometers, crystals, or other external ICs are required to set the rate. The CLC016 fully supports SMPTE 259M data rates as well as non-SMPTE data rates within its operating range.

3.2.3 Typical application

Figure 3.11 shows the typical application circuit for the CLC016. Refer to the CLC016 datasheet for further details.

Serial digital video integrated circuits
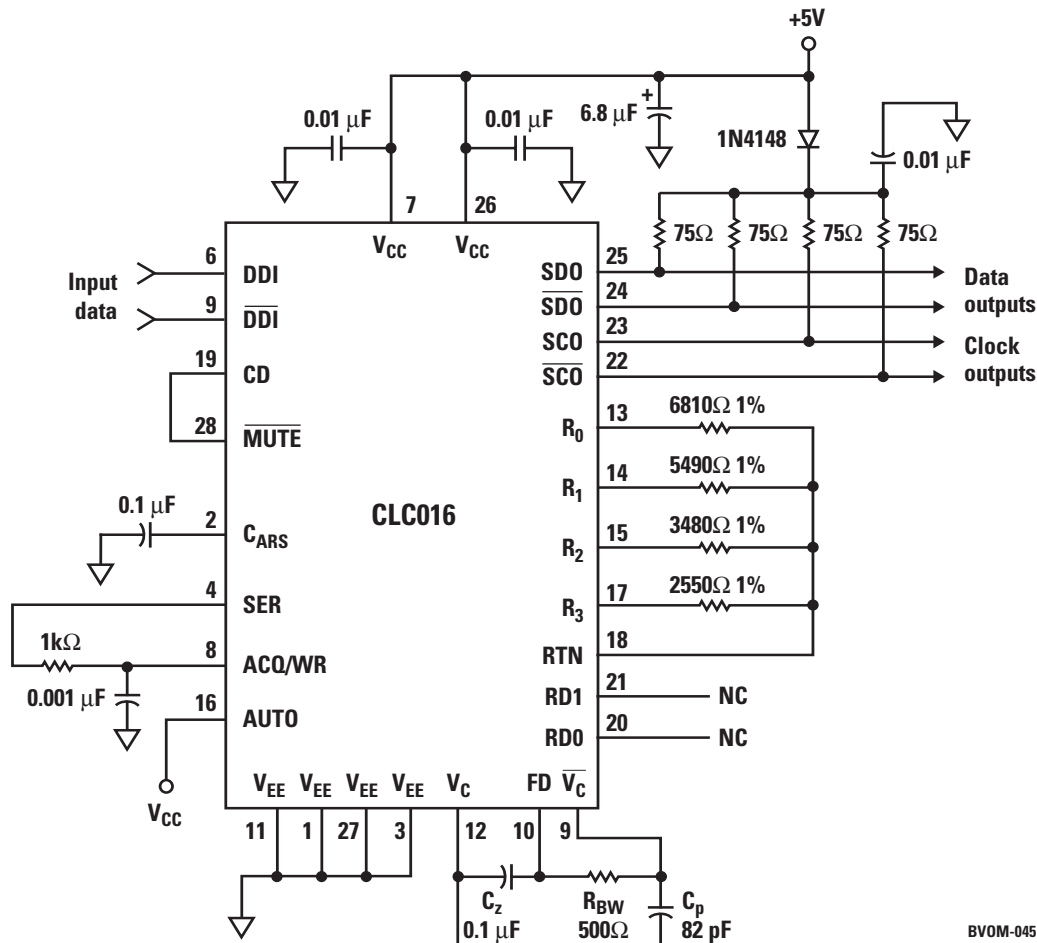
Figure 3.11. CLC016 typical application circuit

- The CLC016 has open collector outputs that require 75Ω resistors connected to V_{CC} to create an output voltage (see Figure 3.5).

- A diode or 75Ω resistor provides a voltage drop from the positive supply to establish proper ECL levels. The diode may not be needed if the device being driven has buffered ECL inputs with input levels that extend to V_{CC}. Refer to Table 3.2 for a list of SDV devices and whether they require the diode voltage dropping circuit or not to interface to the output of the CLC016.

- The placement of the collector load resistors is important. These should be placed as close to the receiving device inputs as possible, preferably as the last component connected to the transmission line. These resistors serve two functions: 1) They provide collector current which sets the operating point and the voltage swing for the output transistors; and 2) they terminate the transmission lines to prevent signal distortion.

- The minimum supply voltage requirement on the CLC016's outputs is V_{CC}-1.6V. This is necessary because the emitters of the output transistors are clamped at about V_{CC}/2, so the output resistors are cut off and will not produce a full output voltage swing if they are operated at a lower DC bias.

3.2.4 Reclocker application tips

3.2.4.1 Fixed rate mode

When attempting to lock the CLC016 to a single data rate, either:

- Use the same value resistor in all four frequency setting inputs.

- Use one input and tie the rest together.

- Use four different values, and set RD1 and RD2 to use to the desired resistor.

3.2.4.2 Loop filter tradeoffs

Narrower bandwidth makes it more difficult to lock to signals but produces lower residual jitter. Wider bandwidth improves jitter tolerance but increases residual jitter.

3.2.4.3 Locking to various data patterns

When using the CLC016 with data that has transitions on both the rising and falling edge of the clock such as Coded Mark Inversion (CMI), the CLC016 should be set for a data rate that is twice that of a similar NRZ encoded signal. For example, when using the CLC016 for 155 Mbps CMI encoded data, it should be set up as if the data rate were 311 Mbps.

3.3 Cable drivers

Cable drivers drive AC-coupled coaxial or twisted pair cable with ECL signal levels of 800 mV p-p ±10%.

Table 3.4. Cable drivers

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC001	Serial digital cable driver	3.3V	Up to 622	Adjustable output amplitude, LVDS- and LVPECL-compliant inputs
CLC005	ITU-T G.703 serial digital cable driver	5V	Up to 622	Adjustable output amplitude
CLC006	Serial digital cable driver	5V	Up to 400	Adjustable output amplitude
CLC007	Serial digital cable driver	5V	Up to 400	Dual complementary outputs

3.3.1 CLC001

The CLC001 is a high-speed cable driver designed for use in SMPTE 259M serial digital video and ITU-T G.703 serial data transmission applications. The CLC001 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 622 Mbps. Controlled output rise and fall times (400 ps typical) minimize transition-induced jitter. The output voltage swing is adjustable from 800 mV p-p to 1.0V p-p using an external resistor.

Serial digital video integrated circuits

3.3.2 Typical application

Figure 3.12 shows the typical application circuit for the CLC001. Refer to the CLC001 datasheet for further details.

BVOM-046
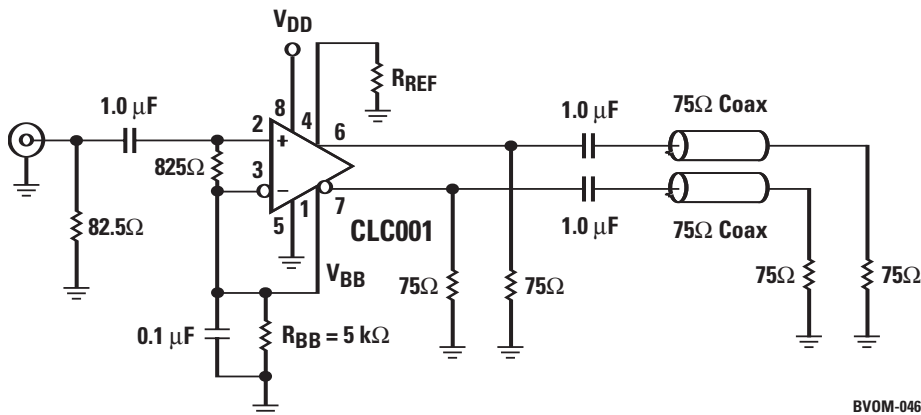
Figure 3.12. CLC001 typical application circuit

- Inputs can be PECL, LVPECL, or LVDS.

- Outputs are high-impedance current sources and require a 75Ω resistor to ground. Outputs must be AC-coupled for correct operation.

- The unused output should be terminated to ensure a balanced output drive. In the typical application circuit, the output sees 75Ω DC-wise and 37.5Ω AC-wise (during transitions). Use a 75Ω resistor to ground on the unused output to meet the DC condition.

3.3.3 CLC005/CLC006/CLC007

The CLC005, CLC006, and CLC007 are monolithic, high-speed cable drivers designed for the SMPTE 259M serial digital video transmission standard (CLC006 and CLC007) and the ITU-T G.703 serial digital data transmission standard (CLC005). They drive 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps (CLC005 up to 622 Mbps). Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing for the CLC006 and CLC007, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable. The output voltage swing for the CLC005 is typically 2.0V and delivers a 1.0V swing to the cable. The CLC005 and CLC006 feature adjustable output swings, while the CLC007 offers two sets of complementary outputs.

The CLC005, CLC006, and CLC007 all have similar operating characteristics. Figure 3.13 shows the typical application circuit for the CLC006.
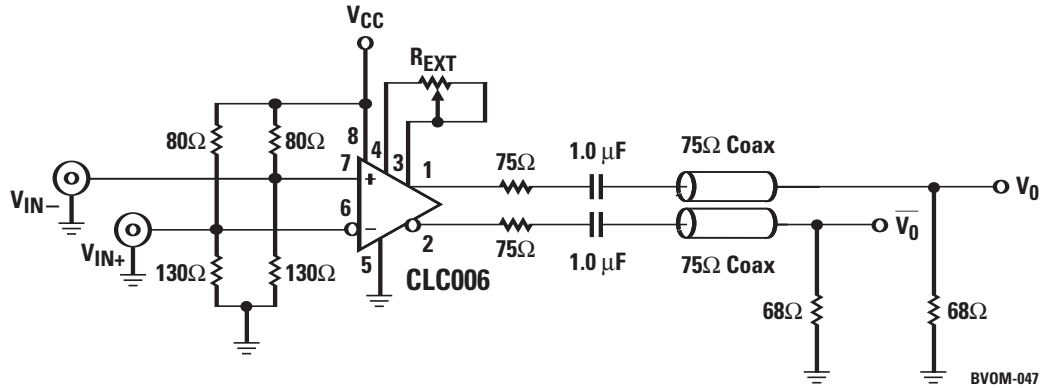
Figure 3.13. CLC006 Typical application circuit

- Inputs are standard ECL.

- Outputs are push/pull class AB and require a series back-matching resistor of 62Ω to 75Ω.

3.3.4 Cable driver application tips

The CLC001 is recommended for applications with data rates over 400 Mbps (up to 622 Mbps). The outputs of the CLC001 and CLC005 are similar at low data rates (311 Mbps and below). At higher data rates (400 Mbps and above), the difference in the quality of the outputs becomes noticeable. The CLC005 has higher output jitter in this range. The CLC001 has faster edge rates than the CLC005 to further enhance signal quality at high data rates. Rise and fall times are typically 400 ps for the CLC001, while they are 650 ps for the CLC005. Refer to Figures 3.14 and 3.15 for a comparison of the two outputs at 622 Mbps.

Time (500 ps/DIV)
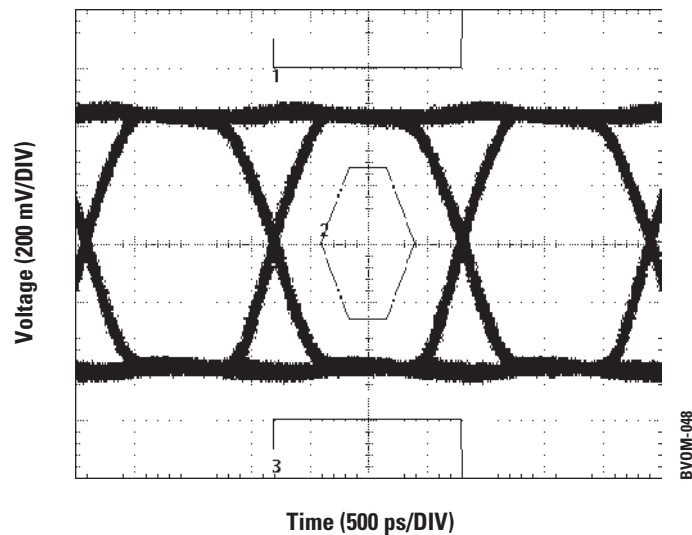
Figure 3.14. CLC001 at 622 Mbps

Serial digital video integrated circuits

Time (500 ps/DIV)
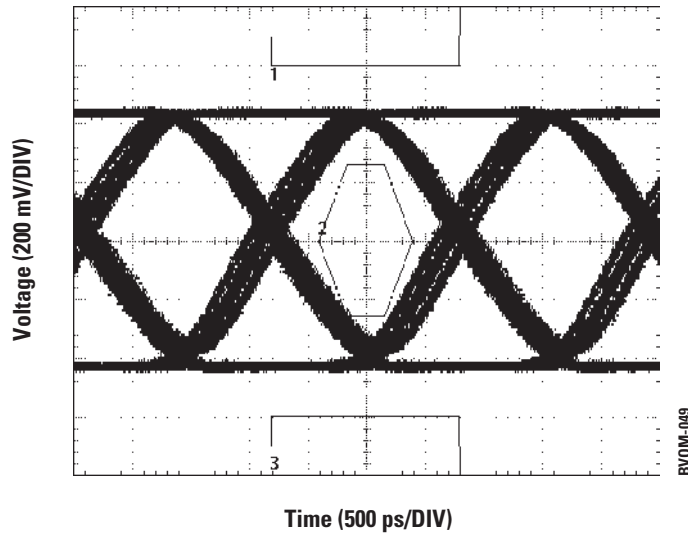
Figure 3.15. CLC005 at 622 Mbps

3.4 Serializers

Serializers are necessary for data transmission over a single coaxial cable. The signal must be modified prior to transmission to ensure that there are sufficient edges for reliable clock recovery, to minimize the low frequency content of the transmitted signal, and to spread the energy spectrum so that RF emission problems are minimized. SMPTE serializers handle all of these tasks; they encode, serialize, and transmit bit-parallel digital data conforming to the SMPTE standards. General-purpose serializers are used to serialize and transmit non-standard bit-parallel digital data without encoding.

3.4.1 Basic operation

Figure 3.16 shows the block diagram for a SMPTE serializer (National's CLC020). The parallel clock, P_{CLK}, is used to clock the parallel data into the input data register. The parallel data is sent to the SMPTE scrambler where it is scrambled by a mathematical algorithm. The PLL uses P_{CLK} as its reference to generate the appropriate frequency for the serial clock rate. This is used by the serializer and NRZI converter to serialize the data and encode it in NRZI. It is then sent to the cable driver for transmission.

Sync detect En.

D[9,0] & P$_{CLK}$

TPG En.

Input data register

TRS detector

TPG & BIST control

SMPTE scrambler

Power-on reset

P$_{CLK}$

PLL

Serializer & NRZI converter

SDO

Lock detect

Test out
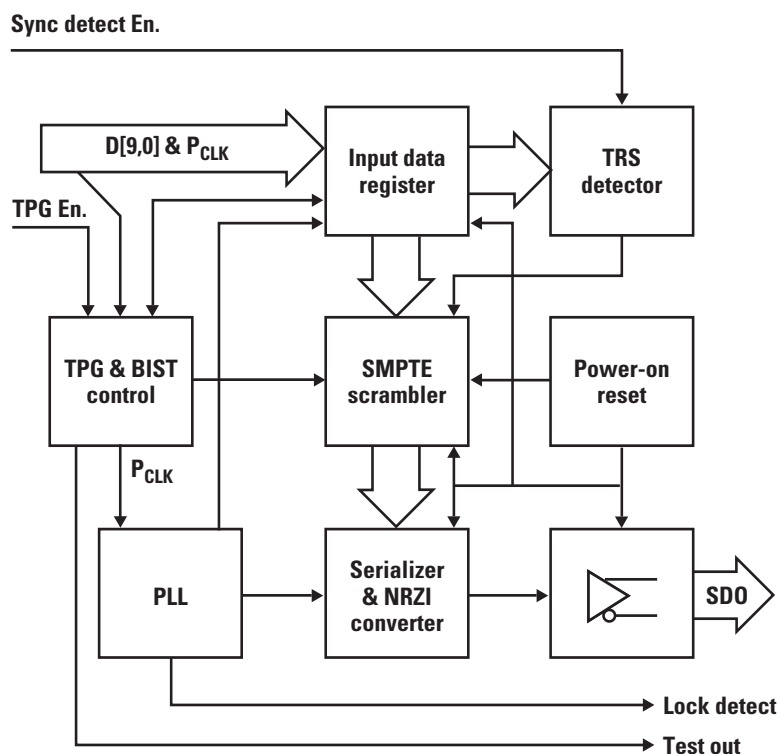
BVOM-050

Figure 3.16. SMPTE serializer block diagram (CLC020)

Table 3.5. Serializers

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC020	SMPTE 259M digital video serializer	5V	100 to 400	SMPTE 259M encoding, TPG, BIST, cable driving
CLC021	SMPTE 259M digital video serializer	3.3V or 5V	100 to 400	EDH generation and insertion
CLC030	SMPTE 292M/259M digital video serializer	3.3V/2.5V	270 to 1,485	SMPTE 292M/259M encoding, ancillary data handling, video FIFOs

Serial digital video integrated circuits

3.4.2 CLC020

The CLC020 is a single-chip SMPTE 259M SDV encoder with integrated cable driver. It encodes, serializes and transmits bit-parallel data conforming to SMPTE 125M and SMPTE 267M component video and SMPTE 244M composite video standards. It can also serialize general 8- or 10-bit parallel data. The CLC020 accepts parallel clock frequencies in the range from below 10 MHz to over 40 MHz. It outputs serial data at rates from below 100 Mbps to over 400 Mbps. An internal phase-locked loop (PLL) generates the serial data clock frequency. The PLL requires no external frequency setting, trimming or filtering components.

Functions performed by the CLC020 include:

- Parallel-to-serial data conversion
- SMPTE polynomial (X^9+X^4+1) data encoding
- NRZ to NRZI data format conversion
- Video test pattern generation and self-testing
- Serial clock generation and encoding with the serial data
- Coaxial cable driving

Input for sync (TRS) detection disabling and a PLL lock-detect indicator output are provided.

The CLC020 has a built-in self-test (BIST) and video test pattern generator (TPG) with four component video test patterns: reference black, PLL and equalizer pathologicals, and modified color bars. (Pathological data patterns are used as stress-testing functions in SDV systems). Test patterns are available in 4:3 and 16:9 raster sizes and both NTSC and PAL formats. Separate power pins for the output driver, PLL, and the digital logic improve power supply rejection, jitter and noise performance.

3.4.3 CLC021

The CLC021 is a companion device to the CLC020 that includes all of the functions of the CLC020 as well as providing EDH generation and insertion, and the capability to independently control each of the sub-functions of the device.

3.4.4 Typical application

Figure 3.17 shows the typical application circuit for the CLC020. Refer to the datasheet for product-specific details.

BVOM-051

Figure 3.17. CLC020 typical application circuit

- Inputs are CMOS/TTL-compatible.

- Outputs are high-impedance current sources and require a 75Ω resistor to ground. Outputs must be AC-coupled for correct operation.

- The unused output should be terminated to ensure a balanced output drive. In the typical application circuit, the output sees 75Ω DC-wise and 37.5Ω AC-wise (during transitions). Use a 75Ω resistor to ground on the unused output to meet the DC condition.

Serial digital video integrated circuits

3.4.5 CLC020/CLC021 application tips

3.4.5.1 V_{DD} and parallel clock

The parallel clock (P_{CLK}) should not be applied before the CLC020 or CLC021 is powered up, unless the manual reset is used (CLC021 only). In the case of the CLC020, the P_{CLK} should not be asserted until at least 30 μs after power-on. The same is true for the CLC021, unless the manual reset is used. If manual reset is used during power-on, then the P_{CLK} may be asserted at any time as long as manual reset is not de-asserted until the part is fully powered.

3.4.6 CLC030

The CLC030 is a monolithic integrated circuit that encodes, serializes and transmits bit-parallel digital video data conforming to SMPTE 125M and 267M standard-definition, 10-bit wide component video and SMPTE 260M, 274M, 295M and 296M high-definition, 20-bit wide component video standards. The CLC030 operates at SMPTE 259M serial data rates of 270 Mbps, 360 Mbps, the SMPTE 344M (proposed) serial data rate of 540 Mbps; and the SMPTE 292M serial data rates of 1.483 and 1.485 Gbps. The serial data clock frequency is internally generated and requires no external frequency setting, trimming or filtering components.

3.4.7 Typical application

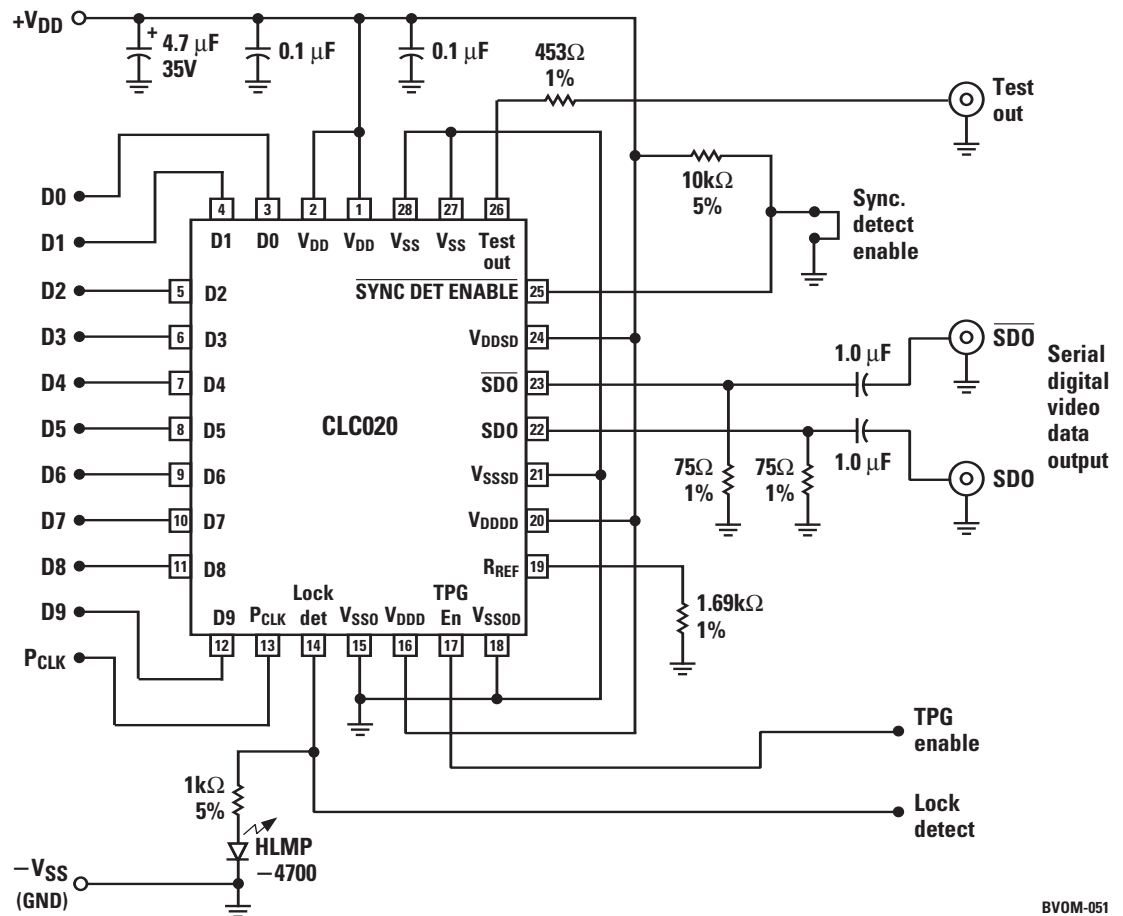Figure 3.18 shows the typical application circuit for the CLC030. Refer to the CLC030 datasheet for further details.

Figure 3.18. CLC030/CLC031 typical application circuit

3.4.8 CLC030 application tips

3.4.8.1 Processing non-supported raster formats

The following guidelines concerning device setup are provided to aid the user in configuring the CLC030 to attempt limited processing of non-supported raster formats. In general, the device is configured to defeat its format and TRS detection function and to limit operation to a general HD format type. (The user should consult Table 4 in the datasheet for guidance on the format groups similar to the non-supported one to be processed). Since most non-supported formats are in the HD realm, the CLC030 should be configured to operate in HD-ONLY mode by setting bit-5 of the FORMAT 0 register (address 0Bh). Also, the device should be further configured by loading the FORMAT SET [4:0] bits of this register with the general HD sub-format code. The complete data word for this general HD sub-format code with HD-ONLY bit set is 3FFh. Since this format differs from those in the table, the EAV/SAV indicators are disabled. Without these indicators, line numbering and CRC insertion are disabled and ancillary data insertion will not function. Pre-processing of the parallel data ahead of the CLC030 will be required to insert CRC data and line numbering.

3.5 Deserializers

Deserializers receive, decode, and descramble serial digital video signals. In the serial digital transmission system, the clock is contained in the data. If a separate reclocker is not used, then the deserializer is required to extract the clock as well. SMPTE deserializers decode and descramble serial digital video signals conforming to the SMPTE standards. General-purpose deserializers are used to deserialize non-standard serial digital datastreams without decoding.

3.5.1 Basic operation

Figure 3.19 shows the block diagram for a deserializer (National's CLC031). A serial rate clock is recovered from the NRZI signal edges. The deserializer then descrambles the data using an algorithm complementary to the scrambling algorithm and outputs a 10- or 20-bit data stream at the parallel rate.

Serial digital video integrated circuits

XTAL/ext clk

XTALo

SDI

SDI

R$_{BB}$

R$_{REF}$

Reference clock/oscillator

Input data samplers clock/data recovery

SDI bias

SMPTE NRZI-NRZ converter descrambler/ deserializer

P$_{CLK}$

De-dithering

AD [9:0]

A$_{CLK}$

RD/$\overline{WR}$

ANC/$\overline{CTRL}$

Ancillary data FIFO

Configuration & control registers

I/O [7:0]

Multi-function I/O port

Reset

Reset control

P$_{CLK}$

Int reset

Master bus

Video data bus

PLL/clock system

BIST & TPG

TRS & format detector

EDH/CRC generators/ checkers

Framing control

Video data FIFO & output

DV [19:10]

DV [9:0]

V$_{CLK}$

System master controller

BVOM-053

Figure 3.19. Deserializer block diagram (CLC031)

Table 3.6. Deserializers

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC011	Serial digital video decoder	5V	100 to 400	Data decoding and deserializing
CLC031	SMPTE 292M/259M digital video deserializer	3.3V/2.5V	270 to 1,485	SMPTE 292M/259M decoding and deserializing

3.5.2 CLC011

The CLC011 decodes and descrambles SMPTE 259M standard serial digital video datastreams with serial clock into 10-bit parallel words and a corresponding word-rate clock. SMPTE 259M standard parallel data is encoded and scrambled using a 9-bit shift register and is also converted from NRZ to NRZI. The CLC011 restores the original parallel data by reversing the encoding process. The CLC011 also extracts timing information embedded in the SDV data. These reserved code words, known as TRS, indicate the start and end of each active video line. By decoding the TRS, the CLC011 correctly identifies the word boundaries of the encoded input data.

3.5.3 Typical application

See the datasheet for details.

- The outputs of the CLC011 may be programmed for any voltage level between 3.0V and 5.5V by using the V_{DP} and V_{CP} pins. The data and clock may be set to separate voltage levels.

3.5.4 CLC011 application tips

- The CLC011 only recognizes TRS characters that comply with SMPTE 259M. The SMPTE 259M TRS sequence is 3FFh, 000h, 000h. The fourth word of the TRS sequence, the XYZ word, contains information about the signal.

- In a non-SMPTE application, an initialization pattern of 3FFh, 000h, 000h should be sent to sync up the CLC011. Then the frame enable (FE) input on the CLC011 should be taken to a low state, which will prevent it from realigning the word boundary if it sees this pattern again in the data being transmitted.

3.5.5 CLC031

The CLC031 SMPTE 292M/259M digital video deserializer is a monolithic integrated circuit that deserializes and decodes SMPTE 292M, 1.485 Gbps (or 1.483 Gbps) serial component video data, to 20-bit parallel data with a synchronized parallel word-rate clock. It also deserializes and decodes SMPTE 259M, 270 Mbps, 360 Mbps and SMPTE 344M, 540 Mbps serial component video data, to 10-bit parallel data. Functions performed by the CLC031 include: clock/data recovery from the serial data, serial-to-parallel data conversion, SMPTE standard data decoding, NRZI-to-NRZ conversion, parallel data clock generation, and automatic video format determination.

3.5.6 Typical application

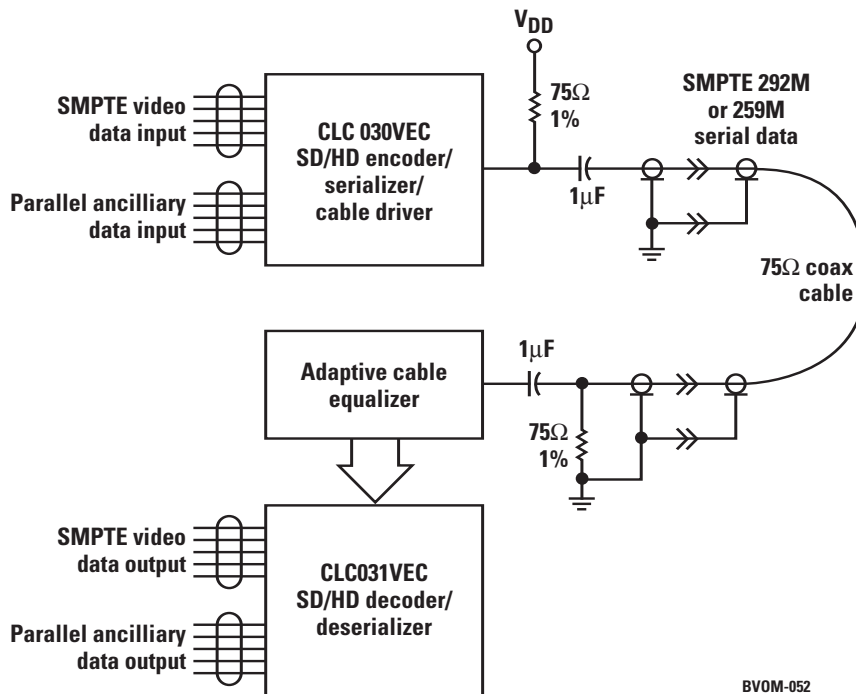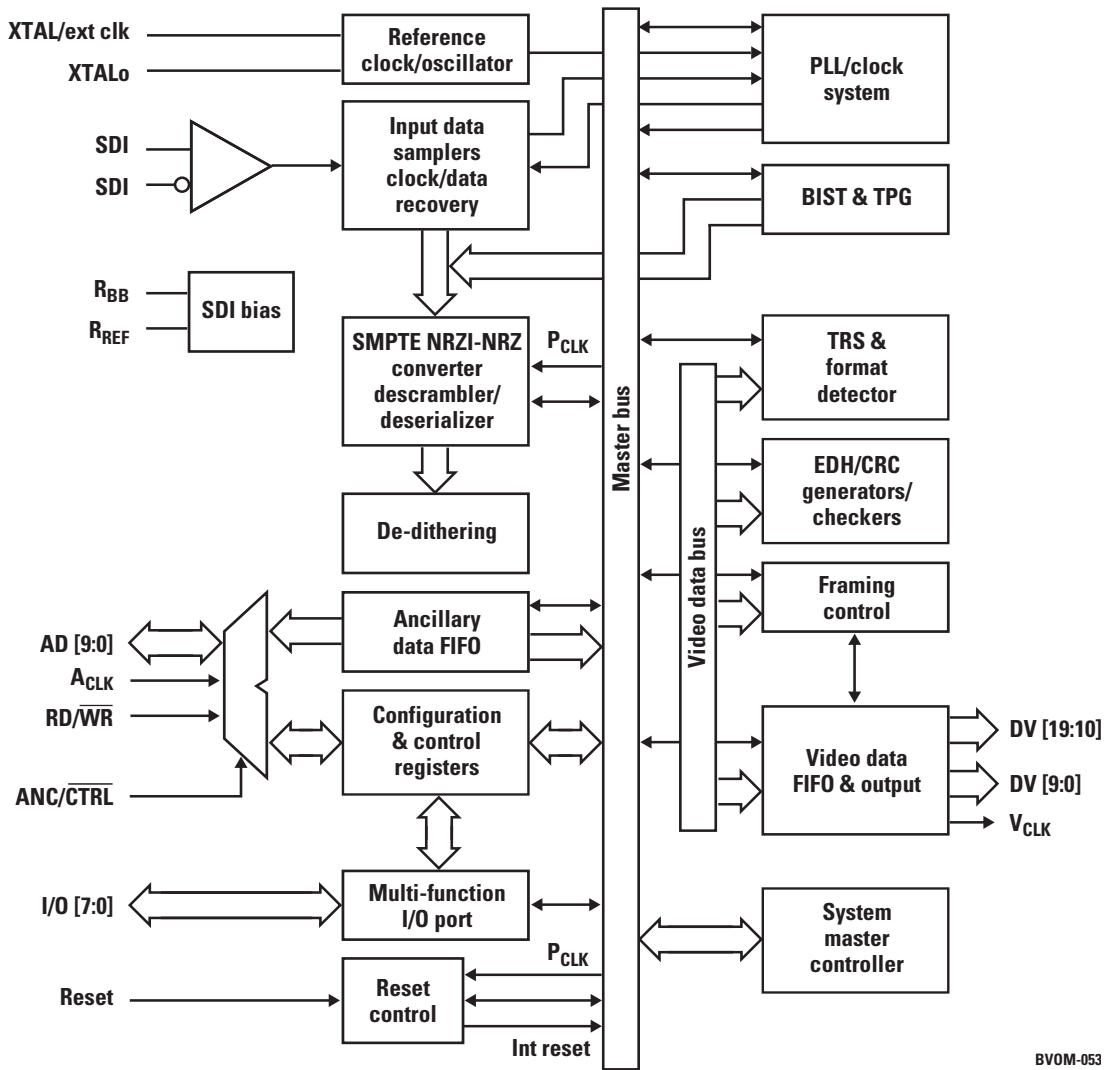Figure 3.18 shows the typical application circuit for the CLC031. Refer to the CLC031 datasheet for further details.

3.5.7 CLC031 application tips

3.5.7.1 Processing non-supported raster formats

In general, the device is configured to defeat its automatic format detection function and to limit operation to a general HD format. (The user should consult Table 4 in the datasheet for guidance on the format groups similar to the non-supported one to be processed). Since most non-supported formats are in the HD group, the CLC031 should be configured to operate in HD-ONLY mode by setting bit-5 of the FORMAT 0 register (address 0Bh). Also, the device should be further configured by loading the FORMAT SET [4:0] bits of this register with the general HD sub-format code. The complete data word for this general HD sub-format code with HD-ONLY bit set is 3FFh. Since this format differs from those in the table, the EAV/SAV indicators are disabled. Without these indicators, line numbering and CRC processing are disabled and ANC data extraction will not function. Output video chroma and luma data will be word-aligned. Post-processing of the parallel data output from the CLC031 will be needed to implement CRC checking or line number tracking.

3.6 Crosspoint switches

Television production and telecommunications facilities share much in common — both make use of large signal switching and routing systems. Serial digital video routers handle continuous streaming data, whereas, in telecommunications systems the data is mostly packetized. Similar digital crosspoint switches serve equally well in both applications.

3.6.1 Basic operation

Figure 3.21 shows the block diagram for a digital crosspoint switch (National's CLC018). Its non-blocking architecture utilizes eight independent 8:1 multiplexers to allow each input to be independently connected to any output, and any input to be connected to multiple (multicast) or all (broadcast) outputs.
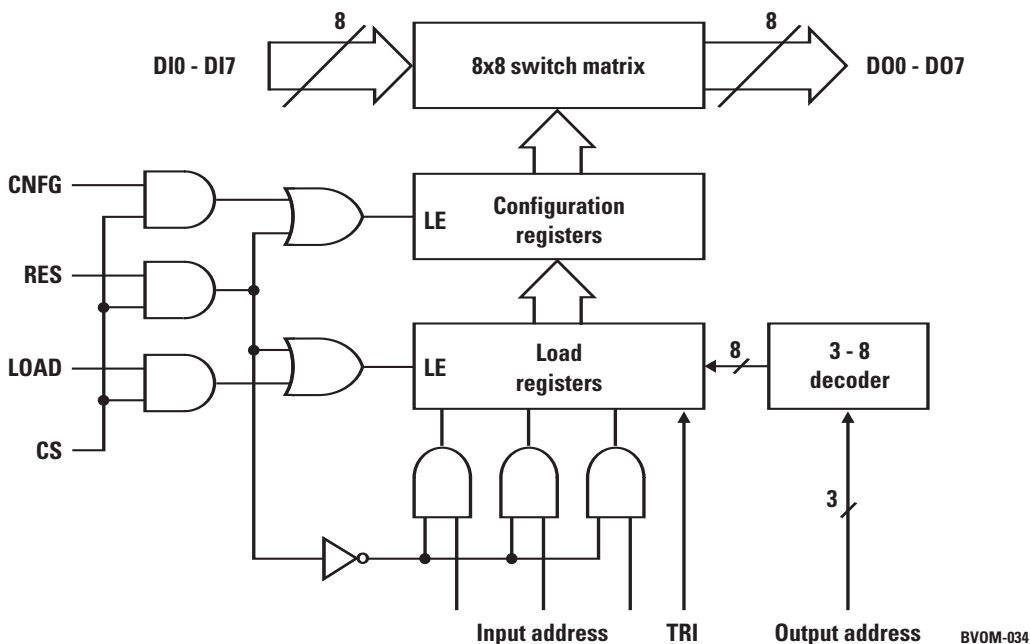
Figure 3.21. Crosspoint block diagram (CLC018)

Table 3.7. Crosspoint switches

Part number	Description	Supply voltage	Data rate (Mbps)	Features
CLC018	8x8 digital crosspoint switch	5V	Up to 1,485	Non-blocking, expandable
DS90CP22	2x2 LVDS crosspoint switch	3.3V	Up to 800	LVDS/LVPECL-compatible inputs
DS90CP04	4x4 LVDS crosspoint switch	2.5V	Up to 2,500	LVDS/LVPECL/CML-compatible inputs
SCAN90CP02	2x2 LVDS crosspoint switch with JTAG	3.3V	Up to 1,500	Pre-emphasis and JTAG

3.6.2 CLC018

The CLC018 digital crosspoint switch is a fully differential, 8x8, non-blocking architecture capable of operating at data rates to 1.5 Gbps. With its multiplexer-based architecture, any input may be simultaneously connected to one or more outputs and any output may be connected to any input. Each output may also be placed independently in TRI-STATE® mode. This permits simple expansion to larger switch arrays.

The CLC018 employs a double-row control signal latch architecture. This permits background switch array reprogramming and one-step configuration of the entire array. Two reset modes are provided: broadcast, where all outputs are connected to DI0, and TRI-STATE, where all outputs are disabled. Also note that inputs are fully differential and output drivers are open collector and are ECL/PECL-compatible.

Chapter 4
System testing

4.1 Digital video system testing

Despite the fact that the data is digital, most DTV system testing relies on analog means and equipment. This is done for operator familiarity and convenience. Video may be "digital" but it originates from cameras, film, and computers. The main difference is that the analog video is converted early in the chain into digital or numeric representation. Since many picture parameters have basically the same meaning, differing only as analog and digital representations, it is natural to convert the digital data into analog format for many testing functions and for direct viewing. The objective is to assure that the video and other data is being correctly processed, stored and transported.

4.1.1 Test equipment

The basic pieces of test equipment needed to test and monitor a DTV system are a signal generator, a video analyzer or waveform monitor and a picture monitor. Oscilloscopes are also useful for troubleshooting and viewing the signals of SDV systems.

4.1.2 Signal generation

The generator provides a set of standardized test signals and test patterns having precisely controlled signal characteristics like signal amplitudes, data and formats. These test signals are commonly the digital representations of traditional analog test signals such as color bars, luminance sweeps and sine-squared pulse and bar. For the unique test situations associated with digital video data systems, other test patterns have been added such as the equalizer and PLL pathological stressing patterns. Signal amplitudes and other characteristics are prescribed in the SMPTE or ITU-R standards. The digital transport signals are based on ECL-like levels of 800 mV p-p and risetimes of 400 ps to 1.5 ns (SD) and <270 ps (HD). The transport system impedance is 75Ω.

4.1.3 Signal and data analysis

Analog video systems tend to degrade gracefully in linear fashion to the point where the degradation becomes noticeable in the picture and sound. Digital systems, on the other hand, tend to be robust up to the point of failure where errors become visible or audible. These considerations have produced the video analyzer that bridges both analog and digital domains. The video analyzer performs the more traditional function of a waveform monitor and the added function of a data analyzer. These instruments monitor the signal and indicate signs of degradation. They also provide a means of viewing the digital data itself.

The video system, whether analog or digital, is a unity-gain signal environment. This allows design of systems for optimum signal-to-noise performance and simple interfacing of signal sources and receivers. Maintaining the correct amplitude level of the digital transport signal that is, in fact, a series of analog voltage changes, is vital to being able to receive that signal across the transport layer which is also analog. The video analyzer acts as a specialized oscilloscope to allow viewing the transport signal and to measure its amplitude, amplitude overshoot, rise time, fall time, jitter, data unit interval and other parameters. In doing these functions, the analyzer employs a representation of overlapping high and low data intervals called an "eye diagram". Some analyzers include synchronizing functions to the digital data that permit identification of errors originating in specific portions of the picture.
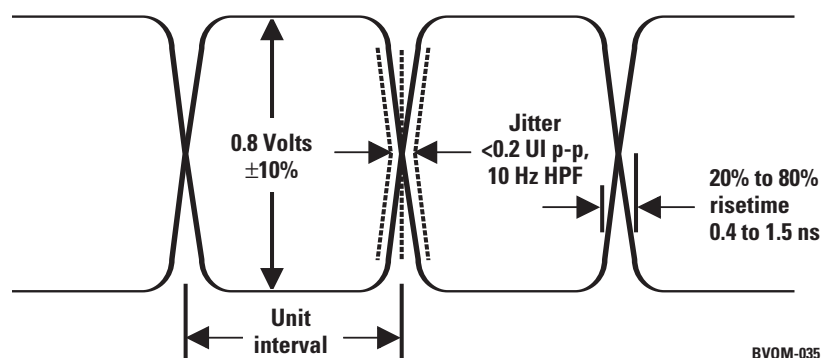
Figure 4.1. Measurements using the eye diagram

Analyzers may also have analog conversion tools such as vector displays and "Lightning" (Tektronix) displays. These permit the interpretation of the digital luminance and chrominance data in terms of their equivalent analog levels and timing.

4.1.4 Eye pattern testing

The eye pattern is an oscilloscope display of the analog digital data transport signal. The parameters normally measured by the eye pattern display are signal amplitude, risetime and overshoot. The receiving system must reliably detect the signal high and low levels to give error-free real-time measurements. The eye pattern is measured and displayed as received without equalization and hence, is usually made near the signal source to avoid noise and frequency rolloff.

The unit interval (UI) is the time between two adjacent signal transitions. The time is the reciprocal of the transport clock frequency. One UI for SMPTE 259M is 3.7 ns and for SMPTE 292M is 673.4 ps. Serial receivers should detect signal polarity near the center of the eye where noise and jitter effects are minimized. Testing attempts to reveal any defects of the received signal that close the eye. Since very low error rates are needed for correct SDV transmission, the eye opening should be as large and clean after equalization as possible under the applicable standard. The amount of jitter allowed in SDV systems is 0.2 UI, 740 ps for SD and 134.6 ps for HD. Though most systems are designed with enough margin to operate reliably with larger amounts of jitter, there is a point where failure occurs. Keeping jitter to a minimum is important for system reliability.

Signal amplitude is monitored to assure that there is sufficient transmitted amplitude so that the equalizer will respond correctly to the received level. The rise time and fall time are monitored at the 20% and 80% levels. Incorrect transition times can indicate signal distortion, ringing or overshoot if too fast, or eye closure if too slow. Overshoot can be the byproduct of fast transition times but more often indicates poor termination or transmission system impedance discontinuities.

System testing

4.1.5 Digital stress testing

As mentioned previously, digital systems tend to be robust right up until they fail. Unfortunately, there are no viable in-service tests that will measure the available margin in the digital system. In order to assess the available margins, the equipment must be taken off line. The amount of change needed to produce a particular failure is the measure of the margin. The simplest type of stress testing that can be done on an SDV system is by adding cable until errors are produced. Other means would be to change signal amplitude or rise time, or add noise or jitter to the transport signal. These tests challenge the receiver characteristics, especially the cable equalizer and reclocker. There is ample evidence to support the results obtained by cable length testing when done using one or more of the stressing data patterns (pathologicals). The pathological test patterns are usually combined into a single pattern as described in SMPTE RP 178 for SD or RP 198 for HD.

Cable length stress tests can be easily performed using actual video coaxial cable. The most important parameter to be measured is the point where the system crashes. From there, adding or removing small increments of cable will determine the characteristic of the error curve.

4.1.6 The SDI check field

The SDI check field or pathological signal is a full-field signal. Testing using this signal is done on equipment that is not in service. The two component data portions of the check field are designed to stress the cable equalizer and the PLL. The equalizer stress test data consists of a sequence of 19-bit intervals of one polarity followed by a single-bit interval of the opposite polarity. The pattern persists for the duration of the video line. This data pattern produces a large DC component that stresses the analog signal handling capability of the receiver and transmission system. When viewed, the picture produced is a shade of mauve or purple.
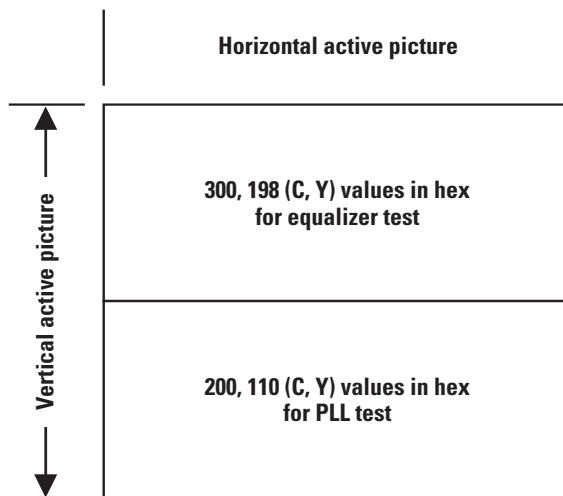
BVOM-036

Figure 4.2 SDI checkfield

The PLL stressing function consists of a signal having 20-bit intervals of one polarity followed by 20 of the opposite polarity. This produces a minimum number of transitions that are used by the receiving system PLL for transport clock extraction. The displayed color is a dark grey.

The SDI check field is a legal test signal only for component digital and not for composite digital video systems.

4.1.7 EDH and CRC error testing

For high-definition systems a cyclic redundancy check or CRC system is used to mark error occurrence. Each video line has a CRC inserted at its end by the transmitter. The receiver checks the CRC and can report any errors to a host or maintenance system.

Standard-definition systems can use an error reporting system called Error Detection and Handling (EDH). Operation of this method is covered in detail in SMPTE RP 165. This system compiles CRC information for specific portions of active picture, full field and ancillary data parts of the video signal. The CRCs are contained in an ancillary data packet inserted in a specific location in the vertical switching interval.

4.1.8 Jitter testing

The transport clock is encoded with the data in SDV systems. This clock must be recovered by the receiving system. This must also be done by the SDV test system analyzer if it is to measure the signal parameters. A PLL is commonly used to detect and lock to transitions in the data stream. Several methods have been proposed to recover the transport clock for use as a test reference. These methods are covered in SMPTE RP 192. Specifics relating to jitter in bit-serial digital video systems are discussed in RP 184. There are two classes of jitter that are important in SDV systems: timing jitter and alignment jitter.

Timing jitter is the deviation from the ideal timing of significant instances of the digital signal, such as zero-crossings, relative to an ideal, jitter-free clock and above some low frequency (usually 10 Hz). Usually the measurement system generates a clock that has been heavily filtered to reduce its intrinsic jitter components.

Alignment jitter (also called relative jitter) is the deviation in time of the significant instants of the digital signal relative to a hypothetical clock recovered from the data signal itself. This recovered clock should track the signal up to the extent of its upper clock recovery bandwidth, typically in the region of about 1 kHz to 100 kHz. Alignment jitter measurement includes jitter terms above this frequency. Alignment jitter is an indicator of the degradation of signal-to-latch clock timing margin.

4.2 The role of built-in self-test in SDV devices and systems

Bringing chip and video system testability to the target system were adopted as design priorities early in the development program of National's first standard-definition digital broadcast video encoder product (CLC020) Functional verification of such devices presents significant challenges both in development testing, production testing and system-application testing. The baseband broadcast digital video data environment is complex and can benefit from built-in testability. Extending the concept of self-testability into the realm of the target application enhances the product and adds value to its role in the system application. This concept has been continued in the CLC021 serializer for SDTV, and the CLC030 serializer and CLC031 deserializer products for HDTV broadcast equipment.

The internal test pattern generator (TPG) used in these products produces four test patterns for each supported SD and/or HD, NTSC and PAL format: a 75%, eight-vertical-color-bar pattern; a full-field equalizer pathological; a full-field PLL pathological and a full-field black raster. The CLC030 and CLC031 added an algorithmic means of generating optional transition coding in the color bar luma and chroma data. The internal self-test circuitry uses CRC (for HD) or EDH (for SD) test techniques described in SMPTE 292M or SMPTE RP 165. Two patterns were selected to act as SD test data, NTSC color bars and the PAL PLL pathological. All HD test patterns are built-in self-test (BIST) patterns. The CRC or EDH circuitry computes check words as the data is applied to the internal circuits of the device. These check words are compared to pre-stored values at the conclusion of the test interval to determine if the device is functioning correctly. The entire system including the CRC or EDH circuitry and the pre-stored check words is thereby self-testing. If any part of the process or data does not agree or produce the desired result, there is a fault in the device. The output of the TPG is available for use in system-level testing. The TPG can also serve as a basic stand-alone generator in a variety of digital video applications.

System testing

4.2.1 Digital video data basics

Baseband HDTV data transmission illustrates the benefits of BIST. HDTV employs serial data rates of 1.483 Gbps and 1.485 Gbps and parallel data rates up to 74.25 MHz. These operating data rates by themselves do not present an insurmountable test challenge. However, there are other complicating factors like the polynomial scrambling and transition minimization techniques used in the data encoding and decoding process. Done to benefit physical layer transmission, this encoding makes direct validation between original unencoded parallel data and encoded transmitted serial data difficult without use of external discrete test instruments. Native code BIST can remove some of the burden of reliance on external test equipment for reliable HDTV system testing.

For these devices, an algorithmic means was developed to produce the DTV data which reduces data storage. The size of the data for one frame of a typical HDTV picture is about 10M-words of 10-bit length. Video system test data is normally a static picture such as color bars, a luminance sweep or a system stressing function such as a pathological. This test data set models the picture data conditions to determine the operational readiness, and test the robustness of DTV data systems. To illustrate, a portion of a HDTV parallel data stream for a video line is shown in Figure 4.3.
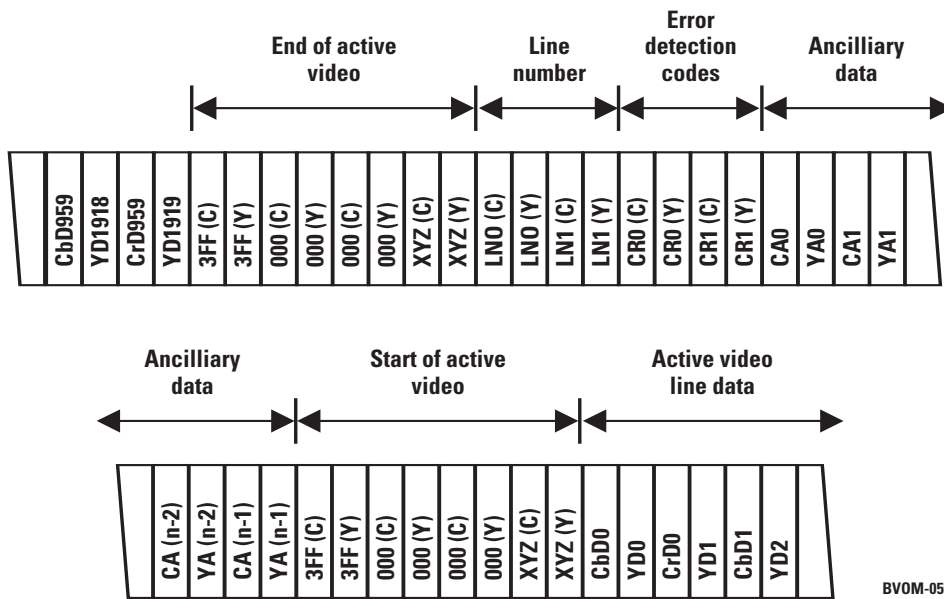
Figure 4.3. HDTV video line data sequence

The data is a regular sequence of words or samples from two channels, chrominance (C) and luminance (Y), which forms the active picture. These samples are interleaved and control sequences such as Start-of-Active-Video (SAV), End-of-Active-Video (EAV), Line Numbers (LN) and Error Detection Codes (CRC) are inserted.

Industry documents like SMPTE RP 178 define test data specifically for the purpose of stressing critical functions of the data transmission chain like the clock-data recovery function and PLL of the deserializer. The test data is usually applied as a diagnostic for equipment that is out of service. The standards also define specific diagnostic and detection methods that work together with the data. Since DTV does not use error correction in serial data transmission, the diagnostics are used to identify elements in the data processing chain that may be contributing to degraded picture or transmission quality. By adopting these methods on-chip, an effective self-diagnostic capability is gained that is simple to extend to the system level.

4.2.2 Device BIST architecture

The CLC031 digital video deserializer/descrambler functional block diagram in Figure 4.4 shows the main functions of the device and illustrates the basic BIST approach. Though testing of all functions shown in the diagram will not be detailed here, the technique of native-code BIST plays a significant role in overall device testability.
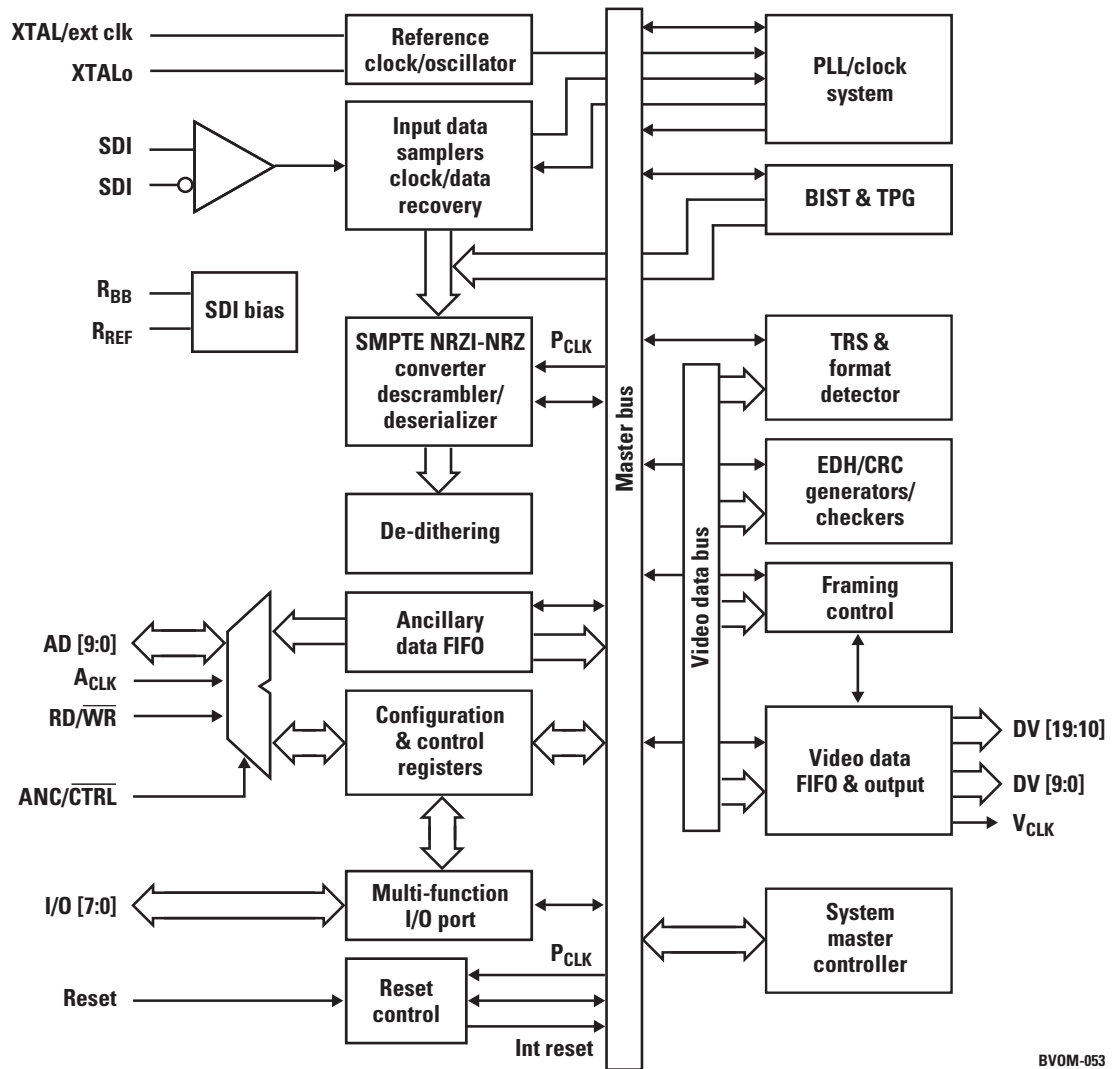
Figure 4.4. CLC031 SD/HDTV deserializer functional block diagram

System testing

The BIST/TPG core achieves the primary objective of producing and checking the data for errors under full operational conditions. Sub-systems used for normal device operation, such as the CRC generator/checker and EDH system, are integral parts of the BIST function.

BVOM-060
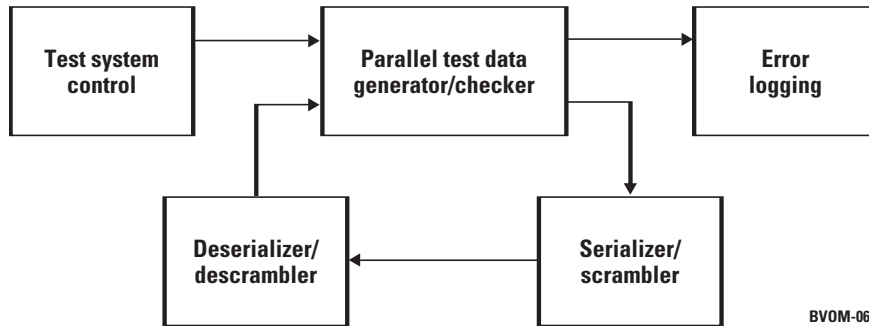
Figure 4.5. Deserializer/serializer BIST core logic functions

An important function for a multi-standard DTV serializer or deserializer is having the ability to automatically determine the format of the data as standard- or high-definition. The CLC030 and CLC031 have such a system of automated picture format detection. Having this capability facilitates the creation of complete frames of test data in any supported SD or HD format. The BIST/TPG process uses the auto-format detection to control and track the data creation and error checking process.

4.2.3 BIST and TPG operation

Expanding the block diagram of the BIST and TPG function in Figure 4.6 shows in simplified form the essential elements and flow making up the BIST system.

BVOM-061
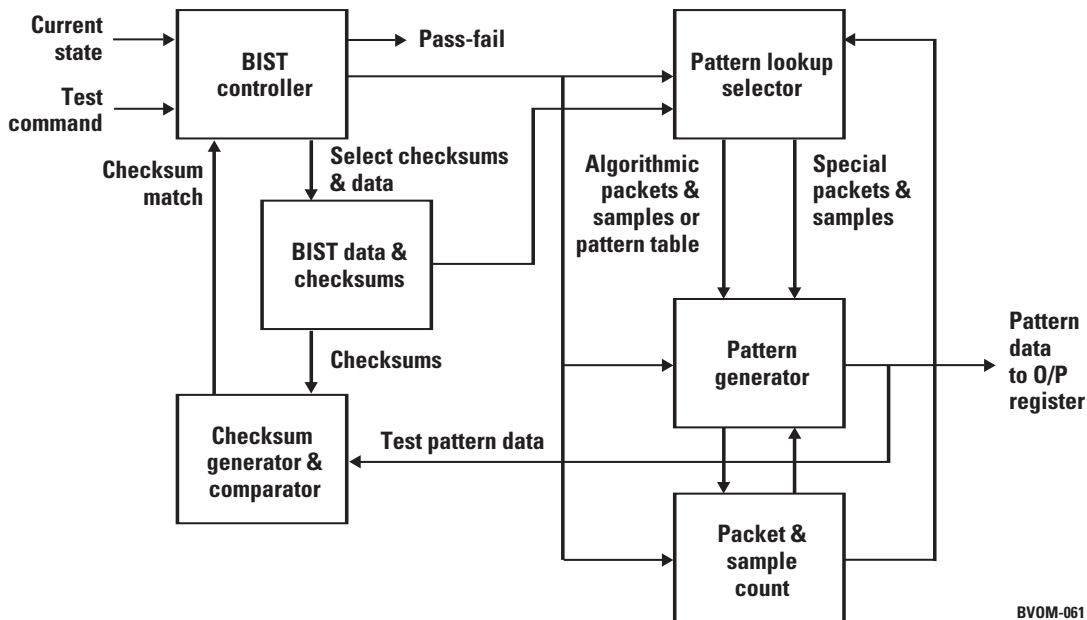
Figure 4.6. BIST system functional diagram

The BIST controller begins the process by clearing the data path scramblers and the error checking systems to an initial state. It then accepts test commands, and monitors the current state of the deserializer. After the BIST/TPG is enabled, further input from the serial data inputs is ignored. The controller uses data stored in the Test 0 register, part of the control register set containing the code for the particular pattern to be used, and the TPG enable-bit to begin the test sequence. The selected format indicates the particular test pattern type and the applicable CRC or error detection codes (EDH) for the checking process.

The TPG enable-control bit directs the BIST engine to begin inserting parallel test data for the selected pattern into the data path. The data may come from a store of complete sample packets, such as an SAV sequence, or be generated algorithmically. The automatic format detection system of the device together with the packet and sample count system instructs the pattern generator from which source and how many of the particular data packets to insert into the data stream. Data is also sent to the checksum generator and comparator and a line number and checksum are inserted at the end of each HD video line. Agreement between the generated and stored checksums confirms that the complete data processing engine and the BIST system are working properly. The CLC030 outputs the test data in serial format and the CLC031 in parallel format.

For testing the standard-definition (SD) functions, the EDH system is used. This system tests using a frame of video data. The SD EDH test checks all portions of the active video fields, the non-video portions of the picture and the entire frame. This test takes at most 16.7 ms for NTSC rasters or 20 ms for PAL video operating at a 50 Hz vertical rate.

The standard- and high-definition BIST sub-systems use portions of the same data path, but different error checking systems. Using both SD and HD data testing assures excellent test coverage. All portions of the device including the stored data samples and CRC data are exercised. Portions not receiving coverage such as the data and other parallel inputs are checked during device manufacture. Malfunction of these elements is testable at the system level.

4.3 Using BIST at the system level

DTV data can pass through many processing elements as shown in Figure 4.7. Each element can contribute to signal degradation or loss of data. Before introduction of devices like the CLC020, CLC030 or CLC031, adding internal native-code test capabilities to a system was difficult and expensive. The standard approach to video system testing usually uses test signals routed to and from centrally located test instruments using a dedicated distribution system consisting of coaxial cable, patch fields and distribution amplifiers. Test signals, such as color bars or reference black raster, are almost universally distributed within the TV plant. It is normal to test signal paths for proper operation before they are used for program transmission while the equipment is not in service.

System testing
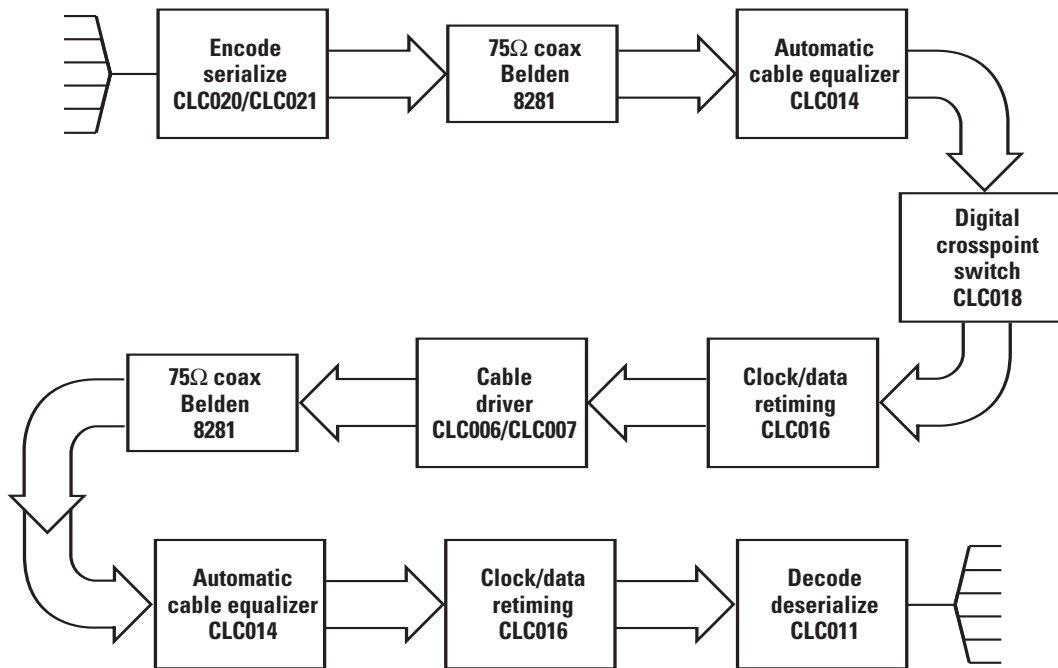
Figure 4.7. Typical DTV data path

By adding test pattern generation and checking to a switcher or router through the use of devices such as the CLC020, CLC021, CLC030, and CLC031, BIST/TPG is then available at low cost to the particular piece of distribution equipment and the entire system. BIST/TPG can also be added at low cost and as a performance and convenience option to video signal origination equipment such as cameras, VTRs, and telecines.

The advantages which devices having native-code BIST/TPG capability add to the system can be seen in the digital video broadcast production switching and mixing system, Figure 4.8. The switcher has both serial and parallel data paths as seen in the partial block diagram. Data manipulation is usually done in parallel format. Data may be altered to add station identifiers, audio data, special effects, overlays, and many others. Data is re-serialized for broadcast. Most switching operations are carried out in serial format.
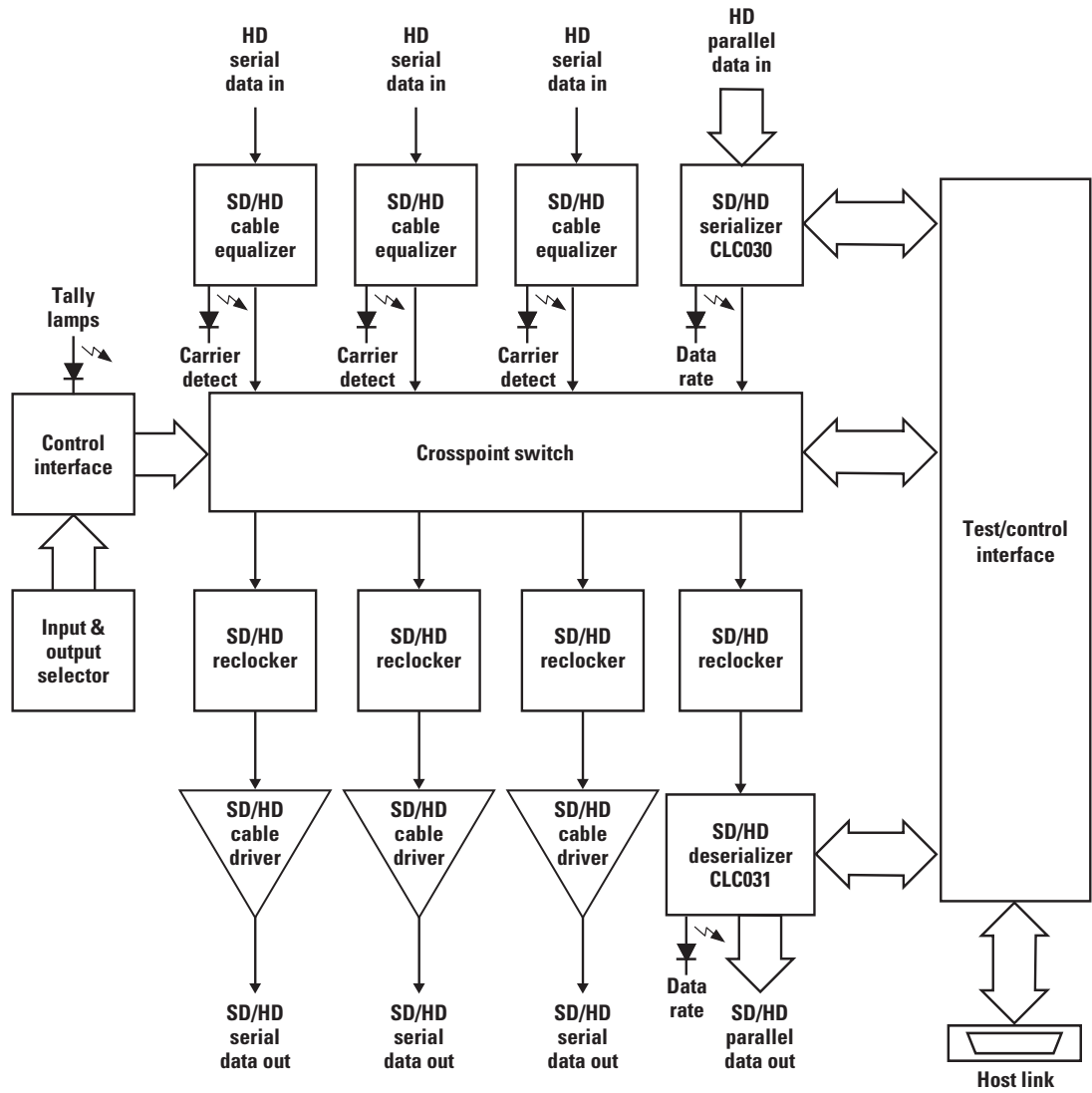
Figure 4.8. Simplified video production switcher

BVOM-063

System testing

The CLC030 and CLC031 add BIST/TPG generation and test capability for transmission path testing in such systems. Separately, both the CLC030 serializer and the CLC031 deserializer are internally self-testing. Using the TPG capabilities, mutual and system test coverage is increased virtually to 100% and can include the circuits between them as well as external video data paths.

In a production switcher, the CLC030 serializer generates the serial test patterns and its output is routed through the switching matrix to one or more serial outputs. These serial outputs are externally or internally looped back to the cable equalizer inputs. The equalizer outputs are routed via the switching matrix to the CLC031 deserializer that is used as a CRC checker. If the external path from cable driver to input equalizer also includes a maximum length of coaxial cable, the equalizer and reclocker may be checked under stressing conditions using the pathological test patterns. With the CLC030 as the generator inserting CRCs in the serial data, the CLC031 deserializer checks the received CRCs and logs error conditions in its control register or by way of the user-configurable I/O port. If the cable equalizer stress test indicates an error condition, the host system can further check the result using a non-stressing test pattern like color bars or it could also make a direct connection to the cable equalizer by removing the test cable.

4.3.1 Conclusions

National constantly strives to deliver added functionality and benefits for system applications using its products. Adding increased test coverage through native code BIST/TPG is one such way. BIST/TPG adds test convenience, coverage and speed while reducing test cost. BIST/TPG also adds utility to the product of which it is a part. This delivers definite value advantages in signal-critical applications such as HDTV broadcasting.

Chapter 5
SDV evaluation boards

5.1 SDV evaluation/demo boards

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the SDV devices. Click the text below to view the evaluation board information.

Table 5.1 provides the product family, PCB description, NSID of devices on the PCB, and the evaluation board order number.

The evaluation boards can be ordered through National's distributors. Supplies are limited, so please check for availability.

Table 5.1 Evaluation board availability

PCB description	NSIDs on PCB	Order number
3.3V serial digital cable driver with adjustable outputs	CLC001	SD001EVK
ITU-T G.703 differential driver with adjustable outputs evaluation board	CLC005	SD005EVK
Serial digital cable driver with adjustable outputs evaluation board	CLC006	SD006EVK
Serial digital cable driver with dual complementary outputs evaluation board	CLC007	SD007EVK
Adaptive cable equalizer for ITU-T G.703 data recovery evaluation board	CLC012	SD012EVK
Adaptive cable equalizer for high-speed data recovery evaluation board	CLC014	SD014EVK
SMPTE 259M digital video deserializer with integrated cable driver evaluation board	CLC020	SD020EVK
SMPTE 259M digital video serializer with EDH generation/insertion evaluation board	CLC021	SD021-5EVK, SD021-3EVK
SMPTE 292M/259M digital video serializer with video and ancillary data FIFOs and integrated cable driver evaluation board	CLC030	SD130EVK
SMPTE 292M/259M digital video deserializer with video and ancillary data FIFOs evaluation board	CLC031	SD131EVK
SMPTE 259M serial digital video receiver	CLC006, CLC014, CLC016, CLC011	SD901EVK

5.2 Adaptive cable equalizer evaluation boards

5.2.1 SD012EVK and SD014EVK — overview

The SD012EVK and SD014EVK evaluation kits for the CLC012 (adaptive cable equalizer for ITU-T G.703 data recovery) or CLC014 (adaptive cable equalizer for high-speed data recovery) provide an operating environment in which the adaptive equalizer can be evaluated by system/hardware designers. The evaluation board has all needed circuitry and connectors for easy connection and checkout of the device using standard test equipment. The board has provisions for constructing several different circuit options as discussed in the CLC012 and CLC014 datasheets. A schematic, parts list and pictorial drawing are provided with the board.

Click the text below view/download the item:

- CLC012 Datasheet and Eval Board User Guide
- CLC014 Datasheet and Eval Board User Guide
- SD012EVK schematic
- SD014EVK schematic
- SD012/014EVK top assembly drawing and BOM
- SD012/014EVK bottom assembly drawing and BOM
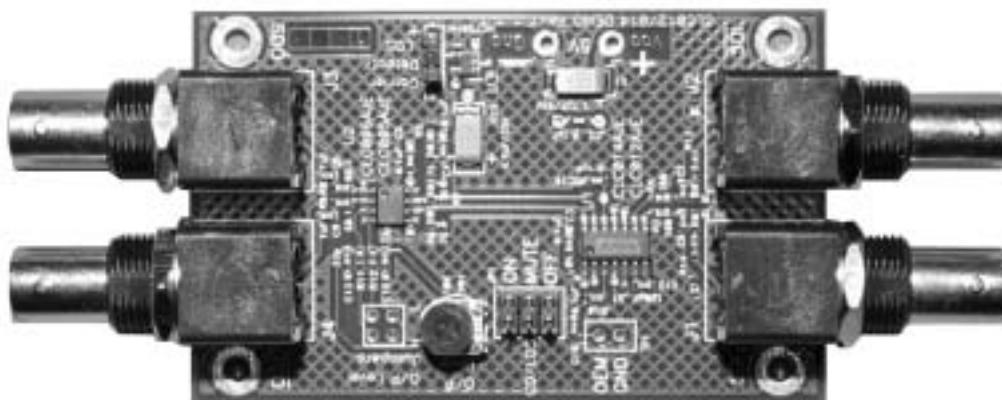
SDV evaluation boards

5.3 Cable driver evaluation boards

5.3.1 SD001EVK/SD005EVK/SD006EVK/SD007EVK — overviews

The SD00xEVK evaluation kits for the CLC001 3.3V serial digital cable driver with adjustable outputs, CLC005 ITU-T G.703 cable driver with adjustable outputs, CLC006 serial digital cable driver with adjustable outputs, and CLC007 serial digital cable driver with dual complementary outputs provide an operating environment in which the cable drivers can be evaluated by system/hardware designers. The evaluation boards have all needed circuitry and connectors for easy connection and checkout of the device using standard digital video or telecom test equipment. The SD001EVK, SD005EVK, and SD006EVK have provisions for adjusting the output swing via a trim pot or jumper on the board. A schematic, parts list and pictorial drawing are provided with the board.

Click the text below view/download the item:

- **SD001EVK**
  – CLC001 Eval Board User Guide
  – SD001EVK schematic
  – SD001EVK top assembly drawing
  – SD001EVK bottom assembly drawing

- **SD005EVK**
  – CLC005 Datasheet and Eval Board User Guide
  – SD005EVK schematic
  – SD005EVK top assembly drawing
  – SD005EVK bottom assembly drawing

- S**D006EVK**
  – CLC006 Datasheet and Eval Board User Guide
  – SD006EVK schematic
  – SD006EVK top assembly drawing
  – SD006EVK bottom assembly drawing

- **SD007EVK**
  – CLC007 Datasheet and Eval Board User Guide
  – SD007EVK schematic
  – SD007EVK top assembly drawing
  – SD007EVK bottom assembly drawing
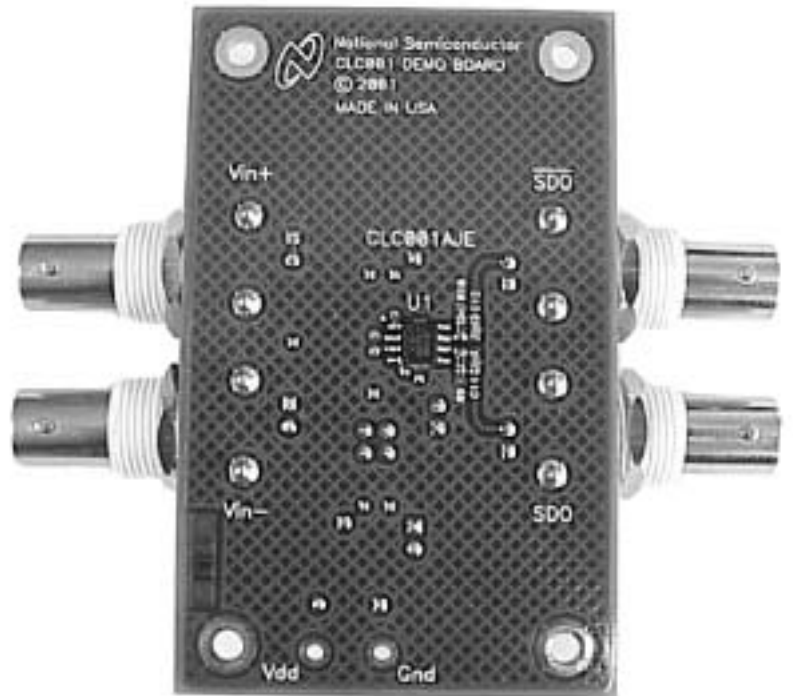
5.4 SMPTE 295 serial digital video receiver (equalizer, retimer and decoder, and cable driver)

5.4.1 SD901EVK — overview

The SD901EVK evaluation kit for the CLC014 equalizer, CLC016 data retimer, CLC011 decoder, and CLC006 cable driver provides an operating environment in which the equalizer, retimer, decoder, and driver can be evaluated by system or hardware designers. The evaluation board has all needed circuitry and connectors for easy connection and checkout of the devices using standard digital video test equipment. A schematic, parts list, and pictorial drawing are provided with the board on CDROM.

Click the text below view/download the item:

- Receiver Evaluation Board User Guide
- SD901EVK schematic
- SD901EVK top assembly drawing
- SD901EVK bottom assembly drawing

SDV evaluation boards

5.5 SD serializers

5.5.1 SD020EVK — overview

The SD020EVK evaluation kit for the CLC020, SMPTE 259M digital video serializer with integrated cable driver, provides an operating environment in which the serializer can be evaluated by system or hardware designers. The evaluation board has all needed circuitry and connectors for easy connection and checkout of the device using standard digital video test equipment. The board has provisions for constructing several different circuit options as discussed in the CLC020 data sheet. In addition, simple jumper connections permit operation of the board in its built-in self-test and test pattern generator modes with a user-supplied, parallel data input clock. A schematic, parts list and pictorial drawing are provided with the board.

Click the text below view/download the item:

- CLC020 Datasheet and Eval Board User Guide
- SD020EVK schematic
- SD020EVK top assembly drawing and BOM
- SD020EVK bottom assembly drawing and BOM
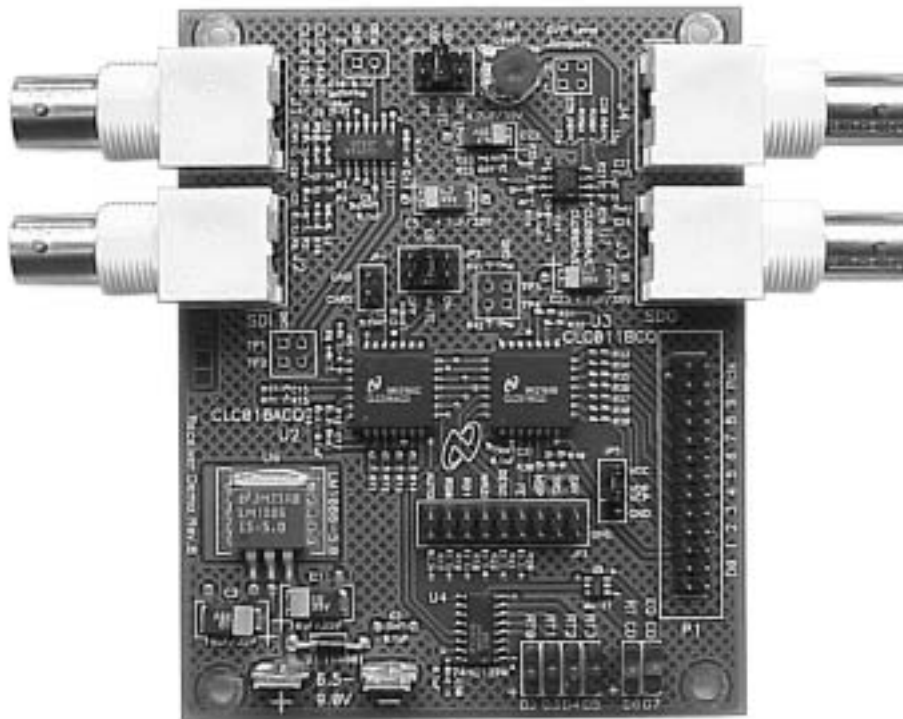
5.5.2 SD021-5EVK and SD021-3EVK — overview

The SD021EVK evaluation kit for the CLC021, SMPTE 259M digital video serializer with EDH generation/insertion, provides an operating environment in which the serializer can be evaluated by system or hardware designers. Two versions are available. The SD021-5EVK uses the CLC021-5.0 device which is powered from a 5V rail, while the SD021-3EVK uses the CLC021-3.3 device and is powered from a 3.3V rail. The evaluation board has all needed circuitry and connectors for easy connection and checkout of the device using standard digital video test equipment. The board has provisions for constructing several different circuit options as discussed in the CLC021 data sheet. In addition, simple jumper connections permit operation of the board in its built-in self-test and test pattern generator modes with a user-supplied, parallel data input clock. A schematic, parts list and pictorial drawing are provided with the board.

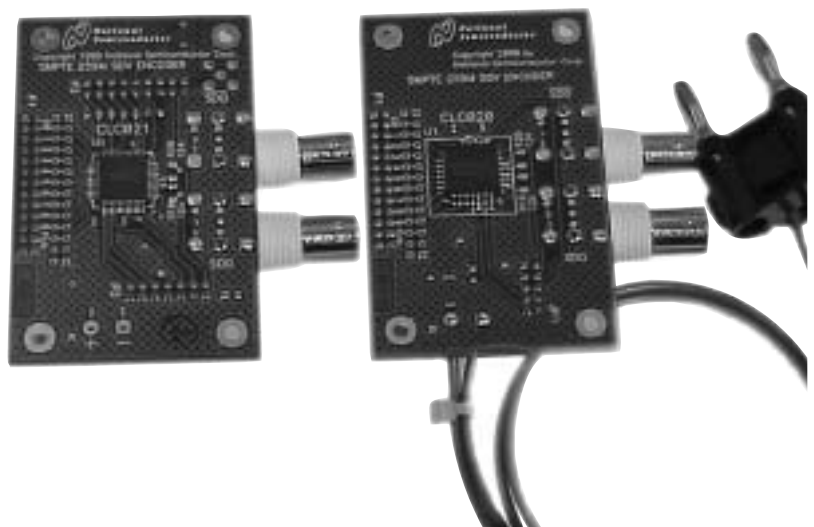Click the text below view/download the item:

- CLC021 Datasheet and Eval Board User Guide
- SD021EVK schematic
- SD021EVK top assembly drawing and BOM
- SD021EVK bottom assembly drawing and BOM

5.6 SD/HD serializer and deserializers

5.6.1 SD130EVK/SD131EVK — overview

The SD130EVK evaluation kit for the CLC030 SMPTE 292M/259M digital video serializer with video and ancillary data FIFOs and integrated cable driver provides an operating environment in which the serializer can be evaluated by system or hardware designers. The SD131EVK evaluation kit for the CLC031 SMPTE 292M/259M digital video deserializer with video and ancillary data FIFOs provides an operating environment in which the deserializer can be evaluated by system or hardware designers. The evaluation boards have all needed circuitry and connectors for easy connection and checkout of the devices using standard digital video test equipment. A schematic, parts list, and pictorial drawing are provided with the board on CDROM.

Click the text below view/download the item:

5.6.2 SD130EVK — CLC030 serializer

- SD130EVK Page 1 schematic
- SD130EVK Page 2 schematic
- SD130EVK top assembly drawing
- SD130EVK bottom assembly drawing
- SD130EVK User Notes
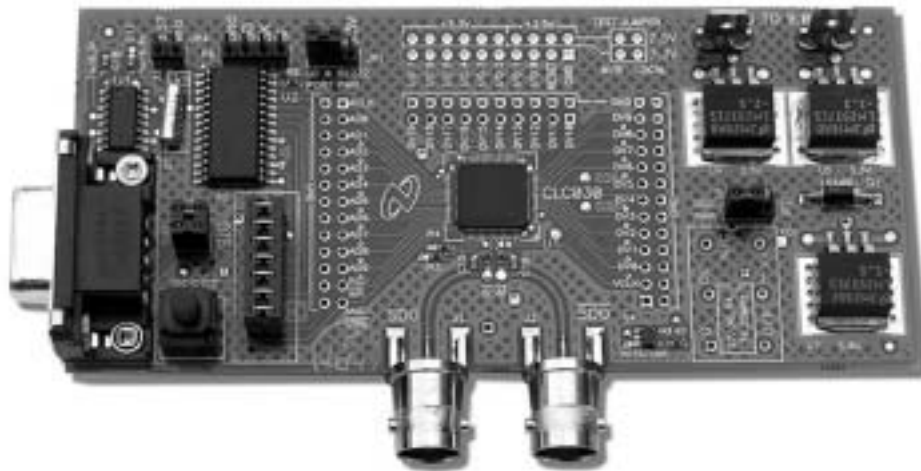
SDV evaluation boards

5.6.3 SD131EVK — CLC031 deserializer

- SD131EVK page 1 schematic
- SD131EVK page 2 schematic
- SD131EVK top assembly drawing
- SD131EVK bottom assembly drawing
- SD131EVK User Notes
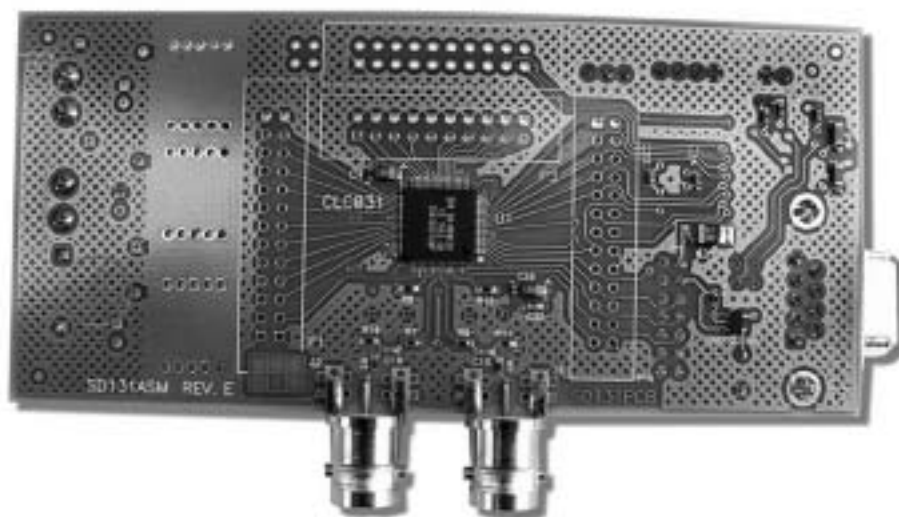
Chapter 6
RAPIDESIGNER slide rule

6.1 RAPIDESIGNER slide rule

National's Transmission Line RAPIDESIGNER slide rule makes quick work of calculations frequently used in the design of data transmission line systems on printed circuit boards.
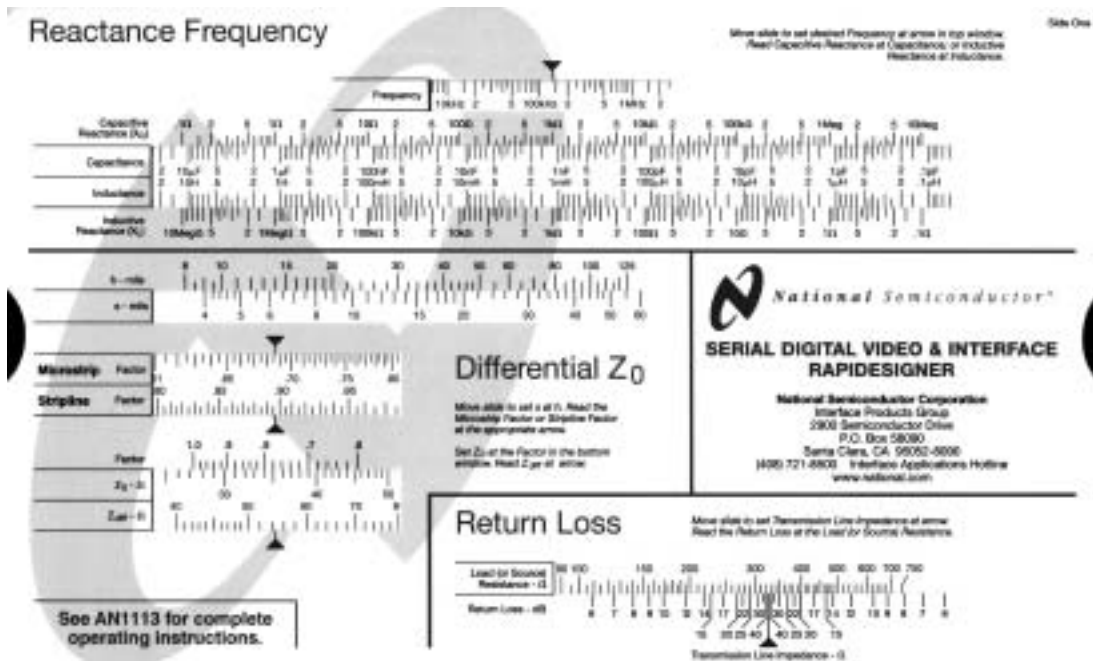
Figure 6.1. Rapidesigner slide rule

The following calculations can be made with the Transmission Line RAPIDESIGNER slide rule for both microstrip and stripline geometries:

- Characteristic impedance (Z_O)
- Intrinsic delay
- Unterminated stub length
- Loaded impedance
- Differential impedance
- Propagation delay
- Reflection coefficient
- C_O and L_O
- Reactance frequency

Two versions of the Transmission Line RAPIDESIGNER slide rule are available. The two RAPIDESIGNER slide rules differ in the dimensions supported; one is for metric units while the other supports English units.

- Transmission Line RAPIDESIGNER slide rule, metric units, Lit# 633200-001
- Transmission Line RAPIDESIGNER slide rule, English units, Lit# 633201-001

The Serial Digital Video & Interface RAPIDESIGNER slide rule adds calculations frequently used in designs using National's Broadcast Video products in video and telecom applications.

- Serial Digital Video & Interface RAPIDESIGNER slide rule, Lit# 633202-001

Full operation and application guides are provided in AN-905 for the Transmission Line RAPIDESIGNER slide rule and AN-1113 for the Serial Digital Video RAPIDESIGNER slide rule. Also included in the application notes are the formulas for the calculations, accuracy information, example calculations, and other useful information.

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Standards

SMPTE 125M–1995 — Component Video Signal 4:2:2–Bit-Parallel Digital Interface

SMPTE 259M–1997 — 10-Bit 4:2:2 Component and 4fSC NTSC Composite Digital Signals–Serial Digital Interface

SMPTE 260M–1999 — 1125/60 High-Definition Production System—Digital Representation and Bit-Parallel Interface

SMPTE 267M–1995 — Bit-Parallel Digital Interface–Component Video Signal 4:2:2 16x9 Aspect Ratio

SMPTE 272M–1994 — Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space

SMPTE 274M–2003 — 1920x1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates

SMPTE 291M–1998 — Ancillary Data Packet and Space Formatting

SMPTE 292M–1998 — Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 334M–2000 — Vertical Ancillary Data Mapping for Bit-Serial Interfaces

SMPTE 344M–2000 — 540Mbps Serial Digital Interface

SMPTE 347M–2001 — 540Mbps Serial Digital Interface — Source Image Format Mapping

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ITU-R-BT.656-4 — Interfaces for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601 (Part A)

ITU-R BT.1120-3 — Digital Interfaces For HDTV Studio Signals

Useful websites

Advanced Television Systems Committee: **www.atsc.org**

Digital Video Broadcasting: **www.dvb.org**

The European Broadcasting Union: **www.ebu.ch/en/index.php**

International Telecommunications Union: **www.itu.int/home/index.html**

National Association of Broadcasters: **www.nab.org**

Society of Motion Picture and Television Engineers: **www.smpte.org**

Glossary

4:2:2 – A term often used to refer to a component digital video format. Refer to SMPTE 125M or ITU-R BT.601 standards for details. The numerals 4:2:2 denote the ratio of the sampling frequencies of the single luminance channel to the two color-difference channels. For every four luminance samples, there are two samples of each color difference channel.

4*f*sc – A term used to signify four times subcarrier sampling rate as used in composite digital systems. In NTSC systems, this is 14.3 MHz and for PAL, it is 17.7 MHz.

A

AES/EBU – Audio Engineering Society and European Broadcasting Union. An informal name for a digital audio standard established jointly by these organizations.

algorithm – A set of rules or processes for solving a problem in a finite number of steps.

aliasing – Defects in the picture typically caused by insufficient sampling or poor filtering of digital video. Defects are typically seen as jaggies on diagonal lines and twinkling or brightening in picture detail.

analog – An adjective describing any signal that varies continuously as opposed to a digital signal that contains discrete levels representing the binary digits 0 and 1.

analog component video – The unencoded output of a camera, videotape recorder, or similar device, consisting of the three primary color signals of red, green, and blue (RGB) that together convey all necessary picture information. Some component video formats translate these three components into a luminance signal and two color-difference signals, for example, Y, B-Y, R-Y.

analog composite video – An encoded video signal, such as NTSC or PAL, which includes horizontal and vertical synchronizing information.

ancillary data – In component digital video, the data carried in the data space corresponding to horizontal blanking between the EAV and SAV TRS or in the data space corresponding to vertical blanking. In composite video, ancillary data is only allowed in the serial data (in the tips of the synchronizing signals). See SMPTE 291M.

asynchronous – A transmission process not synchronized by a clock.

B

bandwidth – 1. The difference between the upper and lower limits of a frequency range, often measured in megahertz (MHz). 2. The complete range of frequencies over which a circuit or electronic system can function with less than a 3 dB signal loss. 3. The information-carrying capability of a particular television channel.

baseline shift – A form of low-frequency distortion resulting in a shift in the DC level of the signal.

bit – The binary representation of a 1 or 0. Also, a quantized level of a pixel.

bit parallel – Byte-wise transmission of a digital video signal via a multi-conductor twisted-pair cable where each pair carries a single (ordered) bit. Refer to SMPTE 125M or ITU-R BT.656.

bit serial – Bit-wise transmission of a digital video signal via a single conductor transmission medium such as coaxial cable or fiber optics. Refer to ITU-R BT.656.

bit slippage – 1. Occurs when word framing is lost in a serial signal so the relative value of a bit is incorrect. This is generally reset at the next serial signal, TRS-ID for composite and EAV/SAV for component. 2. The erroneous reading of a serial bit stream when the recovered clock phase drifts enough to miss a bit. 3. A phenomenon which occurs in parallel digital data buses when one or more bits gets out of time in relation to the rest, resulting in erroneous data. The most common cause is differing cable lengths.

bit stream – A continuous series of bits transmitted on a transmission line.

blocking – A phenomenon which occurs in a multistage routing system when a destination attempts connection to a source but finds that source is unavailable.

BNC – Baby N connector. The cable connector used extensively in television systems.

byte – In digital video, a complete set (sample or word) of quantized levels comprising all of the bits. A byte usually consists of eight bits, while a digital video sample consists of ten bits.

C

cable equalization – The process of compensating for high-frequency attenuation of coaxial cable.

channel coding – Describes the way in which the 1s and 0s of the data stream are represented on the transmission path.

chroma, chrominance – The term used to describe the color-difference signals in a component system. The video signals carrying information about the hue (which color) and saturation (how much color) in a pixel.

clock jitter – Timing uncertainty of the data cell edges in a digital signal.

clock recovery – The process by which timing information is reconstructed from digital data.

coaxial cable – A transmission line with a concentric pair of signal carrying conductors, an inner conductor and an outer conductive metallic sheath or shield. The shield helps prevent external electromagnetic radiation from affecting the signal on the inner conductor and it reduces electromagnetic radiation from the transmission line.

coding – The representation of the levels of a digital video signal by a number, usually of binary form.

coefficients – The quantitative expression of a property of a physical system usually by a number (often a constant).

contouring – Video picture defects resulting from quantizing at too coarse a level.

D

D1 – A component digital video recording format that uses data conforming to the ITU-R BT.601 standard. This term is often used incorrectly to indicate digital component video.

D2 – A composite digital video recording format that uses data conforming to SMPTE 244M. This term is often used incorrectly to indicate digital composite video.

delay – The time required for a signal to pass through a device or conductor.

demultiplexer (demux) – A device used to separate two or more signals that were previously combined by a compatible multiplexer and transmitted over a single channel.

deserializer – A device that converts serial digital information to parallel format.

digital component video – A digital representation of a component analog signal set, most often Y, B-Y, R-Y. The encoding parameters are specified by ITU-R BT.601. The parallel interface is specified by ITU-R BT.656 and SMPTE 125M.

digital composite video – A digitally encoded video signal, such as NTSC or PAL, which includes the horizontal and vertical synchronizing information.

digital word – The grouping of bits which represents a single entity by a digital system.

Glossary

dither – Typically a random, low-level signal (oscillation), which may be added to an analog signal prior to sampling. Often consists of white noise of one quantizing level peak-to-peak amplitude. More recently, a repeated pseudo-random manipulation of the one or two least significant bits of parallel digital video data words. This is done to inhibit the formation of encoded serial digital data streams having excessive low frequency content, pathological data patterns for example.

E

EAV – End of active video in component digital data systems.

EBU – European Broadcasting Union. An organization of European broadcasters that, among other activities, produces technical statements and recommendations for the 625/50-line television system.

EDH (error detection and handling) – A method for identifying and logging errors in the serial digital video data signal. See SMPTE RP 165.

embedded audio – Digital audio which is multiplexed into a serial digital video data stream.

encoder – In digital video, a device that encrypts video data, usually when in parallel format, according to the method defined in SMPTE 259M or SMPTE 292M.

eye pattern – On an oscilloscope display, a waveform pattern formed by the overlapping of consecutive data intervals and resembling an eye. It is used to evaluate signal characteristics.

F

format conversion – The process of both encoding/decoding and resampling of digital rates.

frequency modulation – Modulation of a sinewave or "carrier" by varying its frequency in accordance with amplitude variations of the modulating signal.

G

gain – Any increase or decrease in strength of an electrical signal. Gain is measured in terms of decibels or number of times of magnification.

group delay – Distortion of a signal caused by differing propagation delays occurring for different frequencies in a transmission system or network (i.e., the delay at 1 MHz is different than the delay at 5 MHz).

H

horizontal interval (horizontal blanking interval) – The time period between active video lines.

I

interpolation – In digital video, the creation of new pixels in an image by some method that mathematically manipulates the values of neighboring pixels.

I/O – Input/output. Typically refers to sending information or data signals to and from devices.

ITU-R – The International Telecommunication Union, Radio Communication Sector.

ITU-R BT.601 – An international standard for digital component television from which SMPTE 125M was derived. The standard defines the sampling systems, matrix values, and filter characteristics for Y, B-Y, R-Y and RGB digital component television.

J

jitter – The undesirable random time variation of a signal.

L

luma, luminance – The video signal describing the amount of light in each pixel, equivalent to the signal provided by a monochrome camera. Luma is often generated as a weighted sum of the R', G', and B' signals.

M

MPEG-2 – Motion Pictures Expert Group. An international group of industry experts set up to standardize compressed moving pictures and audio.

multiplexer (mux) – A device that combines two or more electrical signals into a single, composite signal.

N

nonlinear encoding – The process by which relatively more levels of quantization are assigned to small amplitude signals and relatively fewer to the large signal peaks.

nonlinearity – The result of a nonadditive operation. For example: gain variation as a function of signal amplitude.

NRZ – non-return to zero. A coding scheme that is polarity sensitive. 0 = logic low; 1 = logic high.

NRZI – non-return to zero inverse. A coding scheme used in video data scrambling that is polarity insensitive. 0 = no change in logic level; 1 = a transition from the one logic level to the other.

NTSC (National Television Systems Committee) – The organization that formulated standards for the NTSC television system. A term used now to describe the American system of color television broadcasting which is used mainly in North America, Japan, and parts of South America.

O

OEM – Output eye monitor.

orthogonal sampling – The process of sampling a repetitive video signal so that samples in each line are in the same horizontal position.

P

PAL – (Phase Alternate Line) The name of the color television system in which the V component of burst is inverted in phase from one line to the next in order to minimize hue errors that may occur in color transmission. Often used to describe the predominantly European television system of broadcasting.

patch panel – A manual method of routing signals using a panel of receptacles for sources and destinations and wire jumpers to interconnect them.

peak to peak – The amplitude (voltage, current, etc.) difference between the most positive and the most negative excursions (peaks) of an electrical signal.

phase distortion – A signal defect caused by unequal delay (or phase shift) of different frequency components within the signal as they pass through different impedance elements such as filters, amplifiers, and transmission lines.

phase shift – The relative timing movement of a signal in relation to another signal.

pixel – The smallest distinguishable and resolvable area in a video image. A single point on the screen. In digital video, a single sample of the picture. Derived from the words "picture" and "element."

PRBS – Pseudo random binary sequence.

production switcher (vision mixer) – A device or system that allows switching or transitioning between different video pictures or inclusion of mixing or other special effects.

Glossary

propagation delay – The time taken for a signal to travel through a circuit, piece of equipment, or a length of cable.

Q

quantization – The process of converting a continuous analog input into a set of discrete output levels.

quantizing noise – The noise (deviation of a signal from its original or correct value) that results from the quantization process. In serial digital video, a granular type of noise which only occurs in the presence of a signal.

R

rate conversion – Technically, the process of converting from one sample rate to another. Often used incorrectly to indicate both resampling of digital rates and encoding or decoding.

reclocking – The process of clocking the data with a regenerated clock. Intended to correct timing distortion of the digital signal intervals to that of the ideal fundamental bit interval.

resolution – The number of bits (e.g., 4, 8, 10) which determines the resolution of the digital signal. (4 bits is a resolution of 1 in 16, 8 bits is a resolution of 1 in 256, and 10 bits is a resolution of 1 in 1024). Eight bits is deemed the minimum acceptable for broadcast TV.

routing switcher – An electronic device or system that routes a user-supplied signal (i.e., audio, video) from any input to any user-selected combination of outputs.

S

sampling – The process whereby analog signals are measured or sampled. For example: 13.5 millions of times per second for some video.

sampling frequency – The number of discrete sample measurements made in a given period of time, often expressed in MHz for video.

SAV – Start of Active Video in component digital systems.

scrambling – The conversion of digital data according to an ordered process in an attempt to break up the low-frequency patterns associated with serial digital video signals. The digital signal is shuffled to produce a more uniform spectral distribution.

segmented frames – A scanning format in which the picture is captured as a frame in one scan, as in progressive formats. The even lines are then transmitted as one field and the odd lines in the next field as in an interlaced format.

serial digital – Digital information that is transmitted in serial form; often used informally to refer to serial digital television video signals.

serializer – A device that converts parallel digital information to serial digital.

SMPTE – Society of Motion Picture and Television Engineers. A professional organization that recommends and maintains standards for the television and film industries.

still store – A device for the storage of specific frames of digital video.

synchronous – A transmission process whereby the bit or character stream are slaved to accurately synchronized clocks at both the sending and receiving ends.

sync word – A unique pattern of bits or data used to synchronize data reception or to identify unique reference points in the digital television data signal.

T

telecine – A device for converting movie film into video signal format.

temporal aliasing – A visual defect occurring when the image being sampled moves too fast for the sampling rate. A common example is helicopter blades that appear to rotate slowly or in reverse.

TRS (Timing Reference Signals) – The four-word long sequences used to maintain timing in composite digital video systems.

TRS-ID (timing reference signal identification) – A four-word long digital-reference signal used to maintain timing in composite digital video systems.

truncation – The process of deletion of the lower significant bits on a digital data system that usually results in digital noise.

V

VTR (video tape recorder) – A device that permits audio and video signals to be recorded on magnetic tape.

W

waveform – The displayed envelope or shape of an electromagnetic wave. A graphical representation of the relationship between voltage or current and time.

word – See byte.

Y

Y', C'b, C'r – A gamma corrected color-difference signal set used in digital component formats.

Y, Pb, Pr, – A version of (Y R-Y B-Y) specified for the SMPTE analog component standard.

Y, R-Y, B-Y – The general set of CAV signals used in the PAL system as well as for some composite encoder and most composite decoders in NTSC systems. Where: Y is the luminance signal, R-Y is the 1st color-difference signal, and B-Y is the 2nd color-difference signal.

Y, U, V – Luminance and color-difference components for PAL systems. Often imprecisely used to signify Y', P'b, P'r.

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