

# AN-1372 LMH0034 PCB Layout Techniques

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## ABSTRACT

This application report provides PCB layout techniques to achieve optimal performance for the LMH0034 multi-rate adaptive cable equalizer.

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## 1 Introduction

The LMH0034 multi-rate adaptive cable equalizer requires careful attention to PCB layout to achieve optimal performance. It is a high performance analog device and must be treated as such. More specifically, it is a high-gain, wide-band, analog, RF, AGC amplifier-filter. Its successful operation depends on good PCB layout techniques.

## 2 Causes and Effects of Common Equalizer Problems

The gain of the LMH0034 equalizer is at a maximum when the input signal is at a minimum. This occurs at maximum cable length as well as when the cable is unconnected (no input signal). Interfering signals and noise can be amplified under these maximum-gain conditions, severely degrading equalizer performance. Even a small amount of noise or interference can cause major performance problems for an adaptive cable equalizer.

Improper PCB layout leads to a number of problems, including:

- Failure to equalize the maximum cable length
- Data errors at long cable lengths
- Random (garbage) data output when no cable is connected
- Positive carrier detection when no cable is connected

These problems are most commonly caused by failing to isolate the LMH0034 from interference, such as:

- Reception of radiated EMI signals originating in the system enclosure or on the PCB
- Power supply or other noise coupling to the inputs through the input network
- Crosstalk between the input network and adjacent circuits
- Coupling between the input and output circuits of the equalizer
- Crosstalk and noise coupling into the Automatic Equalization Control (AEC) circuit

## 3 Preventing PCB Problems

Good PCB layout techniques are essential to minimize or eliminate the effects of interference on the LMH0034. These techniques include:

- Isolation of the equalizer inputs and the AEC circuit from high level signals
- Shielding of input and AEC networks from external signal pickup
- Suppression or attenuation of unwanted interference signals

[Figure 1](#) shows a typical schematic for the LMH0034 equalizer. The following PCB layout recommendations will ensure optimal performance of the LMH0034 as well as other high-speed analog devices.

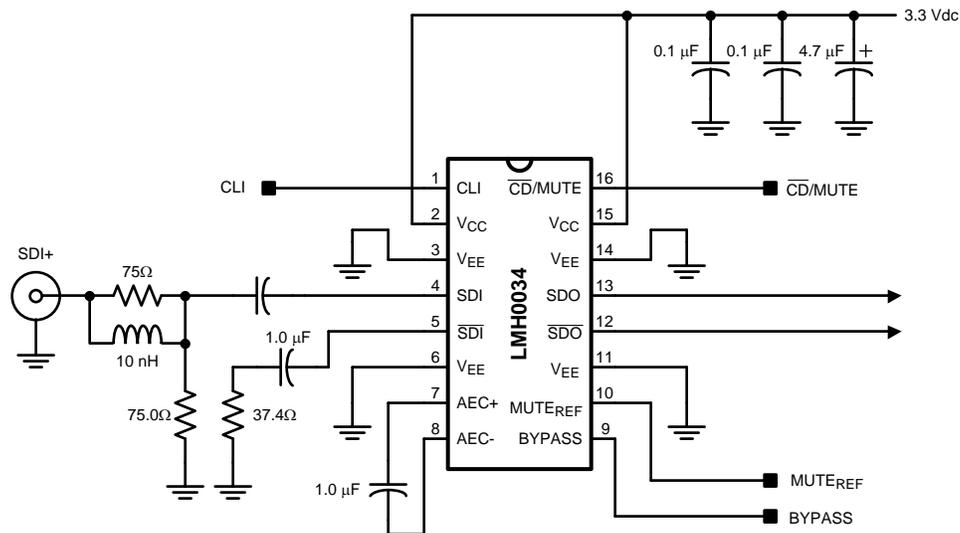


Figure 1. Typical LMH0034 Circuit

### 3.1 Multi-Layer PCB

The LMH0034 requires a multi-layer PCB with separate power and ground layers to achieve the necessary isolation and shielding required for such a high gain and wide bandwidth device. Double-sided PCBs do not offer this and are not appropriate for the LMH0034. A successful LMH0034 PCB design requires a minimum of four layers. Transmission line layers are typically on the top and bottom side (usually microstrip) with separate power and ground planes for the inner layers.

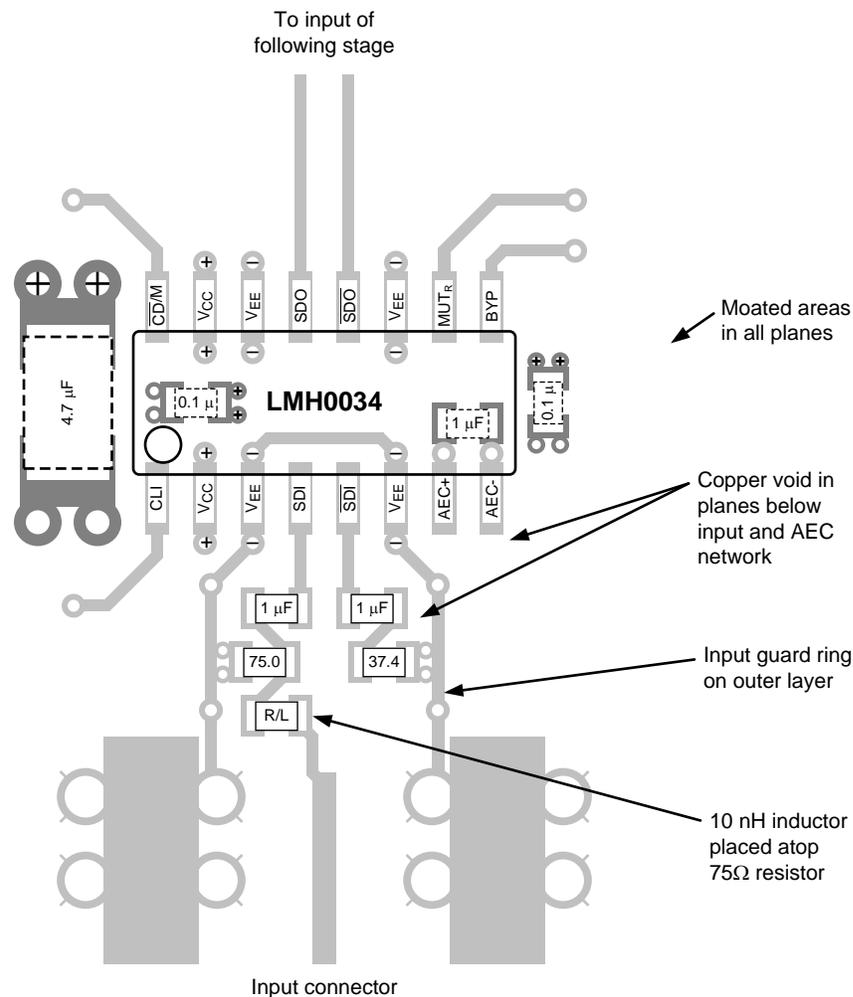
### 3.2 Power-Ground Sandwich

Power and ground layer pairs should be specified with thin dielectrics of 6 mils or less to maximize the intrinsic capacitance of the power-ground “sandwich.” This provides very effective high frequency bypassing. Conventional PCB dielectric materials in sandwiches 10 mils (0.25 mm) and less in thickness can be used to achieve intrinsic capacitance of 100 pF/sq. in. (15.7pF/sq. cm.) or more. This “free” capacitance can increase the effective attenuation of the power supply decoupling by 20dB or greater.

### 3.3 Dual Vias

Dual vias should be used to minimize inductance in power and ground connections for bypass capacitors, termination resistors, and  $V_{CC}$  and  $V_{EE}$  pins of the device. They can reduce the interconnect inductance by up to 50%. This reduced inductance extends the effective operating range of bypass capacitors. Also, multiple power or ground pins of the LMH0034 should not be connected to a single via. Each  $V_{CC}$  and  $V_{EE}$  connection must have its own via (in fact, each connection should have two vias to minimize inductance).

Figure 2 shows an example PCB layout of the LMH0034 equalizer. Note that the bypass capacitors drawn with dashed outlines are intended to be placed on the bottom side of the PCB. This allows the high frequency bypass capacitors to be placed as close as possible to the device power pins without obstructing the layout of the other components. Figure 2 illustrates several important points about isolating the equalizer from interference.



**Figure 2. LMH0034 Layout With Guard Ring**

### 3.4 Copper Voids

Removing, or voiding, the copper in the plane layers below the input network minimizes parasitic capacitance. The dark-shaded area under the input network in [Figure 2](#) indicates where the planes have been removed. These “voids” minimize the capacitance between the component pads, the component bodies, and the planes. [Figure 2](#) also shows the copper removed in the plane layers below the AEC network, which prevents power supply noise from coupling into the AEC feedback loop.

### 3.5 Moats

The LMH0034 is further isolated by removing the copper in all planes in a “moat” surrounding the equalizer. The moat is shown as a dark-shaded rectangle around all circuits in [Figure 2](#). Notice that the rectangle is not complete; there is a small opening at the end farthest from the LMH0034 input network to connect the equalizer to the rest of the planes. The moat prevents unwanted currents from adversely affecting the equalizer. Stray signals from adjacent circuits have a long way to travel to reach the LMH0034 inputs, so they are effectively attenuated.

It is also important to isolate the LMH0034 inputs from its own outputs, or from the output of any nearby cable drivers or other high-level signals. The typical equalizer input tends to be a weak signal (hence the need for equalization) and larger signals can couple into the input signal and corrupt the data.

### 3.6 Guard Rings

A grounded guard ring around the input of the equalizer isolates and protects the LMH0034 even more. This is shown in Figure 2 as a light-shaded ring surrounding the dark-shaded copper void of the input network. The guard ring is grounded by vias in several locations. It should completely enclose the input network.

### 3.7 Common Mode Rejection

The input networks should be symmetrical to take advantage of common mode rejection. Noise and interference picked up by the equalizer input is usually common to both inputs. This noise will be rejected by the differential input of the LMH0034. The layout should be as symmetrical as possible with balanced termination impedances as shown.

### 3.8 Copper Floods

Copper floods can be used on the outer PCB layers in place of the guard ring for additional isolation and shielding, as shown in Figure 3. The techniques explained previously apply to PCBs with copper floods as well. Dashed outlines indicate areas where copper should be removed under the input components and AEC circuit, as well as the location of the surrounding moat. The copper flood should be connected to the ground layers at 1 cm intervals to be effective.

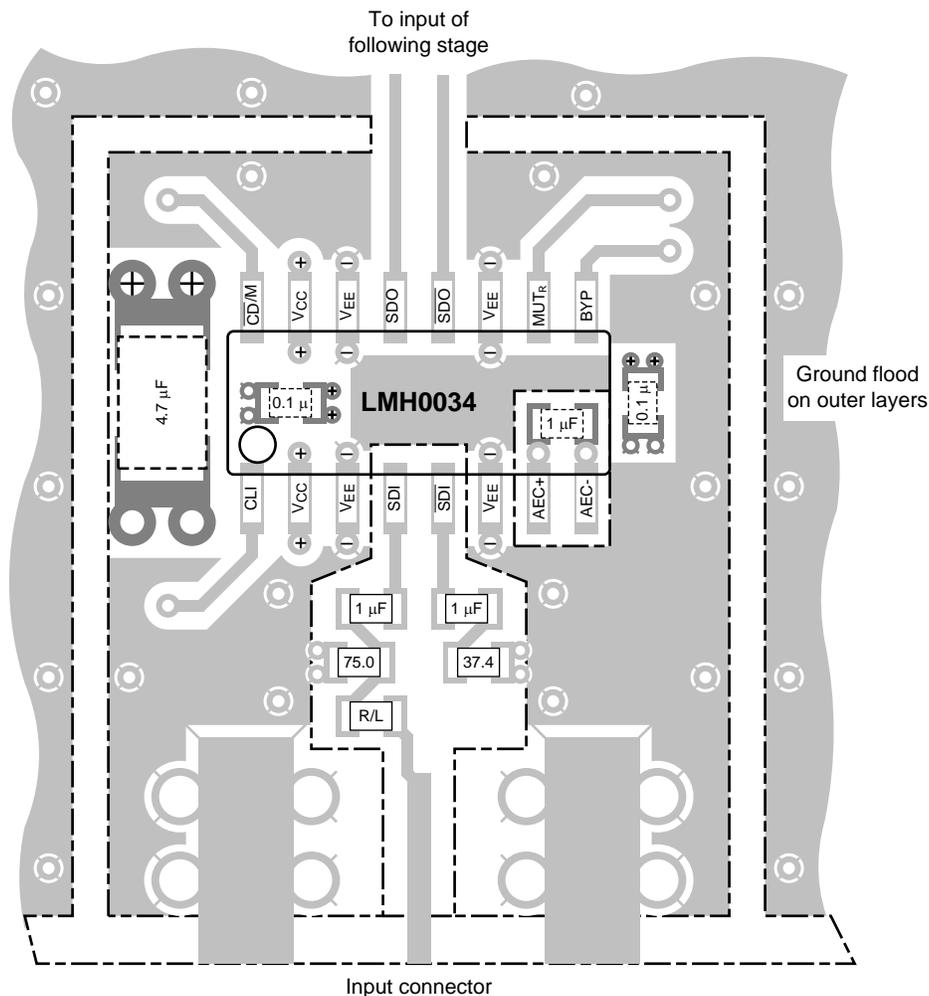


Figure 3. LMH0034 Layout with Copper Floods

### 3.9 Additional Techniques

In addition to reducing or eliminating the effect of interference on the LMH0034, it is important to minimize impedance variations that may cause reflections or otherwise degrade equalizer performance. Additional PCB layout techniques that control impedance and produce a clean PCB layout can improve overall LMH0034 performance.

The BNC input connector shown in the layout diagrams is an in-line surface mount “launcher,” as opposed to a right angle or vertical BNC. This is necessary for tight impedance control in order to meet the return loss requirement of SMPTE 292M and 259M. Right angle BNC connectors are not suitable for controlled impedance situations due to the length of the exposed center pin and ground pins.

Impedance changes can be reduced by routing traces diagonally to the corners of component pads where possible. Rounded corners may be used to further minimize impedance changes caused by the change in PCB trace width. 90-degree corners should never be used with high speed circuits.

The LMH0034 should be placed close to the BNC connector, with the input components as close to the equalizer as possible. Shorter input networks are almost always less troublesome than longer networks. The input network to the LMH0034 should contain no stubs whatsoever. Also note that any termination resistors for the LMH0034 output should be located at the input of the following stage.

## 4 Summary

Following these PCB layout techniques will result in improved LMH0034 performance. In summary:

- Use multi-layer PCBs with an effective power-ground sandwich for isolation, shielding, and improved bypassing.
- Use dual vias to minimize inductance in power and ground connections (at least one via per  $V_{CC}$  and  $V_{EE}$  connection).
- Make use of copper voids to reduce parasitic capacitance and noise.
- Use moats and guard rings for isolation.
- Isolate the LMH0034 inputs from high level signals.
- Take advantage of the common mode rejection offered by differential inputs by using a symmetrical layout.
- Use copper floods for additional shielding and isolation.
- Minimize impedance mismatches.

For a negligible amount of added costs, these techniques will result in less troublesome and all around better performing LMH0034 PCB designs.

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