Application Brief

Replace External Memory for Module Identification With TMP1826 Embedded EEPROM

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Temperature and Humidity Sensing

Memory in systems plays an important role of storing software code, data, and information required for acquiring data from sensors and initiating proper control to keep process parameters within acceptable bounds. Additionally, the memory is also required for storing temperature sensor calibration information. With the increasing complexity in systems, the design modular (sub-systems) must be made so that system components can be easily upgraded, replaced, or updated. This brings about the challenges of adding memory in the sub-system, that can be used to store necessary information about the characteristics, so that the main controller can query and identify the module and the necessary control parameters. To address these challenges, TI developed the TMP1827 and TMP1826, 1-Wire® based temperature sensor with 2048 bits of non-volatile EEPROM which features:

- NIST traceable factory-programmed non-erasable 64-bit identification number for device addressing
- Write operation in block size of 64 bits
- Continuous read mode
- Read with write protection with page size of 256 bits
- Authenticated write protection mode with page size of 256 bits (only available on TMP1827)

Simplified Connectivity

System designers often require that before the sub-system is powered up, the required information is available to the main controller. This requirement results in dedicating a set of pins for the onboard memory of the sub-system to have a dedicated supply and communication bus. Most memory devices require I^2C or SPIs that have 2 or 3 wires respectively for the communication interface. As Figure 1 shows, the TMP182x devices feature bus-powered, 1-Wire® interface which greatly simplifies the backplane connector requirement as only one-pin and PCB trace is required for both powering and communicating with the device.

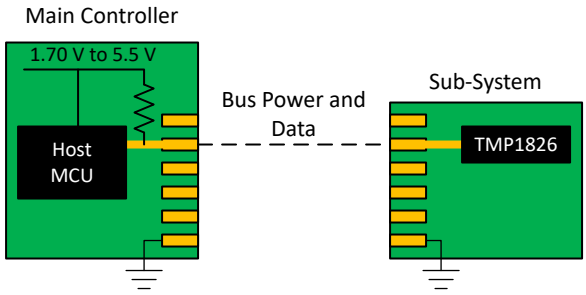

Figure 1. TMP1826 Backplane Connectivity

Identification and Configuration

The 2048 bits of EEPROM on the TMP182x is organized as 8 pages of 256 bits. Each page has 4 blocks of 64 bits each. The basic EEPROM write is done at the block level. Additionally, a page can be protected by changing the page attribute to read-only, applicable on TMP1826 and TMP1827, or authenticated-write that is applicable only on the TMP1827.

As a result, a system designer can now partition the memory to store information such as the board manufacturing date, revision of the sub-system, and so forth, and make the memory read-only to prevent accidental overwrite. On the TMP1827, re-programmable information such as periodic calibration information, counters, and so forth, can be stored in a page marked with authenticated-write, which allows for regular read, but an update only when the host authenticates the transfer, giving the system an extra level of security. Finally, any page marked as write-read (factory default), can be used as a temporary storage for periodic information.

The availability of non-volatile memory with the previously-mentioned page attributes, provides the system designer greater flexibility and efficiency in partitioning the system memory. A mechanism to store sub-system information is often required for identification and configuration of the sub-system in terms of power sequencing, access sequences, and calibration of other components like analog sensors.

Memory Scalability

In applications that require larger memory size or distributed memories, the TMP182x provides a unique capability to expand addressing space using the flexible address scheme using the IO. Figure 2 illustrates two TMP1826 connected on the sub-system, one with all IO0-3 strapped to GND (flexible address = 0h) and another with IO0 strapped to SDQ and IO1-3 strapped to GND (flexible address = 1h).

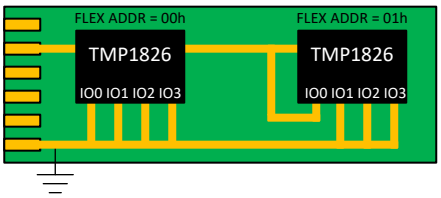

Figure 2. Scaling Memory Using IO

Together the two devices provide 4096 bits of EEPROM. As shown in Table 1, when accessing the devices, the upper byte of the address space forms the flexible address and lower byte of the address space maps to the address byte LSB. The address byte MSB remains 00h for all access. Due to the 2.5 mm × 2.5 mm NGR package, multiple TMP182x devices can be placed without taking up area on the board, and scalability is easily achieved in software without having to develop software to qualify a new device, as up to 64 devices can be strung together on the same bus, if necessary.

Table 1. Accessing 4Kbit Using TMP1826

Address Space	Flex Address	Address Byte MSB	Address Byte (LSB)
0000h - 00FFh	00h	00h	00h - FFh
0100h - 01FFh	01h	00h	00h - FFh

Summary

The high-accuracy TMP1826 and TMP1827 temperature sensors with integrated 2048 bits of EEPROM and multilevel memory protection provides modular applications with the capability to identify and configure onboard sensors and devices, with the right level of scalability. The unique interface and memory scaling features of the TMP182x family of devices, facilitates ease of redesign, mixing and matching memory devices with and without authentication, an increase in memory size or distributed memories, and also eliminates the need for unnecessary system changes for manufacturability and fast time-to-market.

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