EVM User's Guide: LMKDB1204EVM

LMKDB1204 Evaluation Module

Description

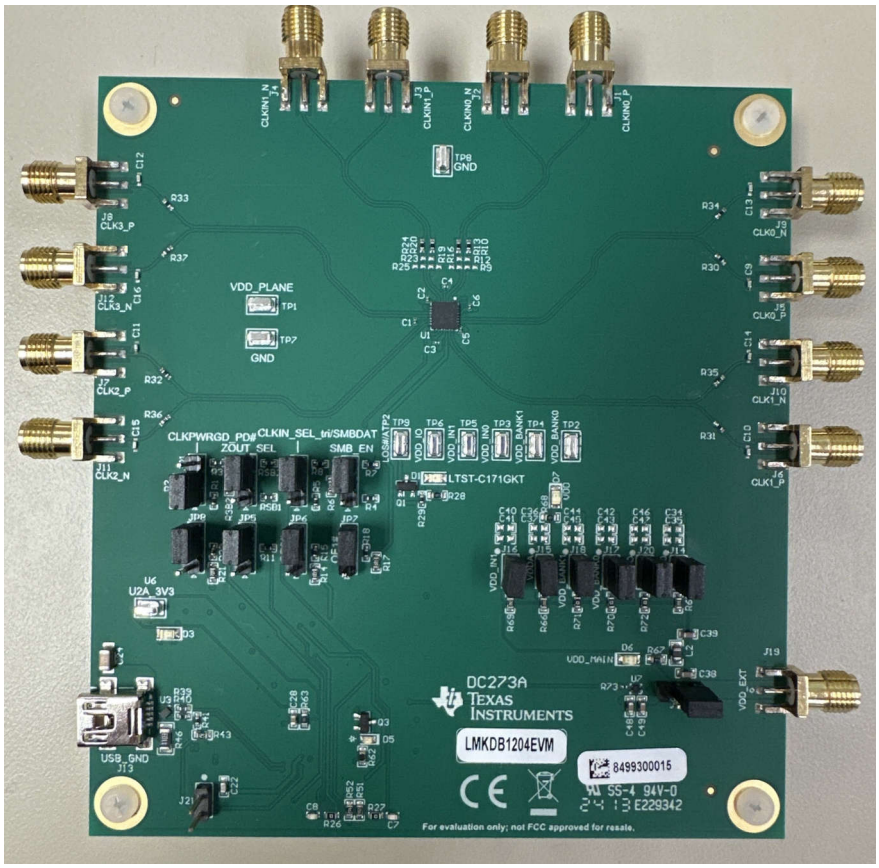
The LMKDB1204 evaluation module (EVM) is designed to provide a quick setup to evaluate the LMKDB1204 LP-HCSL buffer that supports PCIe Gen 1 to Gen 6. The printed circuit board (PCB) contains several jumpers and a USB connection to enable the LMKDB1204 with desired user programming and setup. The evaluation module provides flexibility for compliance testing, system prototyping, and performance evaluation of the LMKDB1204 device.

Features

- PCIe Gen 1 to Gen 6
- External and USB power supply options
- Programmability through TICS Pro Software GUI graphical user interface (GUI)

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator



LMKDB1204EVM

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (MCU) interface using a PC with TI's TICS Pro Software GUI. TICSPro can also be used to import and export register data for flexible programming of device. Input and outputs of LMKDB1204 can be interfaced with external system for evaluating compatibility and performance through coaxial cable. On-board LDOs give user an option to use the USB as power supply to minimize the number of test equipment needed.

This user's guide contains information and support documentation for the LMKDB1204 evaluation module (EVM). Included are the schematics, PCB layouts, and bill of materials of the LMKDB1204EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the LMKDB1204EVM.

1.2 Kit Contents

LMKDB1204EVM box contains:

- One LMKDB1204EVM board (DC273A).
- 3-ft mini-USB cable (MPN 3021003-03).

1.3 Specification

Some key specifications for LMKDB1204 buffer and EVM are noted in Table 1-1.

Table 1-1. LMKDB1204 Key Parameters

Parameter	Value
Ambient temperature	-40 to 105 ºC
Power supply	1.8V ± 10%, 3.3V ± 10%
Operating frequency	1MHz to 400MHz. (*automatic output disable* (AOD) disabled)
	25MHz to 400MHz. (*automatic output disable* (AOD) enabled)
Output format	LP-HCSL

1.4 Device Information

The LMKDB1204 is a high performance LP-HCSL buffer that supports PCIe Gen 1 to Gen 6. LMKDB1204 has extremely low additive jitter, fail safe inputs, flexible power-up sequence, individual output enable pins, loss of input signal detection, and SMBus interface. The EVM has integrated LDOs for excellent power supply noise suppression with an operating supply voltage of 3.3V.

2 EVM Quick Start

Table 2-1 describes the default jumper configuration of the EVM to power the device from an external power supply. Configure the EVM as specified in Table 2-1 for initial bring up. The EVM can also be configured to use an on-board 3.3V LDO with USB supply option by changing the position of jumper JP9 as described in Table 2-1.

Table 2-1. Default Jumper Configuration

Category	Reference Designator	Default Position	Description
Power	J14	1-2	Connect USB or external supply to VDD_IN0 of device.
	J15	1-2	Connect USB or external supply to output bank and digital supply of the chip (VDD).
	J16	1-2	Connect USB or external supply to VDD_IN1 of device.
	J17	1-2	Connect USB or external supply to VDD_BANK0 of device.
	J18	1-2	Connect USB or external supply to VDD_BANK1 of device.
	J20	1-2	Connect USB or external supply to IO pins on board (VDD_IO).
	JP9	1-2	Choose between USB or external power supply. Current configuration is for external power. To change to USB power, change jumper position to 2-3.
Output enable control pins	JP5 through JP8	2-3	Pull down to GND to enable output (OE#0 through OE#3) with pin control option.
Digital pins	JP1	1-2	CLKPWRGD_PD# pulled high.
	JP2	2-3	ZOUT_SEL pulled low setting output impedance to 85Ω.
	JP3	2-3	SMB_EN pin pulled low disabling SMBus.
	JP4	2-3	CLKIN_SEL_tri pulled low to set CLKIN0 as the input source to all the outputs.

2.1 Hardware Setup

LMKDB1204EVM shows default jumper configuration for the EVM.

To begin using the LMKDB1204EVM, follow the steps below.

1. Verify the EVM default jumper as described in Table 2-1 and LMKDB1204EVM.
2. Change jumper JP9 from position 1-2 to position 2-3 to use USB supply.
3. Connect the USB cable to USB port at J13.
4. Connect 100MHz reference clock to CLKIN0_P/N. Refer to Table 3-8 for different input reference configurations.

2.2 Software Setup

2.2.1 TICS Pro GUI Setup

1. If not already installed, then install TICS Pro software from TI website: TICS Pro Software GUI.
2. Start TICS Pro software.
3. Select the LMKDB1204 profile from *Select Device* → *Clock Distribution with Divider* → *LMKDB1204*.
4. Confirm communication with the board:
   a. Click *USB Communication* from the menu bar.
   b. Click *Interface* to launch the *Communication Setup* pop-up window.
   c. Confirm the following fields from the *Communication Setup* pop-up window:
      i. Make sure *USB2ANY* is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then the user must release that interface by changing the interface setting to *DemoMode*.
      iii. Click *Identify* to blink LED shown in Figure 2-1. After clicking the *Identify* button, the LED flashes quickly at about 0.5 second on, 0.5 second off for about 5 seconds. This confirms the connection to the board. However, be aware that USB2ANY devices that are connected to the PC, but not attached to a TICS Pro profile, can blink at a slow rate of 1 second on, 1 second off continuously.

d. Confirm all the fields match the ones shown in Figure 2-2.

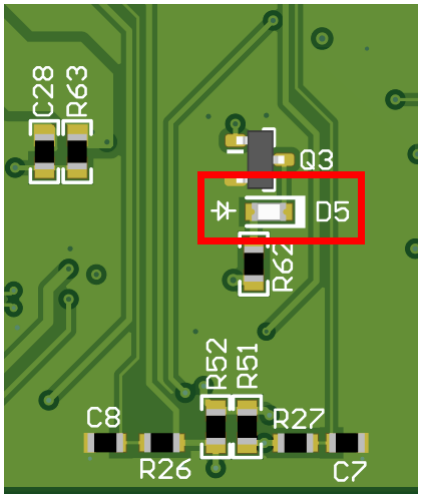


Figure 2-1. USB LED

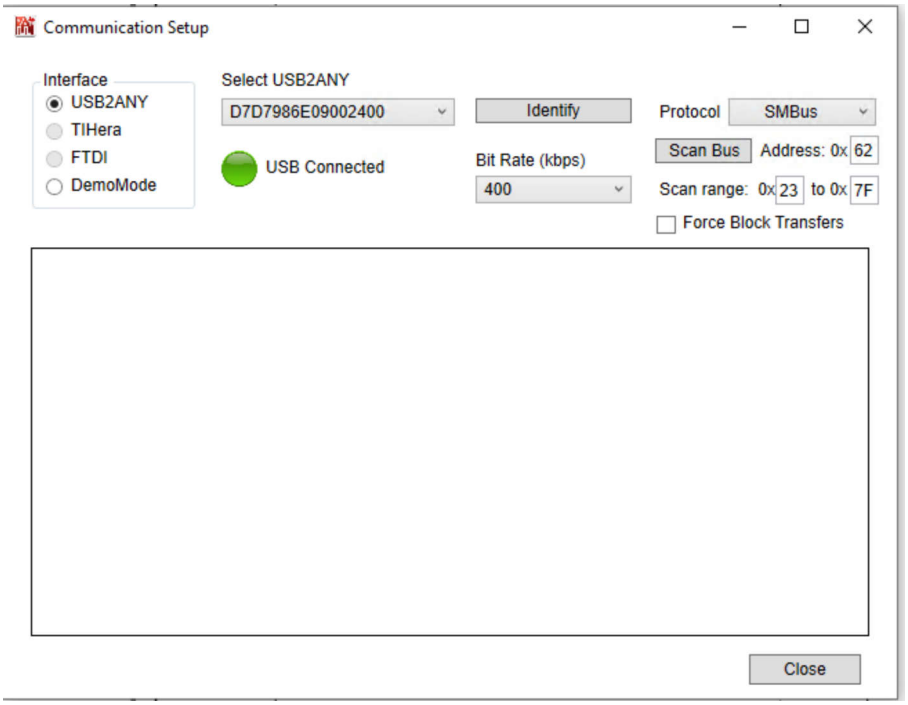


Figure 2-2. Communication Setup

2.2.2 Power Up Sequence

By default, the LMKDB1204 and the GUI are started with the default configuration. When using the on-board USB supply option, the following steps can be followed to avoid any improper power up sequence issue when plugging in the USB cable to the EVM.

1. After all the steps above, toggle the *USB 3V3 Supply* pin *Low* → *High* for power reset. This step is not necessary but recommended if there are any issues with readback or improper start up on EVM.
2. Click on *Scan Bus* in the *Communication Setup* window to find and update device address.
3. Click on *Read All Regs* to update the register readback from the device.

2.3 EVM Measurements

Measurements can now be made on the clock outputs using an oscilloscope or a phase noise analyzer.

3 Hardware

3.1 Device Operation Modes

The LMKDB1204 can be configured to start up in one of two modes during power-on/reset (POR). SMB_EN pin determines the mode of operation during power supply ramp up. Below are both of the modes for the device:

1. **SMBus Mode Disabled** (EVM default): When SMB_EN pin is set to low during the power up, SMBus mode is disabled, output enable (OE) pin control is possible on all outputs, and CLKIN_SEL_tri pin is enabled to select which CLKIN drives which output bank.
2. **SMBus Mode Enabled**: When SMB_EN pin is set to high during power up, SMBus mode is enabled and OE3# and CLKIN_SEL can only be controlled via SMBus.

3.2 EVM Configuration

The LMKDB1204EVM can be configured for multiple modes using on board MCU and external power or USB supply options. The following sections describes power, logic, clock input, and output interfaces on the EVM and how to configure the EVM accordingly.

Some of the key components and the reference designator are noted in Table 3-1.

Table 3-1. Key Components Reference Designator and Descriptions

Item No.	Reference Designators	Description
1	U1	LMKDB1204.
2A	J19	External VDD option through SMA port.
2B	JP9	Jumper header to select between external or onboard 3.3V USB supply option.
3	J1, J2, J3, J4	SMA Ports for clock input (CLKIN#_P, CLKIN#_N).
4	J5 through J12	SMA Ports for clock outputs (CLK#_P, CLK#_N).
5	JP1	CLKPWRGD_PD# pin header jumper to enable or disable the LMKDB1204.
6	JP2	ZOUT_SEL pin header jumper to select 85Ω or 100Ω output impedance.
7	JP3	SMB_EN pin header jumper to enable or disable SMBus mode during power-up.
8	JP4	CLKIN_SEL_tri pin header jumper to select which CLKIN drives which outputs.
9	U7	USB power option LDO.
10	U5	MSP430F5529IPN MCU.

3.2.1 Power Supply

The LMKDB1204 has VDD, VDD_DIG, VDD_IN0, VDD_IN1, VDD_BANK0, and VDD_BANK1 supply pins that operate from 1.8V ± 10% and 3.3V ± 10%.

The EVM has two different method of supplying power to the device as listed in Table 3-2.

For 3.3V supply option, EVM has an on-board LDO to reduce the need for external power supply and operate the EVM using USB cable with a PC. To use 1.8V ± 10% supply on the EVM, J19 can be used to force external supply voltage.

Table 3-2. EVM Power Modes

EVM Power Mode	Designator	Position	Supply Voltage	Description
External (default)	J19	External supply	1.8V ± 10% or 3.3V ± 10%	External supply option is selected.
	JP9	1-2		
USB	J19	Not connected	3.3V ± 10%	USB 3.3V supply option is selected.
	JP9	2-3		

3.2.2 Logic Input and Outputs

The logic input and output pins on LMKDB1204 provides option for selecting different device modes, input clock selection, output enable / disable control, loss of signal (LOS) detection, and output impedance selection. The following section describes the function of different input and output logic pins. Voltage levels for input pins can be set through TICSPro GUI using the MSP430 MCU or using on-board jumper as specified in Table 3-1.

Table 3-3. Device Start-Up Modes

SMB_EN INPUT LEVEL	START-UP MODE
Low (default)	SMBus inactive.
High	SMBus active. On-board jumper headers on JP4 and JP5 need to be removed for proper operation.

Table 3-4. Clock Input Selection

CLKIN_SEL_tri Output Level	Function
Low	CLKIN0 is the input source for all outputs.
High	CLKIN1 is the input source for all outputs.
Hi-Z	CLKIN0 is the input source for BANK0 outputs and CLKIN1 is the input source for BANK1 outputs. JP4 must be removed and *R51* must be depopulated. If SMBus mode needs to be activated after removing *R51*, then on-board header jumper JP4 needs to be set to high.

Table 3-5. Output Enable Pin Control

OE0# to OE3# INPUT LEVEL	OUTPUT STATUS
Low (default)	Enabled.
High	Disabled

Note

For OE3#, when controlling the pin by only using the on-board jumper header on JP5 (and not the MSP430 MCU) and SMBus is disabled/SMB_EN = high, then*R52* must be depopulated. If SMBus mode needs to be activated after removing *R52*, then on-board header jumper on JP5 needs to be set to high.

Table 3-6. Loss of Signal (LOS) Detection (Status pin)

LOSb OUTPUT LEVEL	LOS STATUS
Low	Not detected
High	Detected

Table 3-7. LP-HCSL Differential CLock Output Impedance Select

ZOUT_SEL Output Level	Function
Low	LMKDB1204 has 85Ω output termination.
High	LMKDB1204 has 100Ω output termination.

3.2.3 Clock Input

LMKDB1204 can support different input interfaces for either CLKIN depending on the input swing and common mode voltage. There are four input interfaces type that can be configured on LMKDB1204 using external components and internal termination schemes as shown in Figure 3-1. If using a signal generator, then make sure to populate *R12* and/or *R23* with a *100Ω* resistor or use internal / external 50Ω termination to ground.

1. DC Coupled HCSL / LP HCSL Input.
2. DC Coupled LVDS Input.
3. External AC Coupled Input.
4. Internal 50Ω to ground terminations.

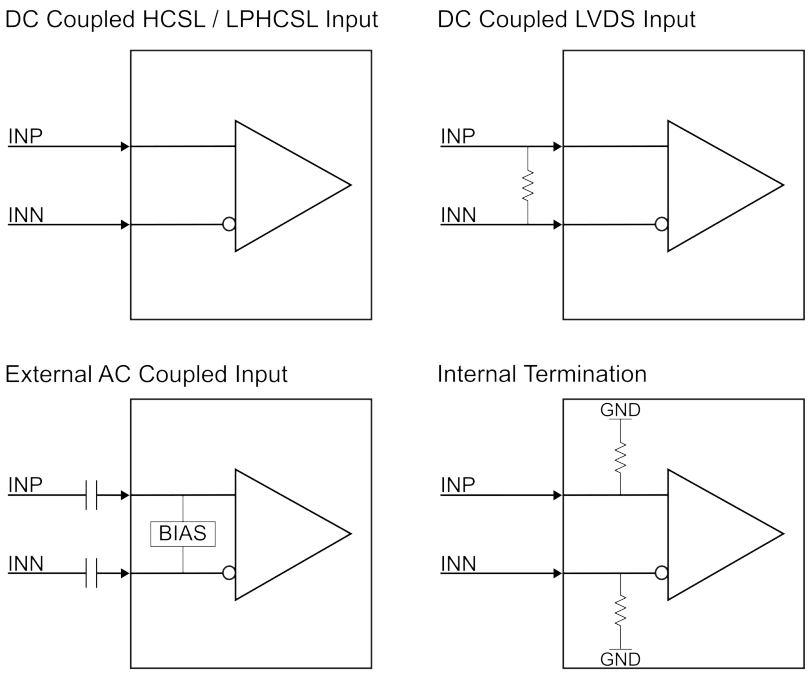


Figure 3-1. Input Interfaces

Table 3-8 outlines how to setup all different interfaces supported by LMKDB1204.

Table 3-8. Input Interfaces

Input Interface	Configuration
DC coupled HCSL / LPHCSL (default)	This is the default for the EVM for both clock inputs. *R10, R13* and/or *R20, R24* values are ***0Ω*** and *Input Interface Type* on *Input* page is selected to *DC Coupled* for each input.
DC coupled LVDS input	Populate *R12* and/or *R23* with a ***100Ω*** resistor and set *Input Interface Type* on *Input* page to *DC Coupled* for each DC coupled LVDS input.
External AC coupled input	Replace *R10, R13* and/or *R20, R24* with ***0.1uF*** capacitor and set *Input Interface Type* on *Input* page to *AC Coupled* for each external AC coupled input.
Internal termination	To enable internal 50Ω to ground terminations. Set the *Input Termination* on *Input* page to *Enabled*.

3.2.4 Clock Outputs

LMKDB1204 has four differential clock outputs (CLK[0:3]_P/N). All the outputs are DC coupled with a capacitive load of 2pF.

WARNING
DC-coupled clocks must not be directly connected to RF equipment which cannot accept DC voltages greater than 0V, such as spectrum analyzers and phase noise analyzers.

Table 3-9. ZOUT_SEL

ZOUT_SEL OUTPUT LEVEL	OUTPUT IMPEDANCE
Low (default)	85Ω output impedance
High	100Ω output impedance

3.2.5 Status Outputs, LEDs, and Test Points

LMKDB1204EVM have status output signal from LMKDB1204, LEDs, and test points to monitor signal and supply voltage on the board. Table 3-10 summarizes all the status signals and test points on the board.

Table 3-10. Status Output, LEDs, and Test Points

Function / Test Signal	Status Pin / LED Designator	Description
LOSb	TP9	Test point to monitor LOSb status.
	D1	LED status light for LOSb detection.
VDD	D7	LED status light for VDD supply pin.
	TP1	Test point for VDD supply pins.
VDD_IN0	TP3	Test point for VDD_IN0 supply pins.
VDD_IN1	TP5	Test point for VDD_IN1 supply pins.
VDD_BANK0	TP2	Test point for VDD_BANK0 supply pins.
VDD_BANK1	TP4	Test point for VDD_BANK1 supply pins.
VDD_IO	TP6	Test point for VDD_IO supply pins.
VDD_MAIN	D6	LED status light for VDD supply selected from USB option or External option through JP17.
GND	TP7, TP8	Test points for GND reference on the board.
USB LED	D5	USB LED status light to verify USB2ANY communication to board.
U2A_3V3	D3	USB2ANY LDO supply status LED.
	U6	Test point for USB2ANY LDO supply pin.

4 Software

4.1 TICS Pro LMKDB1204 Software

LMKDB1204 TICS Pro GUI provides full functionality to interact with the device through SMBus and OE pin options. TI recommends to use this GUI interface while evaluating LMKDB1204EVM to fully utilize all functionalities. The GUI interface consists of *User Controls* and *Raw Register* page to write directly into each register bit or field values. The GUI interface also has *Input*, *Device Info*, and *Output* pages, which can be used to evaluate different device functions. The following sections describe the details of each page.

4.1.1 Input

Input page provides access to configure different input modes and read back live status for loss of signal (LOSb) for both inputs, as shown in Figure 4-1

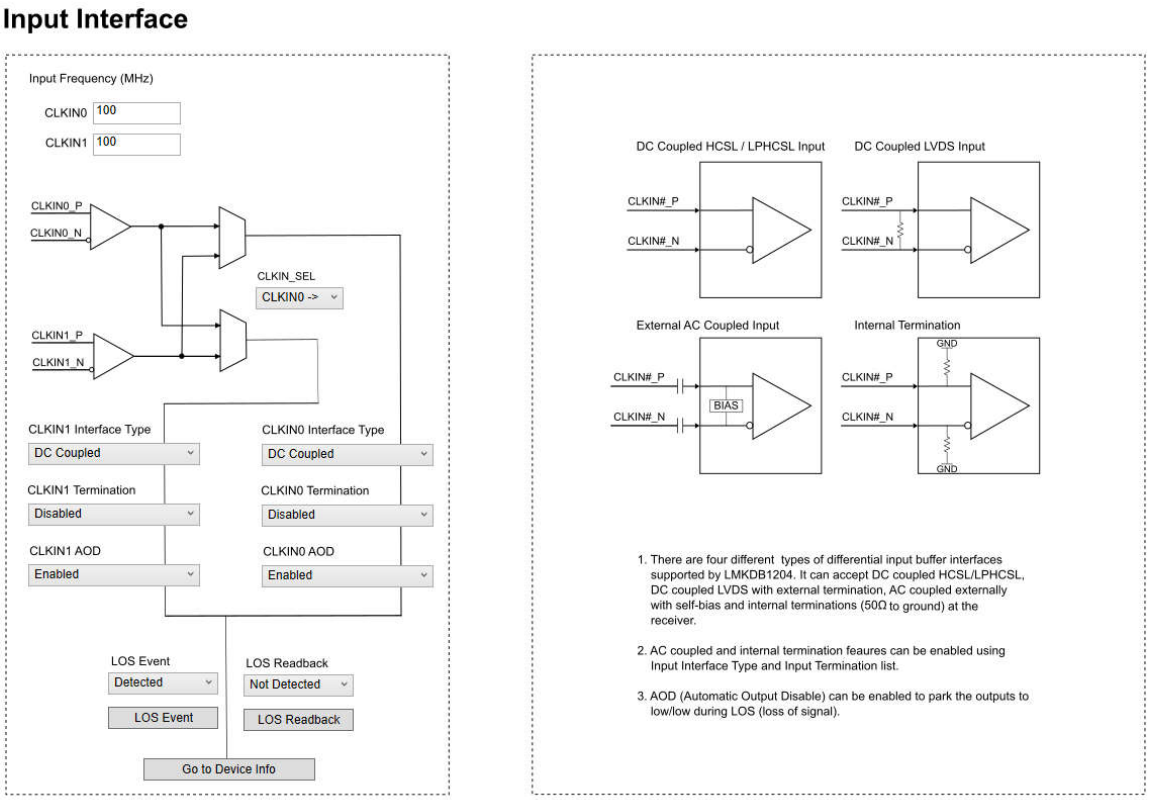


Figure 4-1. Input Interface

4.1.1.1 Input Selection (CLKIN_SEL Register)

The CLKIN_SEL register allows selection to determine which inputs are buffered to which outputs. The drop-down menu options are:

- **0x0:** CLKIN0 → BANK0: Input given to CLKIN0 is buffered to all outputs
- **0x1:** CLKIN0 → BANK0 & CLKIN1 → BANK1: Input given to CLKIN0 is buffered to outputs on BANK0 and inputs given to CLKIN1 is buffered to outputs on BANK1.
- **0x3:** CLKIN1 → BANK1: Input given to CLKIN1 is buffered to all outputs.

4.1.1.2 Input Interface Type

Input interface type for either input can be configured as AC Coupled or DC coupled. AC coupled option provides internal bias to the clock inputs connected.

4.1.1.3 Input Termination

Internal 50Ω to ground terminations can be enabled or disabled using the *Input Termination* drop-down menu for either input.

4.1.1.4 Auto Output Disable (AOD)

Automatic output disable (AOD) can be enabled or disabled using this control for either input. AOD is enabled by default on both inputs on the LMKDB1204. AOD disables the outputs when there is a loss of signal (LOS) detected on the input. When AOD is disabled, outputs follow the input clock in DC state.

4.1.1.5 LOS Event

LOS Event Status gives information when there is a loss of signal (LOS) event. Make sure to clear the LOS event afterward by writing a 1 or selecting the *Detected* option from the LOS Event drop-down menu.

4.1.1.6 LOS Readback

LOS Readback provide live status of loss of signal detection.

4.1.2 Device Info and EVM Setup

Device Info page contains three different sections and the LMKDB1204EVM information.

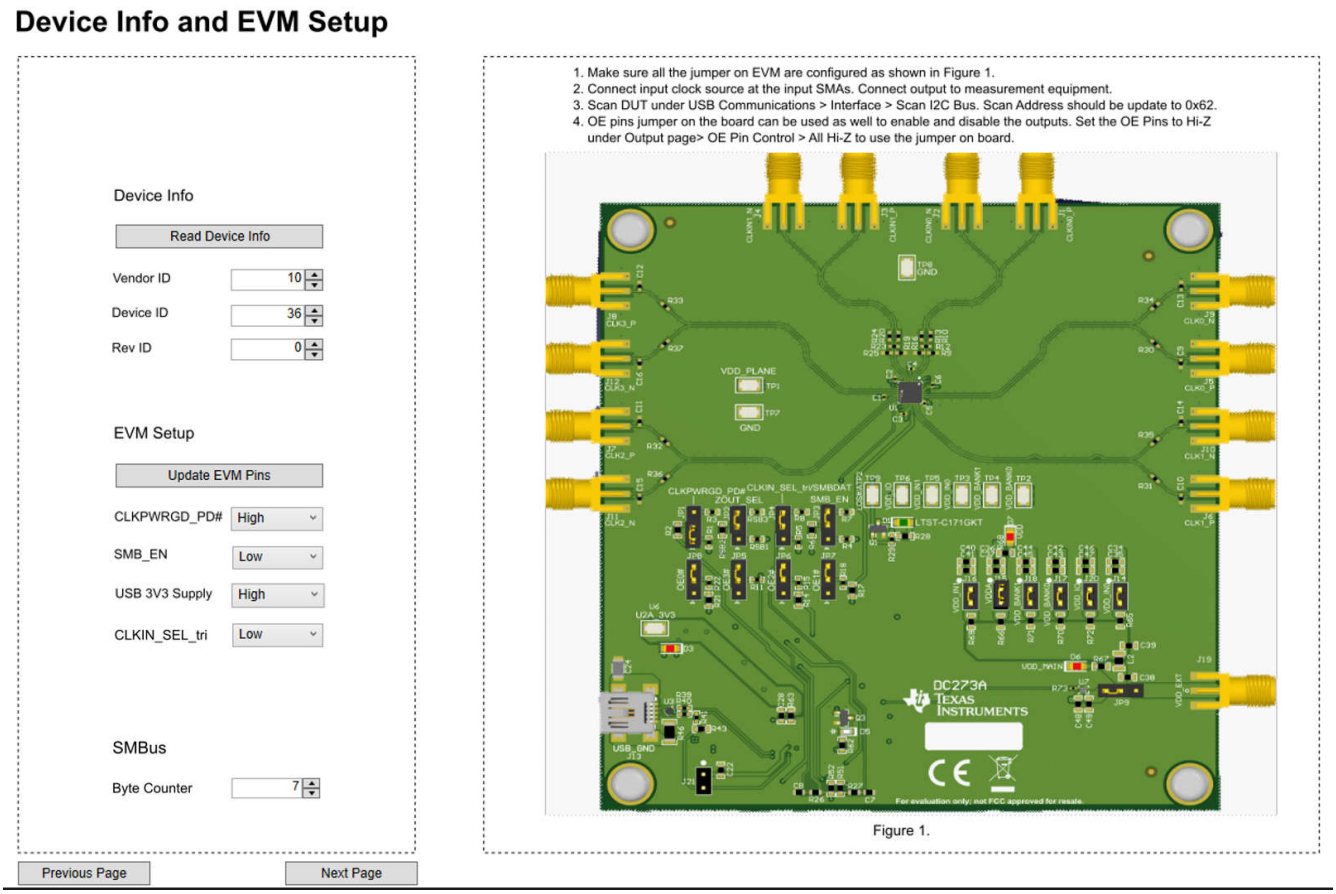


Figure 4-2. Device Info

4.1.2.1 Device Info

This section contains following information related to device which can be read back using *Read Device Info* button.

1. Vendor ID
2. Device ID
3. Rev ID

4.1.2.2 EVM Setup

The EVM setup has key pins to configure the device which can be controlled by software. The tables below outline the usage for each pin option. When Hi-Z is selected for any pin, then the onboard header jumpers can be used to force external voltages on the pins instead of controlling the pins via software.

Table 4-1. CLKPWRGD_PD#

Pin Level	Function
Low	LMKDB1204 power down mode.
High (default)	LMKDB1204 normal operation mode.
Hi-Z	When Hi-Z is selected, on-board header jumper on JP1 can be used to force external voltages on the pin.

Table 4-2. SMB_EN

Pin Level	Function
Low (default)	LMKDB1204 has SMBus inactive. Setting of SMB_EN pin can only be set at power-up.
High	LMKDB1204 has SMBUS active. Setting of SMB_EN pin can only be set at power-up. On-board jumper headers on JP4 and JP5 need to be removed for proper operation.
Hi-Z	When Hi-Z is selected, on-board header jumper on JP3 can be used to force external voltages on the pin. Setting of SMB_EN pin can only be set at power-up.

Table 4-3. CLKIN_SEL_tri

Pin Level	Function
Low	CLKIN0 is the input source for all outputs.
High	CLKIN1 is the input source for all outputs.
Hi-Z	When Hi-Z is selected, on-board header jumper on JP4 can be used to force external voltages on the pin. If selecting the mid-level of CLKIN_SEL_tri pin, (CLKIN0 is the input source for BANK0 outputs and CLKIN1 is the input source for BANK1 outputs), then on-board header jumper on JP4 must be removed and *R51* must be depopulated. If SMBus mode needs to be activated after removing *R51*, then on-board header jumper on JP4 needs to be set to high.

4.1.2.3 SMBus

Byte counter value determines the number of register readback during block read operation.

4.1.3 Output

The output page in TICS Pro has controls for clock outputs through SMBus and OE pins.

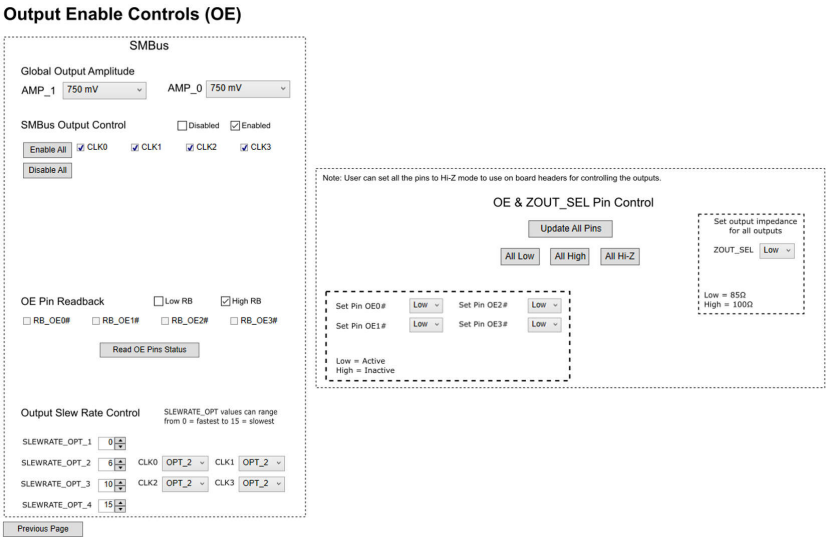


Figure 4-3. Output Enable Controls

4.1.3.1 SMBus

SMBus can be used to control the following parameters on the outputs:

1. Global Output Amplitude: To program output VOD from 600mV to 975mV with a step size of 25mV.
2. SMBus Output Control: To enable or disable CLK0 through CLK3 via register bits.
3. OE# Pin Readback: To read status of OE# pins.
4. Output Slew Rate Control: To program output slew rate values.

4.1.3.1.1 Output Slew Rate Control

The LMKDB1204 has 4 registers where 4 different slew rate values can be stored. After storing the desired slew rate values in SLEWRATE_OPT_# registers, 1 of those 4 slew rates can be assigned to each output by using the drop-down menus next to the desired output. There are 16 different slew rate values possible, where 0x0 is the fastest slew rate and 0xF is the slowest slew rate.

The default slew rate values for each SLEWRATE_OPT_# are shown in Table 4-4. The default slew rate for all outputs is set to SLEWRATE_OPT_2 = 0x6. For more information, refer to the LMKDB1204 data sheet (SNAS855).

Table 4-4. Default SLEWRATE_OPT_# Values

Register Field Name	Default Value	Default Slew Rate
SLEWRATE_OPT_1	0x0	Fastest
SLEWRATE_OPT_2	0x6	Fast (default for all outputs)
SLEWRATE_OPT_3	0xA	Slow
SLEWRATE_OPT_4	0xF	Slowest

4.1.3.2 OE and ZOUT_SEL Pin Control

Low and High voltage levels can be set on all the pins using the GUI without the need of on-board headers. If on-board jumper headers are used, set all the OE# and ZOUT_SEL pins to Hi-Z using the *All Hi-Z* button under the *OE & ZOUT_SEL Pin Control.*

Table 4-5. OE# Pins

Pin Level	Function
Low	LMKDB1204 has CLK# enabled.
High	LMKDB1204 has CLK# disabled.
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin. For OE3# (JP5),*R52* must be depopulated to certify proper operation. If SMBus mode needs to be activated after removing *R52*, then on-board header jumper JP5 needs to be set to high.

Table 4-6. ZOUT_SEL

Pin Level	Function
Low	LMKDB1204 has 85Ω output termination.
High	LMKDB1204 has 100Ω output termination.
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin.

5 Implementation Results

5.1 Typical Phase Noise Characteristic

Figure 5-1 shows a typical phase noise performance for 156.25MHz reference clock input from the SMA100B.

LMKDB1204EVM was configured in cascade mode to get these measurements, which were obtained by following these steps:

1. SMA100B → LMKDB1204EVM input. Then, LMKDB1204EVM to secondary LMKDB1204 EVM. This was done to get a fast slew rate at the input. Other methods like clipping a circuit can be used to get a desired slew rate and square wave form as well outputted from the SMA100B.
2. Output phase noise is measured through a Balun to the differential waveform from the LMKDB1204 into a single-ended waveform for the phase noise analyzer.

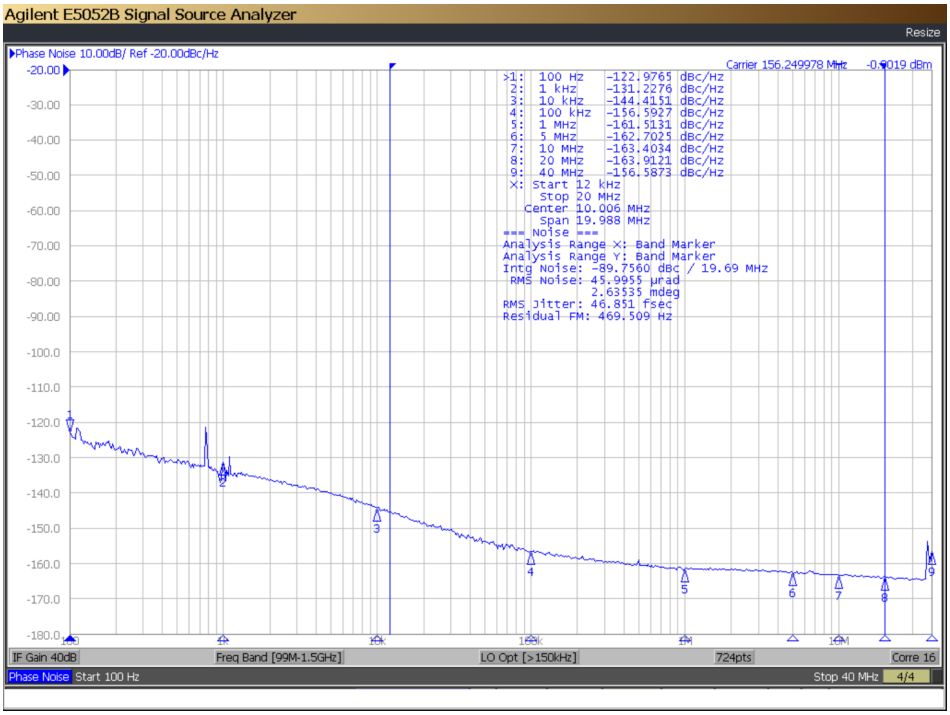


Figure 5-1. LMKDB1204 Output Clock Phase Noise

6 Hardware Design Files

6.1 Schematics

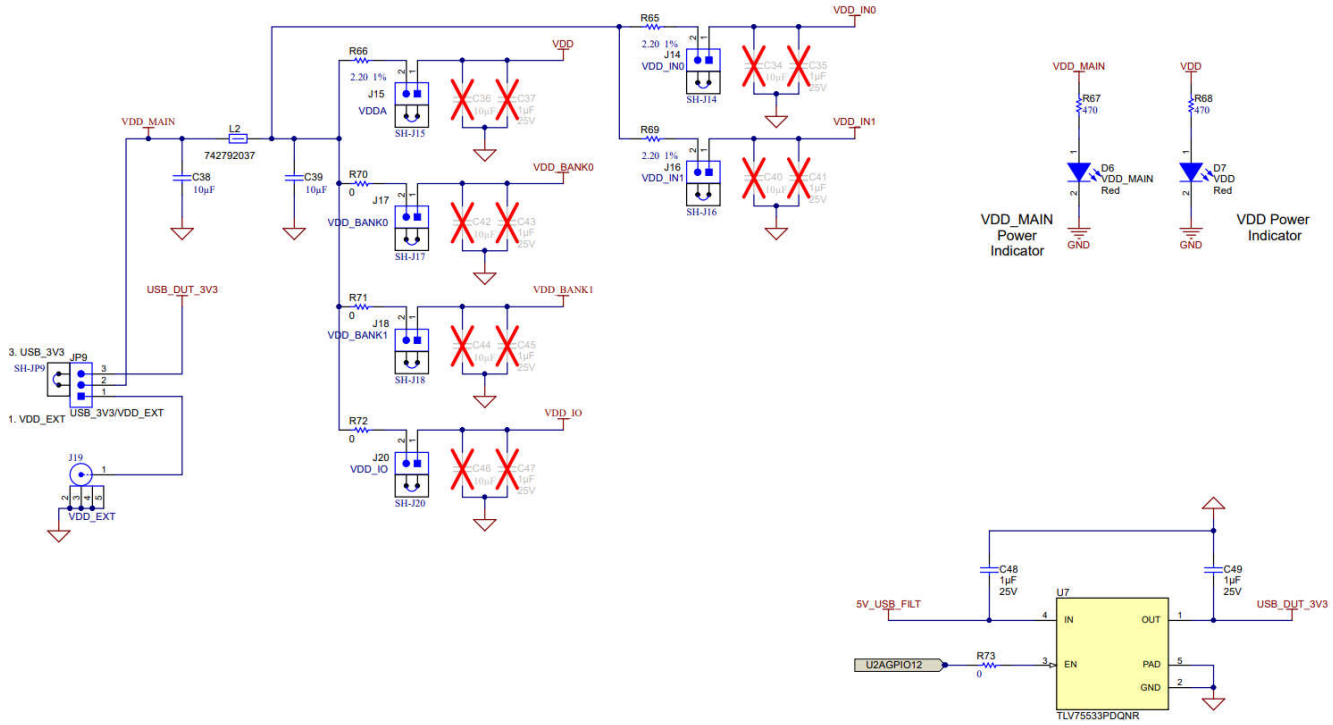


Figure 6-1. Power Supply (External and USB option)

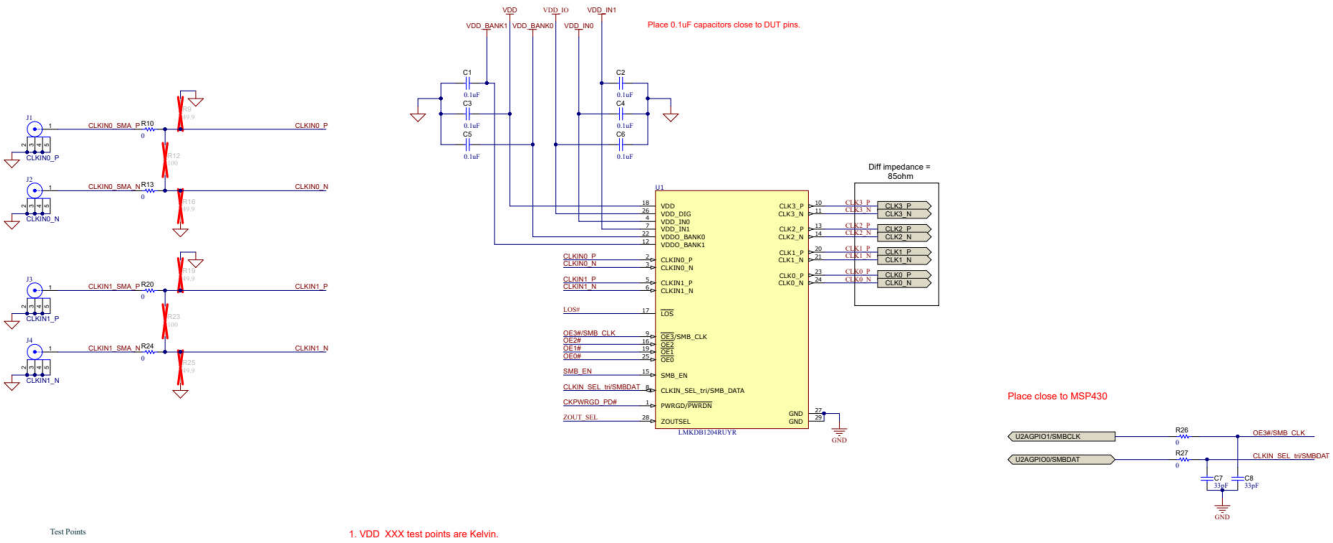


Figure 6-2. LMKDB1204 Device and CLKIN#_P/N Reference

1. Differential impedance is 85 ohms.
2. Trace length should be matched with in +/- 2 MILS
3. Place load capacitor 2pF close to SMA connectors.

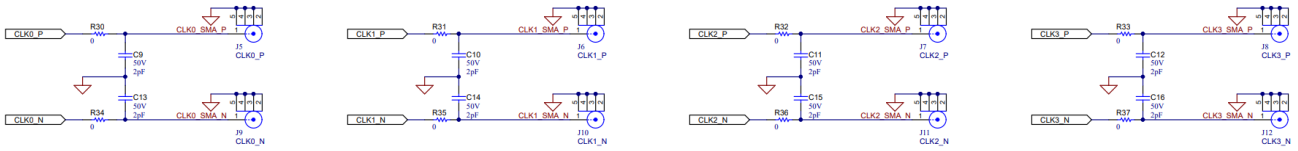


Figure 6-3. Clock Outputs CLK0 to CLK3

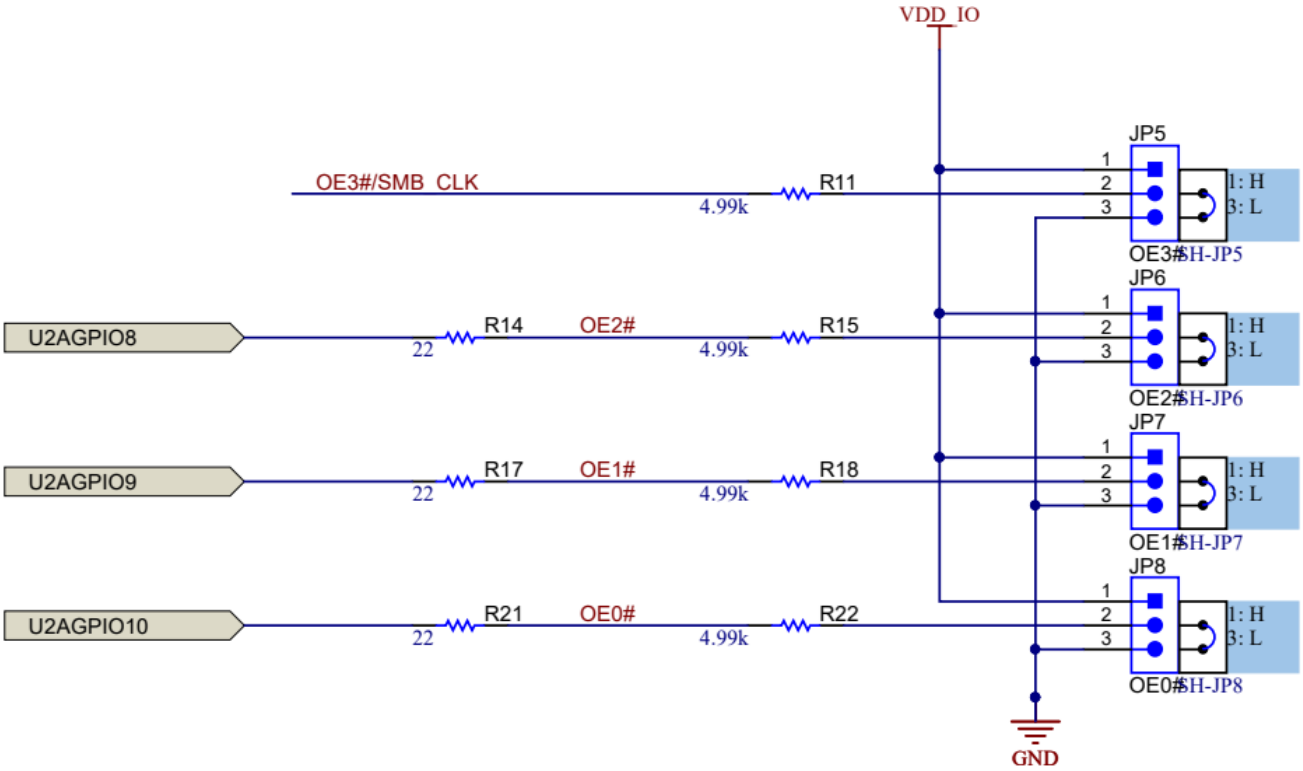


Figure 6-4. Output Enable Pins (OE#)

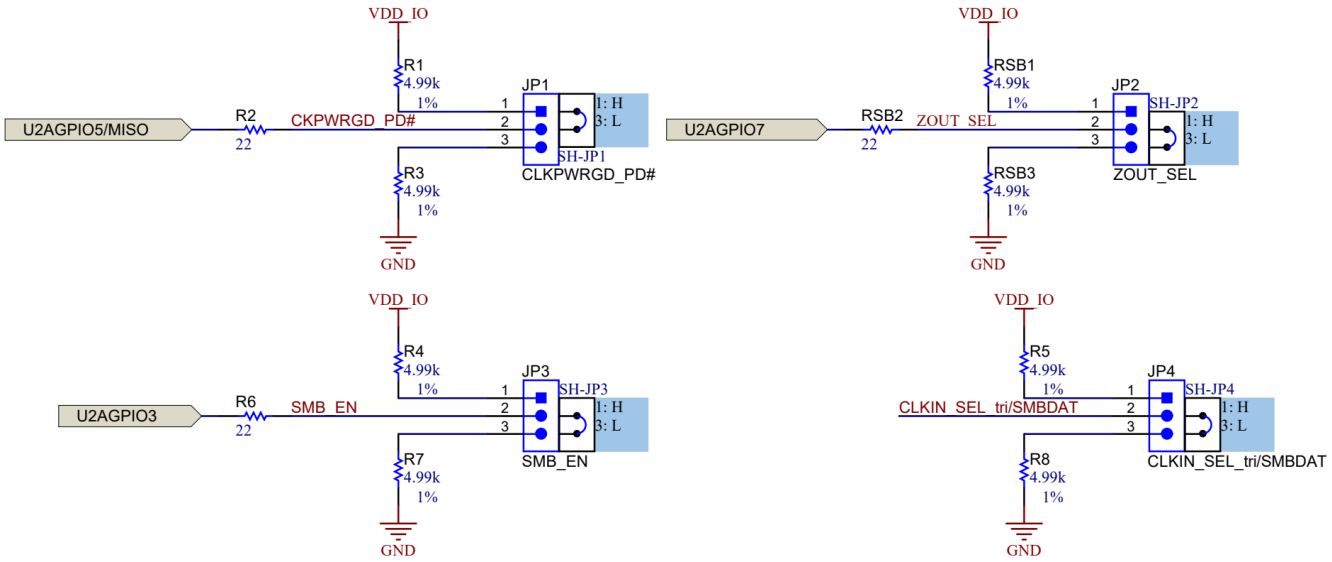


Figure 6-5. Logic I/O Jumpers

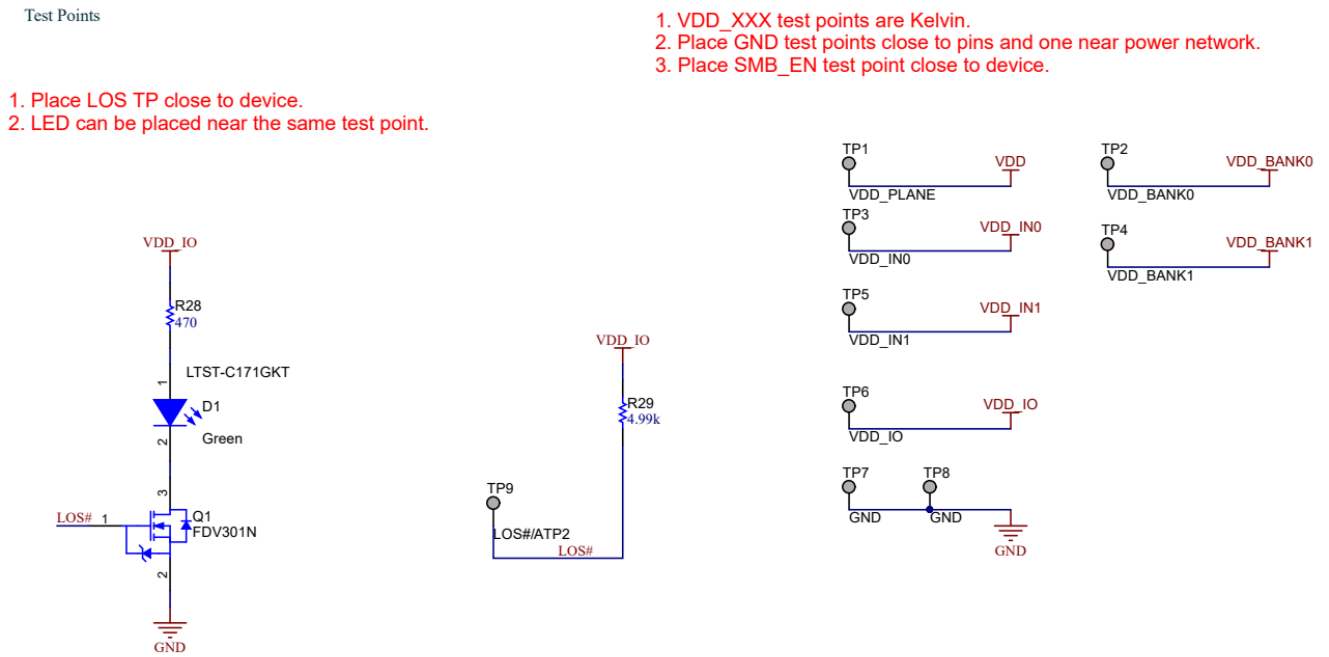


Figure 6-6. Status LEDs and Test Points

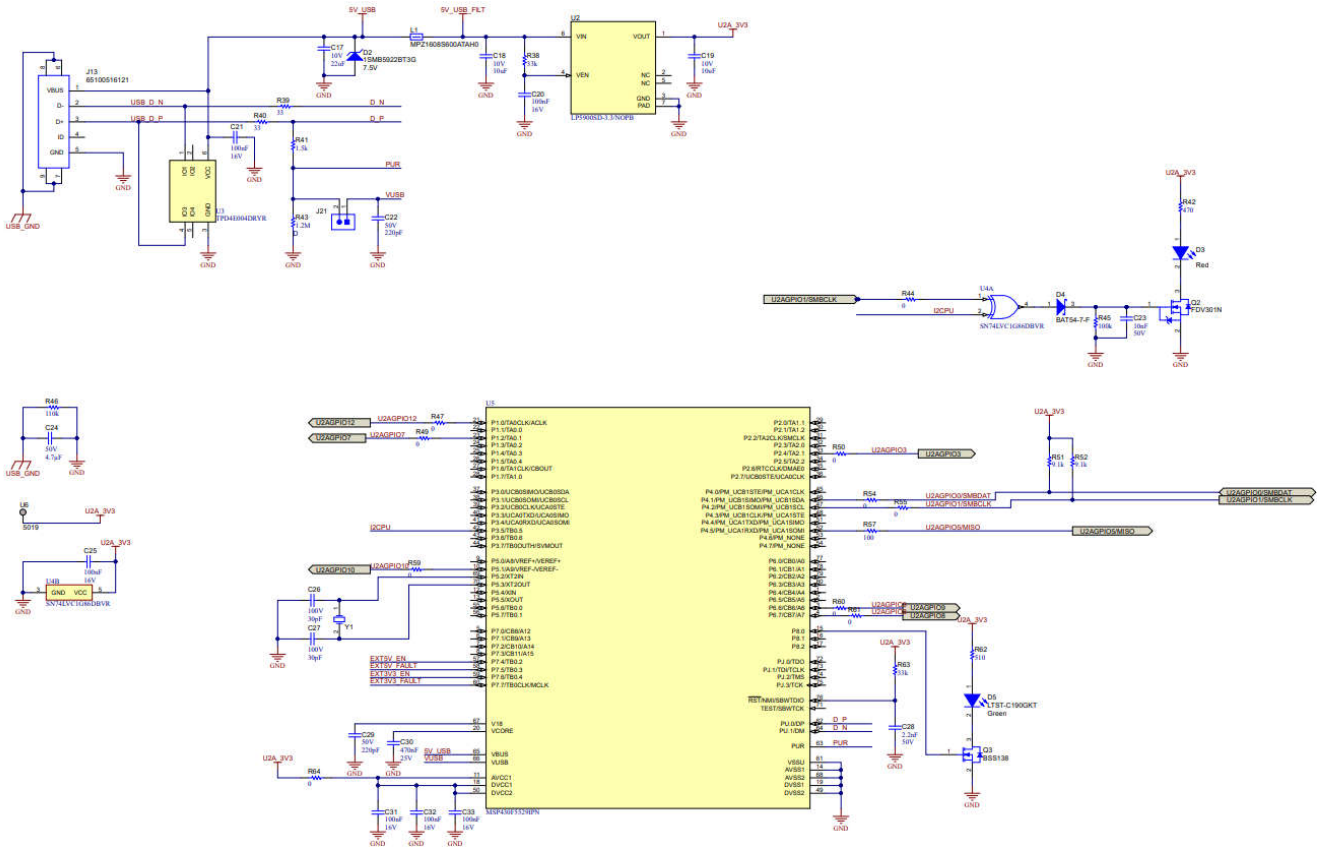


Figure 6-7. USB Schematic

6.2 PCB Layouts

Layer Stackup :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	Top Layer	Copper	2.10mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	GND 1	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	10.00mil	4.2	
3	Signal-1	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	18.60mil	4.2	
4	PWR	Copper	1.40mil		
	Dielectric 4	FR-4 High Tg	10.00mil	4.2	
5	GND 2	Copper	1.40mil		
	Dielectric 5	FR-4 High Tg	6.00mil	4.2	
6	Bottom Layer	Copper	2.10mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

Figure 6-8. Layer Stackup

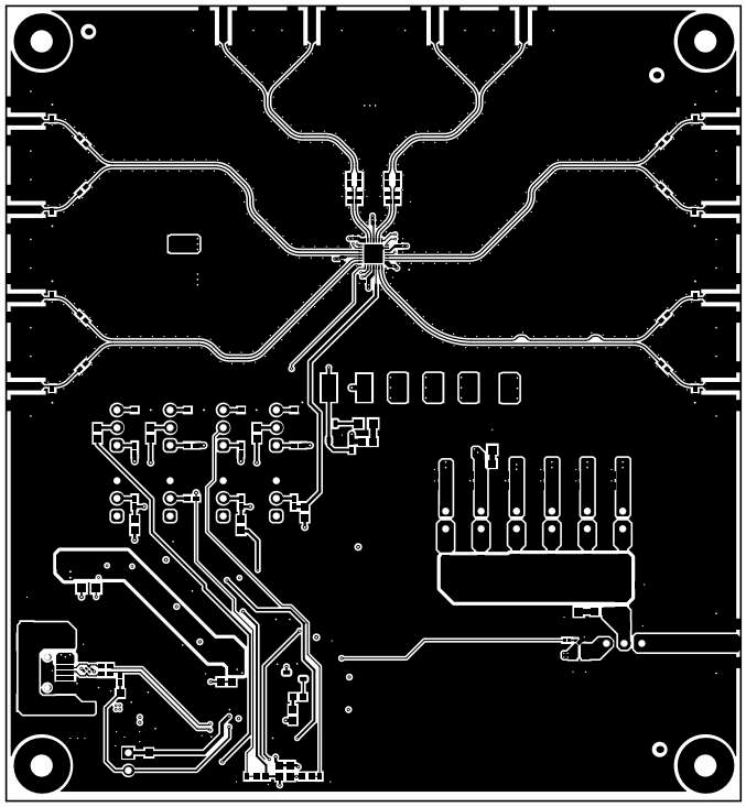


Figure 6-9. Top Layer (CLKIN / CLKOUT Signals)

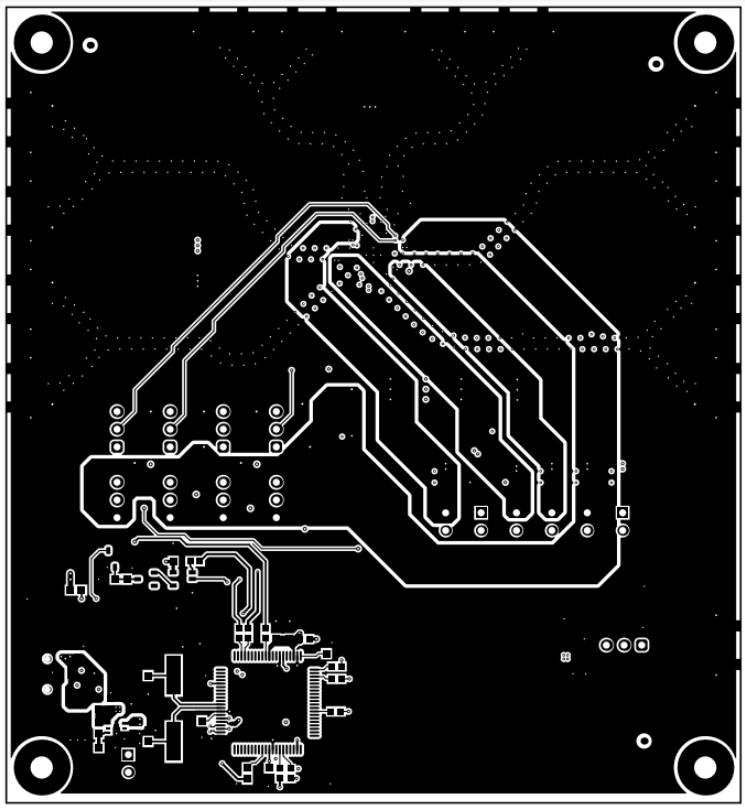


Figure 6-10. Bottom Layer

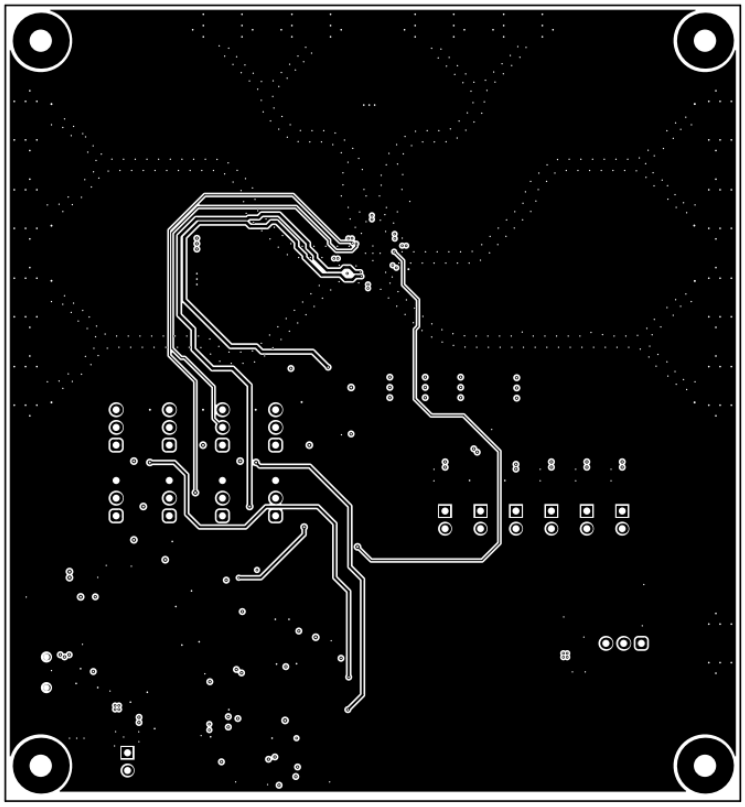


Figure 6-11. Signal 1 Layer

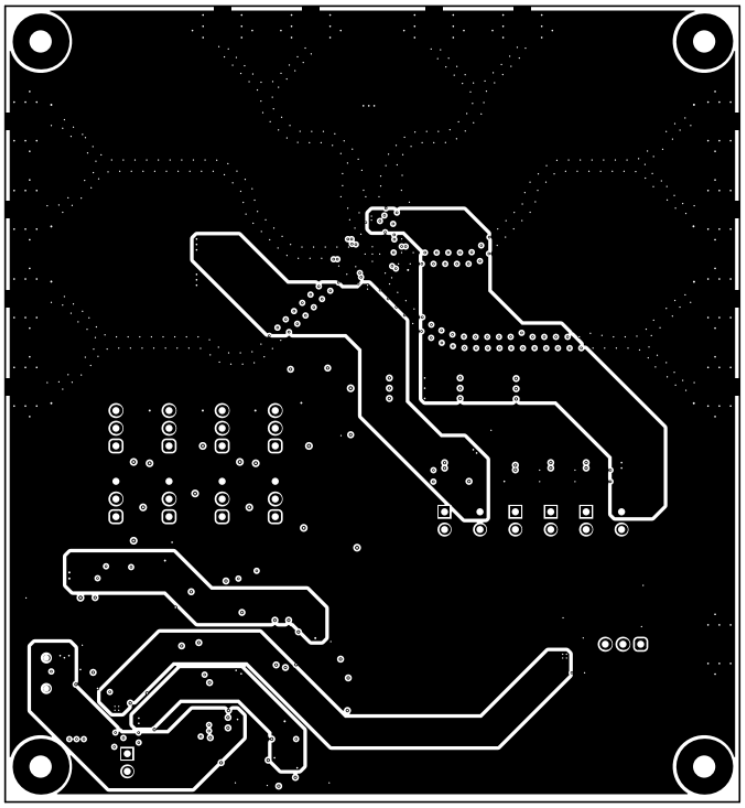


Figure 6-12. PWR Layer

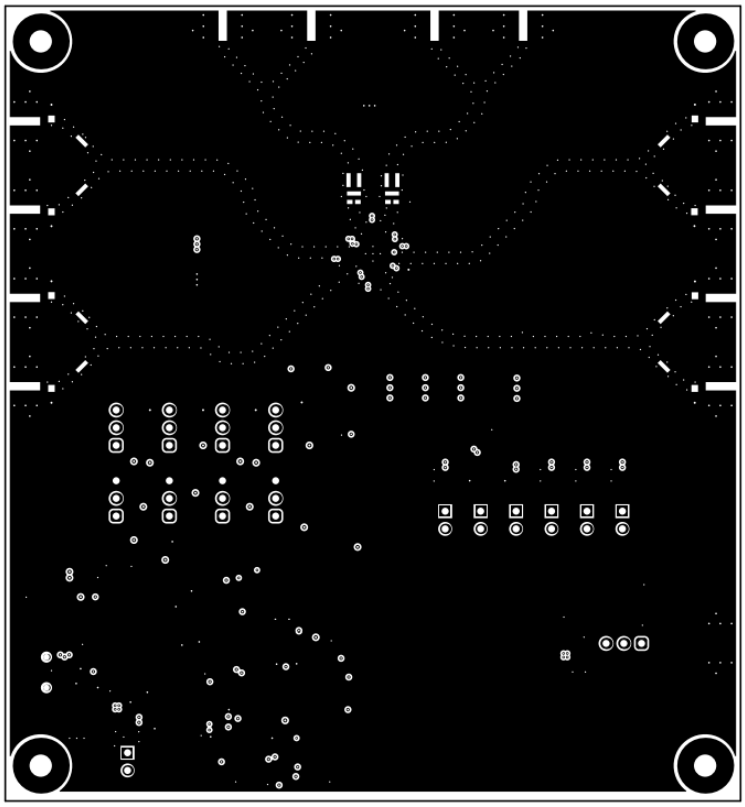


Figure 6-13. GND 1 Layer

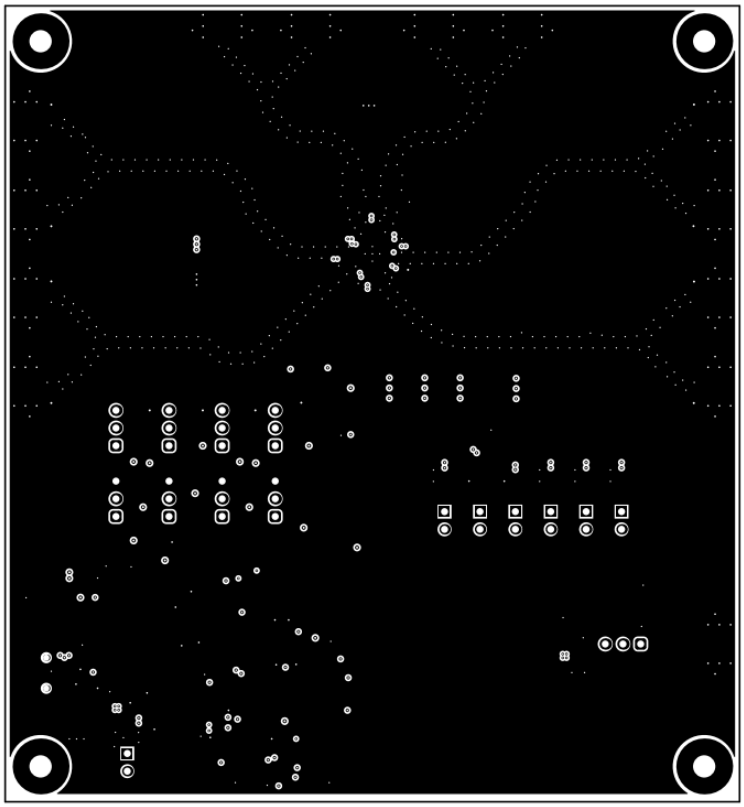


Figure 6-14. GND 2 Layer

6.3 Bill of Materials (BOM)

Table 6-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC273	Any
C1, C2, C3, C4, C5, C6	6	0.1uF	CAP, CERM, 0.1uF, 16V,+/- 10%, X7R, 0201	0201	GRM033Z71C104KE14D	MuRata
C7, C8	2	33pF	CAP, CERM, 33pF, 100V, +/- 5%, C0G/NP0, 0603	0603	06031A330JAT2A	AVX
C9, C10, C11, C12, C13, C14, C15, C16	8	2pF	CAP, CERM, 2pF, 50V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H2R0CA01D	MuRata
C17	1	22uF	CAP, CERM, 22uF, 10V, +/- 20%, X5R, 0805	0805	LMK212BJ226MG-T	Taiyo Yuden
C18, C19	2	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X5R, 0603	0603	GRM188R61A106ME69D	MuRata
C20, C21, C25, C31, C32, C33	6	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 5%, X7R, 0603	0603	C0603C104J4RAC7867	Kemet
C22, C29	2	220pF	CAP, CERM, 220pF, 50V, +/- 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX
C23	1	0.01uF	CAP, CERM, 0.01uF, 50V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C24	1	4.7uF	CAP, CERM, 4.7µF, 50V,+/- 10%, X7R, 1206	1206	C3216X7R1H475K160AE	TDK
C26, C27	2	30pF	CAP, CERM, 30pF, 100V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	GCM1885C2A300JA16D	MuRata
C28	1	2200pF	CAP, CERM, 2200pF, 50V, +/- 10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet
C30	1	0.47uF	CAP, CERM, 0.47F, 25V, +/- 10%, X7R, 0603	0603	GRM188R71E474KA12D	MuRata
C38, C39	2	10uF	CAP, CERM, 10µF, 16V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata
C48, C49	2	1uF	CAP, CERM, 1µF, 25V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105M080AC	TDK
D1	1	Green	LED, Green, SMD	0805 LED	LTST-C171GKT	Lite-On
D2	1	7.5V	Diode, Zener, 7.5V, 550mW, SMB	SMB	1SMB5922BT3G	ON Semiconductor
D3, D6, D7	3	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On
D4	1	30V	Diode, Schottky, 30V, 0.2A, SOT-23	SOT-23	BAT54-7-F	Diodes Inc.
D5	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J19	13		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J13	1		Connector, Receptacle, USB Mini B 2.0, SMT	Connector, Receptacle, USB Mini B 2.0, 5 Position, SMT	65100516121	Wurth Elektronik
J14, J15, J16, J17, J18, J20, J21	7		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9	9		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	60 ohm	Ferrite Bead, 60 ohm @ 100MHz, 3.5A, 0603	0603	MPZ1608S600ATAH0	TDK
L2	1	330 ohm	Ferrite Bead, 330 ohm @ 100MHz, 2A, 0805	0805	742792037	Wurth Elektronik
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1, Q2	2	25V	MOSFET, N-CH, 25V, 0.22A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor
Q3	1	50V	MOSFET, N-CH, 50V, 0.22A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1, R3, R4, R5, R7, R8, R11, R15, R18, R22, R29, RSB1, RSB3	13	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America
R2, R6, R14, R17, R21, RSB2	6	22	RES, 22, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060322R0JNEA	Vishay-Dale
R10, R13, R20, R24, R30, R31, R32, R33, R34, R35, R36, R37	12	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R26, R27, R44, R47, R49, R50, R54, R55, R59, R60, R61, R64, R70, R71, R72	15	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R28, R42, R67, R68	4	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale
R38, R63	2	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333K0JNEA	Vishay-Dale
R39, R40	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R41	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R43	1	1.2Meg	RES, 1.2M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M20JNEA	Vishay-Dale
R45	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R46	1	110k	RES, 110 k, 1%, 0.25 W, 1206	1206	RC1206FR-07110KL	Yageo America

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R51, R52	2	9.1k	RES, 9.1 k, 5%, 0.1 W, 0603	0603	RC0603JR-079K1L	Yageo
R57	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RJNEA	Vishay-Dale
R62	1	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603510RJNEA	Vishay-Dale
R65, R66, R69	3	2.20	RES, 2.20, 1%, 0.1 W, 0603	0603	ERJ-3RQF2R2V	Panasonic
R73	1	0	RES, 0, 5%, .05 W, AEC-Q200 Grade 0, 0201	0201	ERJ-1GN0R00C	Panasonic
SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J20, SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6, SH-JP7, SH-JP8, SH-JP9	15	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, U6	10		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 2:4 LP-HCSL Clock Buffer and Clock MUX	WQFN28	LMKDB1204RUYR	Texas Instruments
U2	1		150mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	NGF0006A	LP5900SD-3.3/NOPB	Texas Instruments
U3	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
U4	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	DBV0005A	SN74LVC1G86DBVR	Texas Instruments
U5	1		25MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U7	1		500mA, Low IQ, Small Size, Low Dropout Regulator, DQN0004A (X2SON-4)	DQN0004A	TLV75533PDQNR	Texas Instruments
Y1	1		Crystal, 24.000MHz, 20pF, SMD	Crystal, 11.4x4.3x3.8mm	ECS-240-20-5PX-TR	ECS Inc.

7 Compliance Information

7.1 Compliance and Certifications

Refer to *LMKDB1204EVM EU Declaration of Conformity (DoC)*

8 Additional Information

8.1 Trademarks

All trademarks are the property of their respective owners.

9 References

For additional information on LMKDB1204, refer to *LMKDB1120/1108/1104/1102/1204/1202 PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX*.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (May 2024)	Page
• Changed default to external power supply instead of USB	3
• Added a step to change to USB supply	3
• Updated *Device Start-Up Modes* table and added note in *Clock Input Selection* and *Clock Output Impedance* tables	6
• Added register writes	9
• Added more information on how the LOS signal is compared and reported back to the user	10
• Added clarification on which jumpers and resistors need to be removed	11

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265