EVM User's Guide: LMX1860SEPEVM

LMX1860-SEP Evaluation Module

Description

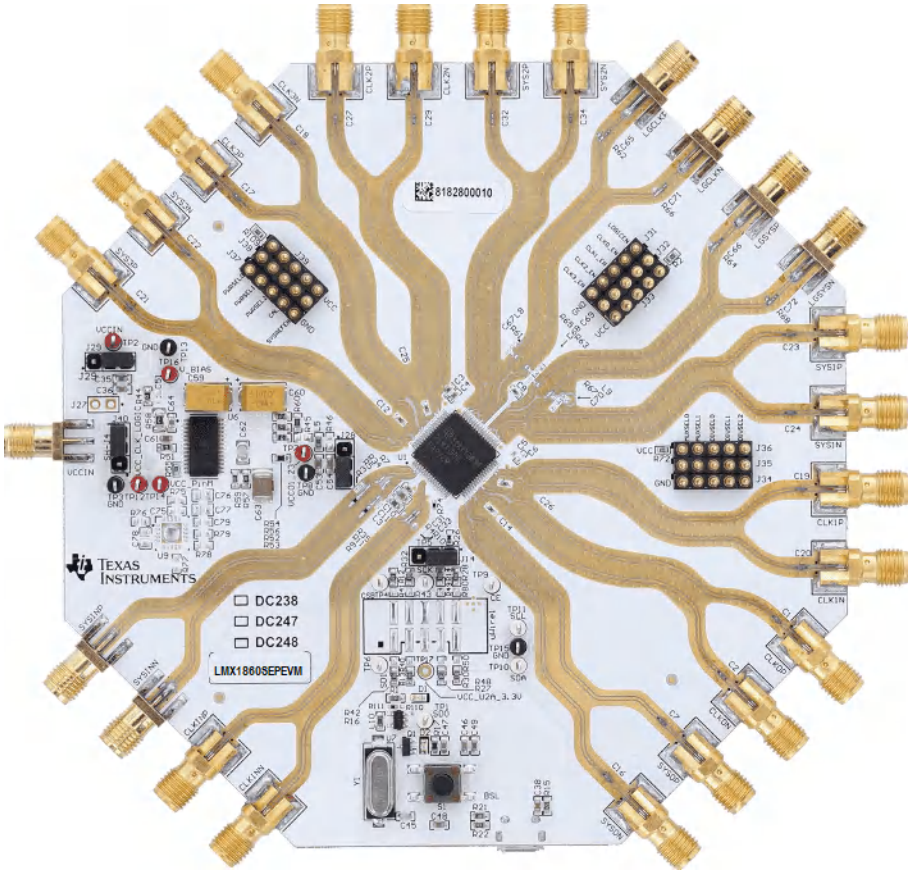
The LMX1860-SEP evaluation module (EVM) is designed to evaluate the performance of the LMX1860-SEP, which is a four-output, ultra-low additive jitter radio-frequency (RF) buffer, divider and multiplier. The device can buffer RF frequencies up to 18GHz, multiply RF outputs up to 6.4GHz, and divide outputs by up to 6.4GHz. This board consists of an LMX1860-SEP device and an integrated USB2ANY programmer.

Features

- 300MHz to 18GHz output frequency
- 4 high-frequency clocks with corresponding SYSREF outputs
  - Shared divide by 2, 3, 4, 5, 6, 7 and 8
  - Shared programmable multiplier ×2, ×3, and ×4
- 3.3V supply voltage (with onboard 2.5V LDOs) or 2.5V supply voltage (with LDOs bypassed)
- –55ºC to +125ºC operating temperature (with onboard MCU bypassed)
- Optional pin mode control without register programming

Applications

- General purpose:
  - Data converter clocking
  - Clock distribution/multiplication/division
- Aerospace and defense:
  - Radar
  - Electronic warfare
  - Seeker front end
  - Phased array antenna/beam forming



1 Evaluation Module Overview

1.1 Introduction

The LMX1860-SEP EVM is an ultra-low additive-jitter RF buffer, divider, and multiplier, with integrated SYSREF generation capability. A separate auxiliary clock divider can be used for FPGAs or other logic ICs. Each RF output (and the logic clock) is paired with a complementary SYSREF output with picosecond-precision delay-tuning capability, and can be operated as a generator (with synchronization capability across multiple devices) or as a repeater.

The EVM can be operated with a 3.3V supply voltage when the onboard LDOs are utilized. The LDOs can be bypassed, in this case the supply voltage is 2.5V.

The EVM contains LMX1860-SEP, two LDOs, a microcontroller and an IO expander. LMX1860-SEP and the LDOs can support –55ºC to +125ºC operation. For high temperature evaluation, use an USB2ANY dongle to control the EVM.

1.2 Kit Contents

Included within each evaluation kit is:

- One LMX1860-SEP EVM board (DC247) with integrated USB2ANY controller
- One USB cable

1.3 Specification

Table 1-1. LMX1860-SEP EVM Specification

Parameter	Value	Conditions	
Supply voltage (VCCIN SMA)	3.1V to 3.5V	On-board voltage regulator outputs are 2.5V	
Supply current	1.3A max.	Various configurations	
CLKIN input frequency	300MHz to 18GHz	Buffer mode	
	150MHz to 6.4GHz	Divider mode	
	3.2GHZ to 6.4GHz	Multiplier mode	CLK_MULT = ×1
	1.6GHZ to 3.2GHz		CLK_MULT = ×2
	1.066GHZ to 2.133GHz		CLK_MULT = ×3
	800MHz to 1.6GHz		CLK_MULT = ×4

1.4 Device Information

The high-frequency capability and extremely low jitter of this device, makes a great design to clock precision, high-frequency data converters without degradation to the signal-to-noise ratio. Each of the four high-frequency clock outputs, and additional LOGICLK output with larger divider range, is paired with a SYSREF output clock signal. The SYSREF signal for JESD interfaces can either be internally generated or passed in as an input and re-clocked to the device clocks. For data converter clocking applications, to have the jitter of the clock be less than the aperture jitter of the data converter is critical. In applications where more than four data converters must be clocked, a variety of cascading architectures can be developed using multiple devices to distribute all the high-frequency clocks and SYSREF signals required. With low jitter and noise floor, this device combined with an ultra-low noise reference clock source is an exemplary design for clocking data converters, especially when sampling above 3GHz.

2 Hardware

2.1 Setup

2.1.1 Evaluation Setup Requirement

At a minimum, evaluation of the buffer mode requires:

- A DC power supply capable of at least 3.1V, 2A
- A high-quality signal source, such as an SMA100B
- A spectrum analyzer or signal analyzer
- A PC with a USB port, running Windows 7 or a more recent version of Windows
- Texas Instruments Clocks and Synthesizers TICS Pro software

Full evaluation requires the following additional hardware:

- A high-speed 4-CH oscilloscope capable of resolving 5ps step size for SYSREF delay tuning
- A 2-CH arbitrary function generator or other pulse source capable of outputting complementary LVDS pulses and DC levels (1.25V ± 0.2V, differential, into 100Ω DC load) for triggering SYSREF, SYNCing the dividers, and determining SYSREF windowing values
- A phase noise analysis system capable of measuring up to 18GHz

2.1.2 Connection Diagram

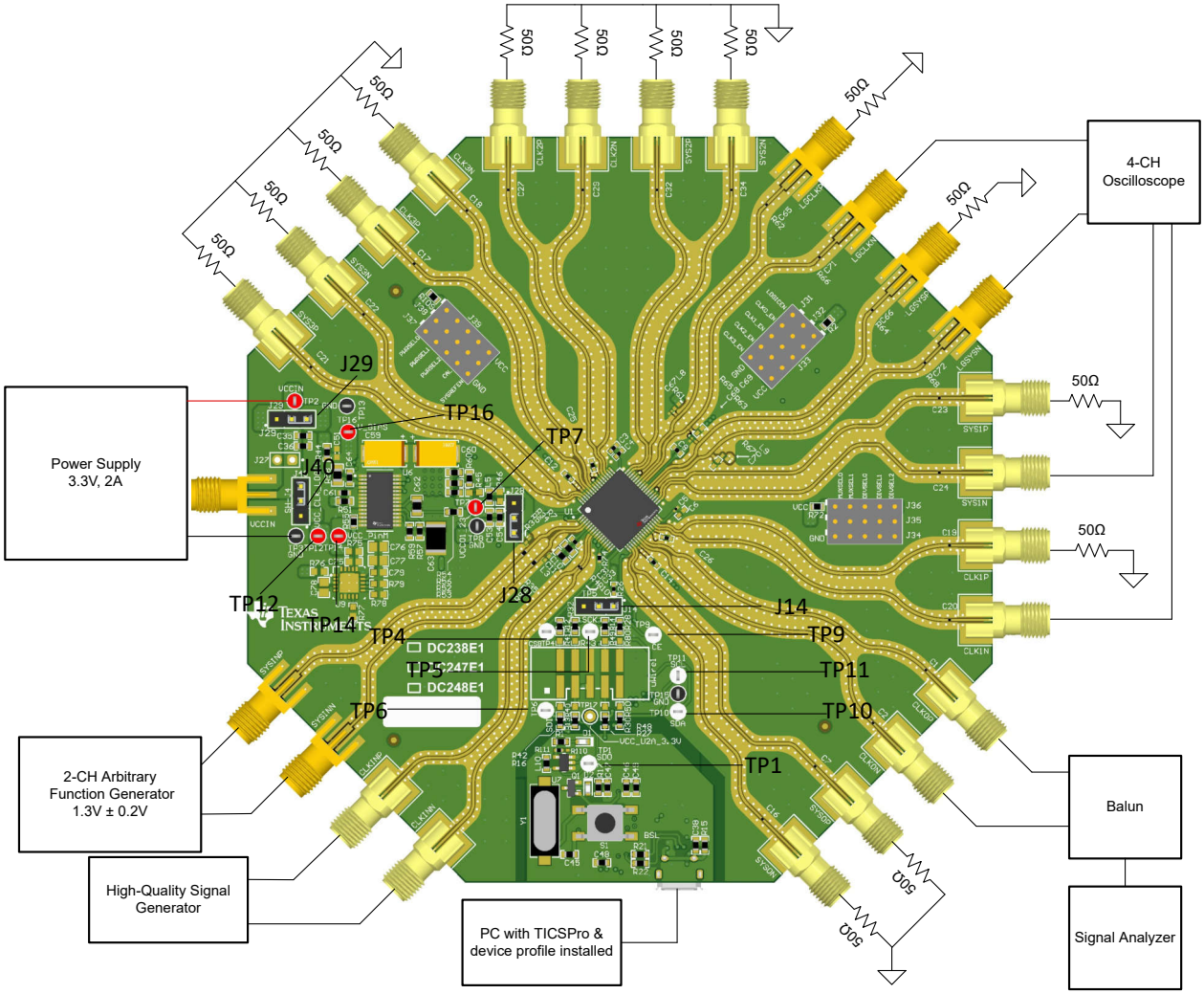


Figure 2-1. EVM Connection Diagram

Table 2-1. SPI Test Points

Test Point	Net
TP1	SDO
TP4	CSB
TP5	SCK
TP6	SDI
TP9	CE

Table 2-2. I2C Test Points for IO Expander

Test Point	Net
TP10	SDA
TP11	SCL

Table 2-3. Supply Voltage Test Points

Test Point	Net
TP7	VCC01_23
TP12	VCC_CLK_LOGIC
TP14	VCC_PinM
TP16	VCC_BIAS

Table 2-4. VCC Power Jumpers

Header	Net	Short Position	Configuration
J14	CE	1-2 (EVM default)	CE pulled high via 10kΩ resistor results in LMX1860-SEP enabled
		2-3	External CE signal from USB2ANY in TICSpro 'pin' tab
J28	VCC_BYPASS or 1st LDO	2-3 (EVM default)	Use on-board LDOS
		1-2	Direct Supply from J23 (VCCIN) SMA connector
J29	VCC_IN or VCC_BYPASS	2-3 (EVM default)	Use on-board LDOS
		1-2	Direct Supply from J23 (VCCIN) SMA connector
J40	VCC_IN or 2nd LDO	2-3 (EVM default)	Use on-board LDOS
		1-2	Direct Supply from J23 (VCCIN) SMA connector

Table 2-5. Pin Control Jumpers (IO Expander Configurable)

Jumper	Short position	Configuration
SYSREFEN (Acts as CE pin for entire SYSREF sub-system)	J38-J39 (Pulled HIGH)	When SYSREFEN is set to HIGH, the entire SYSREF sub-system is enabled with register defaults set accordingly. SPI can still be used to disable.
	J37-J38 (Pulled LOW)	When SYSREFEN is set to low, the entire SYSREF sub-system is deactivated and SPI cannot re-enable.
LOGICEN (Acts as CE pin for LOGICH)	J38-J39 (Pulled HIGH)	When LOGICEN is set to HIGH, the entire SYSREF sub-system is enabled with register defaults set accordingly. SPI can still be used to disable.
	J37-J38 (Pulled LOW)	When LOGICEN is set to low, all FPGA/LOGIC circuits and the SYSREF sub-system are deactivated and SPI cannot re-enable.

Table 2-6. Pin State Headers (IO Expander Configurable)

Header	Short Position	Configuration
PWRSEL[2:0]	000	Output power configurable via SPI
	001 - Lowest output power	Pin Mode (Also controllable via IO expander)
	⋮	
	111 - Highest Output Power	
CLKx_EN	Pulled LOW (GND) J31-J32	Disables corresponding CLKOUTx
	Pulled HIGH (VCC) J32-J33	Enables corresponding CLKOUTx
CAL	Transition from LOW to HIGH	Calibrates the multiplier or Resets the divider
	LOW	Calibration & Reset controllable via SPI

WARNING

If the user wishes to use IO expander, then make sure that no shorts are present on any of the header pins. Otherwise, the IO expander or the MCU is damaged.

The onboard TCA9535 IO expander allows the user to change pin states without the need of physical shorts on the header pin. This allows users to toggle pin modes through the GUI as well. If the user wishes to evaluate the LMX1860-SEP without MCU control (physical pin strapping), then make sure no jumpers are present on any of the pin state headers.

USB POWER needs to be provided if LDOs utilization is desired. VCCIN can have a 3.3V supply connected but, if the USB cable is disconnected, then the board is without power.

Table 2-7. Usage Modes

Usage	Configuration
With USB & DUT LDOs	• Short J28, J29 and J40 jumpers to LDO • Apply 3.3V to VCCIN • Apply USB connection
Without USB & DUT LDOs	• Short J28, J29 and J40 jumpers to LDO • Apply 3.3V to VCCIN • Apply 5V to VBIAS (TP16) - **To avoid damage to host pc usb port, do not apply external source to vbias unless usb is disconnected or R44 has been removed.**
With USB & DUT LDOs bypassed	• Short J28, J29 and J40 jumpers to bypass • Apply 2.5V to VCCIN • Apply USB connection
Without USB & DUT LDOs bypassed	• Short J28, J29 and J40 jumpers to LDO • Apply 2.5V to VCCIN

Note

SPI reading while using DUT LDOs: 3.3V supply can prevent SPI read-back from functioning as intended. Make sure the input voltage to U7 is larger than 0.7 * VCCIN and that output voltage of U7 is greater than 2.31V.

2.1.3 How to Enable Full SPI Control

Short positions for full SPI control (not using IO expander).

Header	Short Position	Configuration
PWRSEL[2:0]	000	Output power configurable via SPI.
CLKx_EN	Pulled HIGH (VCC)	Enables corresponding CLKOUTx, SPI can still disable each output.
MUXSEL[1:0]	000	MUXSEL controlled via SPI.
DIVSEL[2:0]	000	DIVSEL controlled via SPI.
SYSREF_EN	Pulled HIGH (VCC)	Enables entire SYSREF system which is controlled via SPI.
LOGICEN	Pulled HIGH (VCC)	Enables entire LOGICLK system which is controllable via SPI.

2.1.4 Power Requirements

Apply 3.3V to the J23 header. The acceptable supply voltage range is 3.1V to 3.5V, and the board can draw up to 1.3A during operation, so the resistance of the cable is matter. The on-board LDOs have about 40mA ground current for converting 3.3V to 2.5V supply. Furthermore, enabling or disabling various system functions can change the board current by 50% or more.

2.1.5 Pin Mode Strapping

Mode of Operation	Jumper Position	Multiplier/Divider Short Position	Multiplier/Divider Value Short Position
Multiplier mode	Short MUXSEL[1:0] to VCC (J35-J36)	Short DIVSEL[0] & DIVSEL[2] to GND & short DIVSEL[1] to VCC	x2 Multiplier value
		Short DIVSEL[2] to GND	x3 Multiplier value
		Short DIVSEL[1:0] to GND & DIVSEL[2] to VCC	x4 Multiplier Value
Divider mode	Short MUXSEL[0] to GND	Short DIVSEL[2:1] to GND	Div by 2
		Short DIVSEL[0] & DIVSEL[2] to GND	Div by 3
		Short DIVSEL[2] to GND	Div by 4
		Short DIVSEL[1:0] to GND	Div by 5
		Short DIVSEL[1] to GND	Div by 6
		Short DIVSEL[0] to GND	Div by 7
		DIVSEL [2:0] float	Div by 8
Buffer mode	Short MUXSEL[1] to GND	N/A	

Note

1. In multiplier mode, A LOW to HIGH transition on CAL header must be done. This is accomplished using a short on CAL header pin (J38) to VCC.
2. Only divider values of 2/3/4 are available in pin mode. Divider values of 5 , 6 , 7 & 8 are valid divider values only when in SPI mode.

2.1.6 Reference Clock

Connect the CLKINP SMA connector to a high-quality signal source such as an SMA100B signal generator. Both CLKIN inputs are terminated internally with 50Ω to AC-GND (that is, GND connection is formed by an internal capacitor), so no external termination is required or recommended. Input can be driven differentially, connect both CLKINP and CLKINN SMA connectors to a balun or a differential clock source.

The default EVM profile configures the device in buffer mode. LOGICLK is on by default with a predefined output divider value of 128. The input frequency can be modified per the operating range of each functional element if desired. This EVM setup guide and related plots assume 3200MHz input at CLKIN for buffer mode.

To evaluate SYSREF repeater mode, connect the SYSREF input SMAs to a differential output source such as an arbitrary function generator. The EVM connections for the SYSREF input are DC-coupled and provide internal 100Ω termination with several biasing options. At POR, the EVM automatically applies a weak 1.3V common mode bias to the SYSREFREQ pins. However, the default EVM profile configures the SYSREF input for DC-coupled input. In DC-coupled mode, the common mode bias on the SYSREFREQ pins must be between 1V and 2V. The input common mode requirements can be fulfilled with a standard LVDS output buffer.

For evaluating SYNC mode and SYSREF windowing, to have a SYSREFREQ input source capable of consistently meeting setup and hold requirements for a single cycle of the input clock is critical. This can become very challenging at higher frequencies where set up and hold requirements can be < 50ps. Another device capable of picosecond-precision timed pulses, such as LMX2820 or LMX2594, can be used as a reference input to both CLKIN and SYSREF for evaluating these features.

2.1.7 Output Connections

All CLKOUT connections are AC-coupled at the LMX1860-SEP EVM and can be connected directly to RF instruments with 0VDC requirements; an additional DC block is not required. The unused CLKOUT SMA connector must be terminated with a 50Ω load, or a differential connection can be used if a balun with the best frequency range is available.

Recommended oscilloscope connections include one CLKOUT and one SYSREF output from the same channel, as well as the one LOGICLK and one LOGISYS output.

Other unused CLKOUT SMA connectors must be terminated with 50Ω single-ended or 100Ω differential load, or alternately must be disabled in software, to minimize unterminated output effects on performance.

2.1.8 Header Information

The LMX1860-SEP EVM can be operated in either pin mode or SPI mode. Pin mode allows basic configuration of the LMX1860-SEP device without the need of a microcontroller. SPI mode provides full customization of the LMX1860-SEP device. Mode of operation is set via on-board headers J31 to J39 which can also be controlled via the IO expander, more information on this can be found in Section 2.1.13. Other headers are used to select power supply source and set the CE pin.

2.1.9 Default Configuration

The LMX1860-SEP EVM silicon default is buffer mode with all outputs enabled with maximum output power. SPI is disabled in this mode assuming no jumpers are being utilized and neither the IO expander. LOGICLK is also enabled in this mode with a fixed divider value of 128.

2.1.10 How to Generate SYSREF

To generate a continuous SYSREF signal proceed with the following steps:

1. Set SYSREFREQ_MODE (R14[1]) = SYSREF (0x1)
2. Set SYSREF_MODE (R17[1:0]) = Continuous (0x1)
3. Set SYSREFREQ_FORCE (R72[2]) = HIGH

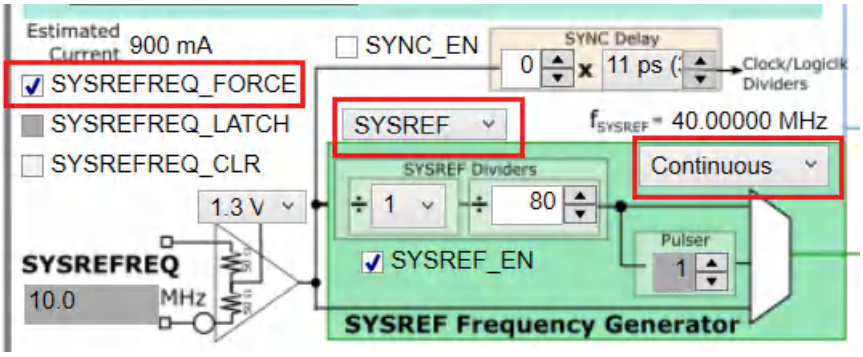


Figure 2-2. Continuous SYSREF Configuration

2.1.11 Multiplier Mode Example

To set LMX1860-SEP to multiplier mode by using SPI, follow the steps below:

1. Set CLK_MUX (R25[2:0] = Multiplier (0x3).
2. Set CLK_MULT (R25[5:3]) to appropriate multiplier value for respective CLKIN frequency.
3. Press Calibrate Multiplier button in GUI.

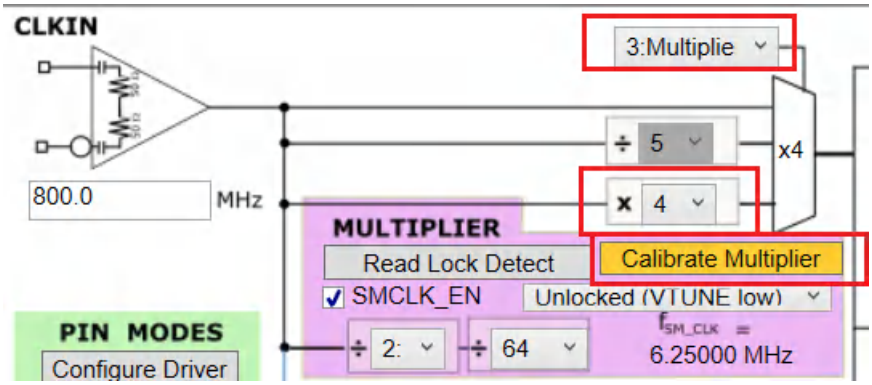


Figure 2-3. Multiplier Mode Configuration

2.1.12 Divider Mode Example

To set LMX1860-SEP to divider mode via SPI do the following:

1. Set CLK_MUX (R25[2:0] = Divider (0x2).
2. Set CLK_DIV (R25[5:3]) to appropriate divider value for respective CLKIN frequency.

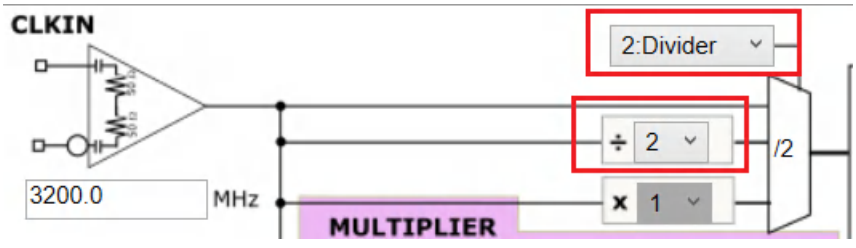


Figure 2-4. Divider Mode Configuration

2.1.13 Hybrid Mode: SPI and Pin Mode

Make sure that no shorts are connected to either GND or VCC on any of the pin mode headers. Once the user has verified that no pins have been shorted and the threat of destroying the IO expander or MCU has been eliminated, then provide power using any of the four scenarios described Table 2-7. Current draw must be less than 1A after power is applied.

Next, the user must configure the IO expander. This is done by pressing the *Configure Driver* button in the GUI under the light green PIN MODES section.

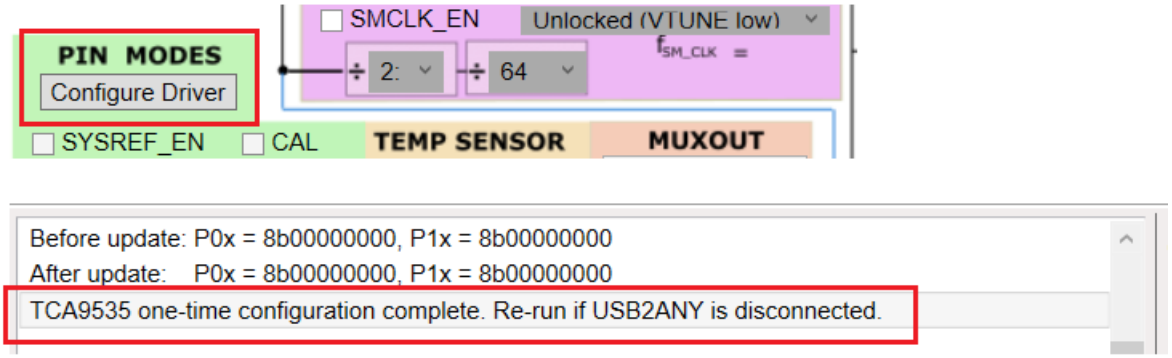


Figure 2-5. Configuration of TCA9535

Successful configuration of the IO expander results in a *TCA9535 one-time configuration complete. Re-run if USB2ANY is disconnected* shown in the message window.

The user is now able to change the states of the pin mode headers via the IO expander by pulling pins either LOW or HIGH directly without the need of a physical short.

- Output Enable and Device mode options.

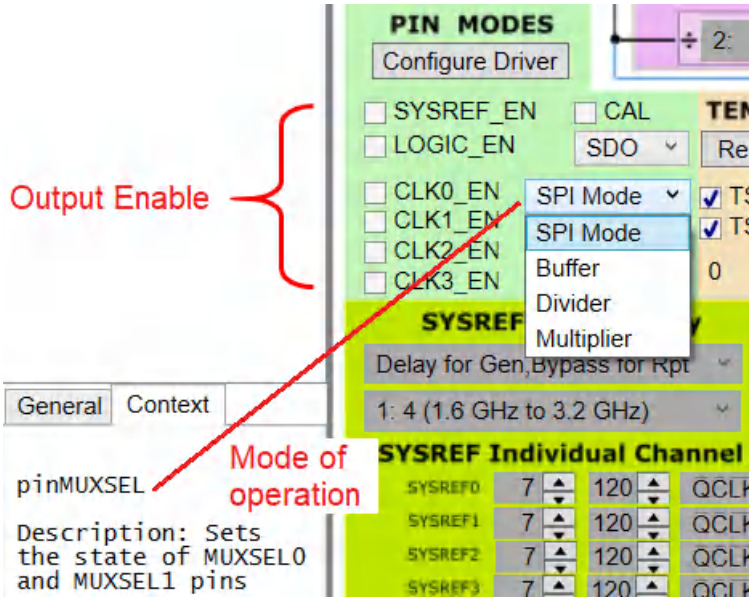


Figure 2-6. Pin Mode Options

- RF output power settings for all CLKOUTx.

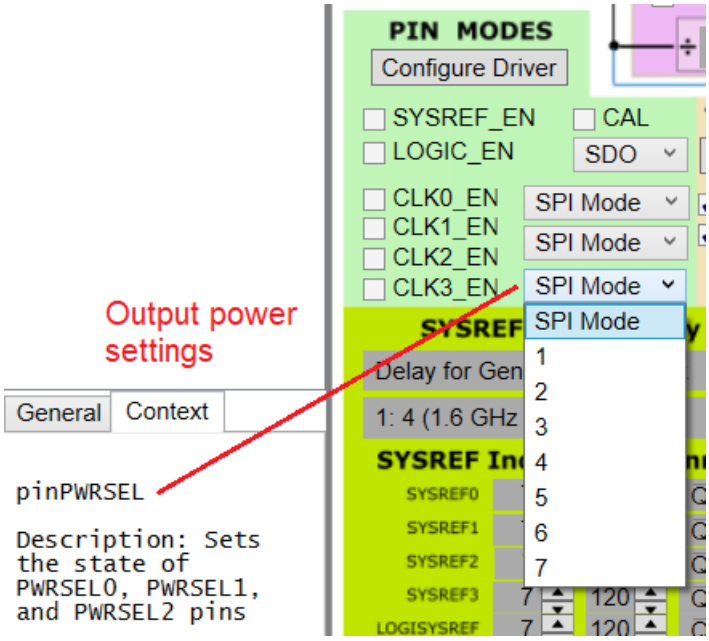


Figure 2-7. pinPWRSEL

- Chooses the corresponding divider value when in divider mode or multiplier value in multiplier mode.

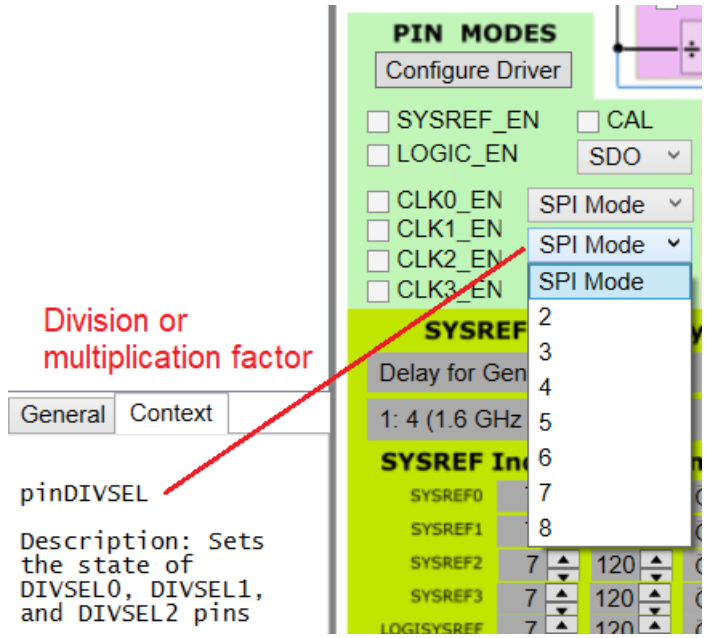


Figure 2-8. pinDIVSEL

3 Software

3.1 Software Installation

Download and install TICS Pro software from www.ti.com/tool/ticspro-sw.

3.2 Software Description

Texas Instruments Clocks and Synthesizers (TICS) Pro software is used to program this evaluation module (EVM) through the on-board USB2ANY interface.

3.3 USB2ANY Interface

The on-board USB2ANY interface provides a bridge between TICS Pro software and the LMX1860-SEP device. When the on-board USB2ANY controller is first connected to a PC, or if the firmware revision for the controller does not match with the version used by TICS Pro, a firmware update to the controller is required.

1. Connect the USB cable from the PC to the EVM. The USB interface provides the necessary power to enable the on-board USB2ANY controller.
2. After **Windows** has set up a USB device, run TICS Pro in the PC.
3. The next screen looks like the image below.

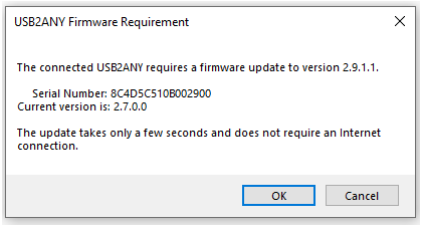


Figure 3-1. Firmware Update

4. Click *OK*, then the screen looks like the image below. Click *Update Firmware*.

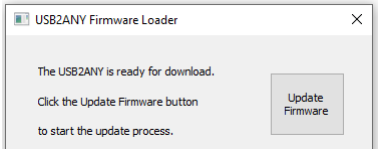


Figure 3-2. Firmware Loader

5. Then the screen below appears.

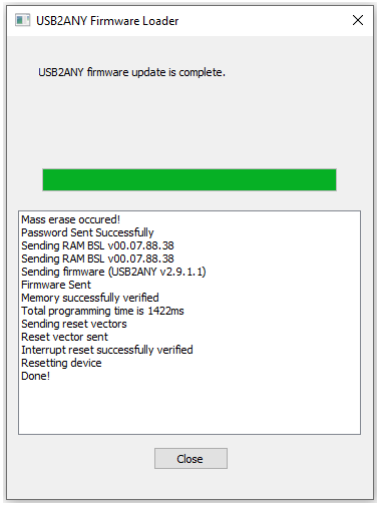


Figure 3-3. Firmware Update Complete

6. Click the *Close* button to close the window.

7. A TICS Pro default device pops up. Check to make sure that we get a green light on Connection Mode at the bottom of the GUI.

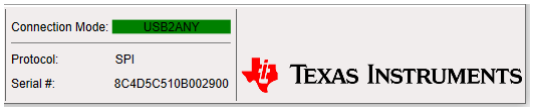


Figure 3-4. Connection Mode

8. Go to the menu bar, click *USB communications*, then select *Interface*.

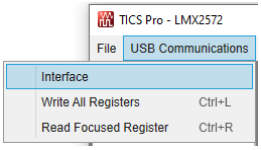


Figure 3-5. USB Communications

9. Click the *Identify* button, the LED in the USB2ANY interface flashes.

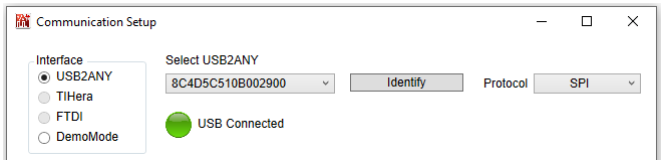


Figure 3-6. Identify USB2ANY Controller

10. Now, the USB2ANY is ready to use. Click the *Close* button to close the window.

4 Implementation Results

4.1 Buffer, Divider, and Multiplier Modes

From the top-menu, click *Default Configuration → 3200MHz Buffer Mode*. This automatically loads the buffer mode profile.

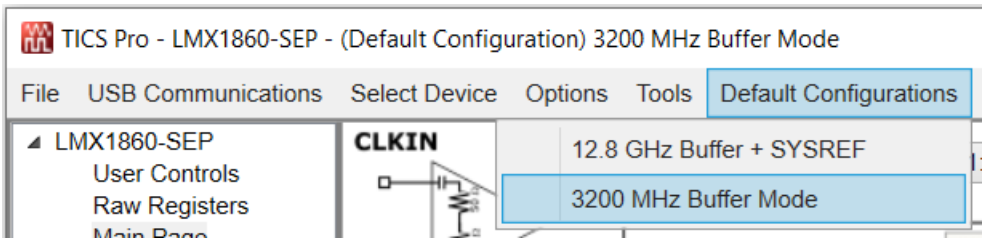


Figure 4-1. Loading the Default Configuration

If termination is not applied on all output pins, then manually disable the unused outputs using the CHx_EN fields (to completely power down unused channels) or the CLKOUTx_EN, SYSOUTx_EN, and LOGICLK_EN/ LOGISYS_EN fields (to power down output buffers only). Powering down unused channels greatly reduces current consumption, and for the logic clocks in particular can reduce spurious interference.

After the profile is loaded and required any changes have been made, click USB Communications → Write All Registers to program the device.

In all of the following plots, the blue trace is the 3.2GHz reference clock from SMA100B and the black trace is the output clock from the device.

Figure 4-2. Buffer Mode Signal Analyzer Plot

To activate the multiplier or the divider, change the CLK_MUX field to specify divider or multiplier modes, and change the CLK_DIV and CLK_MULT fields to specify the frequency scaling factor.

Figure 4-3. Divide-by-2 Mode Signal Analyzer Plot

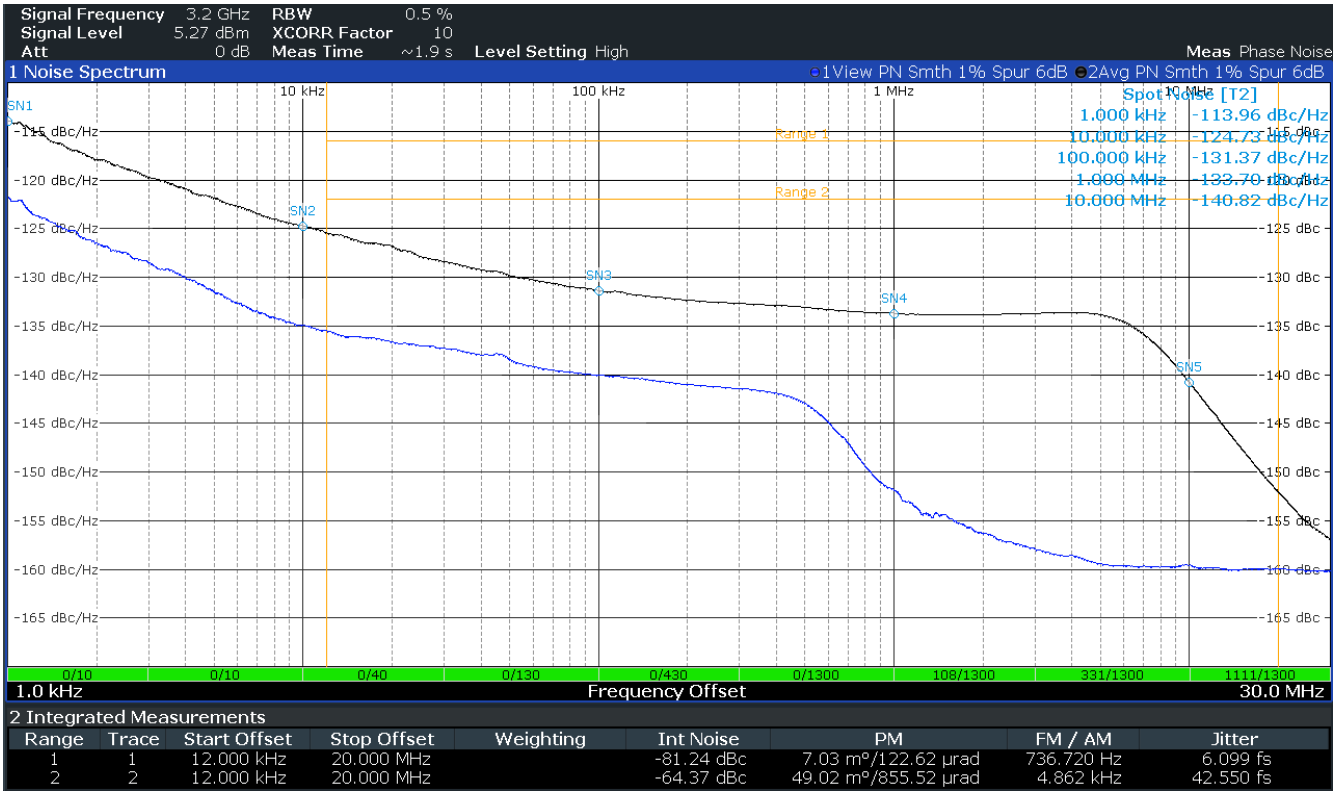


Figure 4-4. Multiplier x4 Mode Signal Analyzer Plot

4.2 SYSREF Generation

The SYSREF generation circuit includes a SYSREF pre-divider and post-divider, a pulser with programmable pulse quantity, and a repeater mode bypass. The SYSREF generator modes re-time the SYSREF signal to the output clock, verifying the SYSREF output is close to the falling edge of the clock output with default delay settings. Repeater mode timing is solely determined by the propagation delay of the device.

To activate the SYSREF generation circuit, the following conditions must be satisfied:

- SYSREFREQ_MODE field must be set to SYSREF mode.
- SYSREF_MODE field must be set to the appropriate condition: Continuous, Pulser, or Repeater.
- In generator modes (continuous or pulser), $F_{INTERPOLATOR}$ % F_{SYSREF} = 0 must be verified.
- SYSREF_DELAY_BYP field must be configured appropriately for generator or repeater modes (a GUI autoset condition normally verifies this whenever SYSREF_MODE is set).
- SYSREFREQ_VCM field must be set to DC-coupled mode for continuous or pulsed generator output. In repeater mode output, the SYSREF input can be AC- or DC-coupled and SYSREFREQ_VCM must be set accordingly.
- For continuous mode, a HIGH signal must be seen on SYSREFREQ pins continuously. For pulsed generator mode, a LOW→HIGH transition must be seen on SYSREFREQ pins to trigger the pulser. For repeater mode, the output follows the input state.

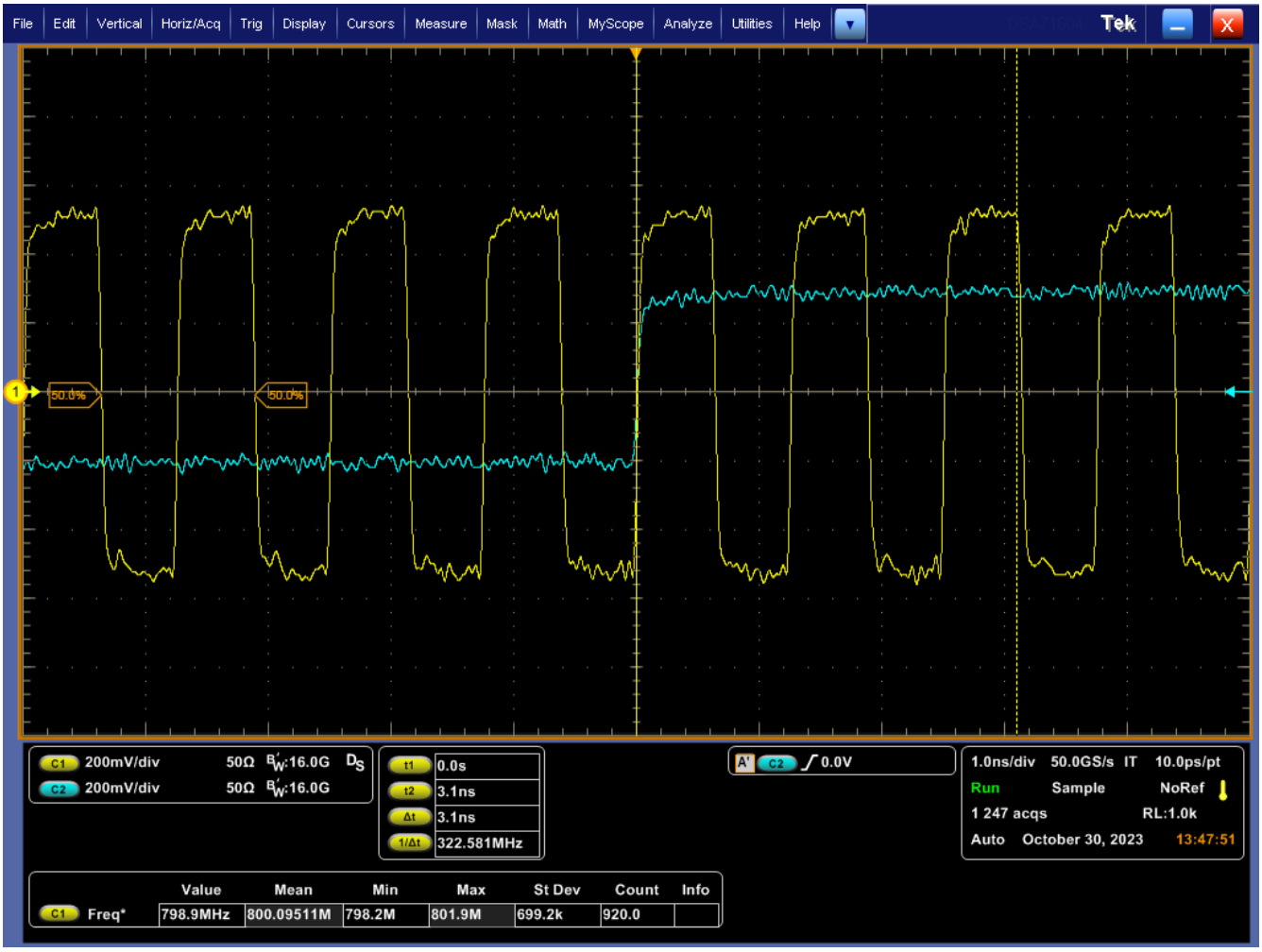


Figure 4-5. Buffer Mode With 10MHz SYSREF

4.3 SYSREF Delay Generators

In generator modes, the SYSREF can be delayed by picosecond-size steps to more closely meet setup and hold requirements for high-frequency clock outputs. A delay divider, SYSREF_DELAY_DIV, generates the interpolator frequency $f_{INTERPOLATOR}$, which is usually in the range of 400MHz to 800MHz. This interpolator frequency is further subdivided into 512 delay codes, allowing approximately 2.5ps to 5ps delay steps across most of the CLKIN frequency range.

Each channel has delay codes, which can be entered. The delay code algorithm is documented in the data sheet. To simplify delay calculation, the GUI provides an estimated relative delay: enter the relative delay, and the GUI calculates the correct step values to achieve the requested delay as closely as possible. Alternately, the register-based delay fields can be stepped through or programmed to achieve the same result.

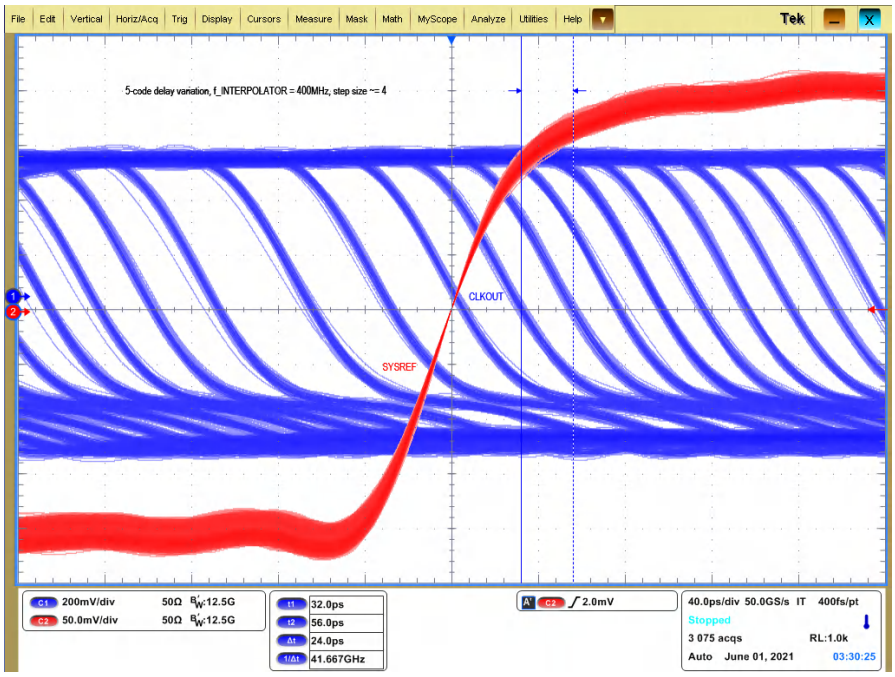


Figure 4-6. SYSREF Delay in 5-Code Steps

5 Hardware Design Files

5.1 Schematic

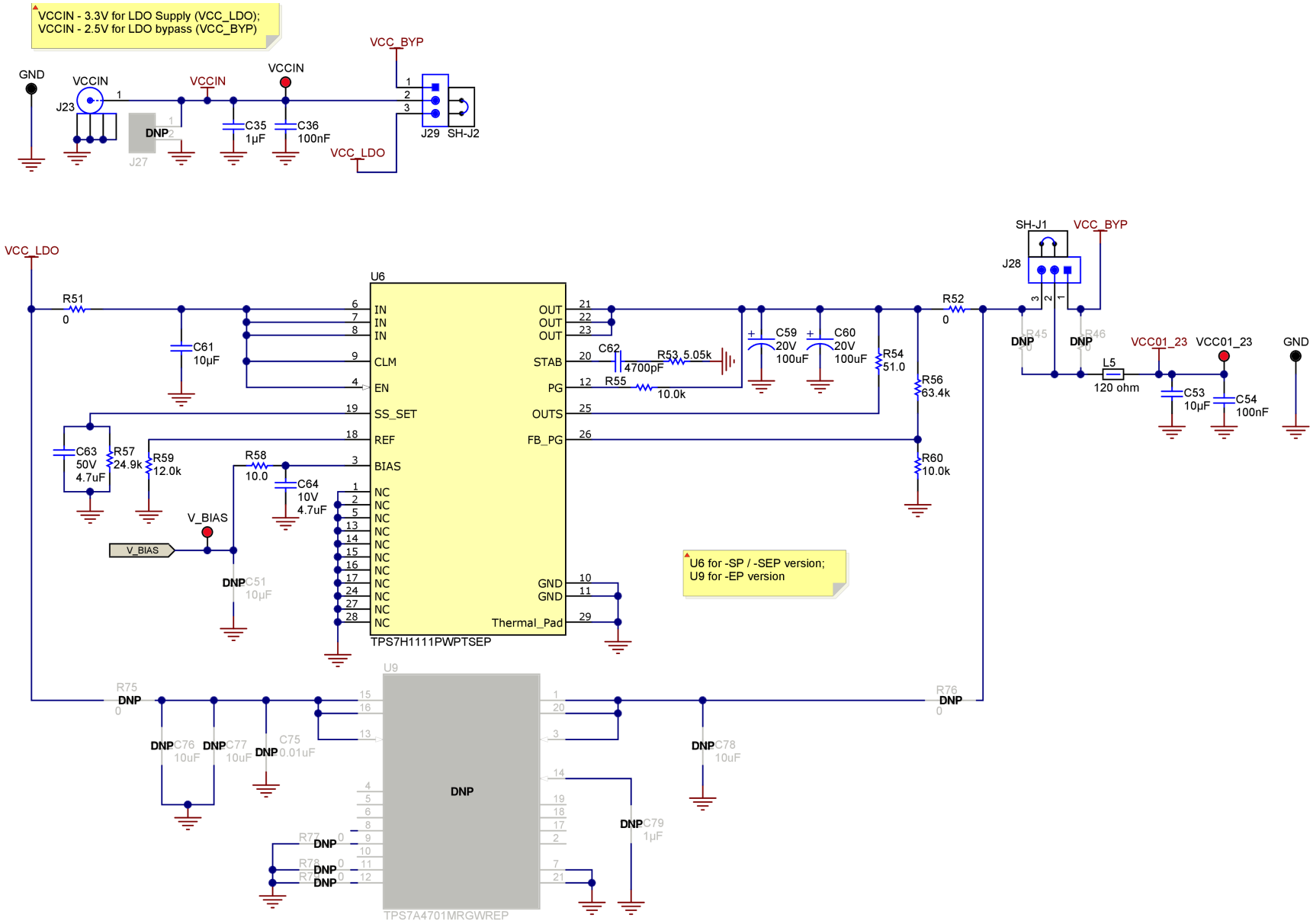


Figure 5-1. Power Supply

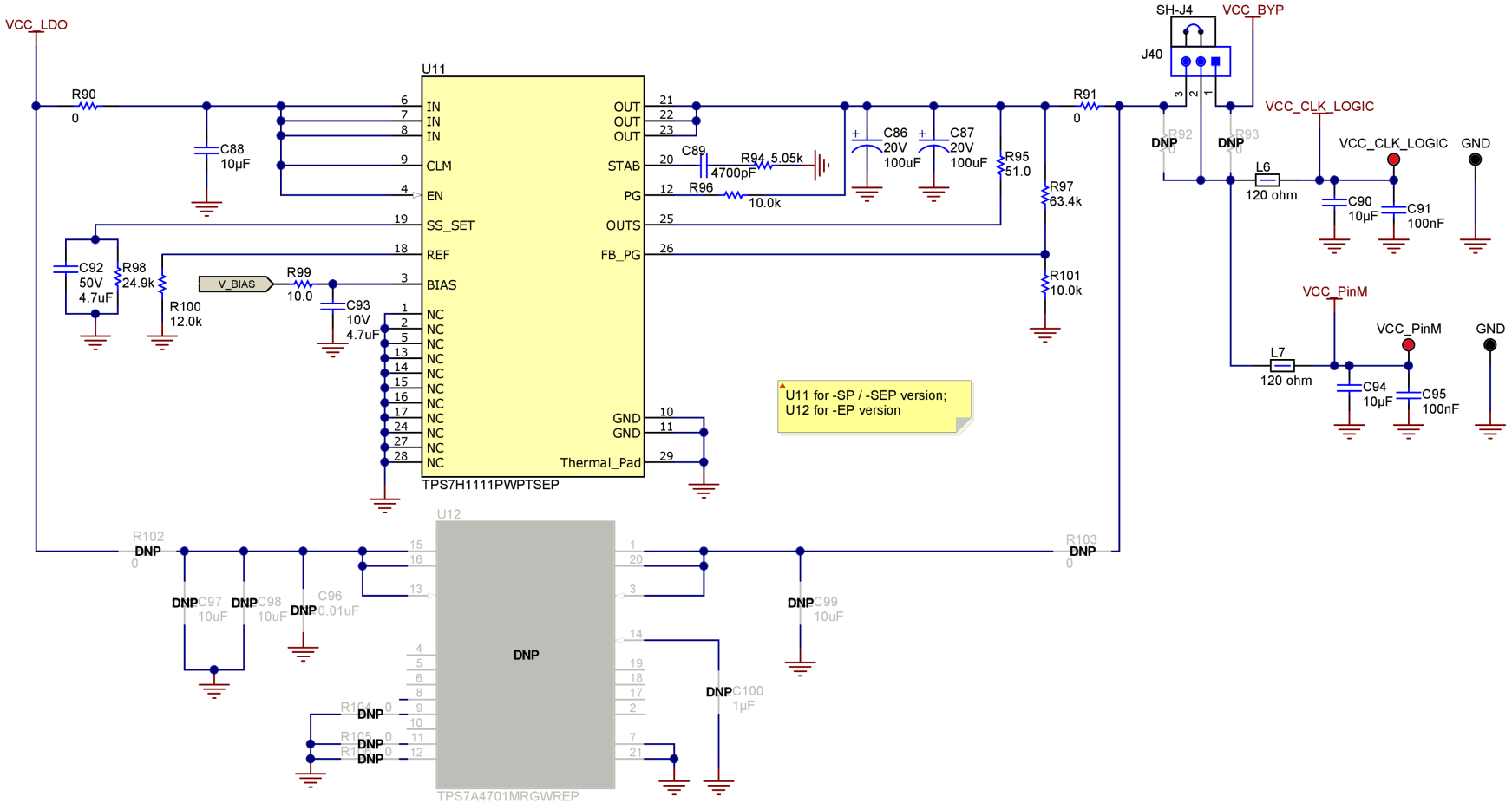


Figure 5-2. Power Supply

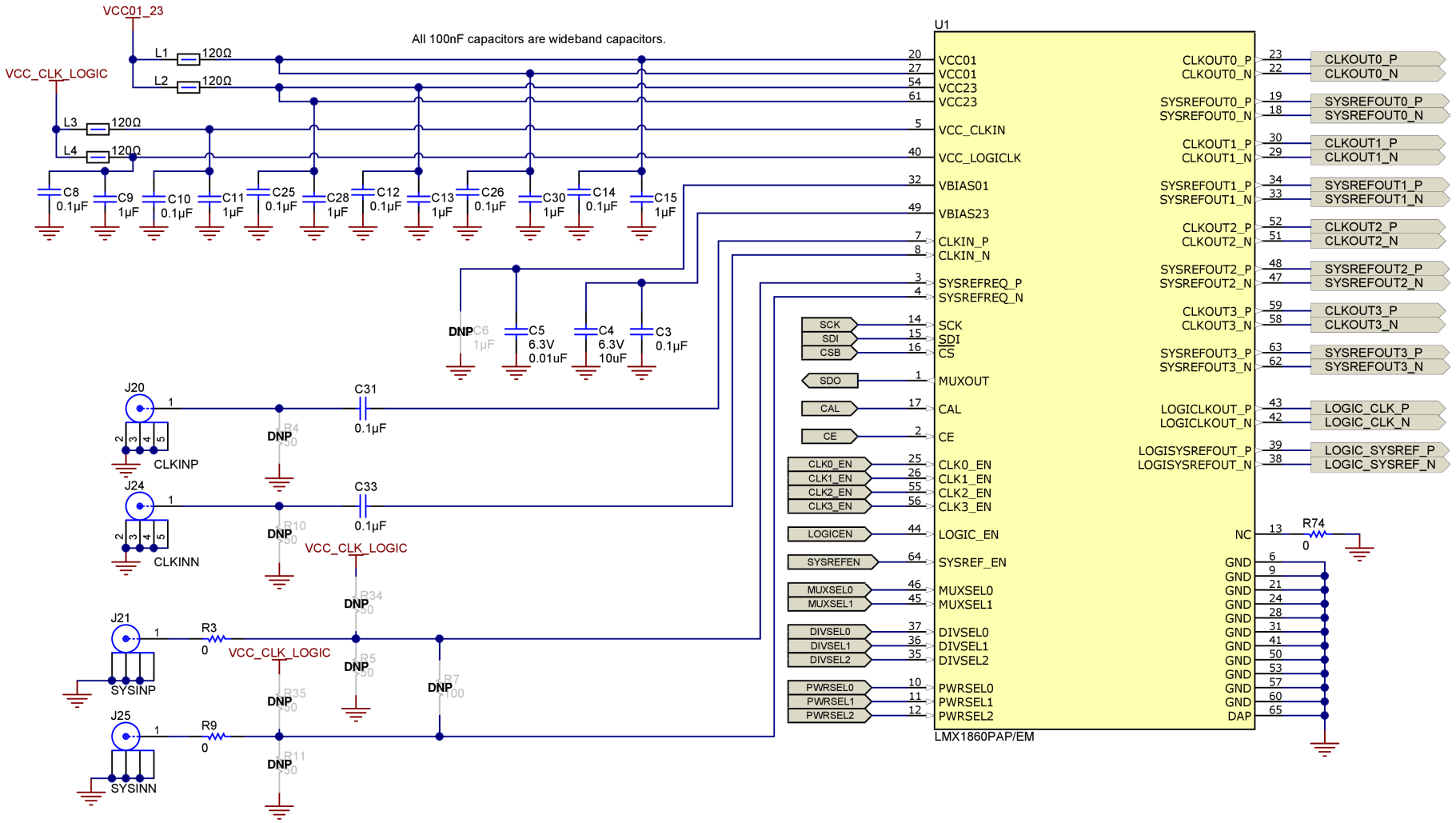


Figure 5-3. LMX1860-SEP

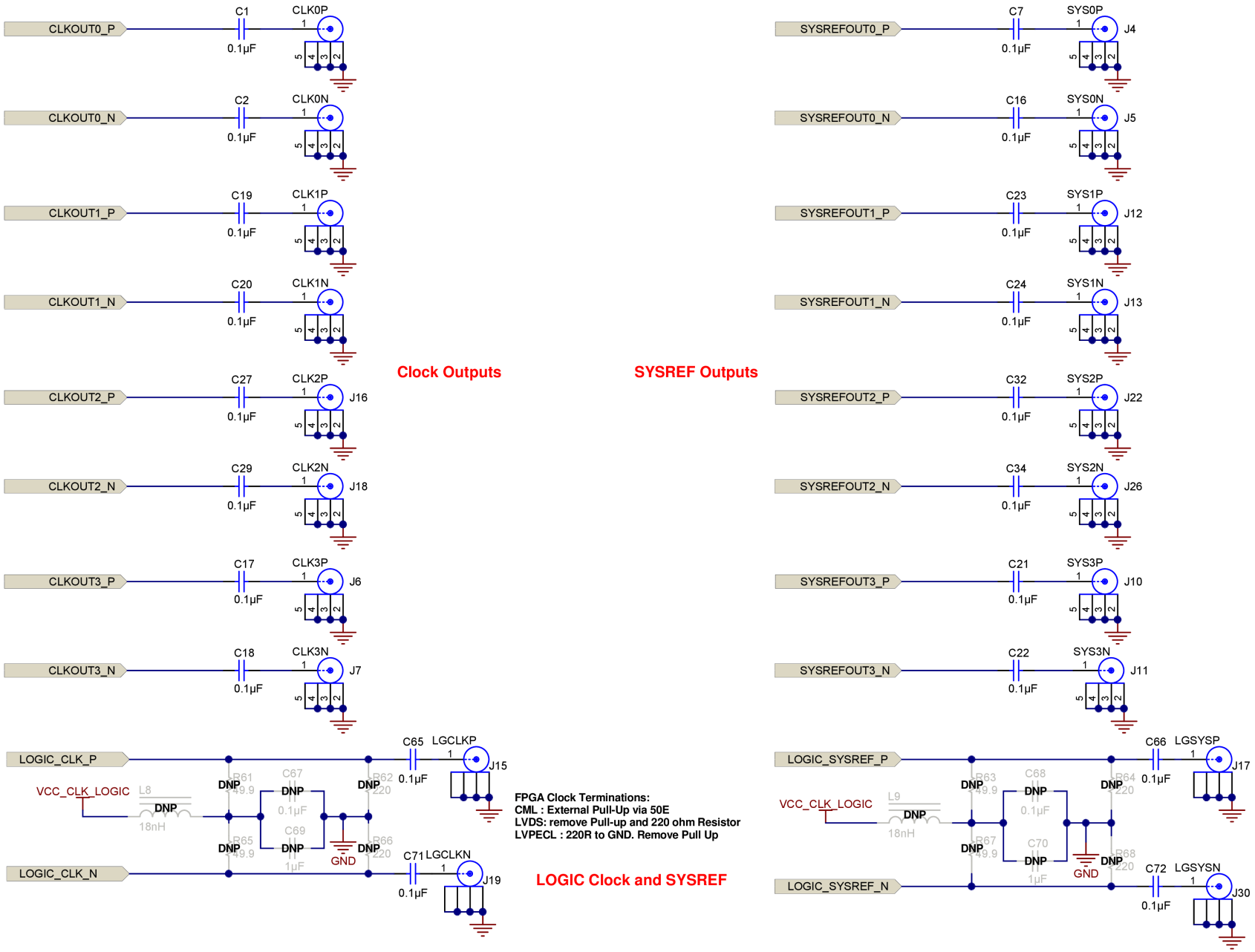


Figure 5-4. Clock Input, Clock Output Interface

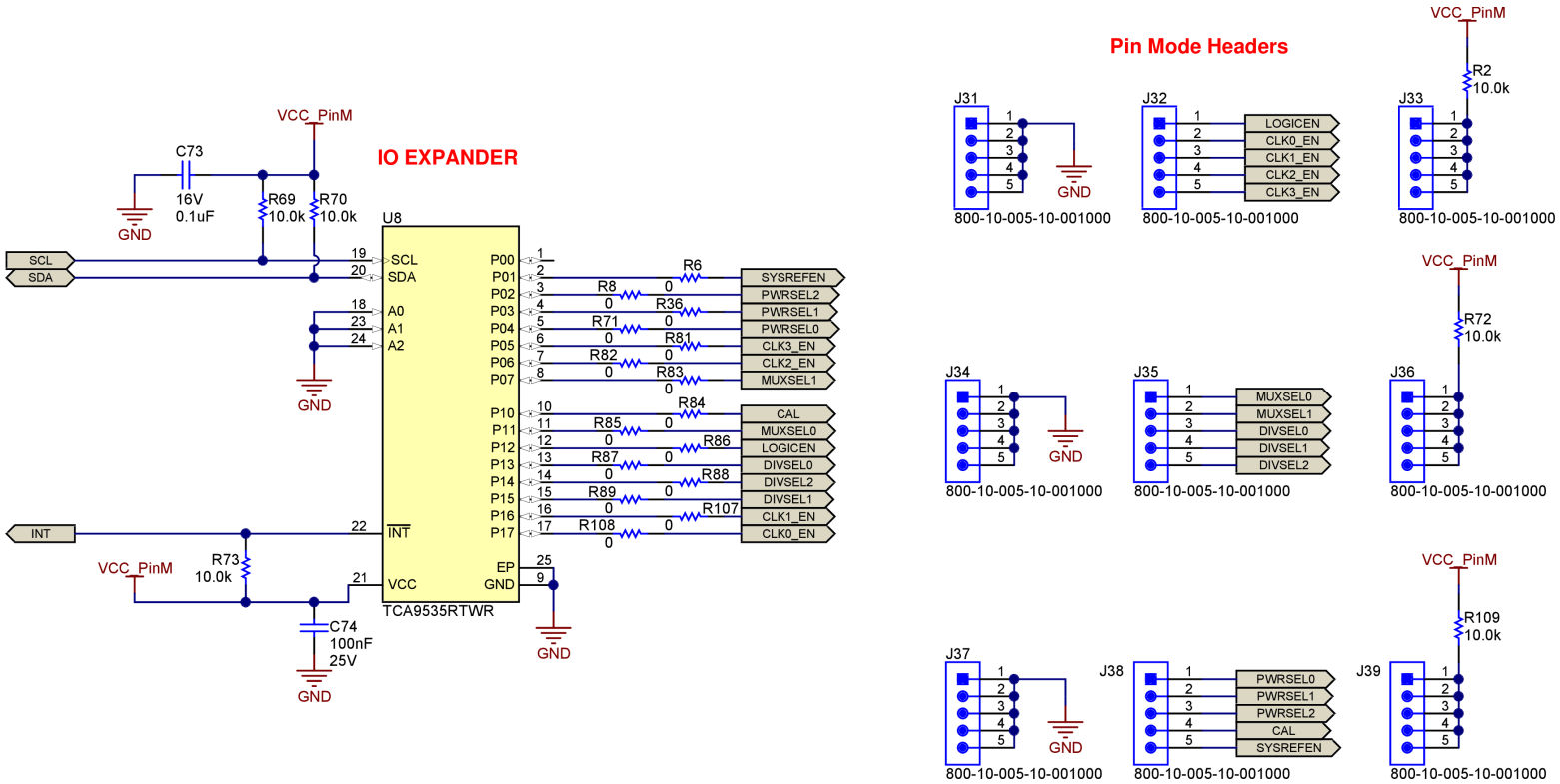


Figure 5-5. IO Interface

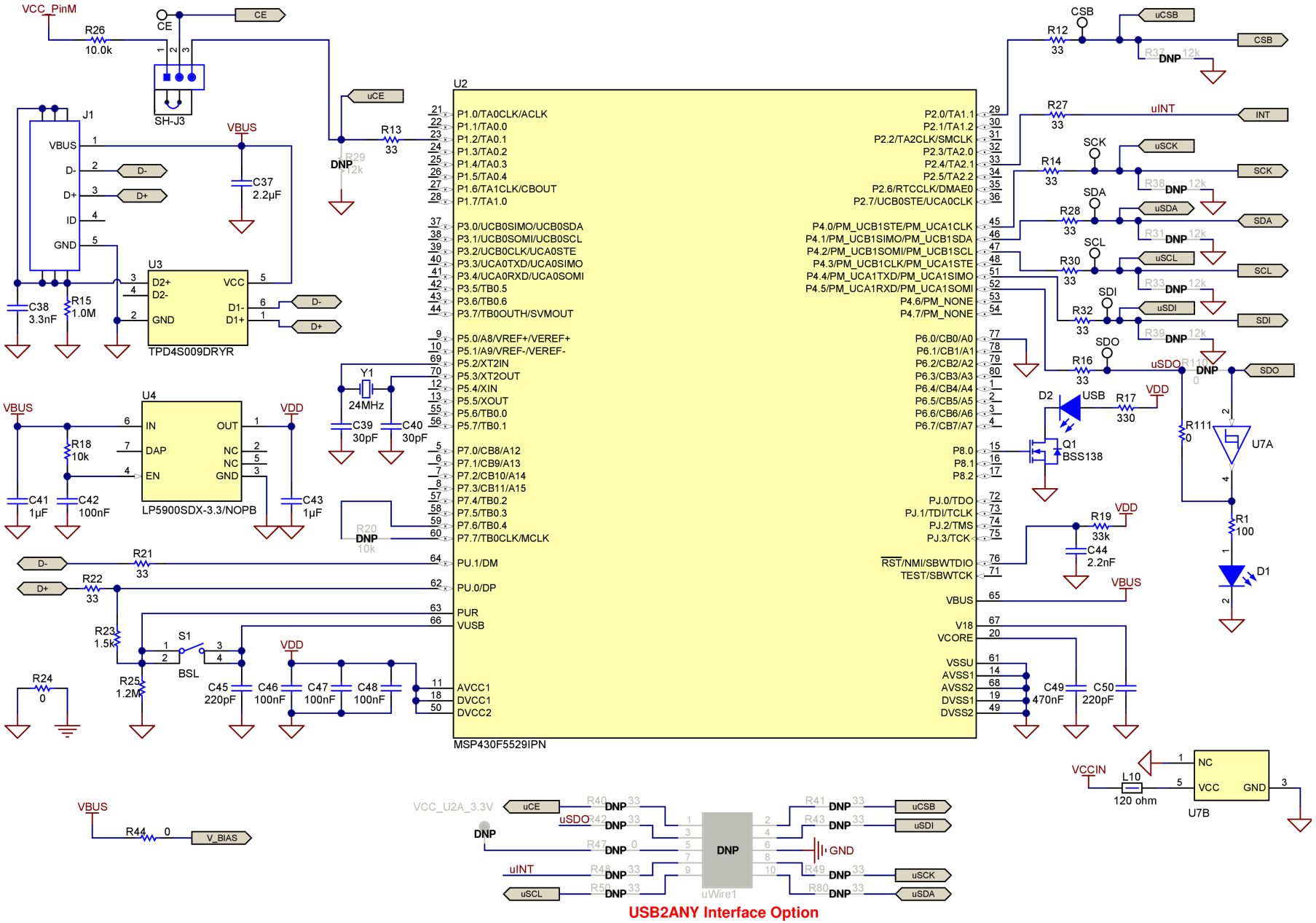


Figure 5-6. USB2ANY Interface

5.2 PCB Layout

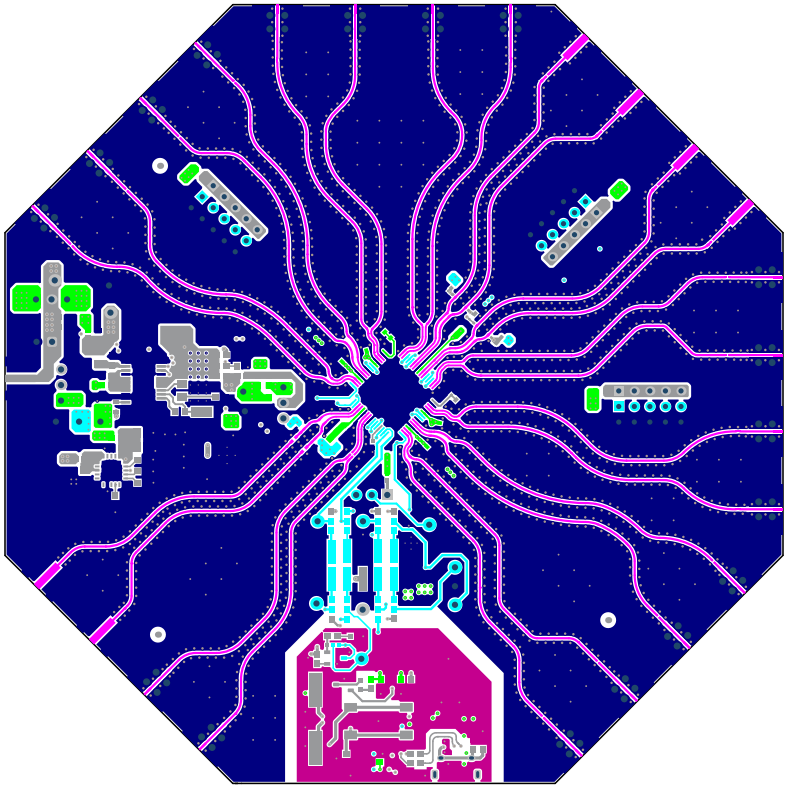


Figure 5-7. Top Layer

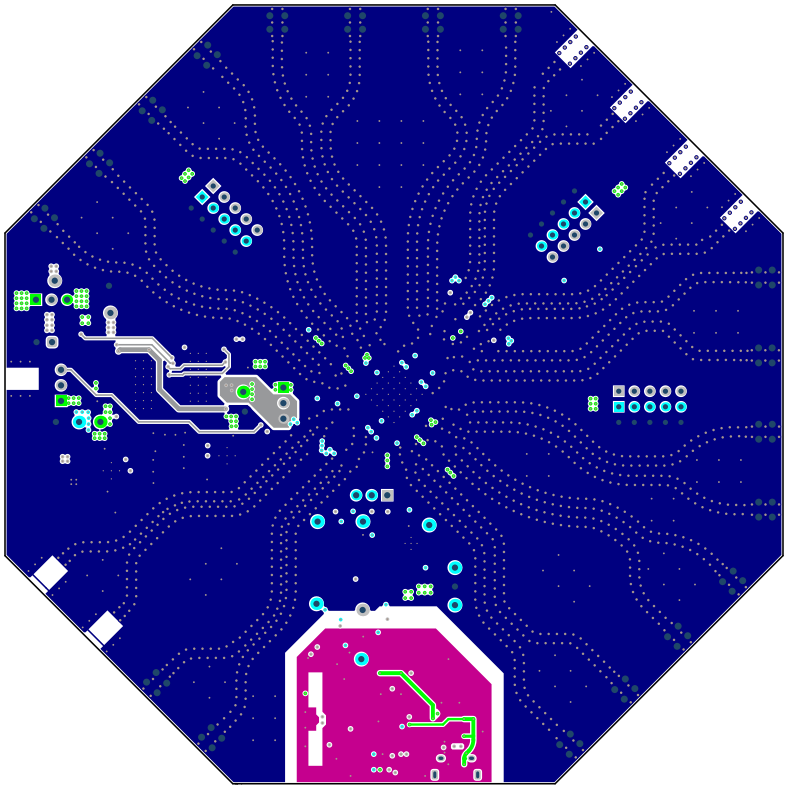


Figure 5-8. Layer 2 (RF GND)

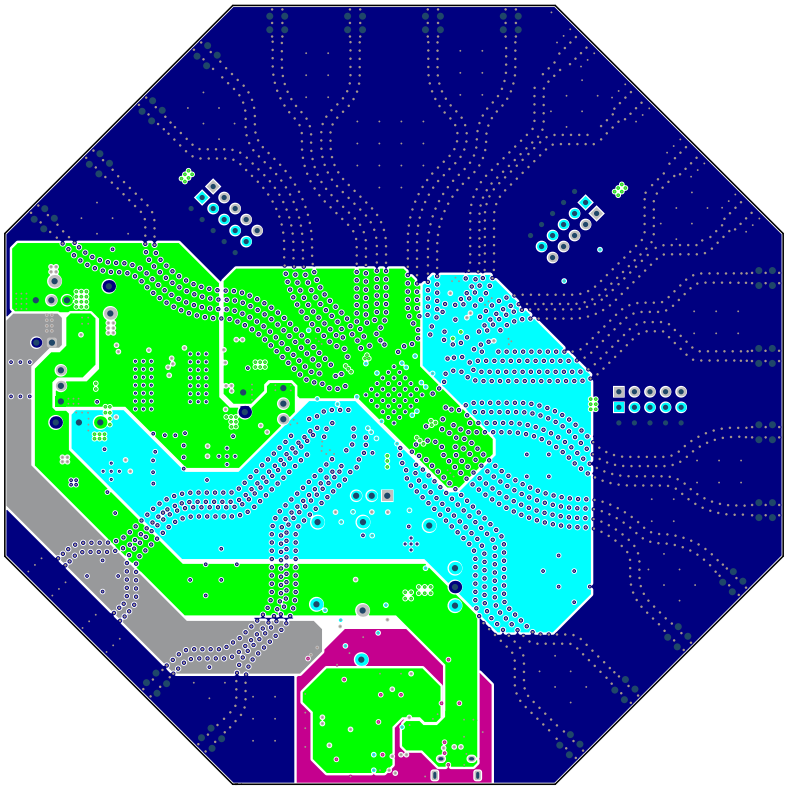


Figure 5-9. Layer 3 (Power)

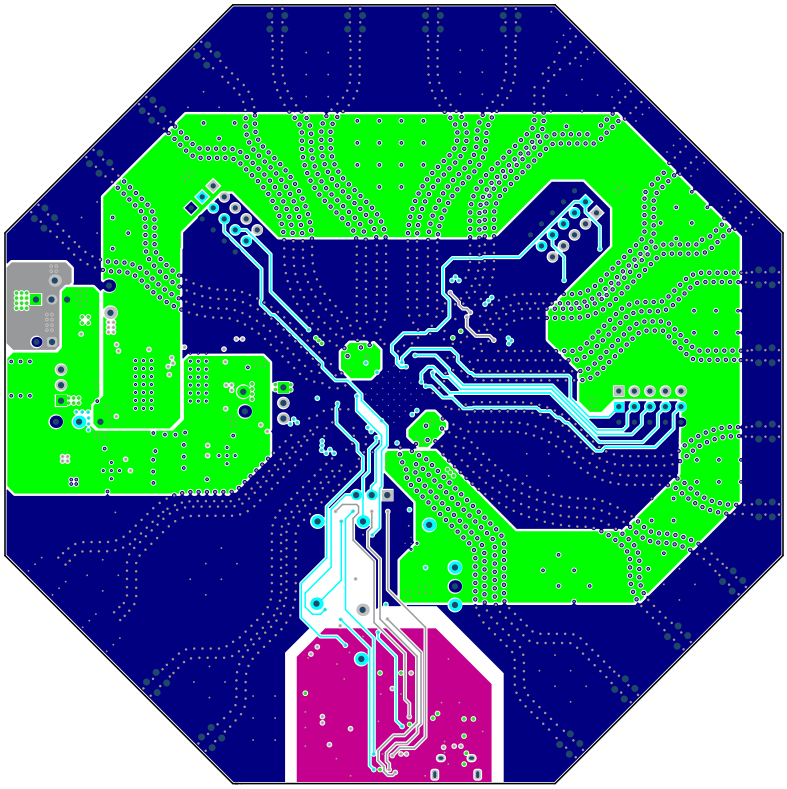


Figure 5-10. Layer 4 (Power)

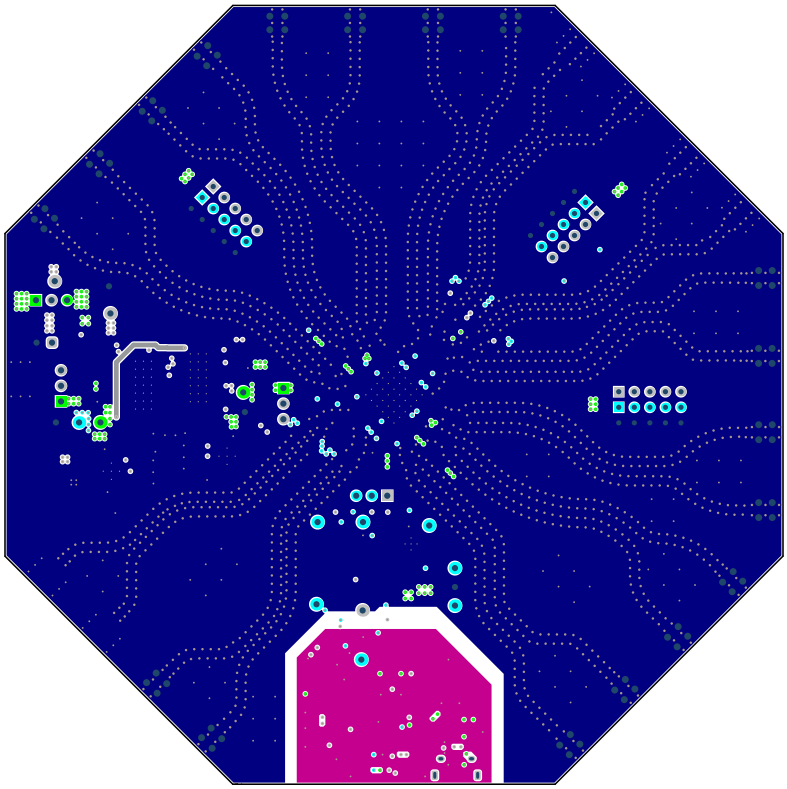


Figure 5-11. Layer 5 (GND)

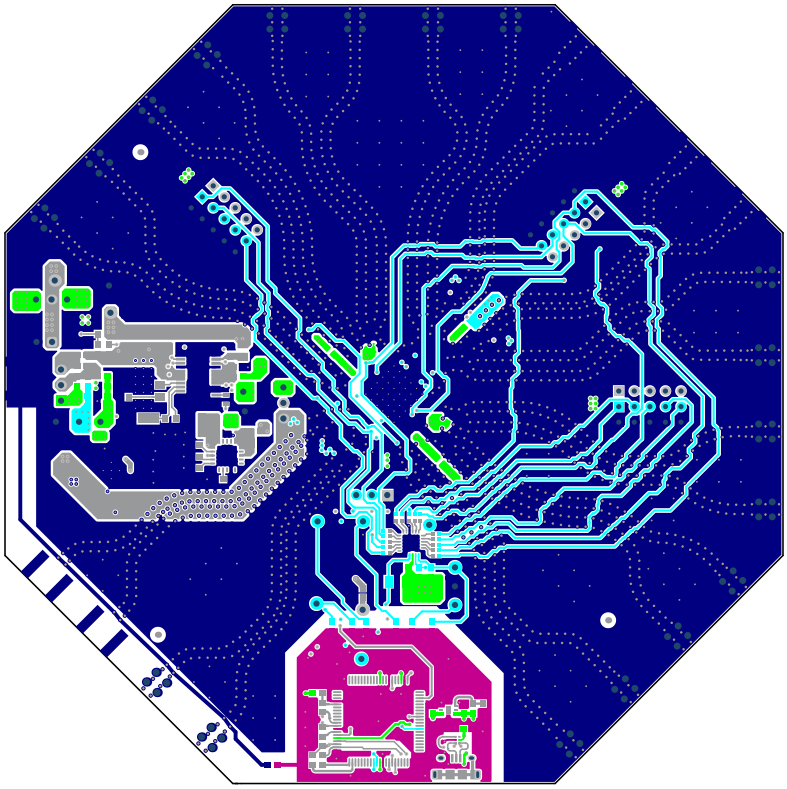


Figure 5-12. Bottom Layer

5.3 PCB Layer Stack-Up

The top layer is 1-oz. copper.

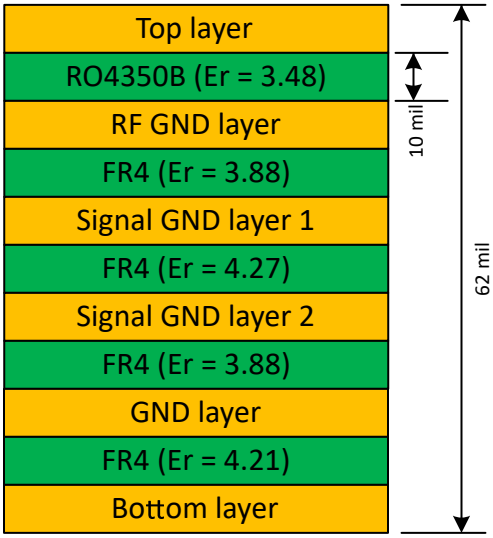


Figure 5-13. PCB Layer Stack-Up

5.4 Bill of Materials

Table 5-1. Bill of Materials (BOM)

Designator	Description	Part Number	Package	Manufacturer
C1, C2, C7, C16, C17, C18, C19, C20, C21, C22, C23, C24, C27, C29, C31, C32, C33, C34, C65, C66, C71, C72	CAP, CERM, 0.1µF, 10V,+/- 10%, X5R, 0201	530Z104KT10T	0201	AT Ceramics
C3, C8, C10, C12, C14, C25, C26	CAP, CERM, 0.1µF, 16V,+/- 10%, X7R, 0402	530L104KT16T	0402	AT Ceramics
C4	CAP, CERM, 10uF, 6.3V, +/- 20%, X5R, 0402	GRM155R60J106ME15D	0402	MuRata
C5	CAP, CERM, 0.01uF, 6.3V, +100/-0%, C0G/NP0, 0201	550Z103PTT	0201	AT Ceramics
C9, C11, C13, C15, C28, C30, C35, C41, C43	CAP, CERM, 1uF, 16V, +/- 10%, X7R, 0603	885012206052	0603	Wurth Elektronik
C36, C42, C46, C47, C48, C54, C91, C95	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0603	885012206046	0603	Wurth Elektronik
C37	CAP, CERM, 2.2uF, 16V, +/- 20%, X5R, 0603	885012106018	0603	Wurth Elektronik
C38	CAP, CERM, 3300pF, 50V,+/- 10%, X7R, 0603	885012206086	0603	Wurth Elektronik
C39, C40	CAP, CERM, 30pF, 50V, +/- 5%, C0G/NP0, 0603	06035A300JAT2A	0603	AVX
C44	CAP, CERM, 2200pF, 16V, +/- 10%, X7R, 0603	885012206036	0603	Wurth Elektronik
C45, C50	CAP, CERM, 220pF, 50V, +/- 5%, C0G/NP0, 0603	06035A221JAT2A	0603	AVX
C49	CAP, CERM, 0.47uF, 16V, +/- 10%, X7R, 0603	C0603C474K4RACTU	0603	Kemet
C53, C90, C94	CAP, CERM, 10µF, 10V,+/- 10%, X5R, 0603	GRM188R61A106KAALD	0603	MuRata
C59, C60, C86, C87	Cap Tant 100µF 20V 10 %	TBME107K020LBLC9945	7.3 × 4.3 × 4.1mm	KYOCERA AVX
C61, C88	CAP, CERM, 10µF, 6.3V,+/- 20%, X7R, 0603	CL10B106MQ8NRNC	0603	Samsung Electro-Mechanics
C62, C89	CAP, CERM, 4700pF, 25V, +/- 5%, C0G/NP0, 0805	08053A472JAT2A	0805	AVX
C63, C92	CAP, CERM, 4.7uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1,	CGA8M3X7R1H475K200KB		TDK
C64, C93	CAP, CERM, 4.7uF, 10V, +/- 10%, X5R, 0603	C0603C475K8PACTU	0603	Kemet
C73	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0402	0402YC104KAT2A	0402	AVX
C74	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	C0603C104J3RACTU	0603	Kemet
D1, D2	LED, Green, SMD	LTST-C190GKT	0603	Lite-On
J1	USB 2.0, Micro-USB Type B	10118194-0001LF	SMT	FCI
J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J16, J18, J20, J22, J24, J26	Connector, End launch SMA 50 ohm,	142-0761-881	End launch SMA	Cinch Connectivity
J14, J28, J29, J40	Header, 100mil, 3x1, Gold,	TSW-103-07-G-S	TH	Samtec
J15, J17, J19, J21, J23, J25, J30	CONN SMA JACK STR	CON-SMA-EDGE-S	EDGE MNT	RF Solutions Ltd.

Table 5-1. Bill of Materials (BOM) (continued)

Designator	Description	Part Number	Package	Manufacturer
J31, J32, J33, J34, J35, J36, J37, J38, J39	Header, 100mil, 5x1	800-10-005-10-001000	TH	Mill-Max
L1, L2, L3, L4	Ferrite Bead, 120 ohm @ 100MHz, 3A, 0603	BLM18SG121TN1D	0603	MuRata
L5, L6, L7, L10	Ferrite Bead, 120 ohm @ 100MHz, 2A, 0603	742792625	0603	Wurth Elektronik
Q1	MOSFET, N-CH, 50V, 0.22A	BSS138	SOT-23	Fairchild
R1	RES, 100, 1%, 0.1 W, 0603	CRCW0603100RFKEA	0603	Vishay-Dale
R2, R55, R69, R70, R72, R96, R109	RES, 10.0 k, 1%, 0.1 W, 0603	ERJ-3EKF1002V	0603	Panasonic
R3, R6, R8, R9, R36, R71, R74, R81, R82, R83, R84, R85, R86, R87, R88, R89, R107, R108, R111	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	0402	Yageo America
R12, R13, R14, R16, R21, R22, R27, R28, R30, R32	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333R0JNEA	0603	Vishay-Dale
R15	RES, 1.0M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M00JNEA	0603	Vishay-Dale
R17	RES, 330, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603330RJNEA	0603	Vishay-Dale
R18	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0JNEA	0603	Vishay-Dale
R19	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333K0JNEA	0603	Vishay-Dale
R23	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50JNEA	0603	Vishay-Dale
R24, R44, R51, R52, R90, R91	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	0603	Vishay-Dale
R25	RES, 1.2M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M20JNEA	0603	Vishay-Dale
R26	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	RMCF0402FT10K0	0402	Stackpole Electronics Inc
R53, R94	RES, 5.05 k, 0.5%, 0.1 W, 0603	RT0603DRE075K05L	0603	Yageo America
R54, R95	RES, 51.0, 1%, 0.1 W, 0603	RC0603FR-0751RL	0603	Yageo
R56, R97	RES, 63.4 k, 0.1%, 0.1 W, 0603	RT0603BRD0763K4L	0603	Yageo America
R57, R98	RES, 24.9 k, 0.1%, 0.1 W, 0603	RT0603BRD0724K9L	0603	Yageo America
R58, R99	RES, 10.0, 1%, .5 W, AEC-Q200 Grade 0, 0805	ERJ-P6WF10R0V	0805	Panasonic
R59, R100	RES, 12.0 k, 0.1%, 0.1 W, 0603	RT0603BRD0712KL	0603	Yageo America
R60, R101	RES, 10.0 k, 0.1%, 0.1 W, 0603	RT0603BRD0710KL	0603	Yageo America
R73	RES, 10.0 k, 1%, 0.25 W, 1206	RC1206FR-0710KL	1206	Yageo America
S1	Switch, Tactile, SPST	FSM4JSMA	6x6 mm	TE Connectivity
SH-J1, SH-J2, SH-J3, SH-J4	Shunt, 2.54mm, Gold, Black	60900213421	2.54mm	Wurth Elektronik
TP1, TP4, TP5, TP6, TP9, TP10, TP11	Test Point, Miniature, White	5002	TH	Keystone

Table 5-1. Bill of Materials (BOM) (continued)

Designator	Description	Part Number	Package	Manufacturer
TP2, TP7, TP12, TP14, TP16	Test Point, Miniature, Red	5000	TH	Keystone
TP3, TP8, TP13, TP15	Test Point, Miniature, Black	5001	TH	Keystone
U1	High-Frequency JESD Buffer/Multiplier/Divider	LMX1860PAP/EM	TQFP64	Texas Instruments
U2	25MHz Microcontroller	MSP430F5529IPN	PN0080A	Texas Instruments
U3	4-Channel ESD diode	TPD4S009DRYR	DRY0006A	Texas Instruments
U4	Ultra Low Noise, 150mA LDO	LP5900SDX-3.3/NOPB	NGF0006A	Texas Instruments
U6, U11	1.5A Radiation Hardened LDO	TPS7H1111PWPTSEP	SOP28	Texas Instruments
U7	Single Schmitt-Trigger Buffer	SN74LVC1G17DBVR	DBV0005A	Texas Instruments
U8	Low-Power I/O Expander	TCA9535RTWR	RTW0024B	Texas Instruments
Y1	Crystal, 24.000MHz, 20pF	ECS-240-20-5PX-TR	11.4×4.3×3.8 mm	ECS Inc.

6 Additional Information

6.1 Troubleshooting Guide

6.1.1 General Guidance

- Do not make modifications to the EVM or change the default settings until after the EVM is verified work.
- Register readback requires programming MUXOUT_EN = 1 and MUXOUT_SEL = 1. The GUI also prompts to configure this register before attempting any readback operation.
- The POR current of the LMX1860-SEP EVM is approximately 17mA with the LDOs bypassed & 975mA with LDOs enabled.
  - **Note**
    Default mode is buffer mode with all outputs enabled as well as LOGICLK.
- The power-down current of the EVM is approximately 10mA with LDOs bypassed and 58mA with LDOs enabled.

6.1.2 If Output Is Not Seen on CLKOUT

After POR, when CLKIN is powered and enabled, CLKOUT oscillates if the EVM is default and is in buffer mode with all outputs enabled. No EVM programming is required just to get output from CLKOUT.

- Confirm the EVM is connected to 3.3V, and draws approximately 980mA before CLKIN is applied.
- Confirm the reference input is connected to CLKIN and the reference source is powered and enabled.
- Confirm reference frequency is at least 300MHz, and input power is at least 0dBm.
- Confirm enabling CLKIN increases the EVM current to approximately 1.1A.

6.1.3 If Device Features Are Not Active

The POR defaults for LMX1860-SEP EVM disables SYSREF, and other features. Only buffer mode & LOGICLK is active by default. Register settings must be updated to observe disabled features.

- Confirm the USB cable is connected to the EVM.
- Confirm the connection mode is SPI and the USB2ANY interface is indicated in green on the bottom bar.
- If multiple USB2ANY boards are connected, then confirm that the correct USB2ANY is connected from USB Communications → Interface pop-up by using the identify button.
- Make sure all registers have been loaded (Ctrl+L), and that the device current has changed proportional to the number of functional blocks enabled in the device.
- If a communication issue with the device is suspected, then try toggling the POWERDOWN bit from the User Controls page and observe the EVM current. Note that the first write to R0 after POR is ignored. If the EVM current does not drop to about 58mA after POWERDOWN is set, then a communication issue can be preventing programming, or the IC can be damaged.

6.1.4 If Multiplier Frequency Is Not Accurate

The multiplier requires several registers to be programmed, and a calibration must be triggered by R0 write whenever the frequency changes or when the multiplier is first selected.

- Confirm the frequency input and output range for the device is appropriate. The GUI indicates if frequencies are out of range by highlighting the input or output box with the range violation.
- Make sure that all registers have been loaded (Ctrl+L). This also calibrates the multiplier.
- Try toggling the RESET bit on the User Controls page before loading all registers again (Ctrl+L).
- Refer to the data sheet to make sure a valid multiplier value is being used for the corresponding input frequency.

6.1.5 If Divider Frequency Is Not Accurate

The main clock output divider is designed with the expectation that the register settings is loaded only once after POR. In some cases, the main clock output divider does not always cleanly transition between divide values if the value is changed after POR. To change the divider value, toggle the RESET bit on the User Controls page and load all registers again (Ctrl+L).

- Refer to the data sheet to make sure a valid divider ratio value is being used for corresponding input frequency.
- A LOW to HIGH transition on the CAL header resets divider in pin mode.
  - This can also be accomplished using IO expander in hybrid mode.

6.1.6 If SYSREF Is Not Observed

There are several settings which must be correct to achieve SYSREF outputs.

- Make sure of the following settings:
  - Set SYSREF_MODE to Continuous (for debugging).
  - SYSREFREQ_MODE field set to SYSREF mode.
  - SYSREFREQ_VCM set for DC-coupled, with about 1.1V on SYSREFREQ_P and 1.5V on SYSREFREQ_N.
  - SYSREF_DELAY_BYP field set to use delay.
  - SYSREF_EN=1.
- Make sure the frequencies of the SYSREF_DELAY_DIV and SYSREF_DIV_PRE are correctly configured. The GUI highlights any frequency violations.
- Make sure that $F_{INTERPOLATOR}$ % F_{SYSREF} = 0. The GUI highlights the SYSREF divider in case of violations.
- Make sure that the output channel (CHx_EN/LOGIC_EN) and the SYSREF buffer (SYSOUTx_EN / LOGISYS_EN) are enabled.
- Confirm that Windowing mode is not enabled on the User Controls page (SYSWND_EN=0).
- Confirm that R15[9]=1. This is set automatically by the GUI, so this potential root cause is rare.
- Confirm the 1.1V and 1.5V source for SYSREFREQ_N and SYSREFREQ_P respectively are actually resulting in the required voltages at the pins. If power supplies are used for these voltages, then for the supplies to be unable to sink current is uncommon. The 1.1V source is not able to sink current from the 1.5V supply through the internal 100Ω impedance. An arbitrary function generator is recommended if possible.

6.2 Trademarks

All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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