LMK05318B EVM

1 Overview

The LMK05318B EVM is an evaluation module for the LMK05318B Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping.

The EVM includes SMA connectors for clock inputs, oscillator inputs, and clock outputs to interface the device with 50-Ω test equipment. The device can be configured through I2C or SPI using the onboard microcontroller. The graphic interface TICS Pro can be used to program the LMK05318B registers and on-chip EEPROM.

2 Trademarks

All trademarks are the property of their respective owners.

3 Features

- LMK05318B DUT:
  - DPLL with programmable loop bandwidth for input jitter and wander attenuation
  - Two Analog PLLs (APLLs) for flexible low-jitter clock generation
  - Two clock inputs supporting hitless switching and holdover
  - Eight differential clock outputs, or combination of differential and up to eight LVCMOS clocks
  - On-chip EEPROM for custom start-up clocks
- SMA ports for clock input, oscillator inputs, and clock outputs
- Onboard 48.0048-MHz XO and option to use external XO
- USB MCU interface for I^2C/SPI and GPIO pin control using TICS Pro GUI
- Status LEDs for power supplies and device status indicators

4 What is Included

- LMK05318BBEVM
- Mini-USB cable

5 What is Needed

- Windows PC with TICS Pro Software GUI
- Test Equipment
  - DC power supply (5 V, 1 A)
  - Real-time oscilloscope
  - Source signal analyzer
  - Precision frequency counter
  - Signal generator and reference clock

LMK05318B EVM User's Guide

1 EVM Quick Start

Follow below steps for EVM quick start:

1. Verify the jumper settings according to Table 1 and Figure 1.
2. Set up the board as shown in Figure 1.
3. Request, download and install Tics Pro: Texas Instruments Clocks and Synthesizers (TICS) Pro Software. In Tics Pro, go to the page *EVM Quick Start* page and follow the instructions.
4. To start a new design, go to the *Wizard* page in Tics Pro.

Table 1. Jumper Settings

DESIGNATOR	NAME	DEFAULT	DESCRIPTION
J2	REFSEL	Tie pin 03	These jumpers control the voltage levels of corresponding pins of the DUT. • Short pin 01 = pulled high • Short pin 02 = controlled by software through onboard microcontroller (USB2ANY) • Short pin 03 = pulled low
J3	HW_SW_CTRL	Tie pin 03	
J7	GPIO0/SYNCN	Tie pin 01	
J8	GPIO1/SCS	Tie pin 02	
J5	GPIO2/SOMI	Tie pin 02	
J10	VDD	Tie pins 1-2	This jumper decides whether the VDD pins are supplied by onboard LDO or external power supply. • Short pins 1-2: VDD is supplied by LDO. • Short pins 2-3: VDD is supplied by VIN1 (external power supply).
J11	VDDO	Tie pins 1-2	This jumper decides whether the VDDO pins are supplied by onboard LDO or external power supply. • Short pins 1-2: VDDO is supplied by LDO. • Short pins 2-3: VDDO is supplied by VIN2 (external power supply).
J12	VDDO level	Tie pin 03	This switch controls the VDDO level when VDDO is supplied by LDO. • Short pin 01: VDDO = 1.8 V. • Short pin 02: VDDO = 2.5 V. • Short pin 03: VDDO = 3.3 V.
J9	XO VCC	Tie pin 01	This jumper powers up or down the onboard XO. • Short pins 1-2: VCC of onboard XO is connected to LDO. • Short pins 2-3: VCC of onboard XO is tied to ground.
J4	I2C/SPI	Tie pin 01, pin 02	This jumper selects between I2C and SPI interface. • To use I2C, short pin 01, pin 02 and leave other pins open. • To use SPI, short pin 04, pin 05, pin 06, pin 07, and leave other pins open.

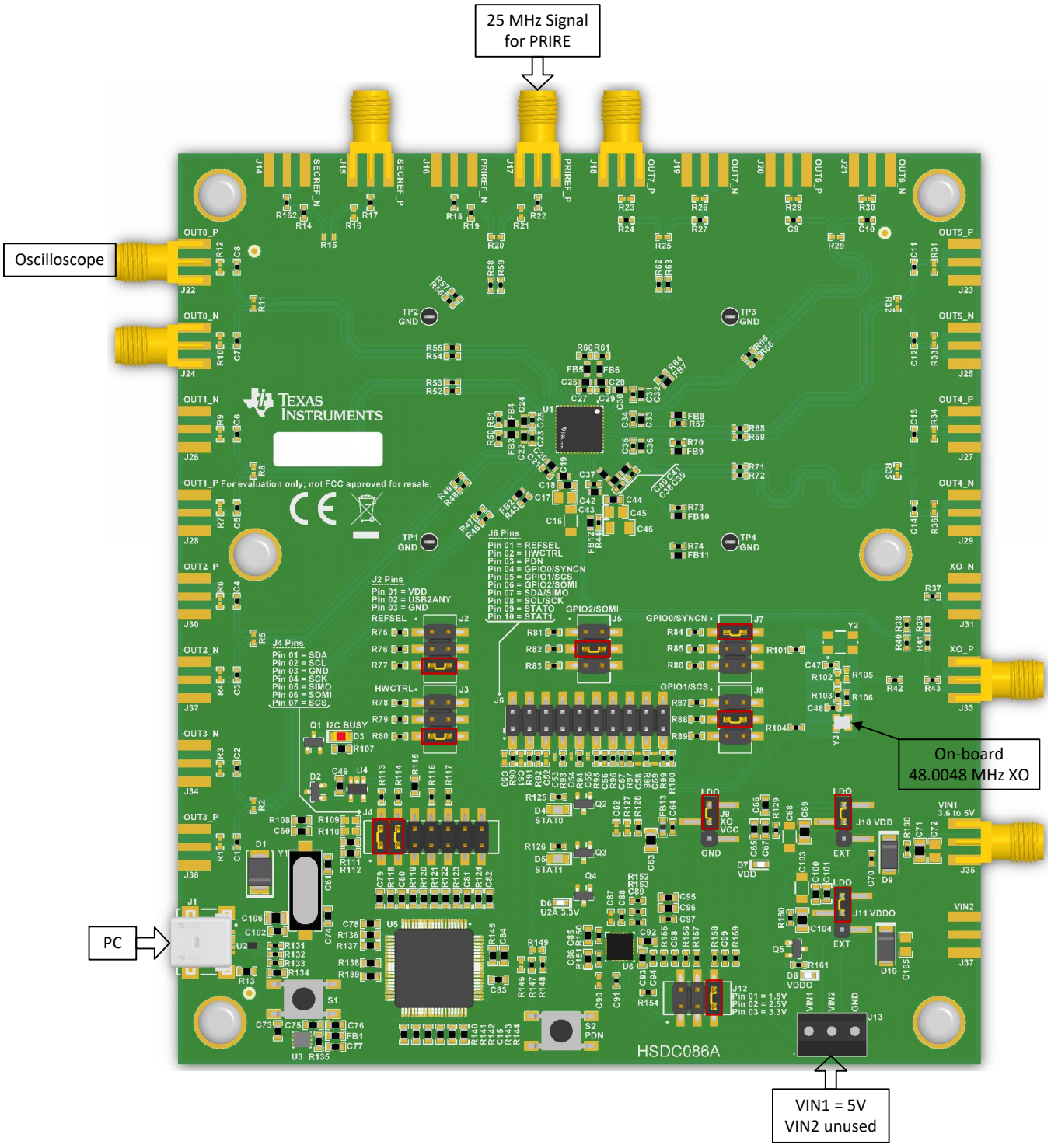


Figure 1. LMK05318B EVM with Default Jumper Settings

2 Device Start-Up Modes

The LMK05318B can start-up in one of three modes depending on the 3-level input level sampled on the HW_SW_CTRL pin upon power-on reset (POR). The start-up modes are listed in Table 2

Table 2. Device Start-Up Modes

HW_SW_CTRL(1) INPUT LEVEL	START-UP MODE	MODE DESCRIPTION	JUMPER CONFIGURATION
0	EEPROM + I²C (Soft pin mode)	Registers are initialized from EEPROM, and I²C interface is enabled with slave address 11001xxb. Logic pins: • SDA/SDI, SCL/SCK: I²C Data, I²C Clock • GPIO0/SYNCN: Output Sync (active low) • GPIO1/SCS(1): I²C Address LSB Select (Low = 00b, Float = 01b, High = 10b) • GPIO2/SDO/FINC(2): DPLL DCO Frequency Increment (active high) • STATUS1/FDEC(2): DPLL DCO Frequency Decrement (active high), or Status output	To select this mode, short pin 03 of J3. Configure the jumpers for I2C mode: 1. For J4, short pin 01, pin 02 and leave other pins open. 2. For J5 and J8, short pin 02.
Float (V_{IM})	EEPROM + SPI (Soft pin mode)	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: • SDA/SDI, SCL/SCK: SPI Data In (SDI), SPI Clock (SCK) • GPIO0/SYNCN: Output Sync (active low) • GPIO1/SCS: SPI Chip Select (SCS) • GPIO2/SDO/FINC: SPI Data Out (SDO)	To select this mode, short pin 02 of J3. Configure the jumpers for SPI mode: 1. For J4, short pin 04, pin 05, pin 06, pin 07 and leave other pins open.
1	ROM + I²C (Hard pin mode)	Registers are initialized from the ROM page selected by GPIO pins, and I²C interface is enabled with the 7-bit slave address of 0x64. Logic pins: • SDA/SDI, SCL/SCK: I²C Data, I²C Clock • GPIO[2:0]: ROM page select at POR • After POR, GPIO2/SDO/FINC and STATUS1/FDEC pins can function the same as for HW_SW_CTRL = 0 if enabled by registers.	To select this mode, short pin 03 of J3. Configure jumpers J7, J8 and J5 to set voltage levels of GPIO0, GPIO1 and GPIO2.

(1) The input levels on these pins are sampled only during POR.
(2) FINC and FDEC pin controls are only available when DCO mode and GPIO pin control are enabled by registers.

NOTE: To ensure proper start-up into EEPROM + SPI Mode, the HW_SW_CTRL, STATUS0, and STATUS1/FDEC pins must all be floating or biased to V_{IM} (0.8-V typical) before the PDN pin is pulled high. These three pins momentarily operate as 3-level inputs and get sampled at the low-to-high transition of PDN to determine the device start-up mode during POR. If any of these pins are connected to a host device (MCU or FPGA), TI recommends using external biasing resistors on each pin (10-kΩ pullup to 3.3 V with 3.3-kΩ pulldown to GND) to set the inputs to VIM during POR. After power-up, the STATUS pins can operate as LVCMOS outputs and overdrive the external resistor bias for normal status operation.

3 EVM Configuration

3.1 Power Supply

The LMK05318B has five core VDD supply pins that operate at 3.3 V ± 5% and six output VDDO supply pins that operate at 1.8 V, 2.5 V, or 3.3 V ± 5%.

- To use onboard LDO, short pins 1-2 of J10 and short pins 1-2 of J11. Then supply 5 V power source to J35 or VIN1 of J13. The VDDO level can be set by J12 (short pin 01 = 1.8 V, short pin 02 = 2.5 V, short pin 03 = 3.3 V).
- To use external power supply, short pins 2-3 of J10 and short pins 2-3 of J11. Then supply 3.3 V to J35 or VIN1 of J13, and supply 1.8 V, 2.5 V or 3.3 V to J37 or VIN2 of J13.
- To power up or power down the onboard XO, short pins 1-2 or pins 2-3 of J9.

3.2 Logic Inputs and Outputs

See Table 1 to set voltage levels for GPIO pins.

Table 3. Logic Pin Descriptions - EEPROM + I²C Mode (HW_SW_CTRL = 0)

PIN NAME (TYPE)	DESCRIPTION		
PDN (2-level input)	**Chip Power-Down/Reset (active low)** When PDN rises to 1, the digital control block triggers the internal POR sequence, initializes all the registers and logic pins for the start-up mode selected by the HW_SW_CTRL input level, restores all the internal circuits including the serial interface to their initial state, and begins normal operation. This pin is pulled high through internal pullup resistor, but can be pulled down by pushing toggle switch S2.		
	PDN STATE	**S2**	**CHIP STATE**
	0	Pushed	Power-down/reset state: Serial interface disabled
	1 (Default)	Released	Normal operation
GPIO0/SYNCN (2-level input)	**Output Synchronization (active low)** GPIO0 (SYNCN) can be used to mute the output clocks and trigger output divider synchronization (SYNC) if the divider SYNC bits are enabled by registers. Alternatively, SYNC can be triggered through register programming instead of using this pin.		
	GPIO0 STATE	**J7**	**OUTPUT SYNC STATE**
	0	Tie pin 03	SYNC asserted: Outputs muted and output dividers held in reset
	1 (Default)	Tie pin 01	SYNC deasserted: Normal output operation
GPIO1/SCS (3-level input)	**I²C Slave Address LSB Select** GPIO1 is sampled on POR to configure the lower 2 bits of the 7-bit I²C address after start-up. The upper 5 bits of the I²C address are initialized from EEPROM (SLAVEADR[7:3] = 11001b).		
	GPIO1 STATE	**J8**	**7-BIT SLAVE ADDRESS**
	0 (Default)	Tie pin 03	1100100b (0x64h)
	Float	Leave all pins open	1100101b (0x65h)
	1	Tie pin 01	1100111b (0x66h)
GPIO2/SDO/FINC (2-level input)	**DPLL DCO Mode Frequency Increment (FINC)** When DCO mode and GPIO pin control are enabled by registers, a high pulse on the FINC input will increment the DCO numerator by the programmable frequency deviation (FDEV) step size to adjust its frequency.		
	FINC STATE	**J5**	**DPLL DCO NUMERATOR**
	0	Tie pin 02 for GPIO2 to be controlled by the MCU	No update
	1 (Pulsed by MCU pin)		Incremented
REFSEL (2-level inputs)	**DPLL Reference Clock Input Selection** The REFSEL pin selects the DPLL reference clock input when Manual Input Select mode and HW Pin Control mode are selected by register configuration. This pin is ignored when Auto Input Select mode or SW Register Control mode is selected.		
	REFSEL STATE	**J2**	**DPLL REF INPUT**
	0 (Default)	Tie pin 03	PRIREF
	Float	Leave all pins open	Auto Select
	1	Tie pin 01	SECREF
STATUS0, STATUS1/FDEC (Logic outputs)	**Status Outputs** Each STATUS pin is a programmable status output that supports NMOS open-drain or 3.3-V LVCMOS driver type. The output states of STATUS0 and STATUS1 are shown on active-high LEDs D4 and D5, respectively. **DPLL DCO Mode Frequency Decrement (FDEC)** When DCO mode and GPIO pin control are enabled by registers, a high pulse on the FDEC input will decrement the DCO numerator by the programmable frequency deviation (FDEV) step size to adjust its frequency.		
	FDEC STATE	**N/A**	**DPLL DCO NUMERATOR**
	0	STATUS1/FDEC is always controlled by the MCU	No update
	1 (Pulsed by MCU pin)		Decremented

Table 4. Logic Pin Descriptions - EEPROM + SPI Mode (HW_SW_CTRL = Float)

PIN NAME (TYPE)	DESCRIPTION
GPIO1/SCS (2-level input)	**SPI Chip Select (SCS)** See Table 2.
GPIO2/SDO/FINC (2-level input)	**SPI Data Out (SDO / SOMI)** See Table 2
STATUS0, STATUS1 (Logic outputs)	**Status Outputs** Each STATUS pin is a programmable status output that supports NMOS open-drain or 3.3-V LVCMOS driver type. The output states of STATUS0 and STATUS1 are shown on active-high LEDs D4 and D5, respectively. (1)

(1) When HW_SW_CTRL = Float, STATUS[1:0] pins must not be pulled high or low externally during POR to ensure proper start-up into EEPROM+SPI Mode.

Table 5. Logic Pin Descriptions - ROM + I²C Mode (HW_SW_CTRL = 1)(1)

PIN NAME (TYPE)	DESCRIPTION	
GPIO[2:0] (2-level inputs)	**GPIO[2:0] Function at POR: ROM Page Selection** GPIO[2:0] pins are sampled on POR to select the ROM page settings used to initialize the registers. The GPIO[2:0] pins are controlled by J5, J8 and J7, respectively. **GPIO2 Function after POR: DPLL DCO Mode Frequency Increment (FINC)** After POR, the GPIO2 pin can be operated as an FINC input in the same way described for EEPROM + I²C mode (see the GPIO2/FINC description in Table 3).	
	GPIO[2:0] STATES	**ROM PAGE SELECT**
	000b (Default)	ROM Page 0
	001b	ROM Page 1
	010b	ROM Page 2
	...	...
	110b	ROM Page 6
	111b	ROM Page 7
STATUS0, STATUS1/FDEC (Logic outputs)	**Status Outputs** Each STATUS pin is a programmable status output that supports NMOS open-drain or 3.3-V LVCMOS driver type. The output states of STATUS0 and STATUS1 are shown on active-high LEDs D4 and D5, respectively. **DPLL DCO Mode Frequency Decrement (FDEC)** After POR, the STATUS1 pin can be operated as an FDEC input in the same way described in Table 3.	

(1) In ROM + I²C Mode, the two I²C address LSBs are forced to 00b (address = 0x64h).

4 EVM Schematics

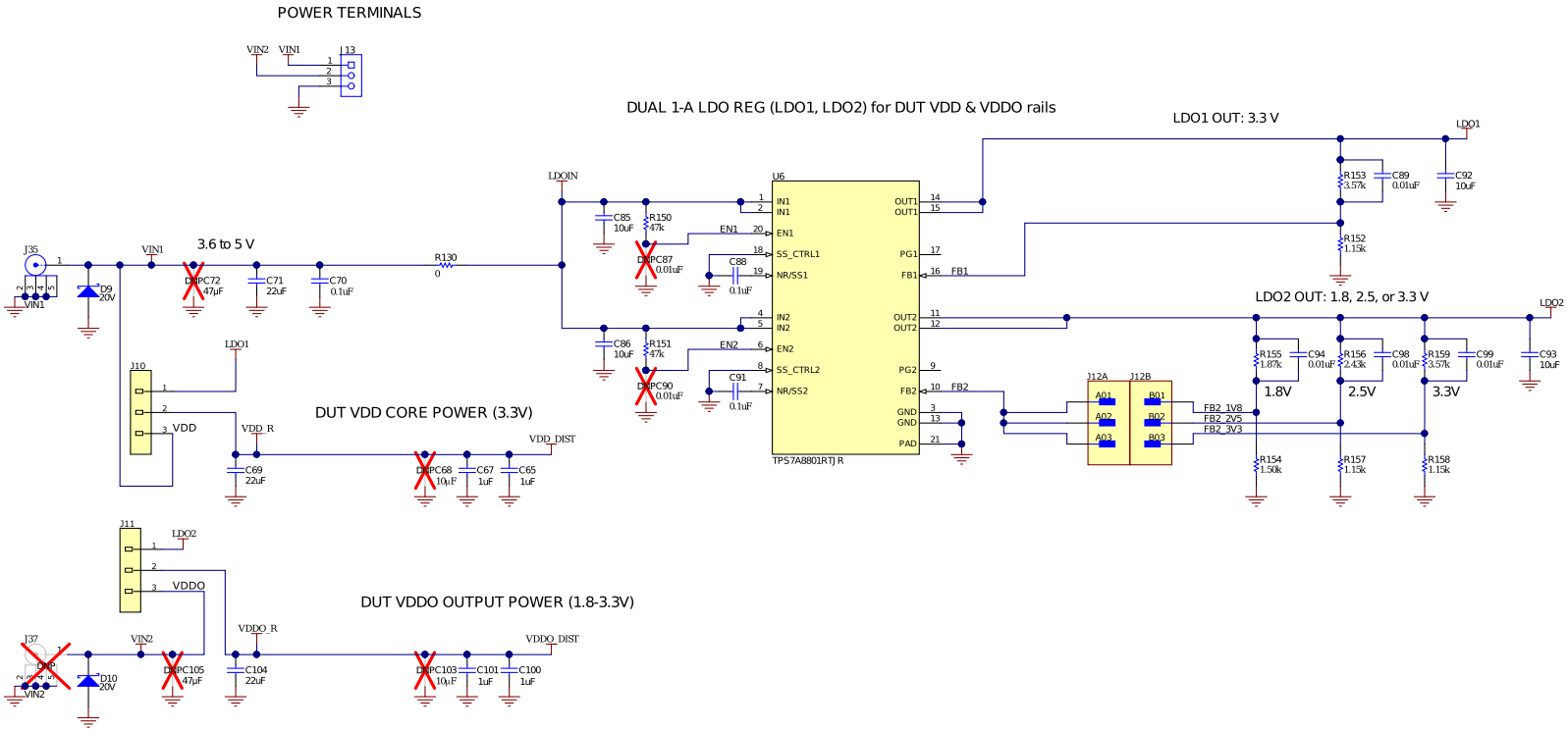


Figure 2. Schematic 1 - Power Supply

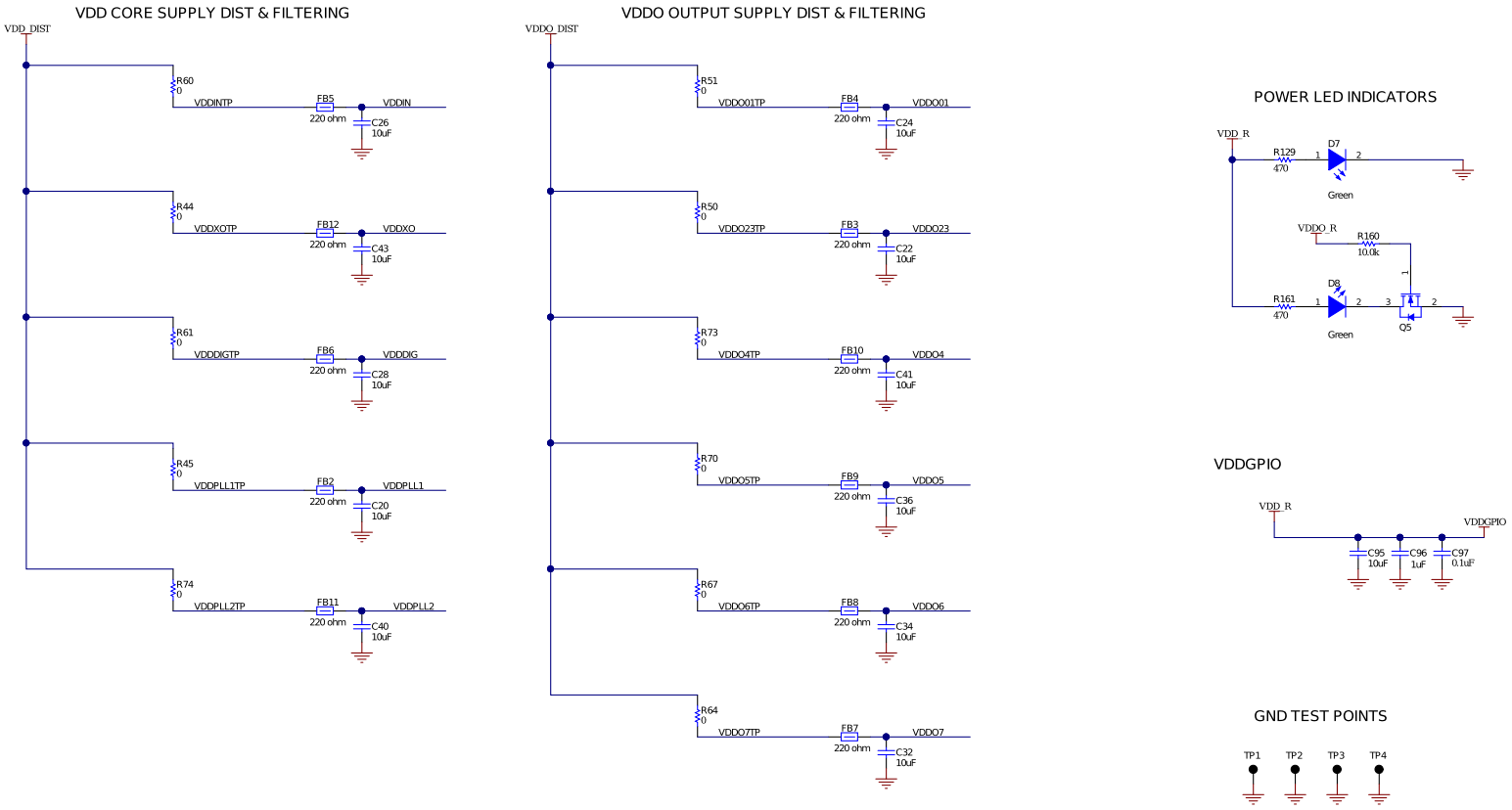


Figure 3. Schematic 2 - Power Distribution

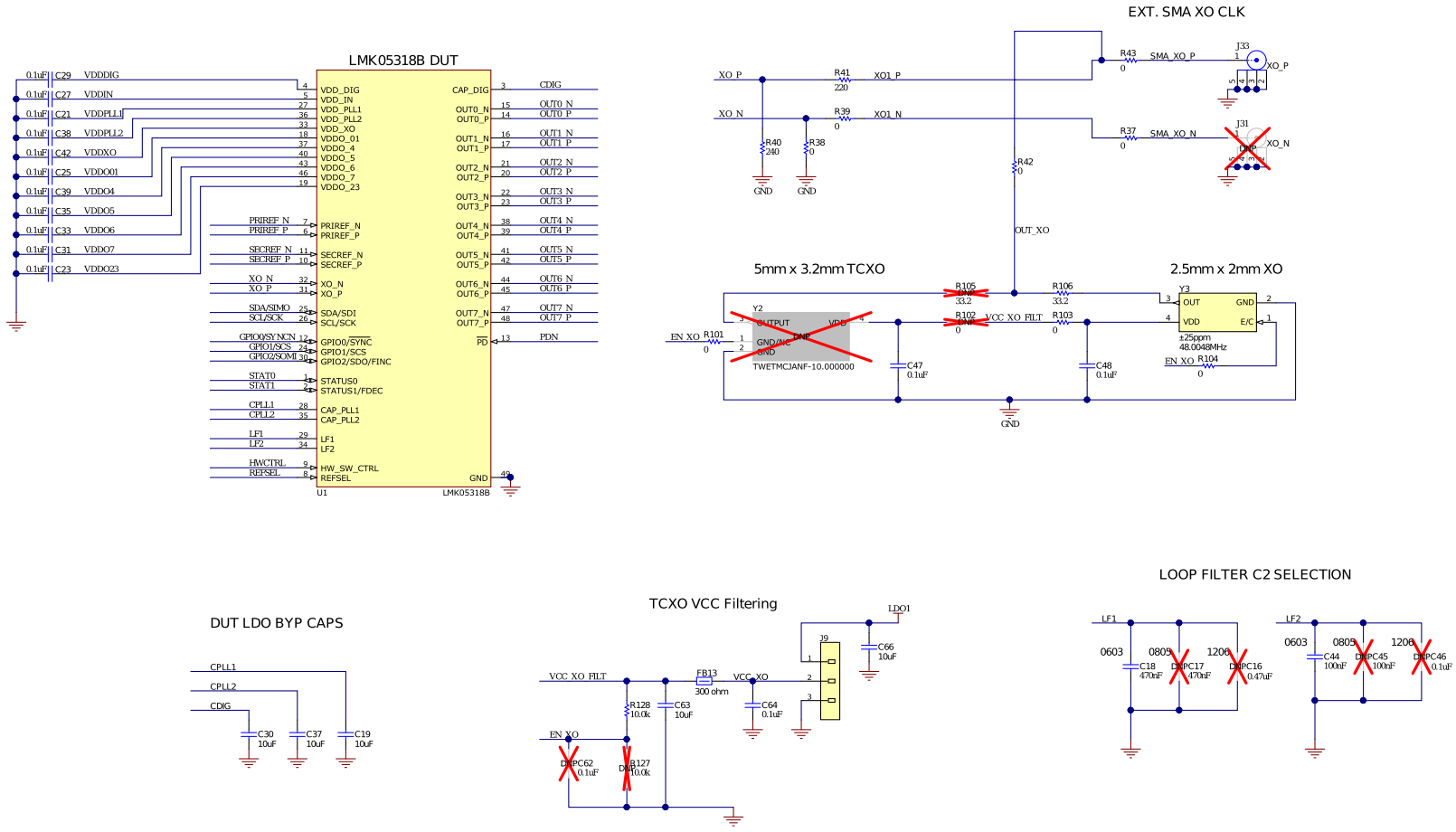


Figure 4. Schematic 3 - LMK05318B and XO Input Interfaces

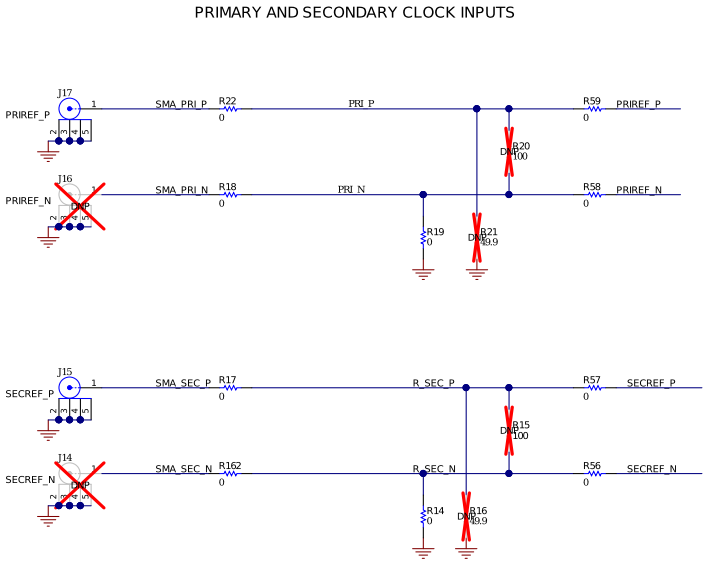


Figure 5. Schematic 4- Clock Input Interfaces

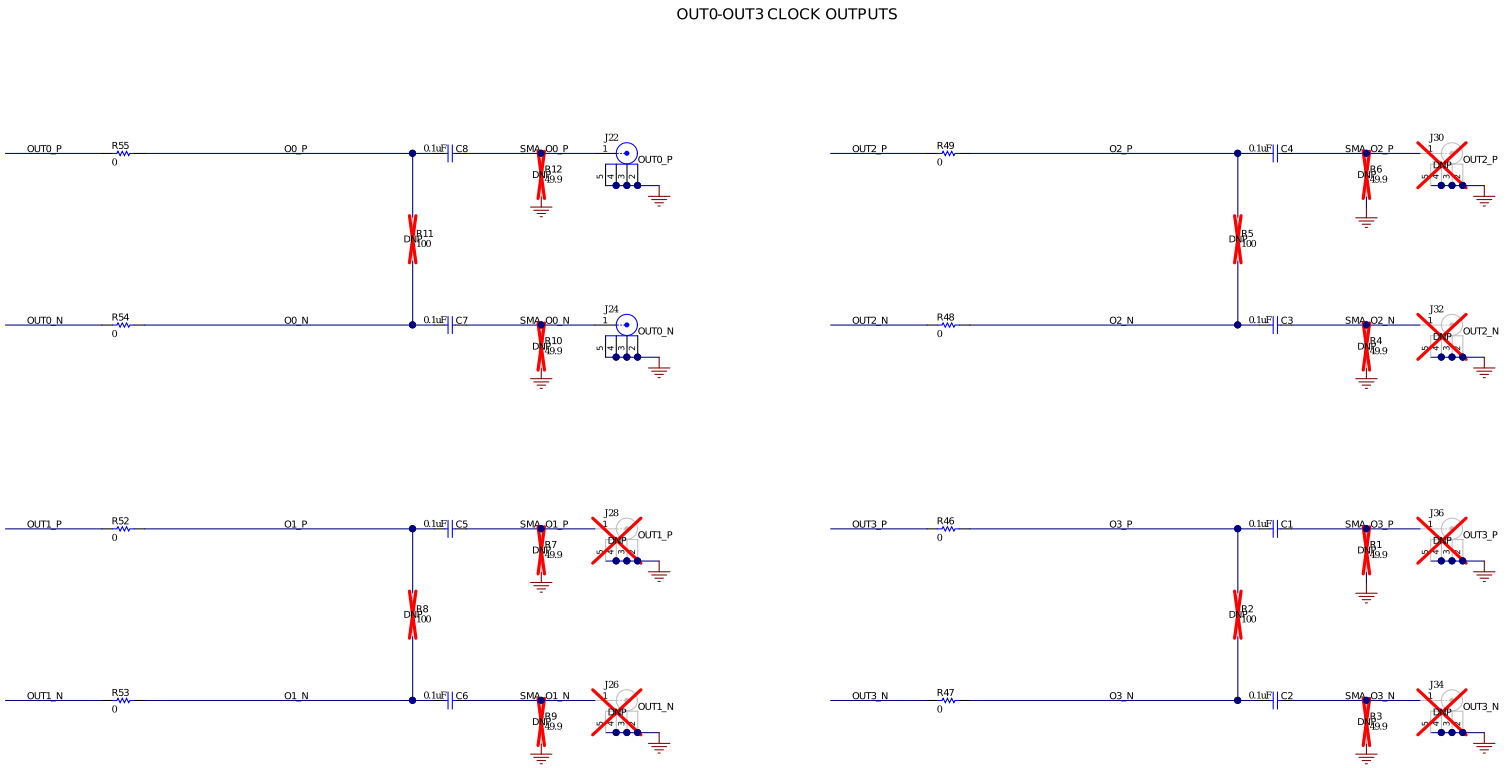


Figure 6. Schematic 5 - Clock Output Interfaces (OUT0 to OUT3)

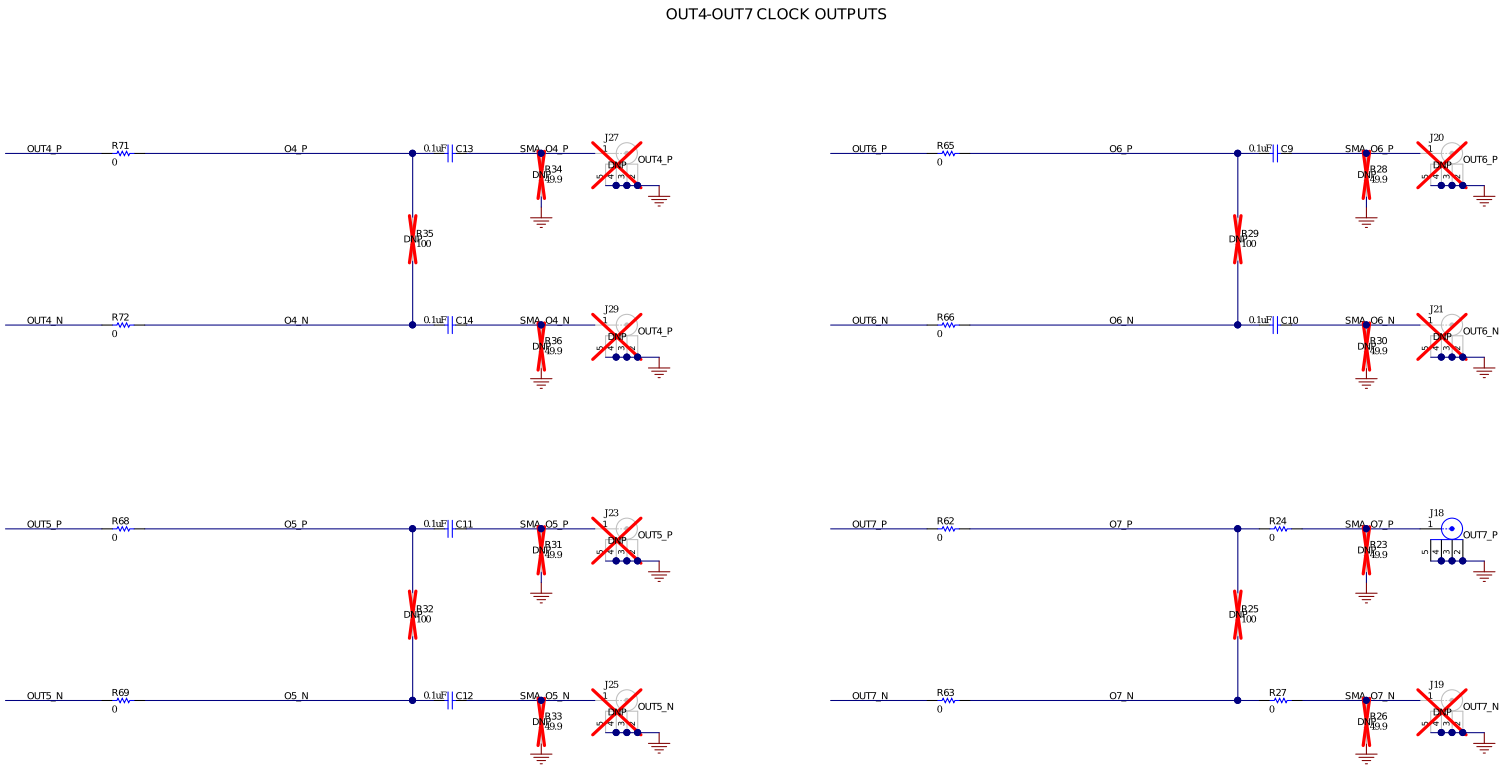


Figure 7. Schematic 6- Clock Outputs (OUT4 to OUT7)

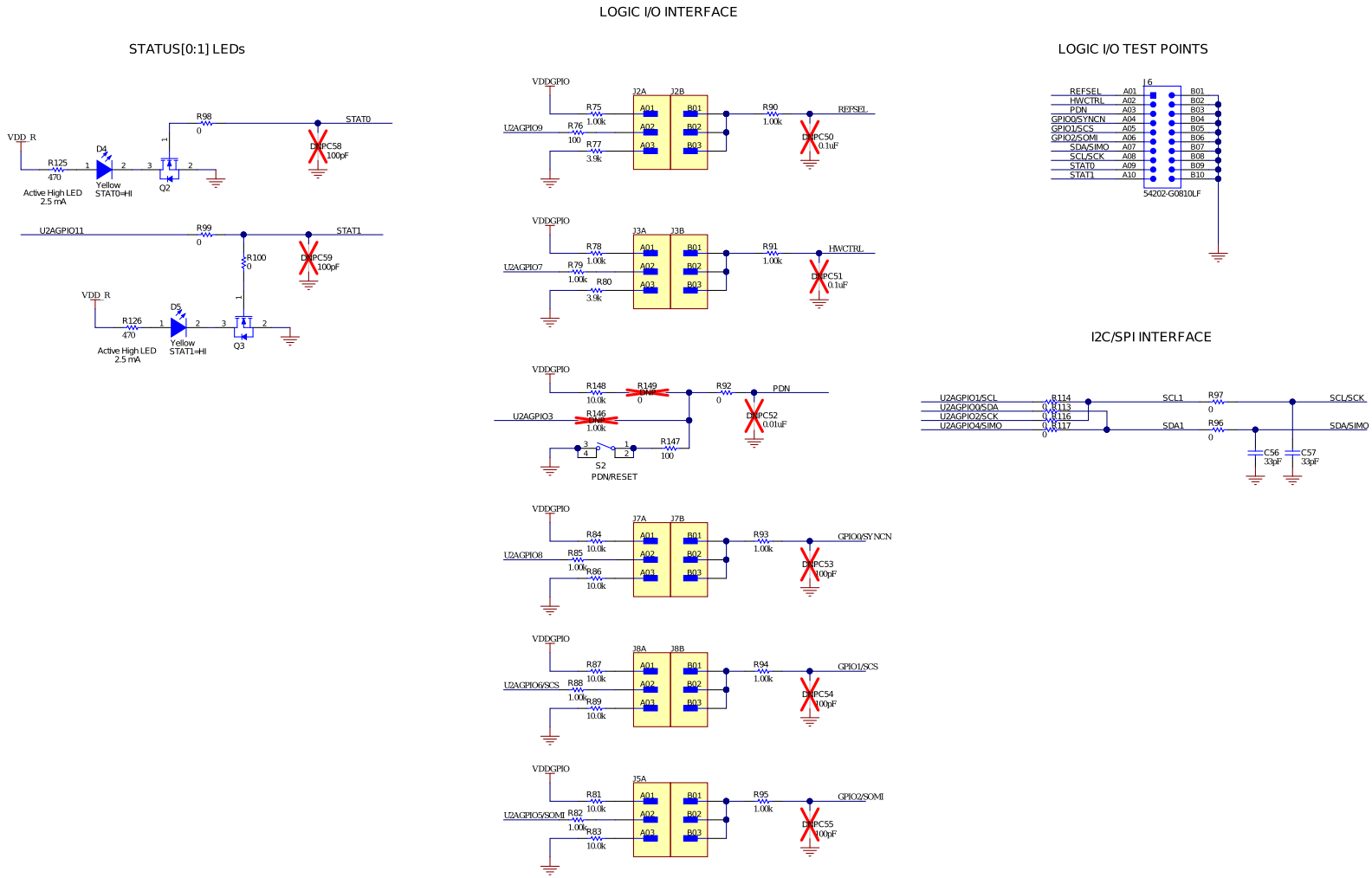


Figure 8. Schematic 7 - Logic I/O Interfaces

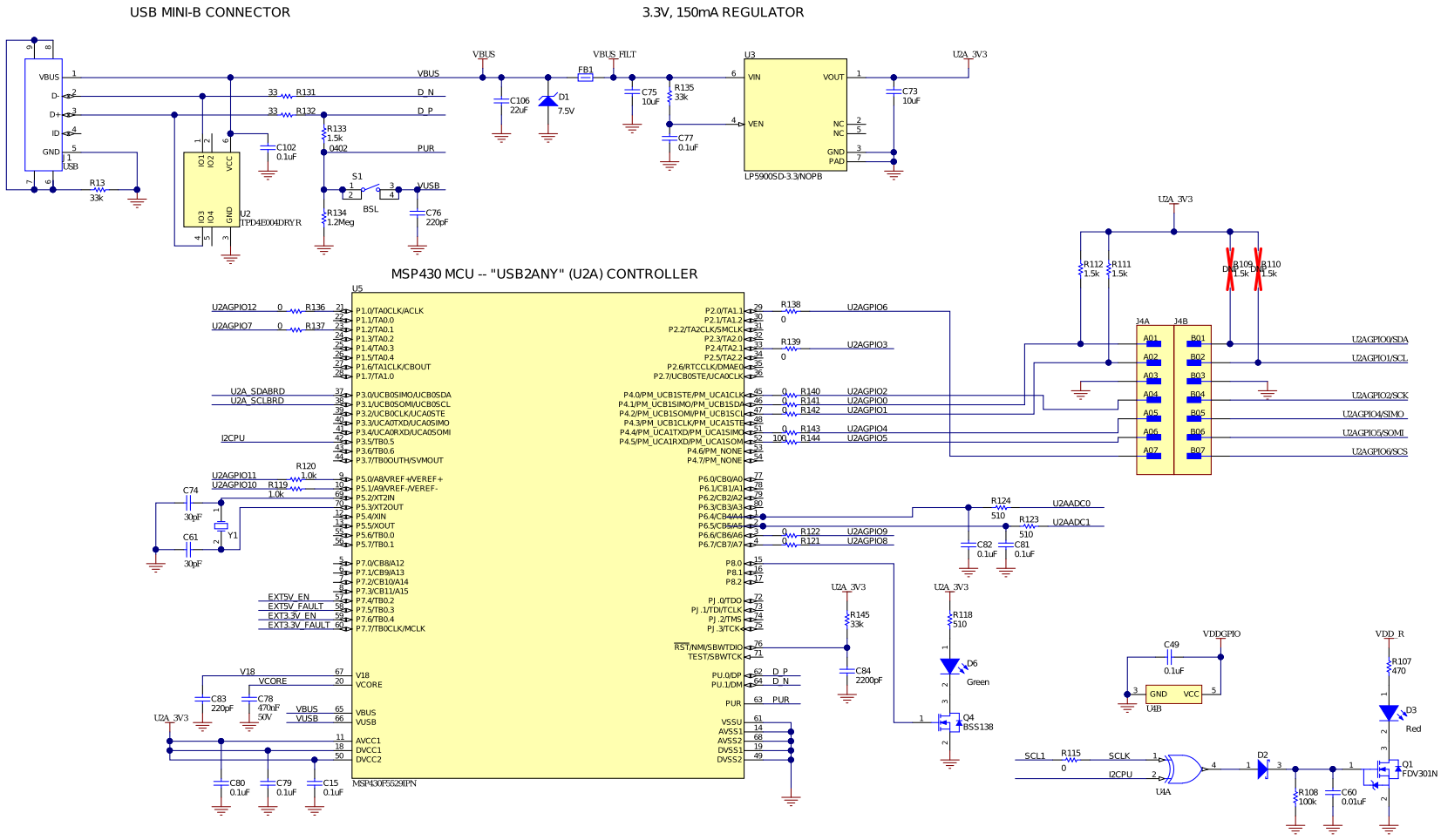
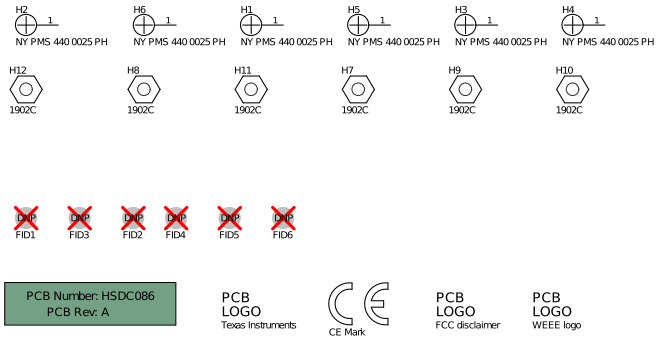


Figure 9. Schematic 8 - USB MCU and I²C/SPI Jumper Block



Default Jumper Table	
Header	Jumper connection
J10	short pin 1-2
J11	short pin 1-2
J12	short pin A03 and B03
J9	short pin 1-2
J2	short pin A02 and B02
J3	short pin A03 and B03
J7	short pin A01 and B01
J8	short pin A02 and B02
J5	short pin A02 and B02
J4	short pin A01 and B01, A02 and B02

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Variant/Label Table	
Variant	Label Text
001	LMK05318BEVM

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Figure 10. Schematic 9 - Hardware

5 EVM Layouts

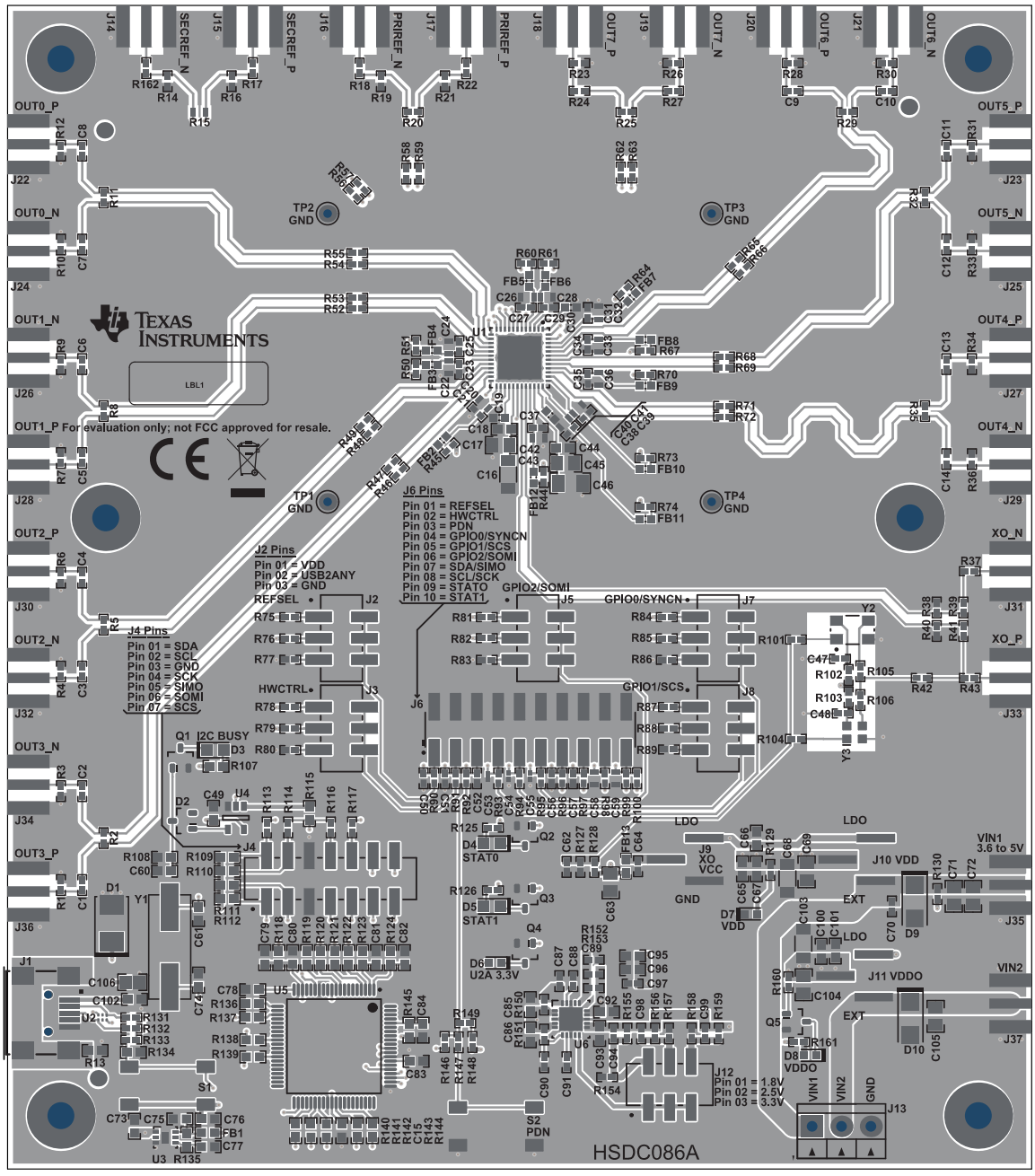


Figure 11. Top Layer Composite View

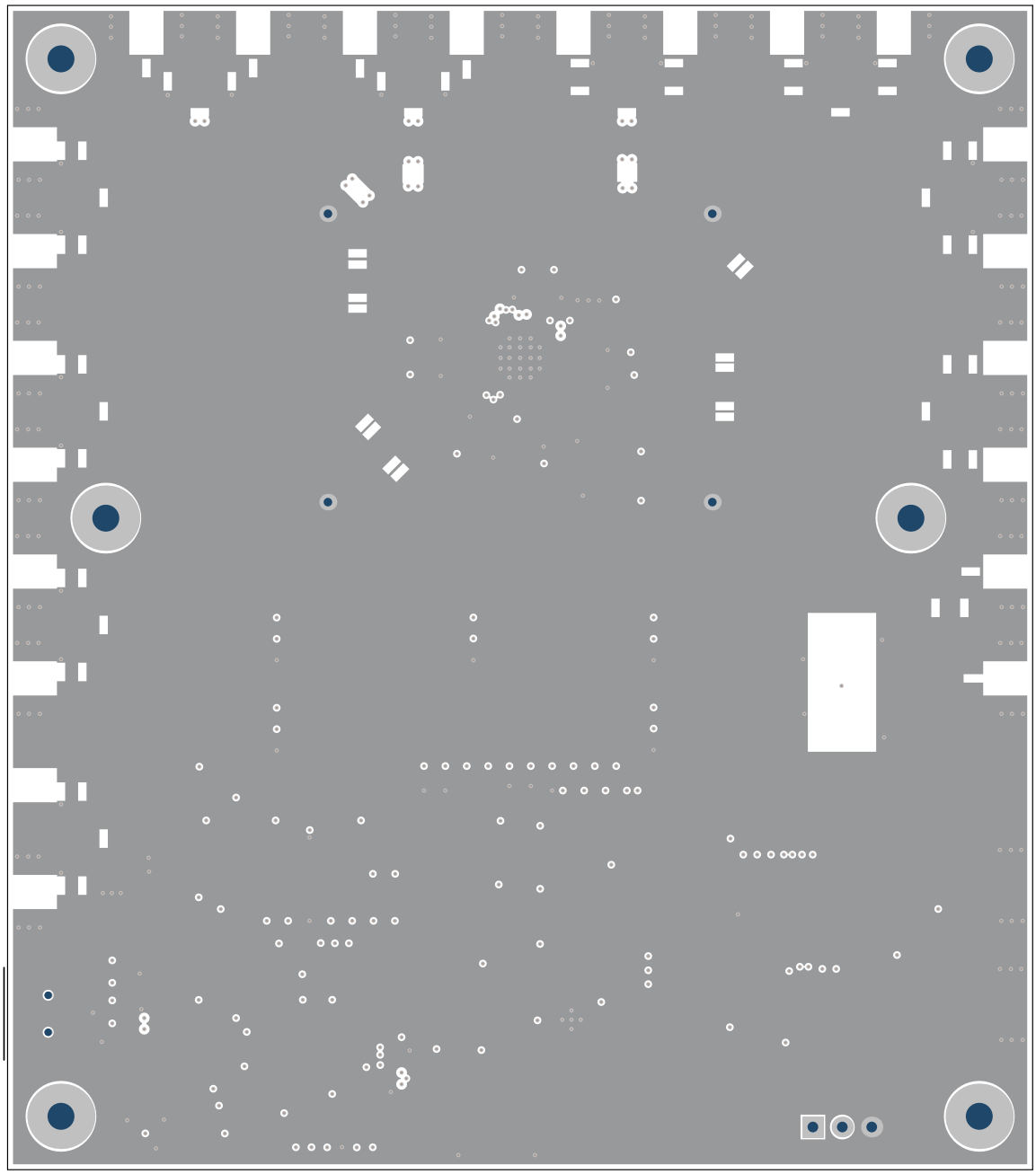


Figure 12. Layer 2 - Ground Plane

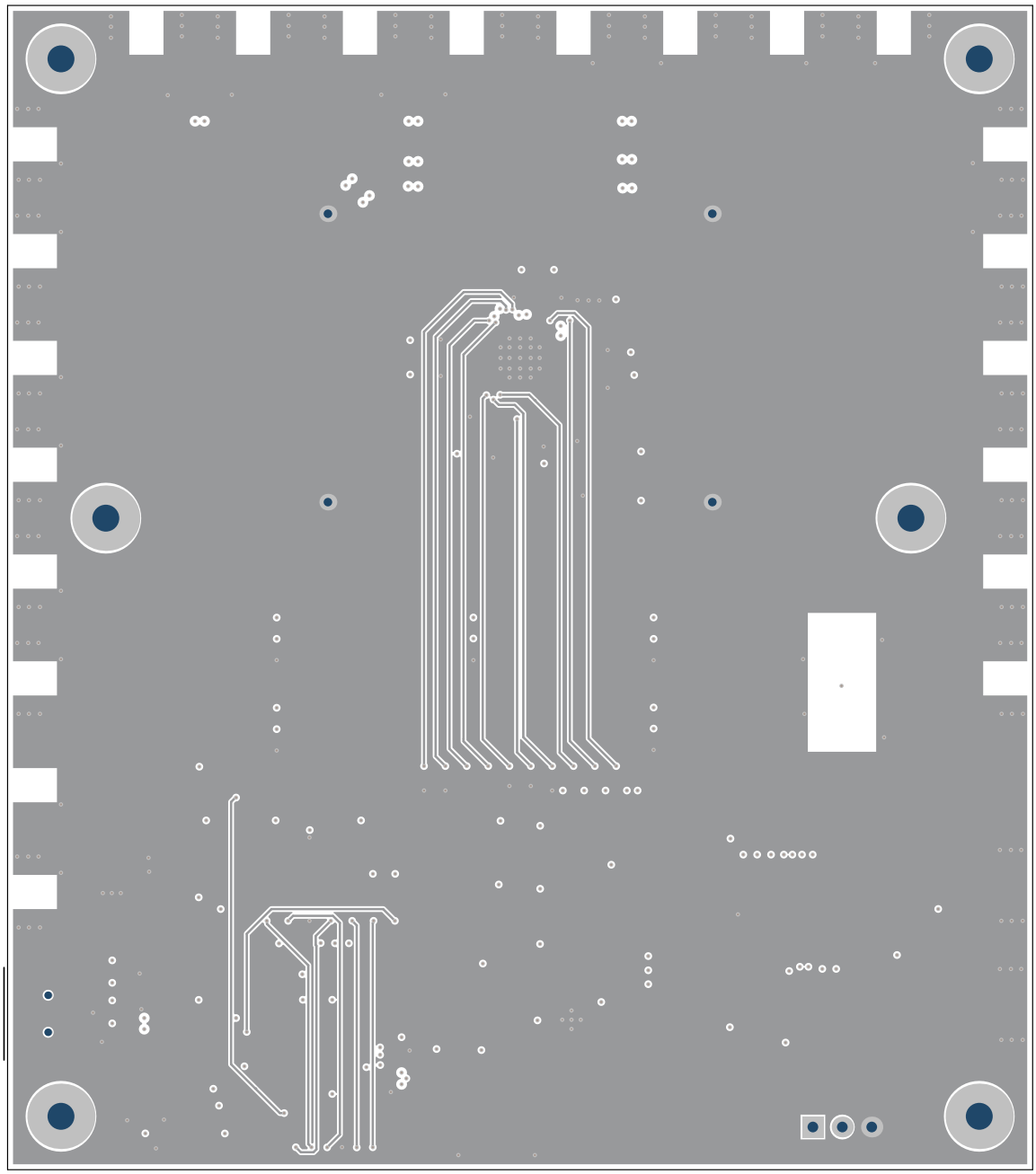


Figure 13. Layer 3 - Signal Routing

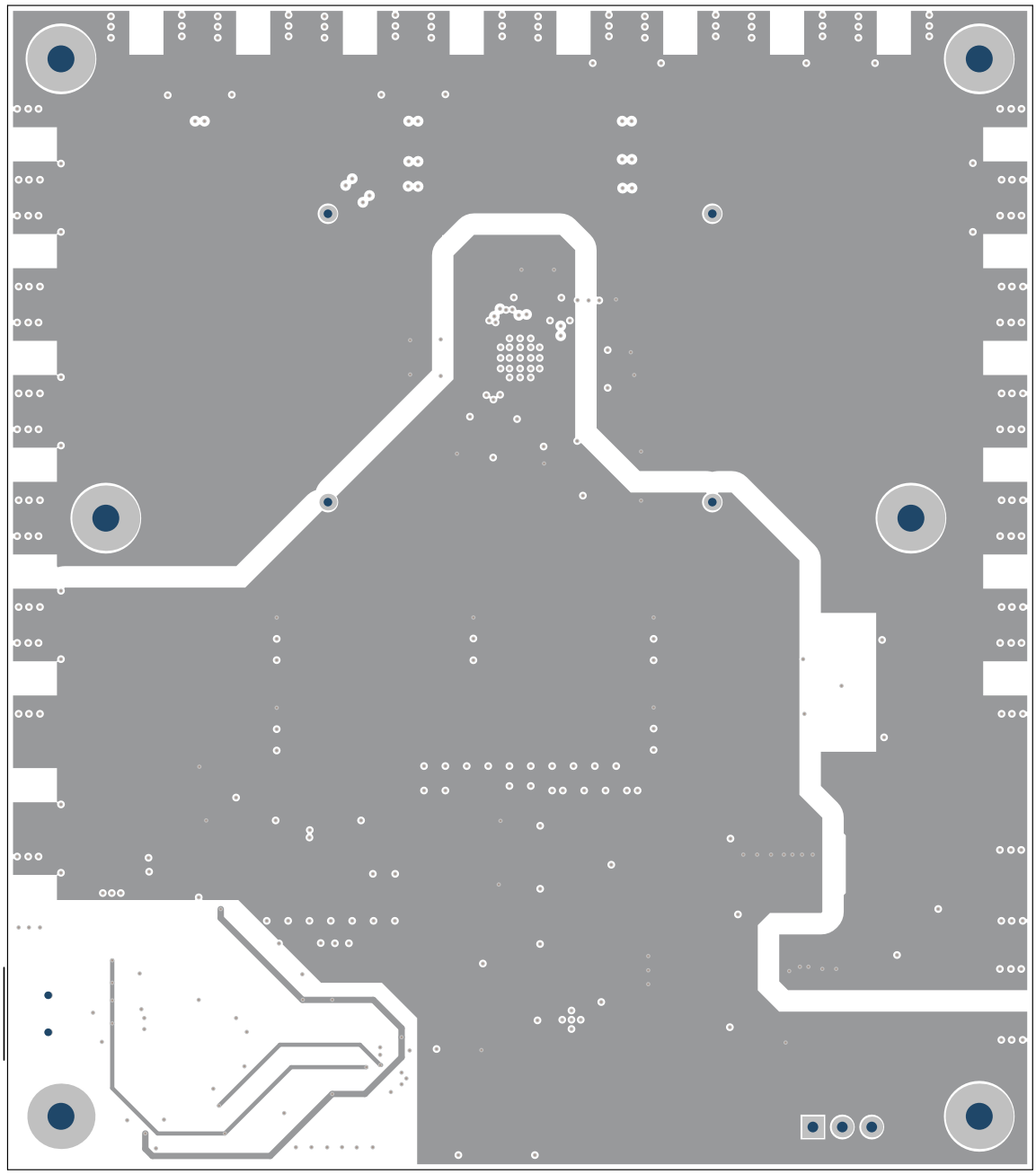


Figure 14. Layer 4 - Power Routing

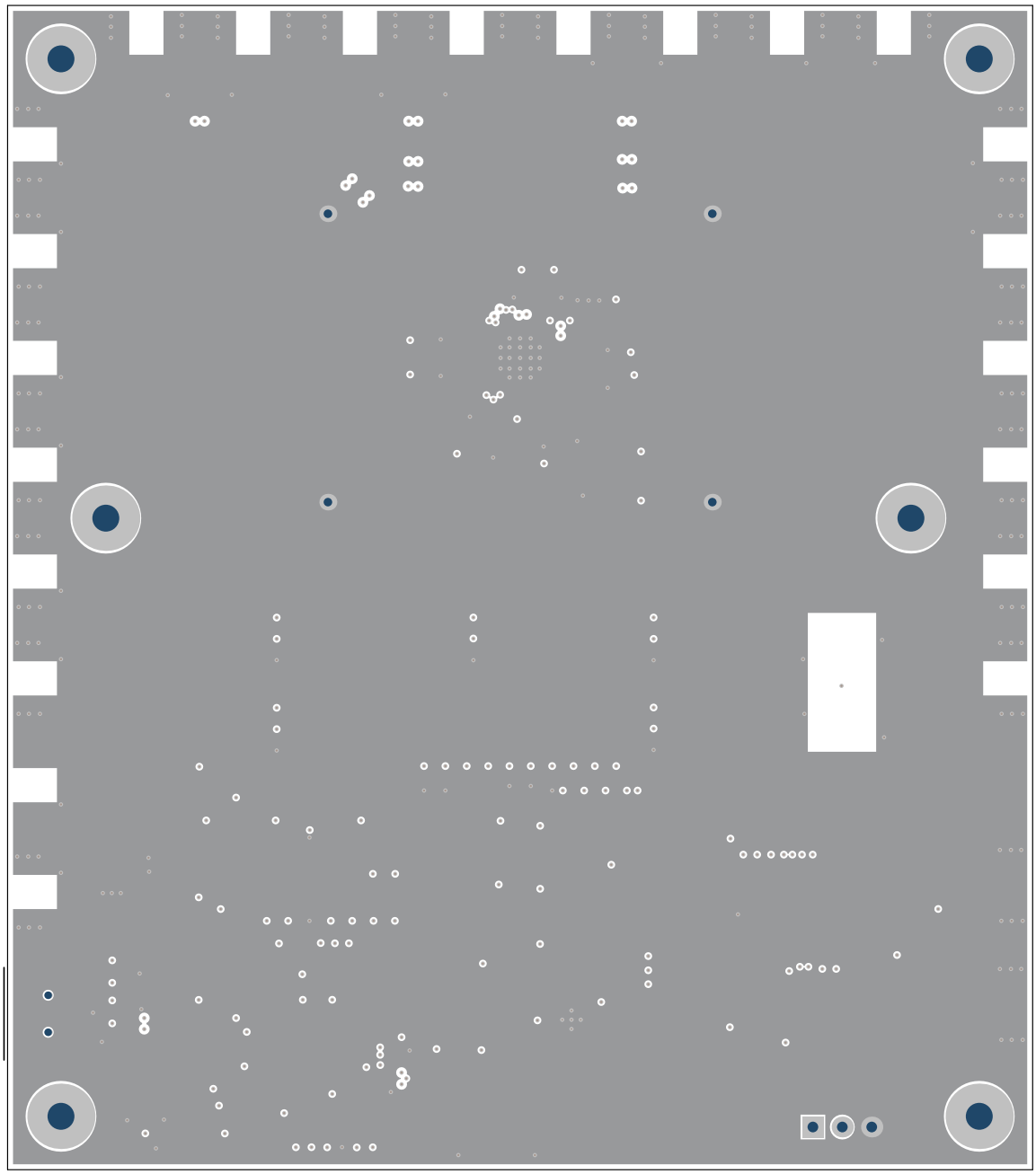


Figure 15. Layer 5 - Ground Plane

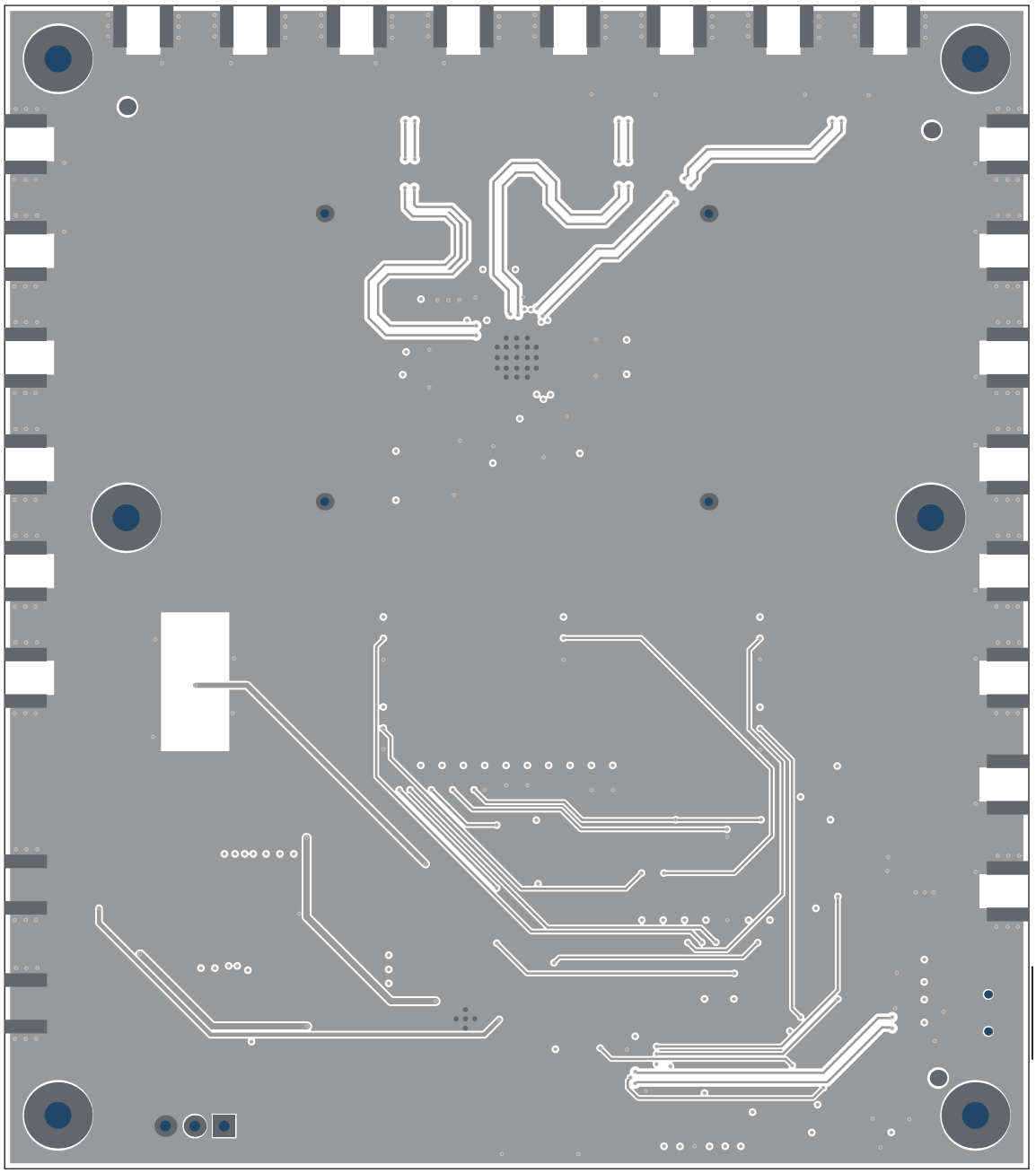


Figure 16. Bottom Layer Composite View

6 EVM Bill of Materials

Table 6. BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		HSDC086	Any
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C21, C23, C25, C27, C29, C31, C33, C35, C38, C39, C42, C47, C48, C64, C70, C88, C91, C97	32	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C15, C49, C77, C79, C80, C81, C82, C102	8	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 5%, X7R, 0603	0603	C0603C104J4RACTU	Kemet
C18, C78	2	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ± 10%, X7R, 0603	0603	C1608X7R1H474K080AC	TDK
C19, C20, C22, C24, C26, C28, C30, C32, C34, C36, C37, C40, C41, C43, C66, C73, C75, C85, C86, C92, C93, C95	22	10 µF	CAP, CERM, 10 µF, 10 V, ± 20%, X5R, 0603	0603	C1608X5R1A106M080AC	TDK
C44	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0603	0603	06035C104KAT2A	AVX
C56, C57	2	33 pF	CAP, CERM, 33 pF, 50 V, ± 5%, C0G/NP0, 0402	0402	GRM1555C1H330JA01D	MuRata
C60	1	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ± 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C61, C74	2	30 pF	CAP, CERM, 30 pF, 50 V, ± 5%, C0G/NP0, 0603	0603	06035A300JAT2A	AVX
C63	1	10 µF	CAP, CERM, 10 µF, 10 V, ± 10%, X5R, 0805	0805	LMK212BJ106KG-T	Taiyo Yuden
C65, C67, C96, C100, C101	5	1 µF	CAP, CERM, 1 µF, 10 V, ± 10%, X5R, 0603	0603	C0603C105K8PACTU	Kemet
C69, C71, C104, C106	4	22 µF	CAP, CERM, 22 µF, 10 V, ± 20%, X5R, 0805	0805	LMK212BJ226MG-T	Taiyo Yuden
C76, C83	2	220 pF	CAP, CERM, 220 pF, 50 V, ± 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX
C84	1	2200 pF	CAP, CERM, 2200 pF, 50 V, ± 10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet
C89, C94, C98, C99	4	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ± 10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
D1	1	7.5 V	Diode, Zener, 7.5 V, 550 mW, SMB	SMB	1SMB5922BT3G	ON Semiconductor
D2	1	30 V	Diode, Schottky, 30 V, 0.2 A, SOT-23	SOT-23	BAT54-7-F	Diodes Inc.
D3	1	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On
D4, D5	2	Yellow	LED, Yellow , SMD	0805 LED	LTST-C170KSKT	Lite-On
D6, D7, D8	3	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
D9, D10	2	20 V	Diode, Schottky, 20 V, 2 A, SMA	SMA	B220A-13-F	Diodes Inc.
FB1	1	60 Ω	Ferrite Bead, 60 Ω @ 100 MHz, 3.5 A, 0603	0603	MPZ1608S600ATAH0	TDK
FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11, FB12	11	220 Ω	Ferrite Bead, 220 Ω @ 100 MHz, 2.5 A, 0603	0603	BLM18SG221TN1D	MuRata
FB13	1	300 Ω	Ferrite Bead, 300 Ω @ 100 MHz, 0.4 A, 1.6x0.8x0.95 mm	1.6x0.8x0.95 mm	LI0603D301R-10	Laird-Signal Integrity Products
H1, H2, H3, H4, H5, H6	6		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B and F Fastener Supply
H7, H8, H9, H10, H11, H12	6		Standoff, Hex, 0.5 in L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	USB Mini Type B	1734035-2	TE Connectivity
J2, J3, J5, J7, J8, J12	6		Connector Header Surface Mount 6 position 0.100 in (2.54 mm)	HDR6	54202-G0803LF	Amphenol ICC
J4	1		Connector Header Surface Mount 14 position 0.100 in (2.54 mm)	HDR14	54202-G0807LF	Amphenol ICC
J6	1		Header, 2.54 mm, 10x2, Tin, SMT	Header, 2.54 mm, 10x2, SMT	54202-G0810LF	FCI
J9, J10, J11	3		3 Positions Header, Unshrouded Connector 0.100 in (2.54 mm) Surface Mount Tin	HDR3	NREC003SABC-M30RC	Sullins Connector Solutions
J13	1		Terminal Block, 3.5 mm Pitch, 3x1, TH	10.5x8.2x6.5 mm	ED555/3DS	On-Shore Technology

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J15, J17, J18, J22, J24, J33, J35	7		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
LBL1	1		Thermal Transfer Printable Labels, 0.650 in W x 0.200 in H - 10,000 per roll	PCB Label 0.650 x 0.200 in	THT-14-423-10	Brady
Q1	1	25 V	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor
Q2, Q3, Q4, Q5	4	50 V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R13, R135, R145	3	33 k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333K0JNEA	Vishay-Dale
R14, R17, R18, R19, R22, R24, R27, R37, R38, R39, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R92, R96, R97, R98, R99, R100, R101, R103, R104, R113, R114, R116, R117, R130, R162	58	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R40	1	240	RES, 240, 5%, 0.063 W, 0402	0402	CRCW0402240RJNED	Vishay-Dale
R41	1	220	RES, 220, 5%, 0.063 W, 0402	0402	CRCW0402220RJNED	Vishay-Dale
R75, R78, R79, R82, R85, R88, R90, R91, R93, R94, R95	11	1.00 k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R76, R147	2	100	RES, 100, 5%, 0.063 W, 0402	0402	CRCW0402100RJNED	Vishay-Dale
R77, R80	2	3.9 k	RES, 3.9 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K90JNED	Vishay-Dale
R81, R83, R84, R86, R87, R89, R128, R148, R160	9	10.0 k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R106	1	33.2	RES, 33.2, 1%, 0.063 W, 0402	0402	CRCW040233R2FKED	Vishay-Dale

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R107	1	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale
R108	1	100 k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R111, R112	2	1.5 k	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K50JNEA	Vishay-Dale
R115, R121, R122, R136, R137, R138, R139, R140, R141, R142, R143	11	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R118, R123, R124	3	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603510RJNEA	Vishay-Dale
R119, R120	2	1.0 k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R125, R126, R129, R161	4	470	RES, 470, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402470RJNED	Vishay-Dale
R131, R132	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R133	1	1.5 k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R134	1	1.2 Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M20JNEA	Vishay-Dale
R144	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RJNEA	Vishay-Dale
R150, R151	2	47 k	RES, 47 k, 5%, 0.063 W, 0402	0402	CRCW040247K0JNED	Vishay-Dale
R152, R157, R158	3	1.15 k	RES, 1.15 k, 1%, 0.063 W, 0402	0402	CRCW04021K15FKED	Vishay-Dale
R153, R159	2	3.57 k	RES, 3.57 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K57FKED	Vishay-Dale
R154	1	1.50 k	RES, 1.50 k, 1%, 0.063 W, 0402	0402	CRCW04021K50FKED	Vishay-Dale
R155	1	1.87 k	RES, 1.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K87FKED	Vishay-Dale

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R156	1	2.43 k	RES, 2.43 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K43FKED	Vishay-Dale
S1, S2	2		Switch, Tactile, SPST-NO, 0.05 A, 12 V, SMT	SW, SPST 6x6 mm	FSM4JSMA	TE Connectivity
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11	11	1x2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4	4		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1	1		Ultra-Low Jitter Network Synchronizer Clock With Two Frequency Domains	VQFN48	LMK05318B	Texas Instruments
U2	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
U3	1		150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	NGF0006A	LP5900SD-3.3/NOPB	Texas Instruments
U4	1		Single 2-Input Exclusive-OR Gate, DBV0005A, LARGE T and R	DBV0005A	SN74LVC1G86DBVR	Texas Instruments
U5	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 °C, 80-pin QFP (PN), Green (RoHS and no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U6	1		Dual 1A Low-Noise (3.8μVRMS) LDO Voltage Regulator, RTJ0020D (WQFN-20)	RTJ0020D	TPS7A8801RTJR	Texas Instruments
Y1	1		Crystal, 24 MHz, 20 pF, SMD	Crystal, 11.4x4.3x3.8 mm	ECS-240-20-5PXDN-TR	ECS Inc.
Y3	1		Crystal, 48.0048 MHz, 15 pF, SMD	Crystal Oscillator	8W48070002	TXC Corporation

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C16	0	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ± 10%, X7R, 1206	1206	C3216X7R1H474K160AA	TDK
C17	0	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ± 10%, X7R, 0805	0805	GRM21BR71H474KA88L	MuRata
C45	0	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0805	0805	CC0805KRX7R9BB104	Yageo America
C46	0	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 20%, X7R, 1206	1206	12065C104MAT2A	AVX
C50, C51, C62	0	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C52, C87, C90	0	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ± 10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata
C53, C54, C55	0	100 pF	CAP, CERM, 100 pF, 16 V, ± 10%, X7R, 0201	0201	GRM033R71C101KA01D	MuRata
C58, C59	0	100 pF	CAP, CERM, 100 pF, 50 V, ± 5%, C0G/NP0, 0603	0603	06035A101JAT2A	AVX
C68, C103	0	10 µF	CAP, CERM, 10 µF, 25 V,± 20%, X5R, 1206	1206	GRM31CR61E106MA12L	MuRata
C72, C105	0	47 µF	CAP, CERM, 47 µF, 10 V,± 20%, X5R, 0805	0805	GRM21BR61A476ME15L	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J14, J16, J19, J20, J21, J23, J25, J26, J27, J28, J29, J30, J31, J32, J34, J36, J37	0		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
R1, R3, R4, R6, R7, R9, R10, R12, R16, R21, R23, R26, R28, R30, R31, R33, R34, R36	0	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	CRCW040249R9FKED	Vishay-Dale
R2, R5, R8, R11, R20, R25, R29, R32, R35	0	100	RES, 100, 5%, 0.063 W, 0402	0402	CRCW0402100RJNED	Vishay-Dale
R15	0	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RFKEA	Vishay-Dale
R102, R149	0	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R105	0	33.2	RES, 33.2, 1%, 0.063 W, 0402	0402	CRCW040233R2FKED	Vishay-Dale

Table 6. BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R109, R110	0	1.5 k	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K50JNEA	Vishay-Dale
R127	0	10.0 k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R146	0	1.00 k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	CRCW04021K00FKED	Vishay-Dale
Y2	0		10 MHz TCXO CMOS Oscillator 3.3 V 4-SMD, No Lead	SMT4_5MM0_3MM2	TWETMCJANF-10.000000	Taitien

7 References

- TICS Pro Software GUI
- Texas Instruments Clocks and Synthesizers (TICS) Pro Software

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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