LMK04832EVM-CVAL User's Guide

The LMK04832EVM-CVAL evaluation module (EVM) provides a platform to evaluate the performance and features of the LMK04832-SP Space Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner from Texas Instruments. The user's guide describes how to set up and operate the EVM. The LMK04832-SP device on each EVM is an Engineering Model, intended for engineering evaluation only. The devices and EVMs are not suitable for qualification, production, radiation testing or flight use.

Contents

List of Figures

List of Tables

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1 Evaluation Board Kit Contents

Table 1 lists the components found in the evaluation board kit.

Table 1. EVM Contents

HSDC005	
Evaluation Board	(1) LMK04832EVM-CVAL Evaluation Board with VCXO
Communication Interface	(1) USB2ANY

2 Quick Start

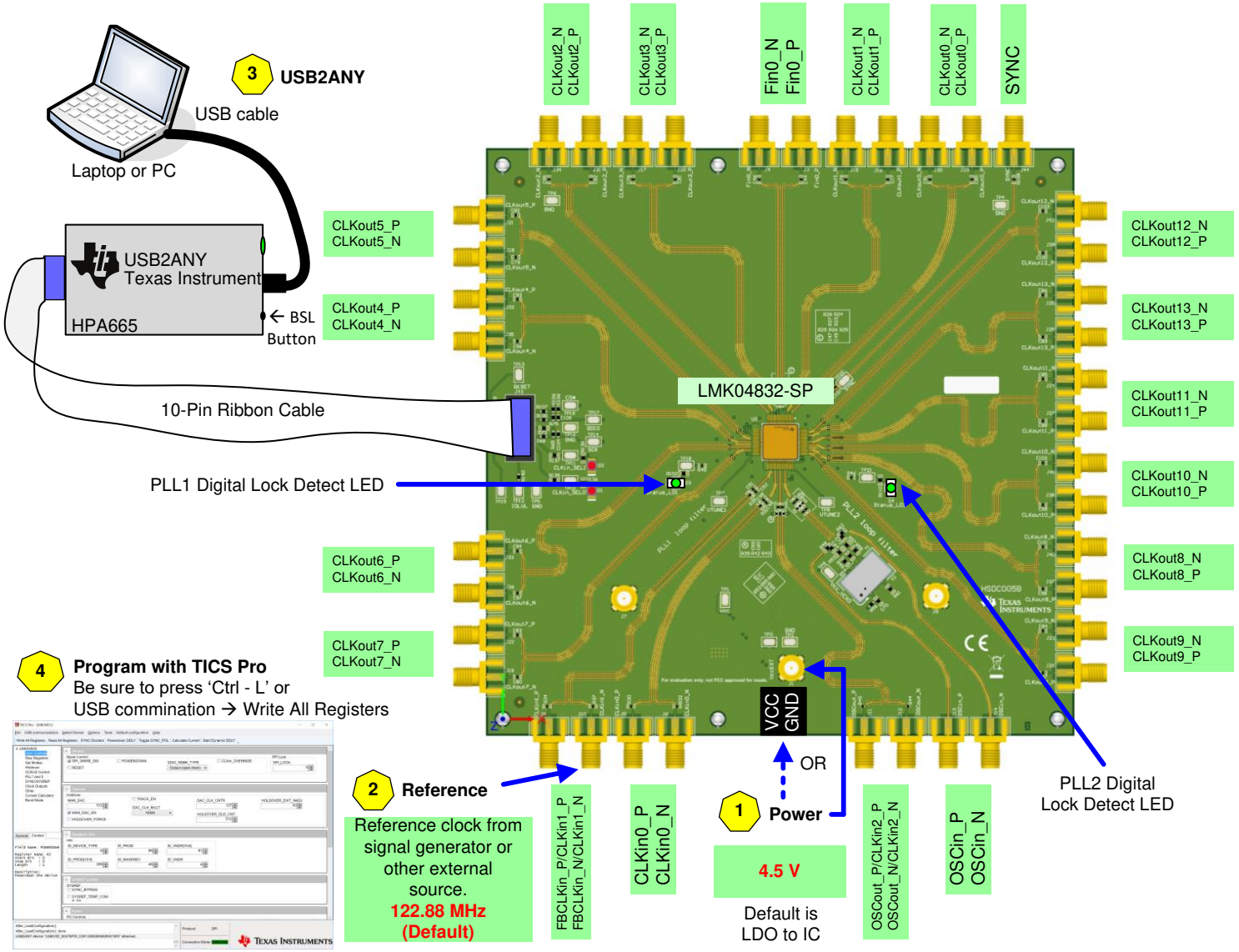

Figure 1. Quick Start Diagram

2.1 Quick Start Description

The LMK04832EVM-CVAL allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Connect a voltage of **4.5** volts to the V_{CC} SMA connector or terminal block. The LMK04832-SP and on-board VCXO operate at 3.3 V provided by the onboard TPS7A4501-SP LDO.
2. Connect a reference clock to the CLKin1* port from a signal generator or other source. Use **122.88 MHz** for default configuration.
3. Connect USB2ANY to a PC and the EVM.
4. Program the device with TICS Pro. TICS Pro is available for download at: http://www.ti.com/tool/ticspro-sw.
   a. Select LMK04832-SP from the *Select Device* Menu. Click *Select Device → Clock Generator/Jitter Cleaner (Dual Loop)*.
   b. Select **USB2ANY mode** from the Communication Setup window. To access this, select *USB communications → Interface*. Confirm that the PC to USB communication is working by clicking on *Identify.* A blinking green LED on the USB2ANY indicates the PC is able to communicate through the USB2ANY.
   c. Select a default mode from the *Default configuration* Menu. For the quick start use, *CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz*.
   d. **Ctrl+L** must be pressed at least once to load all registers. Alternatively, click the *USB communications → Write All Registers* menu, the *Write All Registers* button on toolbar, or the **Raw Registers** page shown in Section A.3.
5. Measurements may be made at an active CLKout port through the SMA connector.

2.1.1 Clock Outputs Page Description

Clock outputs are grouped in pairs. This description applies for all clock outputs on the Clock Outputs page of the TICS Pro GUI shown in Section A.9.

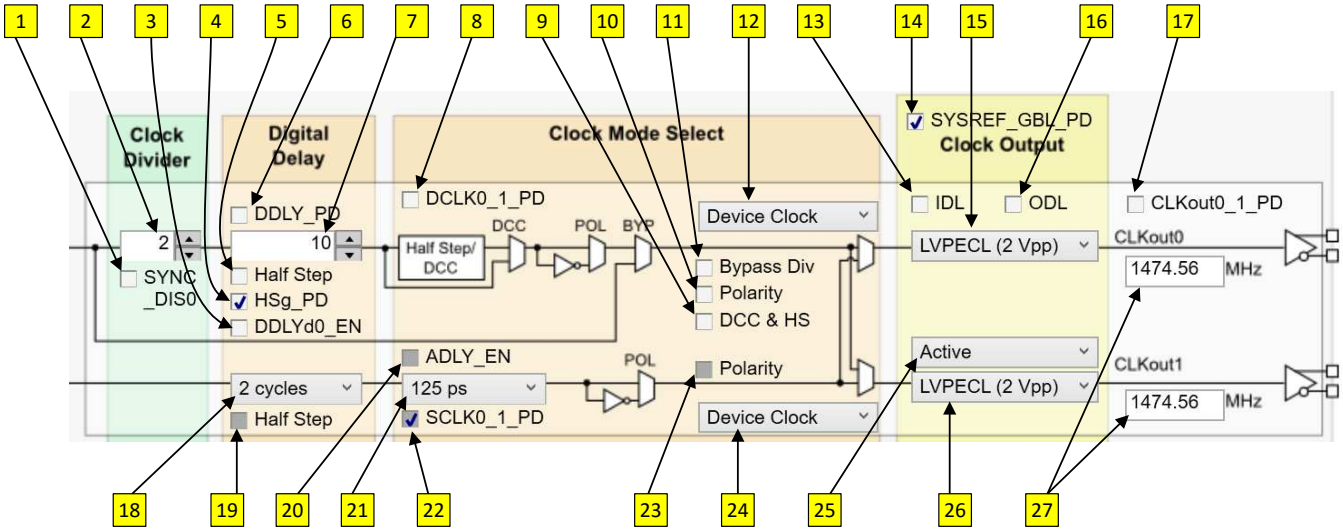

Figure 2. Clock Outputs Page Description Diagram

1. SYNC_DISX: Prevent the divider from being reset by SYNC/SYSREF path.
2. DCLKX_Y_DIV: Divide value for the device clock. If set to 1, then DCLKX_Y_DCC (DCC & HS) must = 1.
3. DDLYdX_EN: Enable dynamic digital delay for this divider.
4. DCLKX_Y_HSg_PD: If clear, glitchless half-step adjustments are enabled.
5. DCLKX_Y_HS: Set half step for this divider. DCLKX_Y_DCC (DCC & HS) must = 1.
6. DCLKX_Y_DDLY_PD: If clear, the digital delay value is assured when a SYNC occurs.
7. DCLKX_Y_DDLY: The digital delay value to be used when a SYNC occurs.
8. DCLKX_Y_PD: Power down the device clock divider and path.
9. DCLKX_Y_DCC: Enable duty cycle correct and half-step for this device clock divider.
10. DCLKX_Y_POL: If set, polarity of device clock is inverted.
11. DCLKX_Y_BYP: If set, the device clock divider is bypassed for CLKoutX and #15 must be CML.
12. CLKoutX_SRC_MUX: Select device clock or SYSREF clock path for CLKoutX.
13. CLKoutX_Y_IDL: Increase input drive level to improve noise floor at cost of power (~2 mA).
14. SYSREF_GBL_PD: Set the conditional for SCLKX_Y_DIS_MODE registers.
15. CLKoutX_FMT: Set the clock output format for CLKoutX.
16. CLKoutX_Y_ODL: Increase output drive level to improve noise floor at cost of power (~3 mA). No effect for CLKoutX in bypass mode.
17. CLKoutX_Y_PD: Power down the entire CLKoutX_Y clock pair.
18. SCLKX_Y_DDLY: The SYSREF clock digital delay setting.
19. SCLKX_Y_HS: Set half step for the SYSREF output.
20. SCLKX_Y_ADLY_EN: Enable analog delay for the SYSREF clock path.
21. SCLKX_Y_ADLY: If enabled, set the analog delay for the SYSREF clock path.
22. SCLKX_Y_PD: Power down the SYSREF clock path.
23. SCLKX_Y_POL: If set, polarity of SYSREF output clock is inverted.
24. CLKoutY_SRC_MUX: Select device clock or SYSREF clock path for CLKoutY.
25. SCLKX_Y_DIS_MODE: Set the output state of output clock drivers for the SYSREF clock. For values

of 1 and 2 works in conjunction with control on this list #14, SYSREF_GBL_PD.

26. CLKoutY_FMT: Set the clock output format for CLKoutY.
27. Clock output frequency for CLKoutX and CLKoutY.

2.1.2 TICS Pro Tips

Mousing over different controls will display a help prompt with the register address, the data bit location and length, and a brief register description in the lower-left *Context* help pane.

Setting a register equal to 0 or un-checking a register's checkbox performs the same action. Similarly, setting a register equal to 1 *is the same as* checking that register's checkbox.

3 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO) for the phase noise of a dirty reference clock. The first PLL is typically configured with a narrow loop bandwidth to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK04832EVM-CVAL evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 1 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. Table 2 and Table 3 contain the parameters for PLL1 and PLL2 for each oscillator option.

TI's PLLatinum™ Sim tool can be used to optimize PLL phase noise/jitter for given specifications. See http://www.ti.com/tool/pllatinumsim-sw for more information.

3.1 PLL1 Loop Filter

Table 2. PLL1 Loop Filter Parameters for Crystek 122.88-MHz VCXO(1)

122.88-MHz VCXO PLL			
Phase Margin	50˚	**Kφ (Charge Pump)**	450 µA
Loop Bandwidth	14 Hz	**Phase Detector Freq**	1.024 MHz
		VCO Gain	2.5 kHz/V
Reference Clock Frequency	122.88 MHz	**Output Frequency**	122.88 MHz (To PLL 2)
Loop Filter Components	LF1_C1 (C75) = 100 nF	LF1_C2 (C73) = 680 nF	LF1_R2 (R64) = 39 kΩ

(1) Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

3.2 PLL2 Loop Filter

Table 3. Integrated VCO PLL(1)

PARAMETER	LMK04832-SP		UNIT
	VCO0	VCO1	
LF2_C1 (C58)	0.047		nF
LF2_C2 (C56)	3.9		nF
C3 (internal)	0.03		nF
C4 (internal)	0.01		nF
LF2_R2 (R41)	0.62		kΩ
R3 (internal)	0.2		kΩ
R4 (internal)	0.2		kΩ
Charge Pump Current, Kφ	3.2		mA

(1) PLL Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

Table 3. Integrated VCO PLL[1] (continued)

PARAMETER	LMK04832-SP		UNIT
	VCO0	VCO1	
Phase Detector Frequency	122.88		MHz
Frequency	2457.6	2949.12	MHz
Kvco	13.0	25.0	MHz/V
N	20	24	
Phase Margin	68	71	degrees
Loop Bandwidth	210	326	kHz

4 Default TICS Pro Mode

TICS Pro saves the state of the selected LMK04832-SP device when exiting the software. To ensure a common starting point, the following modes listed in Table 4 may be restored by clicking *Default configuration* and selecting the appropriate device configuration.

Table 4. Default TICS Pro Modes for the LMK04832-SP

DEFAULT TICS PRO MODE	DEVICE MODE	CLKin FREQUENCY	OSCin FREQUENCY
CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz

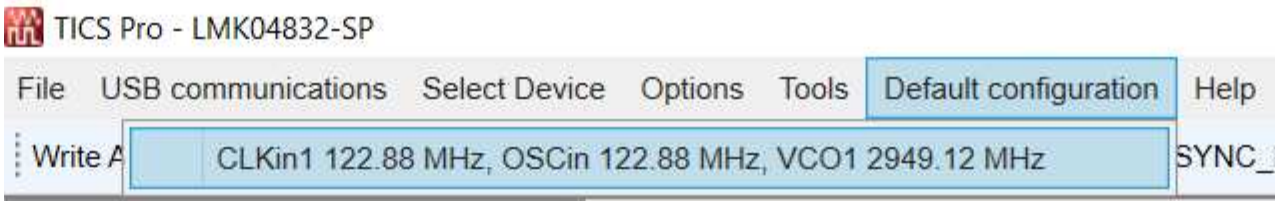

Figure 3. Selecting a Default Mode for the LMK04832-SP Device

5 Using TICS Pro to Program the LMK04832-SP

This section will demonstrate how to use TICS Pro. For more information on using TICS Pro, refer to Appendix A. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

Before proceeding, be sure to follow the instructions in Section 2 to ensure proper hardware connections.

5.1 Start TICS Pro Application

Click *Start* → *Programs* → *Texas Instruments* → *TICS Pro*.

The TICS Pro program is installed by default to the Texas Instruments application group.

5.2 Select Device

Click *Select Device* → *Clock Generator/Jitter Cleaner (Dual Loop)* → *LMK04832-SP*.

Once started, TICS Pro will load the last used device. A recent history of used devices can be quickly accessed under the *File* Menu. To load a new device, click *Select Device* from the menu bar, select the subgroup, then select the device to load.

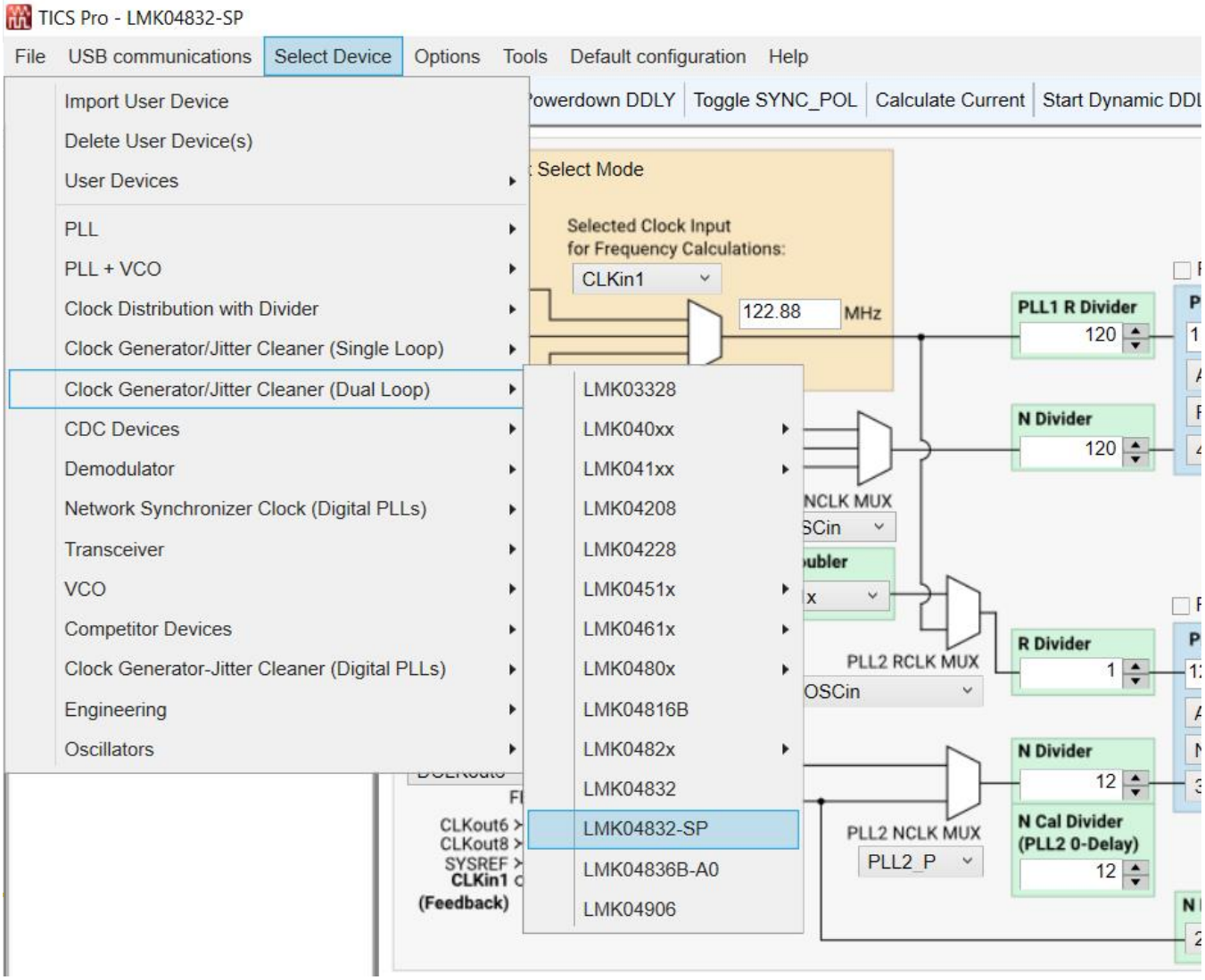

Figure 4. Selecting the LMK04832-SP

5.3 Program the Device

To program, press *Ctrl+L*.

Alternatively, click *USB communications → Write All Registers* from the menu to program the device to the current state of the register map to the device. *Ctrl+L* is the accelerator key assigned to the *Write All Registers* option and is very convenient.

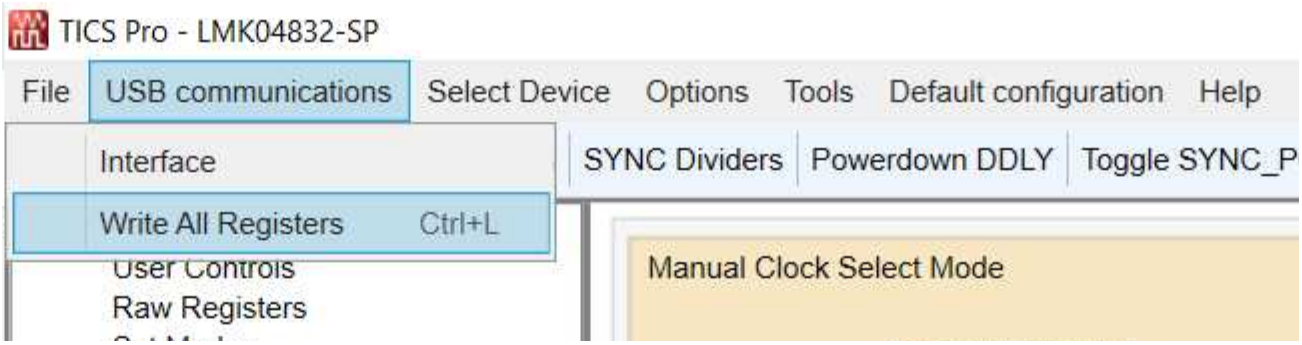

Figure 5. Loading the Device

Once the device has been initially loaded, TICS Pro will automatically program changed registers, so it is not necessary to reload the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the *Options → AutoUpdate*.

A default mode will be restored in the next step, therefore this step is not necessary. It is included, however, to emphasize the importance of pressing *Ctrl+L* to load the device at least once after starting TICS Pro, restoring a mode, or restoring a saved setup using the File menu.

See TICS Pro instructions located at http://www.ti.com/tool/ticspro-sw/.

5.4 Restoring a Default Mode

Click *Default configuration → CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz*.

Press *Ctrl+L* to restore the default configuration.

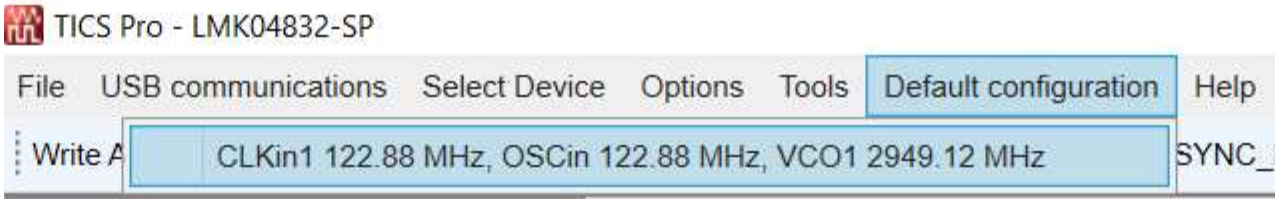

Figure 6. Setting the Default Configuration for LMK04832-SP

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when TICS Pro is closed, it remembers the last settings used for a particular device. Again, remember to press *Ctrl+L* as the first step after loading a default mode.

5.5 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded LED D3 and D4 must illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes PLL1_LD_MUX = *PLL1_DLD*, PLL2_LD_MUX = *PLL2_DLD*, and PLLX_LD_TYPE = Output (Push-Pull).

5.6 Enable Clock Outputs

The LMK04832-SP offers programmable clock output buffer formats, the evaluation board is shipped with pre-configured output terminations. Refer to Table 5 to see a list of the outputs what the output format the hardware is configured for out of the factory.

To measure Phase noise at one of the clock outputs, for example CLKout0:

1. Click on the **Clock Outputs** page, Section A.9
2. Uncheck *CLKoutX_Y_PD* in the Clock Output box to enable the channel,
3. Set the following as needed:

a. For Device Clock:
   - DCLKX_Y_PD = 0 in Clock Mode Select box.
   - Set Bypass Div (DCLKX_Y_BYP) or Clock Divider (DCLK0_1_DIV) as desired for device clock frequency.
     – If bypass mode is set, CLKoutX must be set to a CML output format. Bypass mode is not available on CLKoutY.
     – If Clock Divider = 1, then DCLKX_Y_DCC must be set for clock output.
   - Phase of the device clock can be adjusted with:
     – Static Digital delay (DCLKX_Y_DDLY) after a SYNC. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up.
     – Dynamic Digital delay (DDLYdX_EN), then programming DDLYd_STEP_CNT. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up. Press the *Send* button at top right of Clock Outputs window to program the DDLYd_STEP_CNT field multiple times.
     – Half Step bit (DCLKX_Y_HS) if DCC & HS (DCLKX_Y_DCC) is set.
     – The Polarity bit (DCLKX_Y_POL)
   - Select the Device Clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 0 (Device Clock) as desired.

b. While the phase noise of a SYSREF Clock is typically not of concern, to configure an output for SYSREF:
   - SCLKX_Y_PD = 0 in Clock Mode Select box.
   - Phase of the SYSREF clock can be adjusted.
     – Local digital delay can be set with SCLKX_Y_DDLY.
     – Local analog delay can be set by enabling with ADLY_EN = 1 (SCLKX_Y_ADLY_EN) and then setting SCLKX_Y_ADLY to the desired time delay.
     – Global digital delay can be set with SYSREF_DDLY, but this delay change will take effect only after a SYNC.
   - Globally SYSREF output must be enabled. The necessary bits depend upon the type of SYSREF to be enabled. For a simple continuous SYSREF (not recommended in final application due to extra power consumption and crosstalk), set SYSREF_PD = 0, SYSREF_MUX = 0x03 (Continuous), and SYNC_DISSYSREF = 1.
   - Select the SYSREF clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 1 (SYSREF) as desired.

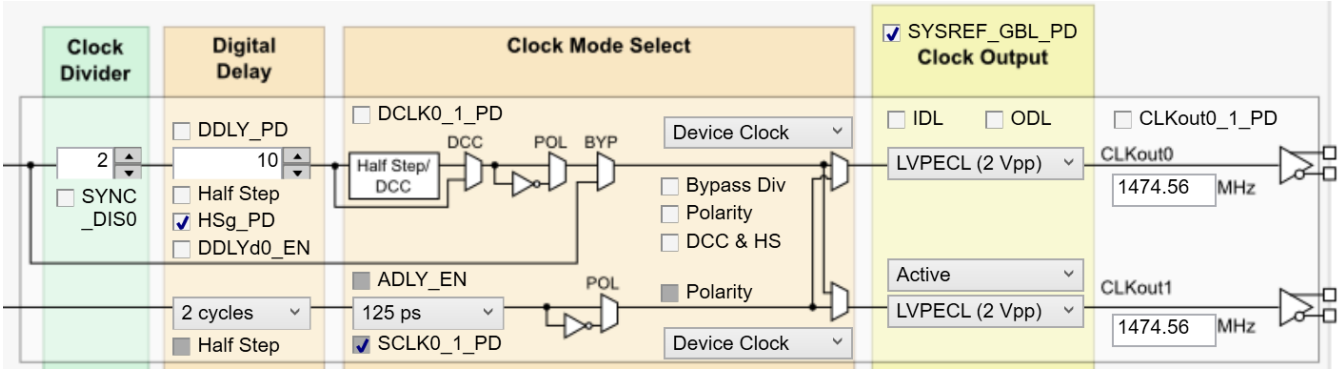

Figure 7. Setting Digital Delay, Clock Divider, Analog Delay, and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended, 50-Ω input as follows.
   a. For LVDS:
      i. A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.

b. For LVPECL:
   I. A balun can be used, or
   II. One side of the LVPECL signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
c. For HSDS:
   I. A balun (like ADT2-1T or high-quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
d. For CML:
   I. A balun can be used, or
   II. One side of the CML signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
e. For LVCMOS:
   I. Connect the LVCMOS signal to measurement equipment as desired. If an output of a pair is not used, TI recommends leaving the output floating close to the IC. Alternatively, place a 50-Ω termination at the end of an unused trace.

5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

6 Evaluation Board Inputs and Outputs

Table 5 contains descriptions of the inputs and outputs for the evaluation board. Additionally, some applicable TICS Pro programming controls are noted for convenience.

Table 5. Description of Evaluation Board Inputs and Outputs

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION	
Clock Outputs CLKout0_P(J29), CLKout0_N(J30), CLKout1_P(J16), CLKout1_N(J15), CLKout2_P(J31), CLKout2_N(J34), CLKout3_P(J20), CLKout3_N(J17), CLKout4_P(J32), CLKout4_N(J35), CLKout5_P(J21), CLKout5_N(J18), CLKout6_P(J33), CLKout6_N(J36), CLKout7_P(J22), CLKout7_N(J19), CLKout8_P(J37), CLKout8_N(J40), CLKout9_P(J26), CLKout9_N(J23),CLKout10_P(J38), CLKout10_N(J41), CLKout11_P(J27), CLKout11_N(J24), CLKout12_P(J39), CLKout12_N(J42), CLKout13_P(J28), CLKout13_N(J25)	Analog, Output	Clock outputs with programmable output buffers.	
		The output terminations by default on the evaluation board are shown here:	
		Clock Output Pair	**Default Board Termination**
		CLKout0	LVPECL / LCPECL, 240 Ω
		CLKout1	LVPECL / LCPECL, 240 Ω
		CLKout2	LVPECL / LCPECL, 120 Ω
		CLKout3	LVPECL / LCPECL, 120 Ω
		CLKout4	CML, 68 nH - 20 Ω
		CLKout5	CML, 50 Ω
		CLKout6	CML, 68 nH - 20 Ω
		CLKout7	CML, 50 Ω
		CLKout8	CML, 50 Ω
		CLKout9	LVDS / HSDS
		CLKout10	CML, 13 nH - 20 Ω
		CLKout11	LVDS / HSDS
		CLKout12	LVPECL / LCPECL, 180 Ω
		CLKout13	LVPECL / LCPECL, 180 Ω
		Each CLKout pair has a programmable LVDS, LVPECL, LCPECL, HSDS, CML, or LVCMOS buffer. The output buffer type can be selected in TICS Pro in the **Clock Outputs** page Section A.9 through the CLKoutX_FMT control. All clock outputs are AC-coupled to allow safe testing with RF test equipment. If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is not recommended to use Norm/Norm or Inv/Inv mode.	

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION
OSCout OSCout_P(J11) OSCout_N(J12)	Analog, Output	Buffered outputs of OSCin port. The output terminations on the evaluation board are shown here.: **OSC Output Pair** / **Default Board Termination** OSCout / LVPECL, 240 Ω OSCout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout buffer type can be selected in TICS Pro on the **Clock Outputs** page Section A.9 through the OSCout_FMT control. Note that OSCout is DC-coupled by default. In case RF test equipment cannot handle the OSCout voltage, please AC-couple OSCout by replacing C59 and C60 with capacitors. If OSCout is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is NOT recommended to use Norm/Norm or Inv/Inv mode.
Power VccEXT(J1/J2/TP3) Vcc(TP1)	Power, Input	Main power supply input for the evaluation board. The LMK04832EVM-CVAL default is setup to use the TPS7A4501HKU/EM voltage regulator. This is a space grade voltage regulator. 0-ohm resistors R3, R5, R6, R14 and R15 can be re-configured to route power through the on-board commercial grade LDO, the TPS7A4533KTTR. The LMK04832-SP contains internal voltage regulators for the VCO and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance. If using an external voltage please ensure the voltage is filtered to get the best performance on the outputs. Apply power to either Vcc SMA(J1) or terminal block(J2), but not both.
Clock Inputs CLKin0_P(J5), CLKin0_N(J6), CLKin1_P(J8), CLKin1_N(J10) OSCout_P(J11), OSCout_N(J12) Fin0_P(J3),Fin0_N(J4)	Analog, Input	**Reference Clock Inputs for PLL1 or PLL1 (CLKin0, CLKin1, CLKin2)** CLKin1_N is configured by default for a single-ended reference clock input from a 50-ohm source. The non-driven input pin CLKin1_P is connected to GND with a 0.1 uF. CLKin0 is configured by default for a differential reference clock input from a 50-ohm source. CLKin1 is the default reference clock input selected in TICS Pro. If OSCout is to be used as a CLKin2, then the PCB must be updated to operate as an input instead of an output. **Clock Distribution with Fin0 or CLKin1/Fin1** Fin0 and CLKin1 (Fin1) are shared for use as an RF Input for Clock Distribution mode or for an external VCO mode. **External Feedback Input (FBCLKin) for 0-Delay** CLKin1 is shared for use as an external feedback clock input (FBCLKin) to PLL1 N or PLL2 N for 0-delay mode. Refer to the LMK04832-SP (SNAS698) data sheet for more details on using 0-delay mode with the evaluation board and the evaluation board software.
OSCin, PLL2 reference/PLL1 feedback OSCin_P(J13), OSCin_N(J14)	Analog, Input	Feedback VCXO clock input to PLL1 and Reference clock input to PLL2. The single-ended output of the onboard VCXO (Y1/Y2) drives the OSCin_N input of the device and the OSCin_P input of the device is connected to GND with 0.1 uF. VCXO Y1 and Y2 may also be used with differential VCXOs. An external VCXO may be optionally attached through these SMA connectors with minor modification to the components going to the OSCin pins of device. A single-ended or differential signal may be used to drive the OSCin pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF. Refer to the LMK04832-SP (SNAS698) data sheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications (SNAS698).
VCO Tuning Voltages VTUNE1 (TP7/J7) VTUNE (TP8/J9)	Analog, Input/Output	Tuning voltage output from the loop filter for PLL1 and PLL2 of the LMK04832-SP. If an external VCXO is used, this tuning voltage can be connected to the voltage control pin of the external VCXO. The default board does not come with J7 and J9 populated.

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION
SPI Header USB2ANY (J43) SDIO (TP17),SCK (TP14),CS* (TP19) CLKin_SEL0(TP10),CLKin_SEL1(TP11) RESET(TP13)	CMOS, Input/Output	10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04832-SP. SPI signals include SDIO (TP17), SCK (TP14) and CS* (TP19). The programmable logic I/O signals accessible through this header include: RESET (TP13), SYNC (TP20/J44), CLKin_SEL0 (TP10), and CLKin_SEL1 (TP11).
		Input Clock Switching – Pin Select Mode By default CLKin_SEL0 and CLKin_SEL1 are input pins. To enable input clock switching, CLKin_SEL_AUTO_EN = 0, CLKin_SEL_PIN_EN = 1, CLKin_SEL_PIN_POL = 0, and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input). When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the Status_CLKinX pins select which clock input is active as follows:
		CLKin_SEL1 / **CLKin_SEL0** / **Active Clock** 0 / 0 / CLKin0 0 / 1 / CLKin1 1 / 0 / CLKin2 1 / 1 / Holdover
SYNC SYNC (TP20/J44)	CMOS, Input/Output	Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect. SYNC/SYSREF_REQ pin forces the SYSREF_MUX into SYSREF Continuous mode (0x03) when SYSREF_REQ_EN = 1. SYNC/SYSREF_REQ pin can hold outputs in a low state, depending on system configuration. SYNC_POL adjusts for active low or active high control. A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the **SYNC/SYSREF** page Section A.8 in TICS Pro.
Status LEDs Status_LD1(TP18),Status_LD2(TP21)	CMOS, Input/Output	Programmable status output pin. By default, Status_LD1 and Status_LD2 are set to output the digital lock detect status signal for PLL1 and the digital lock detect status signal for PLL2 respectively. By default TICS Pro configuration, LEDs will illuminate green when lock is detected (output is high) and turned off when lock is lost (output is low).

7 Recommended Test Equipment

Power Supply

The Power Supply must be a low-noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

TI recommends that an Agilent E5052 Signal Source Analyzer or comparable test equipment is used to measure phase noise and RMS jitter.

Oscilloscope

To measure the output clocks AC performance, such as rise time or fall time, propagation delay, or skew, TI suggests using a real-time oscilloscope with 8+ GHz analog input bandwidth with 50-Ω inputs. To evaluate clock synchronization or phase alignment between multiple clock outputs, TI recommends using phase-matched, 50-Ω cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

8 Length Matching

Specific traces on the LMK04832EVM-CVAL were length matched to ensure device functions such as skew and 0-delay mode phase could be tested. Table 6 contains the lengths of each of the traces on the EVM.

Table 6. Differential Pair Lengths

Function	Net Names	Length (mil)
Skew	CLKout0_P, CLKout0_N, CLKout1_P, CLKout1_N	3977.5 ± 0.5
0-delay Mode Phase, Skew	CLKin1_P, CLKin1_N, OSCout_P, OSCout_N CLKout6_P, CLKout6_N, CLKout7_P, CLKout7_N, CLKout8_P, CLKout8_N SYNC	4539.5 ± 0.5
Skew	CLKout2_P, CLKout2_N, CLKout3_P, CLKout3_N, CLKout4_P, CLKout4_N, CLKout5_P, CLKout5_N, CLKout9_P, CLKout9_N,CLKout10_P, CLKout10_N, CLKout11_P, CLKout11_N, CLKout12_P, CLKout12_N, CLKout13_P, CLKout13_N	4240.5 ± 0.5

9 Schematics

The components on the EVM, can be found on the following schematic by searching for their reference designators.

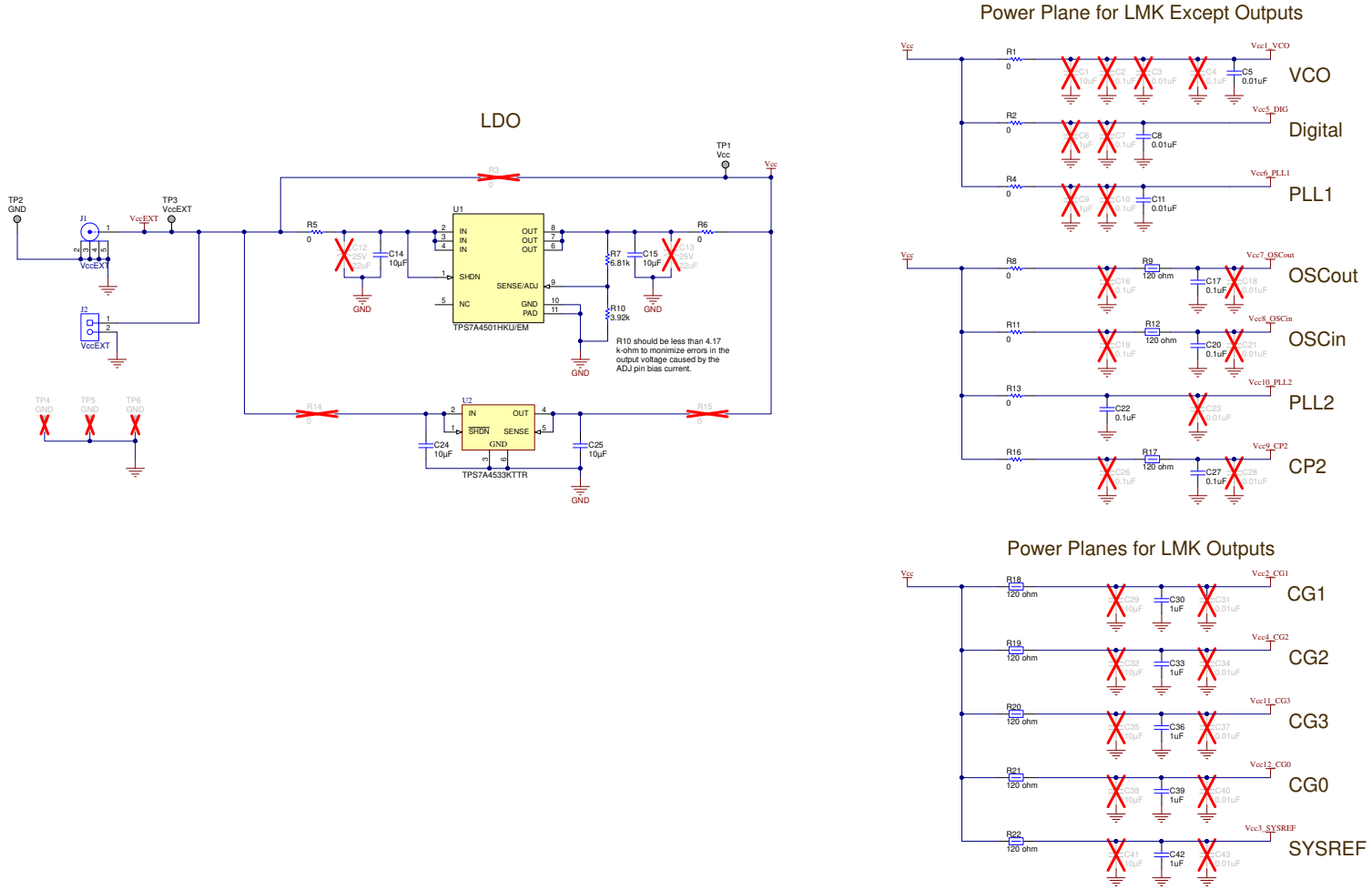

Figure 8. Schematic - Power Supply

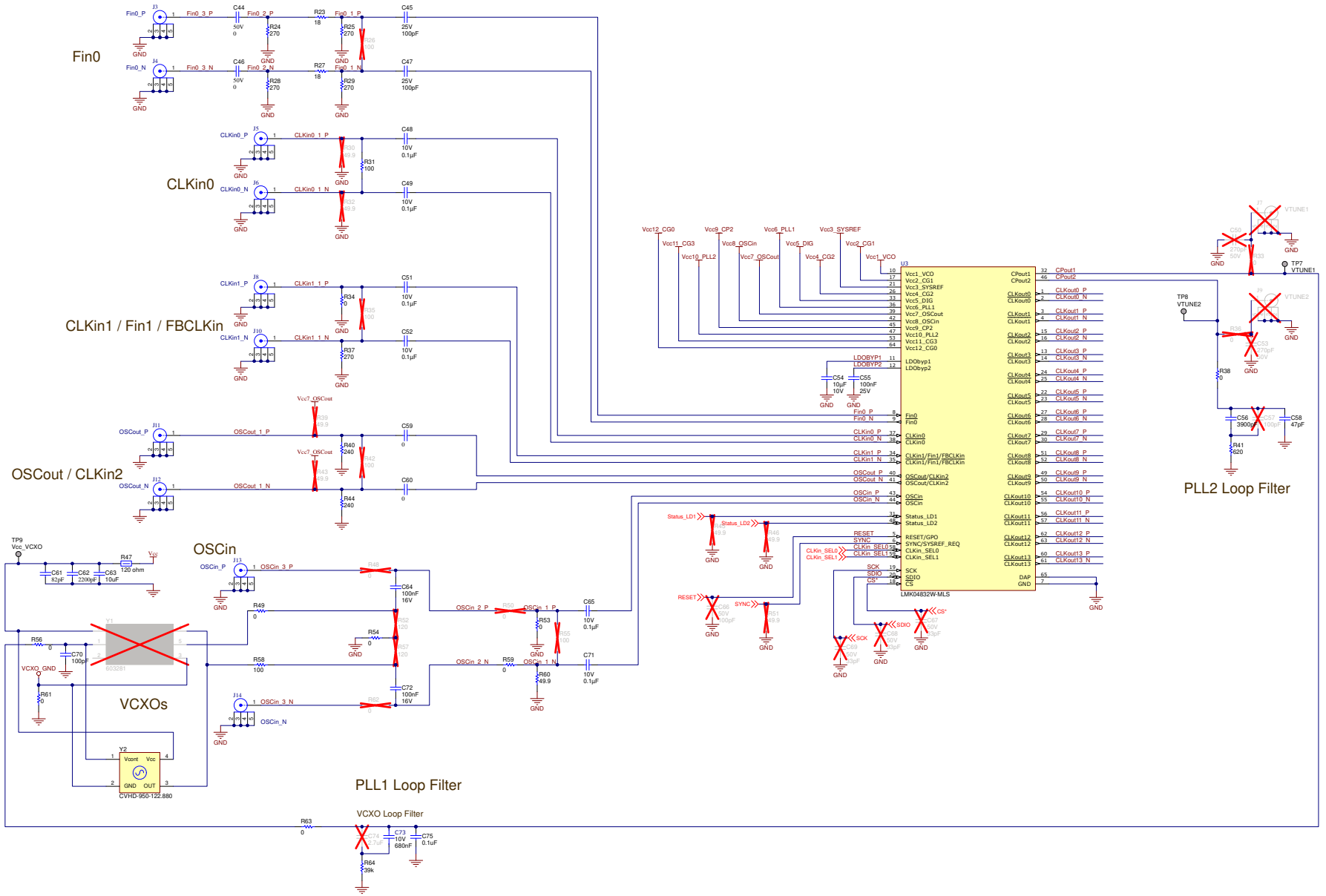

Figure 9. Schematic - LMK04832-SP

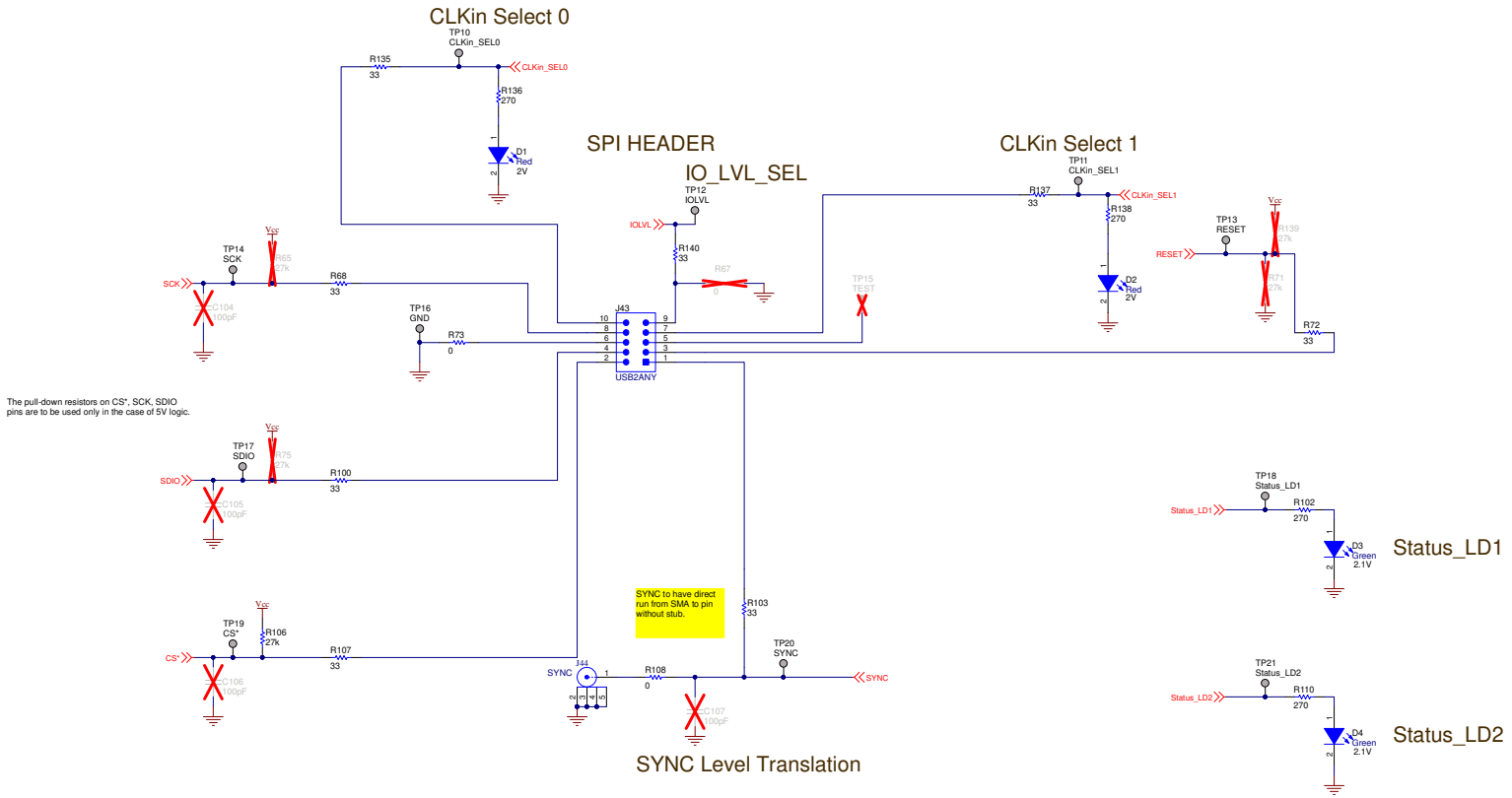

Figure 10. Schematic - Digital

EVEN CLOCK OUTPUTS

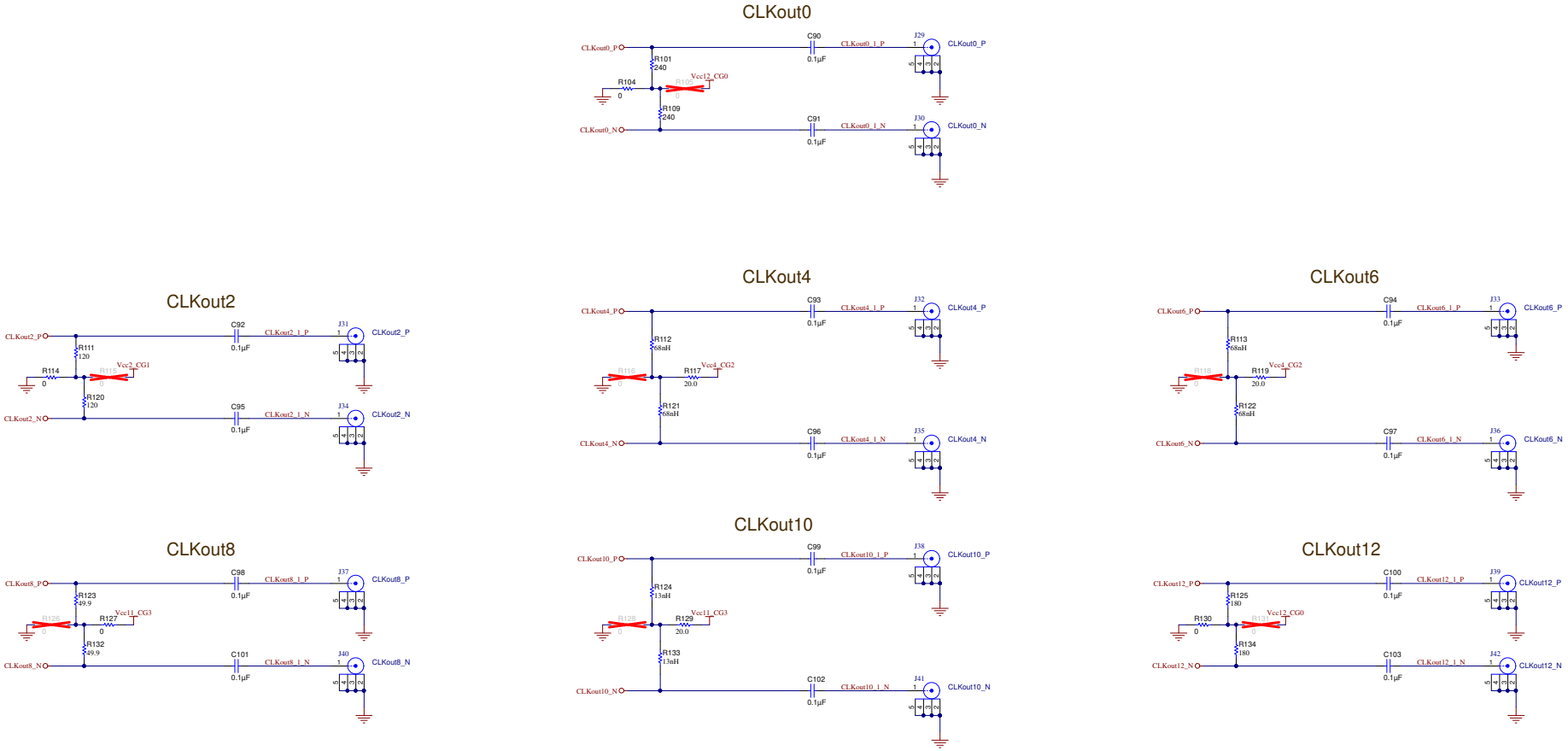

Figure 11. Schematic - Clock Outputs 1 of 2

ODD CLOCK OUTPUTS

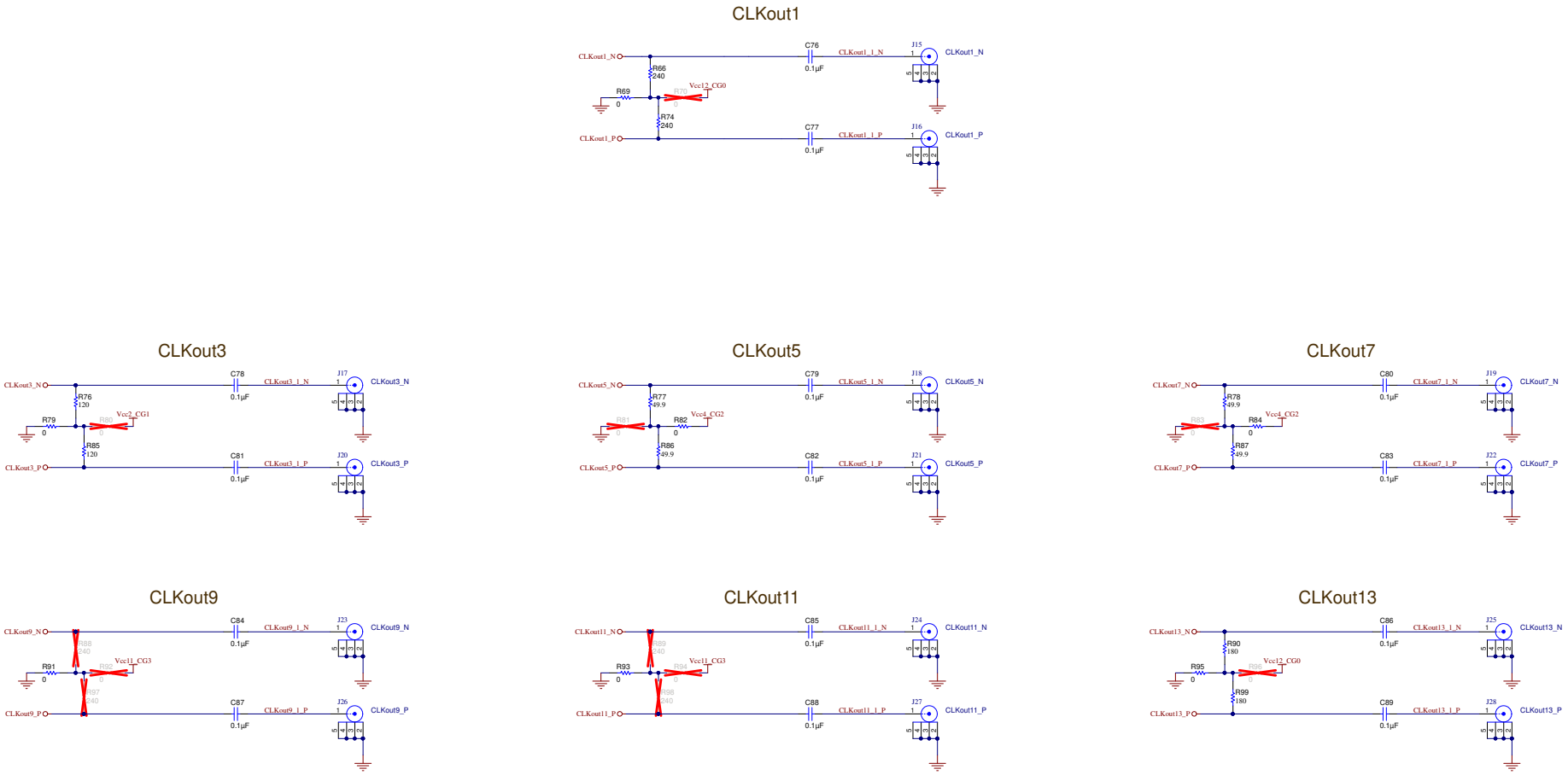

Figure 12. Schematic - Clock Outputs 2 of 2

10 Bill of Materials

Table 7. Bill of Materials

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
1	PCB	Printed Circuit Board	Any	HSDC005	1
2	C5, C8, C11	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GCM155R71E103KA37D	3
3	C14, C15, C24, C25	CAP, CERM, 10 µF, 6.3 V,+/- 20%, X7R, 0603	Samsung Electro-Mechanics	CL10B106MQ8NRNC	4
4	C17, C20, C22, C27	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E104KE14D	4
5	C30, C33, C36, C39, C42	CAP, CERM, 1 uF, 10 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0402	MuRata	GCM155C71A105KE38D	5
6	C44, C46, C59, C60, R34, R53, R59, R69, R79, R82, R84, R91, R93, R95, R104, R114, R127, R130, R108	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	19
7	C45, C47	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0402	Kemet	C0402C101J3GACTU	2
8	C48, C49, C51, C52, C65, C71, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X7R, 0402	Kemet	C0402C104K8RACTU	34
9	C54, C63	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	MuRata	GCM21BR71A106KE22L	2
10	C55, C75	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	Kemet	C0603C104J3RACTU	2
11	C56	CAP, CERM, 3900 pF, 100 V,+/- 5%, X7R, 0603	AVX	06031C392JAT2A	1
12	C58	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C470J5GACTU	1
13	C61	CAP, CERM, 82 pF, 50 V, +/- 10%, C0G/NP0, 0603	Kemet	C0603C820K5GACTU	1
14	C62	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603C222K5RACTU	1
15	C64, C72	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C104K4RACTU	2

Table 7. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
16	C70	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	1
17	C73	0.68µF ±10% 10V Ceramic Capacitor X7R 0603 (1608 Metric)	Yageo	CC0603KRX7R6BB684	1
18	D1, D2	LED, Red, SMD	Lumex	SML-LX2832IC-TR	2
19	D3, D4	LED, Green, SMD	Lumex	SML-LX2832GC-TR	2
20	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
21	H1, H2, H3, H4, H5, H6	HEX STANDOFF SPACER, 9.53 mm	Richco Plastics	TCBS-6-01	6
22	J1	Connector, SMA, TH	Cinch Connectivity	142-0701-201	1
23	J2	Terminal Block, 5.08mm, 2x1, TH	Molex	0395443002	1
24	J3, J4, J5, J6, J8, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J44	Connector, End launch SMA, 50 ohm, SMT	Cinch Connectivity	142-0701-851	39
25	J43	Header (shrouded), 100mil, 5x2, Gold, SMT	FCI	52601-S10-8LF	1
26	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
27	R1, R2, R4, R5, R6, R8, R11, R13, R16, R38, R49, R54, R56, R61, R63, R73	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	16
28	R7	RES, 6.81 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06036K81FKEA	1
29	R9, R12, R17, R18, R19, R20, R21, R22	Ferrite Bead, 120 ohm @ 100 MHz, 0.4 A, 0402	TDK	MMZ1005Y121CT000	8
30	R10	RES, 3.92 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06033K92FKEA	1
31	R23, R27	RES, 18, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040218R0JNED	2
32	R24, R25, R28, R29, R37	RES, 270, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402270RJNED	5
33	R31	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100RFKED	1

Table 7. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
34	R40, R44, R66, R74, R101, R109	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402240RJNED	6
35	R41	RES, 620, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603620RJNEA	1
36	R47	Ferrite Bead, 120 ohm @ 100 MHz, 0.5 A, 0603	MuRata	BLM18AG121SN1D	1
37	R58	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RJNEA	1
38	R60, R77, R78, R86, R87, R123, R132	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040249R9FKED	7
39	R64	RES, 39 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060339K0JNEA	1
40	R76, R85, R111, R120	RES, 120, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402120RJNED	4
41	R90, R99, R125, R134	RES, 180, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402180RJNED	4
42	R112, R113, R121, R122	Inductor, Multilayer, Air Core, 68 nH, 0.16 A, 2 ohm, AEC-Q200 Grade 1, SMD	MuRata	LQG15WZ68NJ02D	4
43	R117, R119, R129	RES, 20.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040220R0FKED	3
44	R124, R133	Inductor, Multilayer, Air Core, 13 nH, 0.4 A, 0.26 ohm, AEC-Q200 Grade 1, SMD	MuRata	LQG15WZ13NH02D	2
45	R135, R137, R140, R68, R72, R100, R103, R107	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333R0JNEA	8
46	R136, R138, R102, R110	RES, 270, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603270RJNEA	4
47	R106	RES, 27 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060327K0JNEA	1
48	TP1, TP2, TP3, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP16, TP17, TP18, TP19, TP20, TP21	Test Point, Miniature, SMT	Keystone	5019	17
49	U1	Wide Vin Low-Dropout Voltage Regulator, HKU0010A (CFP-10)	Texas Instruments	TPS7A4501HKU/EM	1

Table 7. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
50	U2	Single Output Fast Transient Response LDO, 1.5 A, Fixed 3.3 V Output, 2.1 to 20 V Input, 5-pin DDPAK (KTT), -40 to 125 degC, Green (RoHS and no Sb/Br)	Texas Instruments	TPS7A4533KTTR	1
51	U3	Space Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner	Texas Instruments	LMK04832W/EM	1
52	Y2	VCXO, CMOS 122.880 MHz, 3.3V, SMD	Crystek Corporation	CVHD-950-122.880	1
53	C1	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0603	Kemet	C0603C106M9PACTU	0
54	C2, C4, C7, C10, C16, C19, C26	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E104KE14D	0
55	C3, C18, C21, C23, C28, C31, C34, C37, C40, C43	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GCM155R71E103KA37D	0
56	C6, C9	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1C105K080AC	0
57	C12, C13	CAP, TA, 22 uF, 25 V, +/- 10%, 0.2 ohm, SMD	Kemet	T495D226K025ATE200	0
58	C29, C32, C35, C38, C41	CAP, CERM, 10 µF, 6.3 V,+/- 20%, X7R, 0603	Samsung Electro-Mechanics	CL10B106MQ8NRNC	0
59	C50, C53	CAP, CERM, 270 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603C271K5RACTU	0
60	C57, C66, C104, C105, C106	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	0
61	C67, C68, C69	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C330J5GACTU	0
62	C74	CAP, CERM, 2.7 uF, 10 V, +/- 10%, X5R, 0805	Kemet	C0805C275K8PACTU	0
63	C107	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0402	Kemet	C0402C101J3GACTU	0
64	J7, J9	Connector, SMA, TH	Cinch Connectivity	142-0701-201	0
65	R3, R14, R15, R33, R36, R48, R62, R67	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	0
66	R26, R35, R42, R55	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100RFKED	0

Table 7. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
67	R30, R32, R39, R43, R45, R46, R51	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040249R9FKED	0
68	R50, R70, R80, R81, R83, R92, R94, R96, R105, R115, R116, R118, R126, R128, R131	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	0
69	R52, R57	RES, 120, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603120RJNEA	0
70	R88, R89, R97, R98	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402240RJNED	0
71	R139, R65, R71, R75	RES, 27 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060327K0JNEA	0
72	TP4, TP5, TP6, TP15	Test Point, Miniature, SMT	Keystone	5019	0
73	Y1	Ultra-Low Noise LVPECL VCXO with 162dBc/Hz NOISE Floor, SMD	Crystek Corporation	603281	0

TICS Pro Usage

TICS Pro is used to program the evaluation board with the USB2ANY interface adapter. TICS Pro can also be used to generate register maps for programming the device and current consumption estimates. This appendix outlines the basic purpose and usage of each page. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

A.1 Communication Setup

The **Communication Setup** window allows the USB2ANY or DemoMode to be selected. In case multiple evaluation boards are to be connected and run with multiple instances of TICS Pro, the drop-down box will allow specific USB2ANY devices to be selected. Pressing the *Identify* button will identify which USB2ANY is currently selected. Devices used by other instances of TICS Pro will not display in this list.

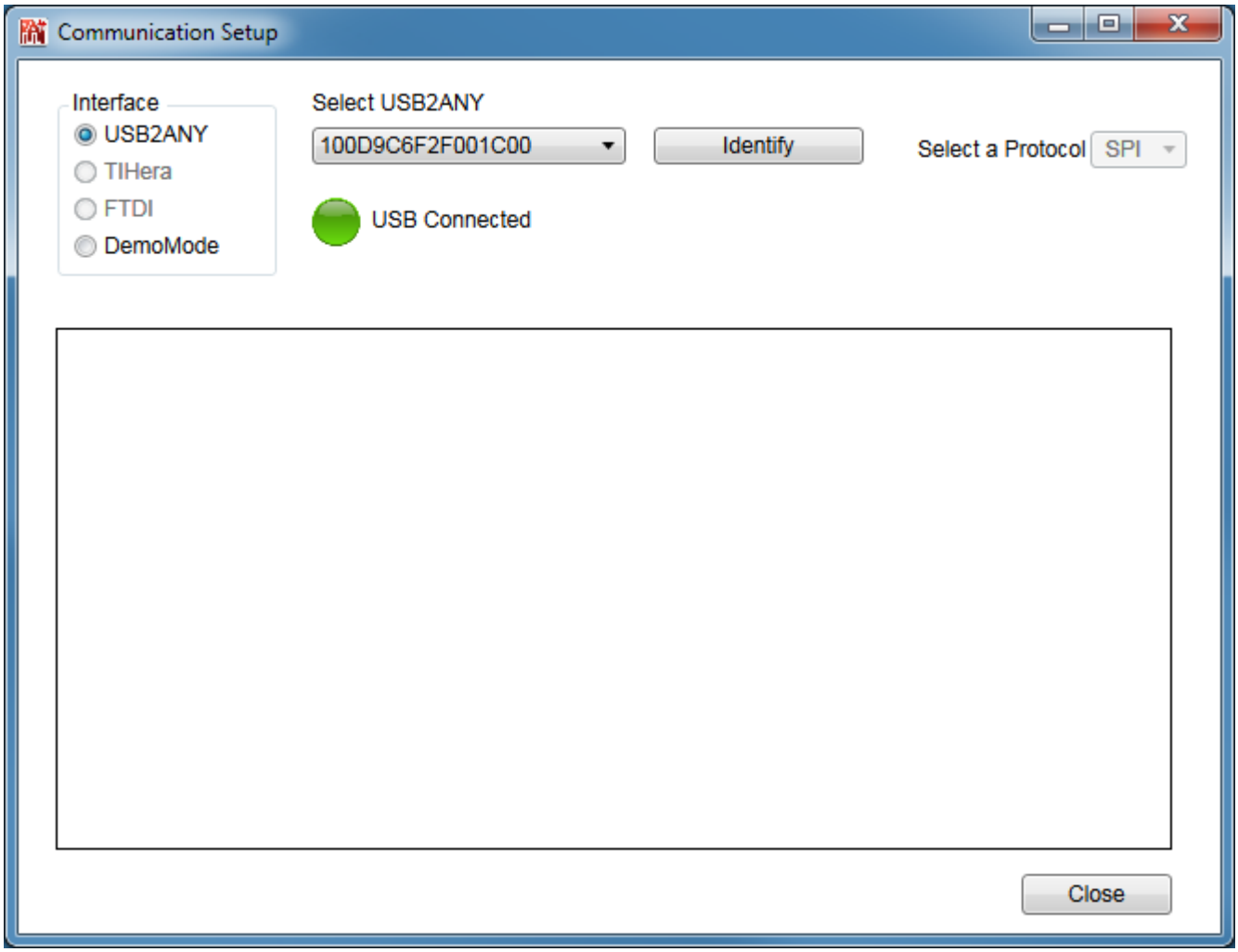

Figure 13. TICS Pro - Communication Setup Window

A.2 User Controls

The **User Controls** page has controls typically not included on one of the other dedicated pages.

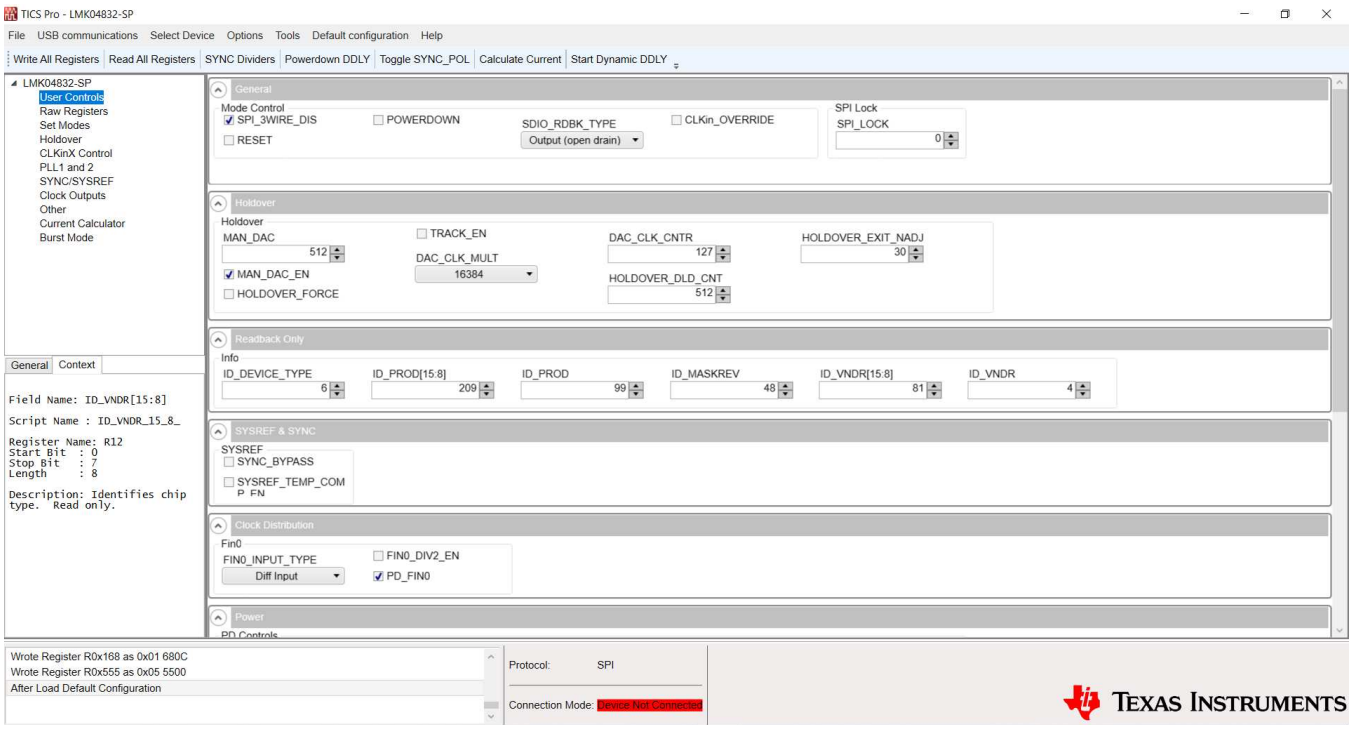

Figure 14. TICS Pro - User Controls Page

A.3 Raw Registers Page

The **Raw Register** page displays the register map including address. The address bits have the shaded background and are not editable. The unshaded bits are the data bits. This register map may be directly manipulated by clicking into the bit field, moving around with the arrow keys, and typing 1 or 0 to change a bit.

All registers may be read or written in addition to individual registers. For individual register read or write, the active register is highlighted in the list of registers and displayed in the top right. An individual register or field may be read back by entering the name into the bottom right and clicking the *Read* button.

Register maps may be exported, but also imported. The import format may simply be the address and register data in hex format as illustrated in the address/value column, one register to a line.

NOTE: Use the Export Register Map to create a text file with the register values for simple re-use of the register configuration.

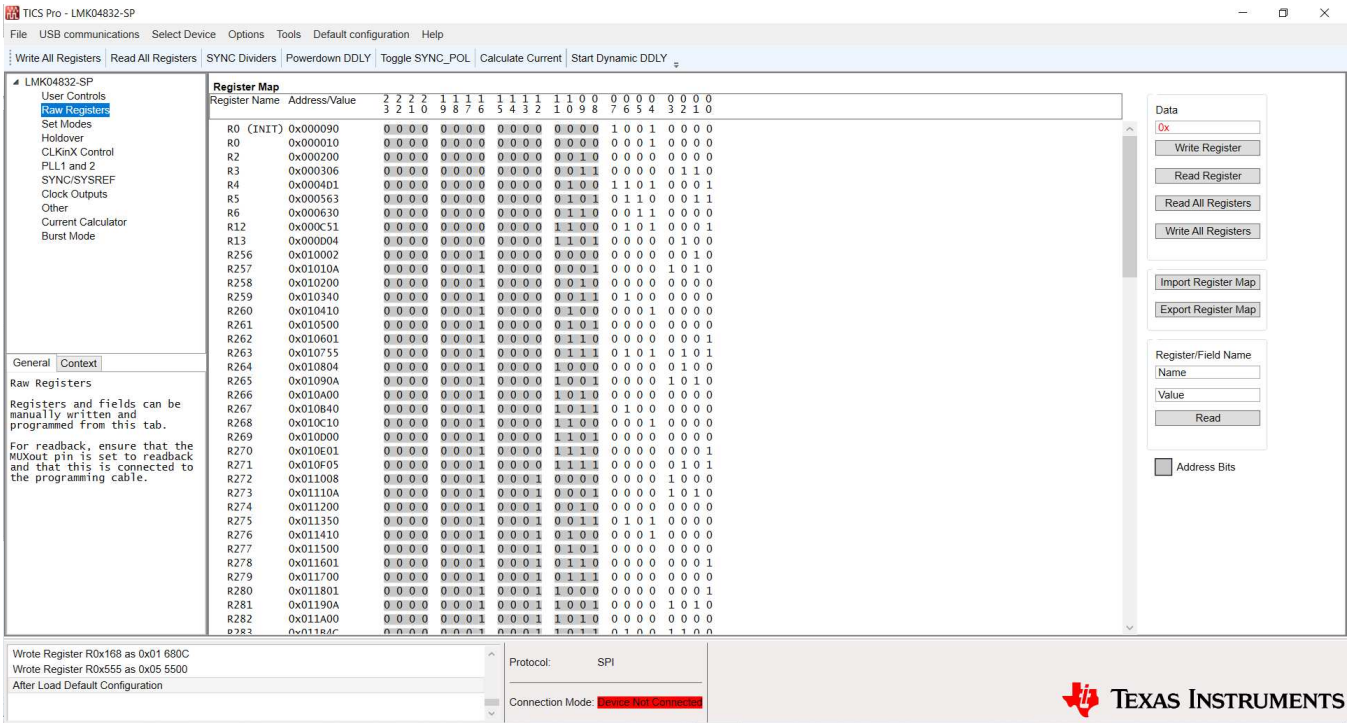

Figure 15. TICS Pro - Raw Registers Page

A.4 Set Modes Page

The **Set Modes** page allows the user to quickly configure the LMK04832-SP into a desired mode. If the LMK04832-SP is already in the desired mode, or several registers are already programmed as needed, the log will not display any or many register writes.

The top LMK04832-SP modes section allows the user to set high level usage profiles to allow the device to operate in dual loop, single loop, or distribution mode.

The bottom LMK04832-SP sub-modes section allows further JESD204B configuration, 0-delay configuration, or clock input configuration which may apply for many of the LMK04832-SP modes of operation.

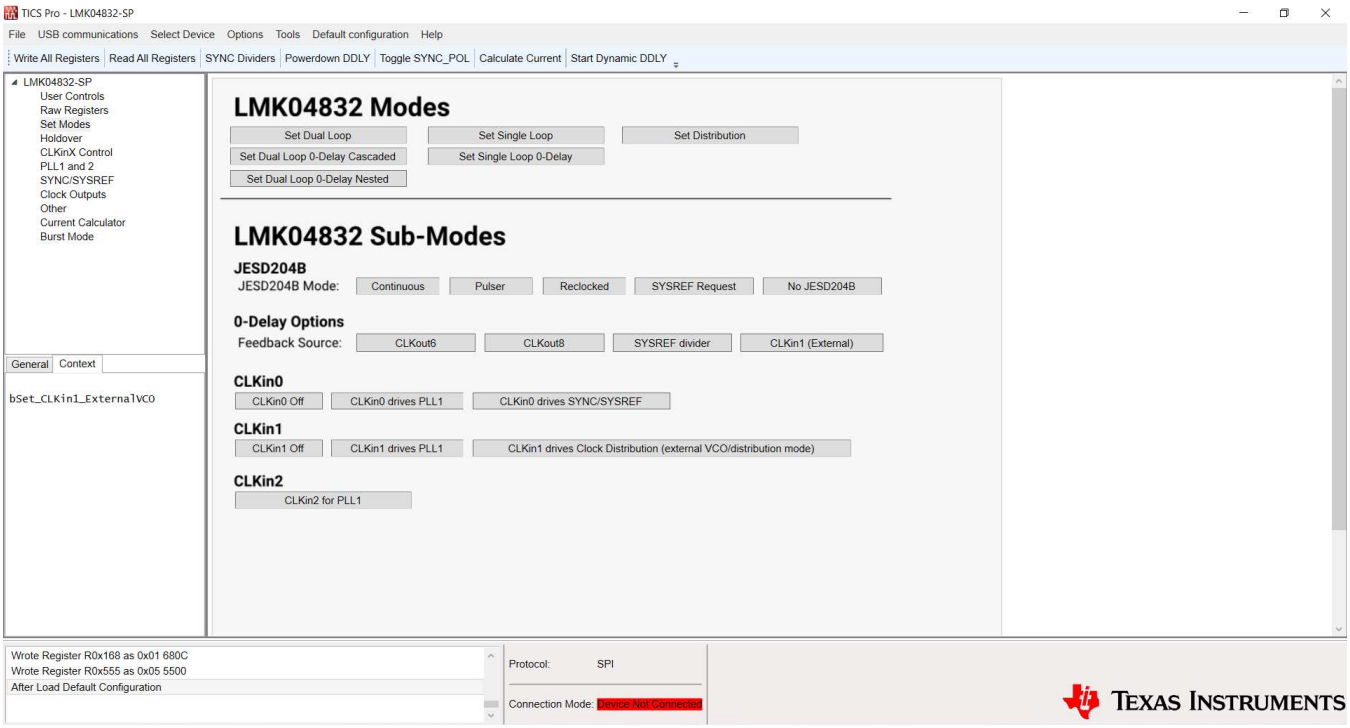

Figure 16. TICS Pro - Set Modes Page

A.5 Holdover Page

The **Holdover** page contains many registers pertaining to how the device will enter and exit holdover. To enable holdover and LOS detect for entry and exit of holdover:

- Set HOLDOVER_EN = 1 (checked).
- Set HOLDOVER_EXIT_MODE combo box to 0x00 (Exit based on LOS).
- Set LOS_EN = 1 (checked).
- Set LOS_TIMEOUT combo box to the LOS frequency threshold as desired. For example, if 200 MHz is set as the frequency threshold, the input must be above approximately 200 MHz to lock, otherwise PLL1 will enter holdover. If holdover is not enabled, PLL1 will be prevented from locking if the input frequency is less than the threshold frequency and LOS is enabled.

In addition to the above steps, auto clock selection mode must be used to allow the LMK04832-SP to automatically switch to holdover when enabled clocks for auto switching (CLKinX_EN) are lost.

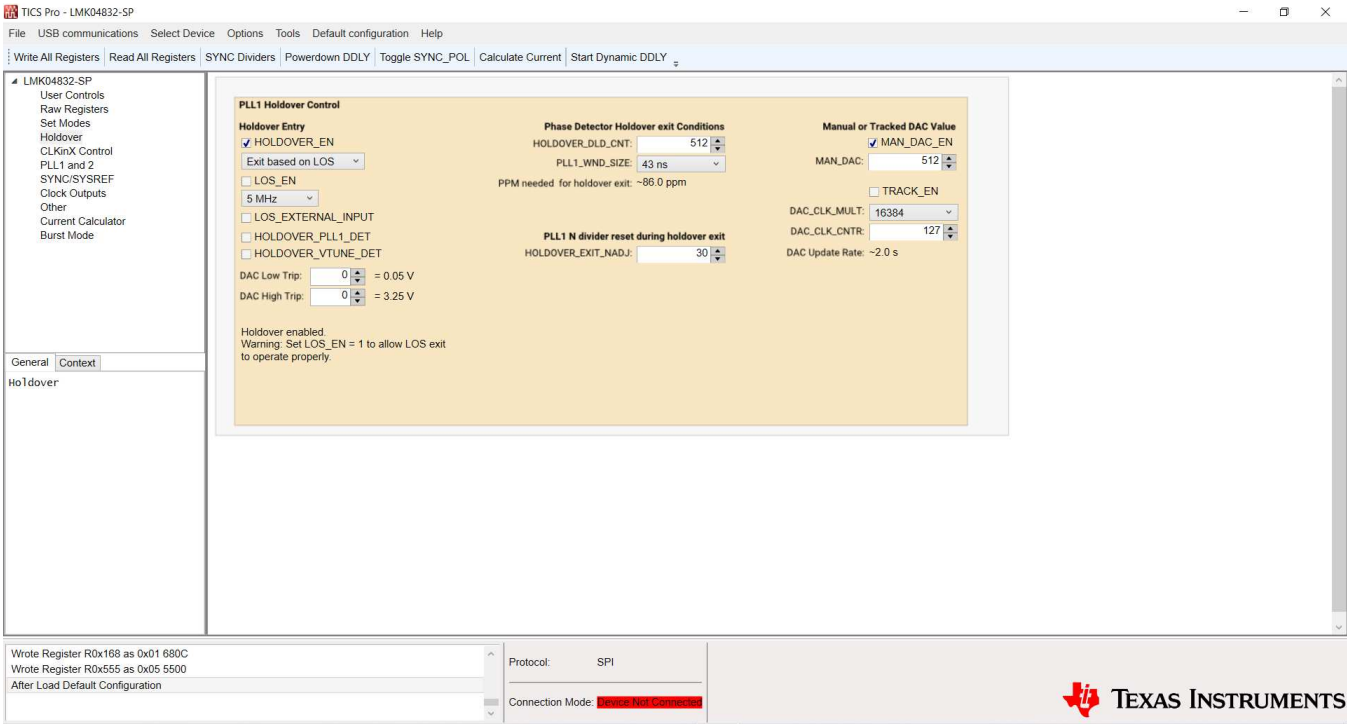

Figure 17. TICS Pro - Holdover Page

A.6 CLKinX Control Page

The **CLKinX Control** page allows entry of the input frequency at the different CLKinX pins, the mode by which the active CLKinX is selected, where the CLKinX inputs are routed to.

Also on this page are controls to reset the PLL1 R or PLL2 N divider.

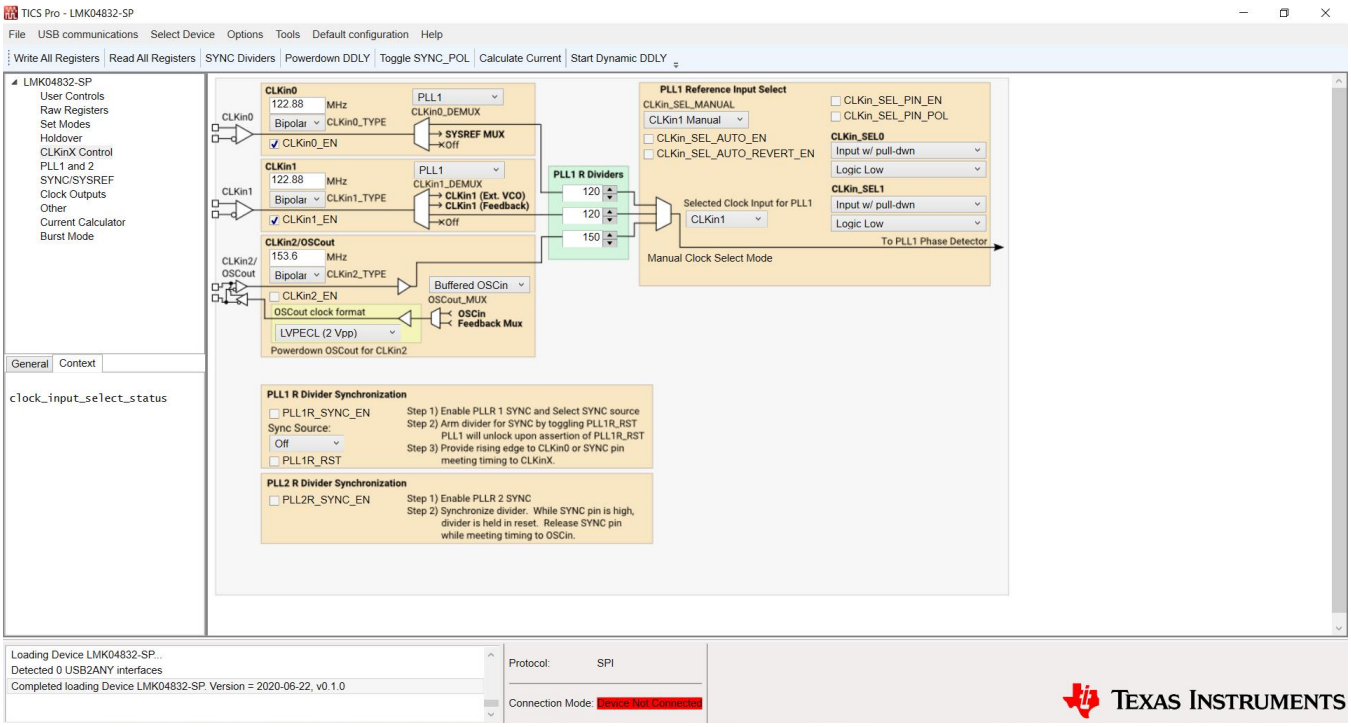

Figure 18. TICS Pro - CLKinX Control Page

A.7 PLL1 and 2 Page

The **PLL1 and PLL2** page shows the frequencies that the PLL1 and PLL2 operate at. In distribution mode, the CLKin1 frequency will directly be connected to the VCO/clock distribution path frequency. In addition to the basic PLL dividers and controls, when the PLLX_NCLK_MUX selects the feedback mux as a source, 0-delay modes are achieved. When enabling 0-delay red text will help guide the user through properly setting up 0-delay mode.

When using dual PLL mode, the OSCin Source combo box can be set to *External VCXO* which links the OSCin frequency with the external VCXO frequency. When using single PLL2 mode, the OSCin Source combo box can be set to *Independent* to allow the OSCin frequency to be unlinked from the external VCXO frequency.

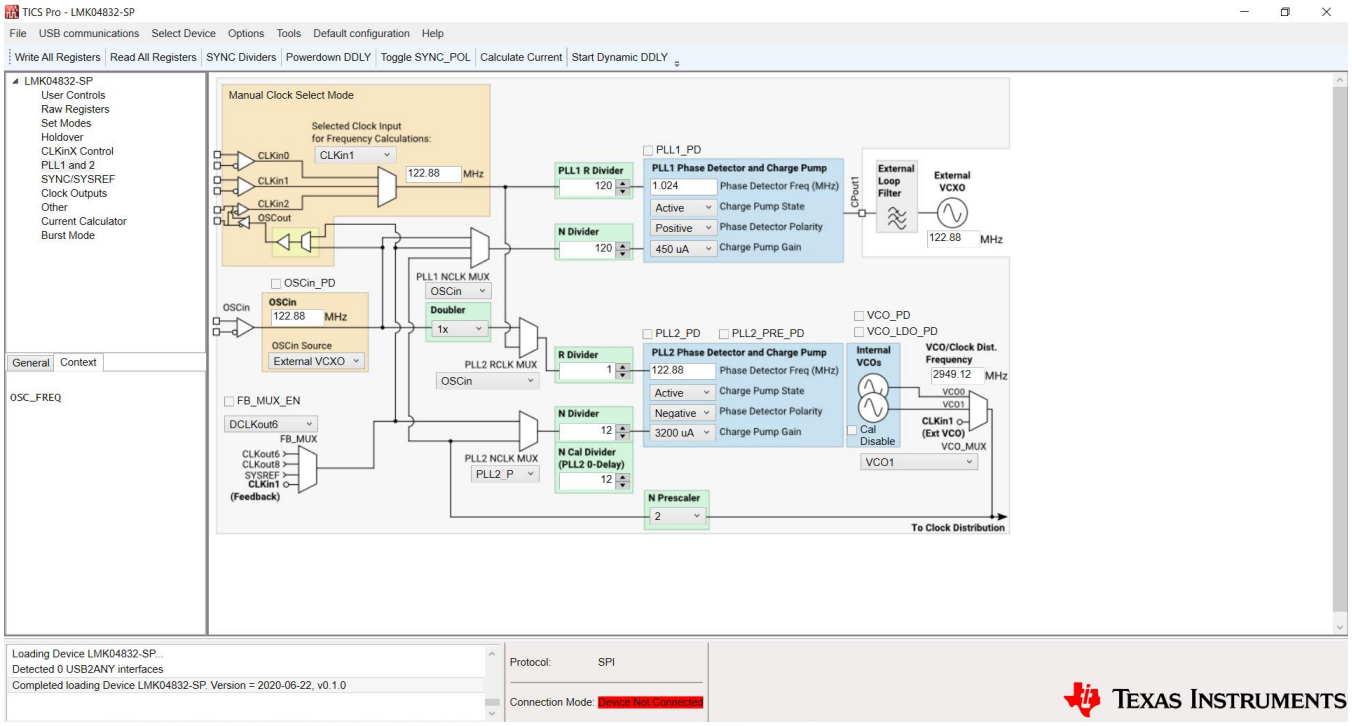

Figure 19. TICS Pro - PLL1 and 2 Page

A.8 SYNC / SYSREF Page

The **SYNC / SYSREF** page allows some mode set buttons for JESD204B features. The SYNC dividers button will stop all SYNC inputs, set normal SYNC mode, enable all dividers for SYNC, issue a SYNC by toggling SYNC_POL, set all dividers to ignore SYNC, then return any other changed parameter to its original state. This is a nice feature to ensure all outputs are synchronized together or to be run after changing the digital delay value which requires a SYNC to update. This functionality is also available on any other page through the toolbar as *SYNC Dividers*.

NOTE: To use SYNC or SYSREF, ensure that SYNC_EN = 1. To use SYSREF in continuous, pulser, or reclocked modes, be sure SYSREF_PD = 0.

The SCLKX_Y_DIS_MODE bits allow the clock outputs to be disabled or set to a low state. Because values 1 and 2 are only conditionally set by the SYSREF_GBL_PD bit, it is possible to power up or power down several SYSREF outputs by programming only one register. When changing between 0x00 (Active) and (0x01) Conditional Low, keeping the SYSREF_CLR = 1 during transition will prevent glitch pulses from the SYSREF output.

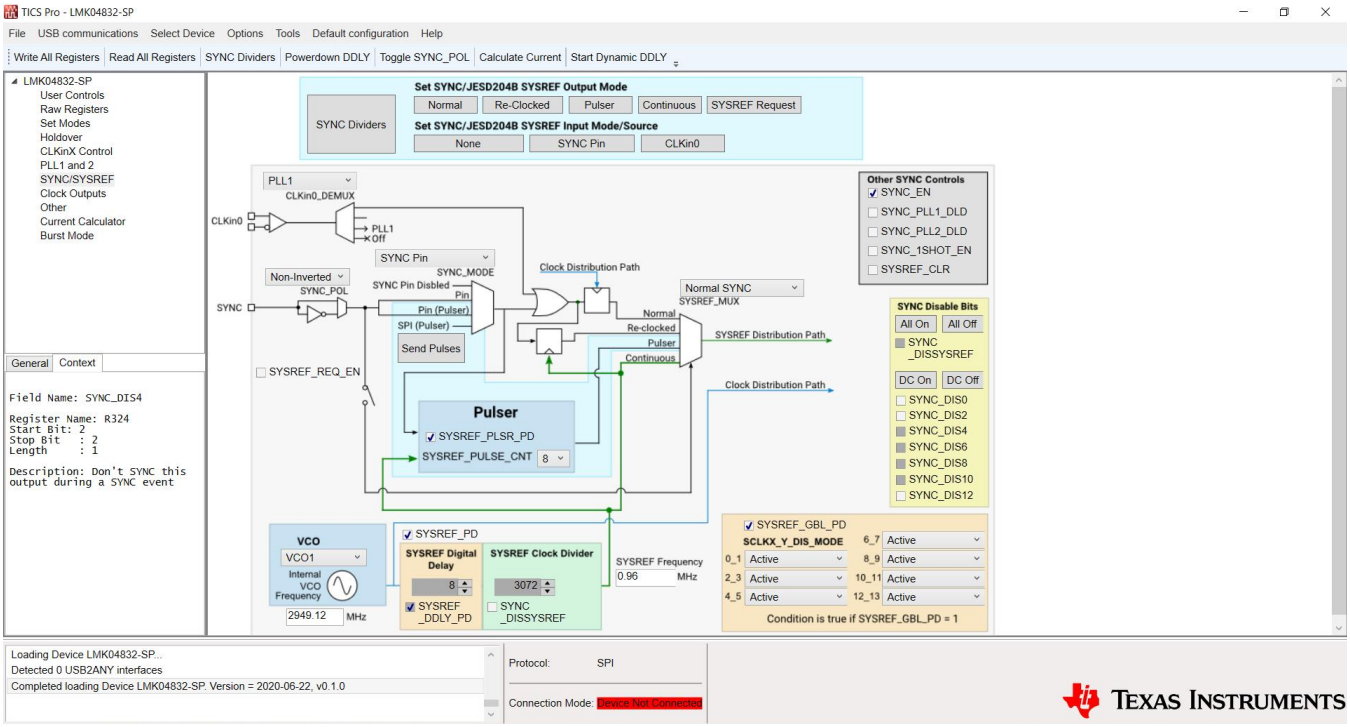

Figure 20. TICS Pro - SYNC / SYSREF Page

A.9 Clock Outputs Page

The **Clock Outputs** page allows control of all the clock outputs format and other options relating to the clock outputs. All the clock outputs are paired and allow two device clocks, two SYSREF clocks, or one of each. The naming convention uses X_Y for controls which can impact both CLKoutX (even clock) and CLKoutY (odd clock), X for controls impacting only CLKoutX and Y for controls impacting only CLKoutY.

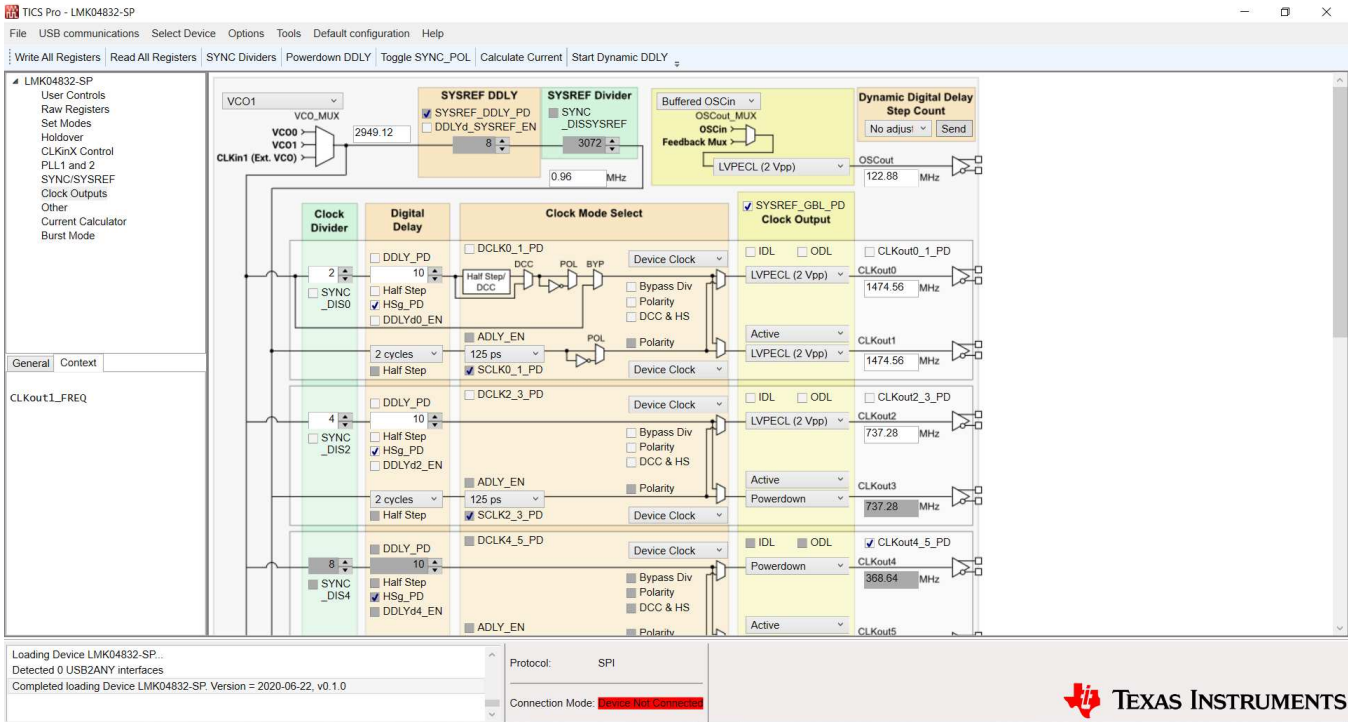

Figure 21. TICS Pro - Clock Outputs Page

A.10 Other Page

The **Other** page contains some registers to control the GPIO pins of the LMK04832-SP. Each pin has two fields, the first is the _TYPE field which allows the input or output mode of the pin to be defined. The second is the _MUX field which, when set for output, controls what the pin will output.

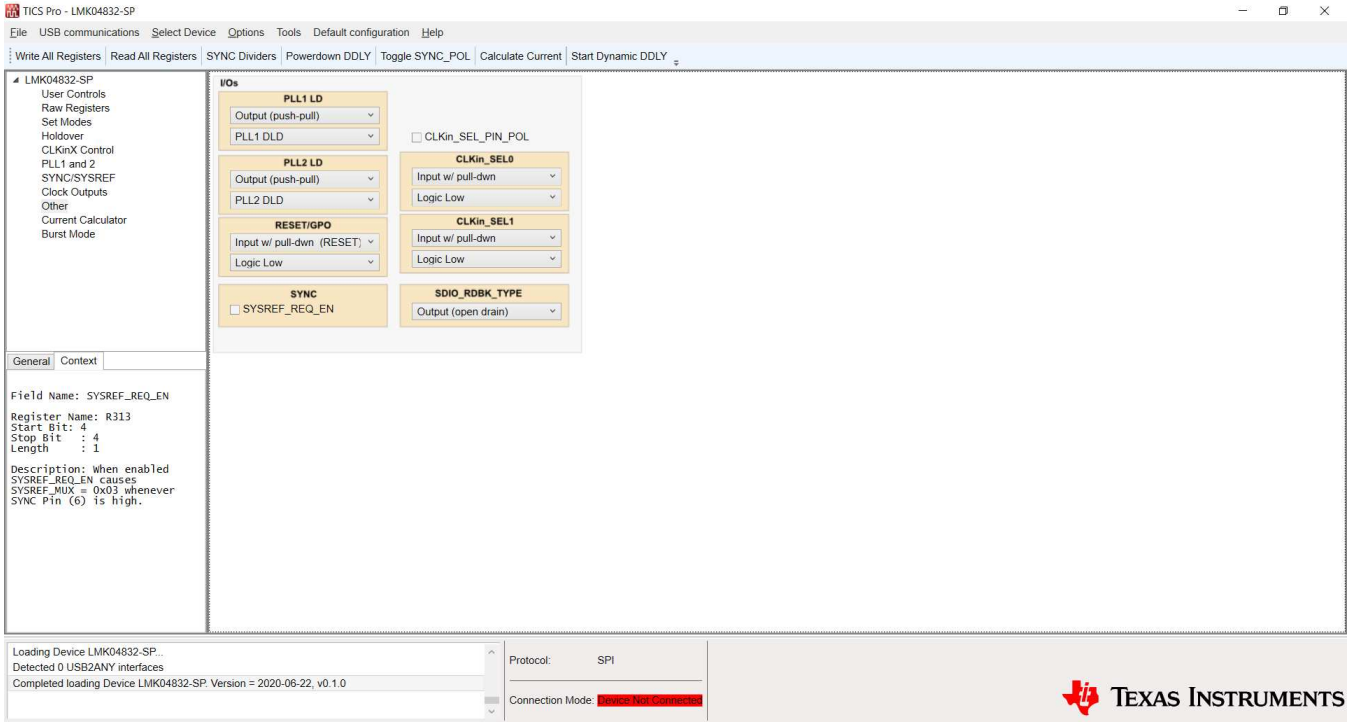

Figure 22. TICS Pro - Other Page

A.11 Current Calculator Page

The **Current Calculator** page allows the user to also set the same output format register as in the **Clock Outputs** page, but also set the hardware configuration connected to that output. With this information, along with the other programmed fields a current calculation estimate is made for the LMK04832-SP. Also, power dissipated externally in emitter resistors, and so forth, is estimated and subtracted from the total power to find the IC Power the device must dissipate.

In the lower left is some boxes to account for extra I_{CC} due to LEDs, VCXO, or other.

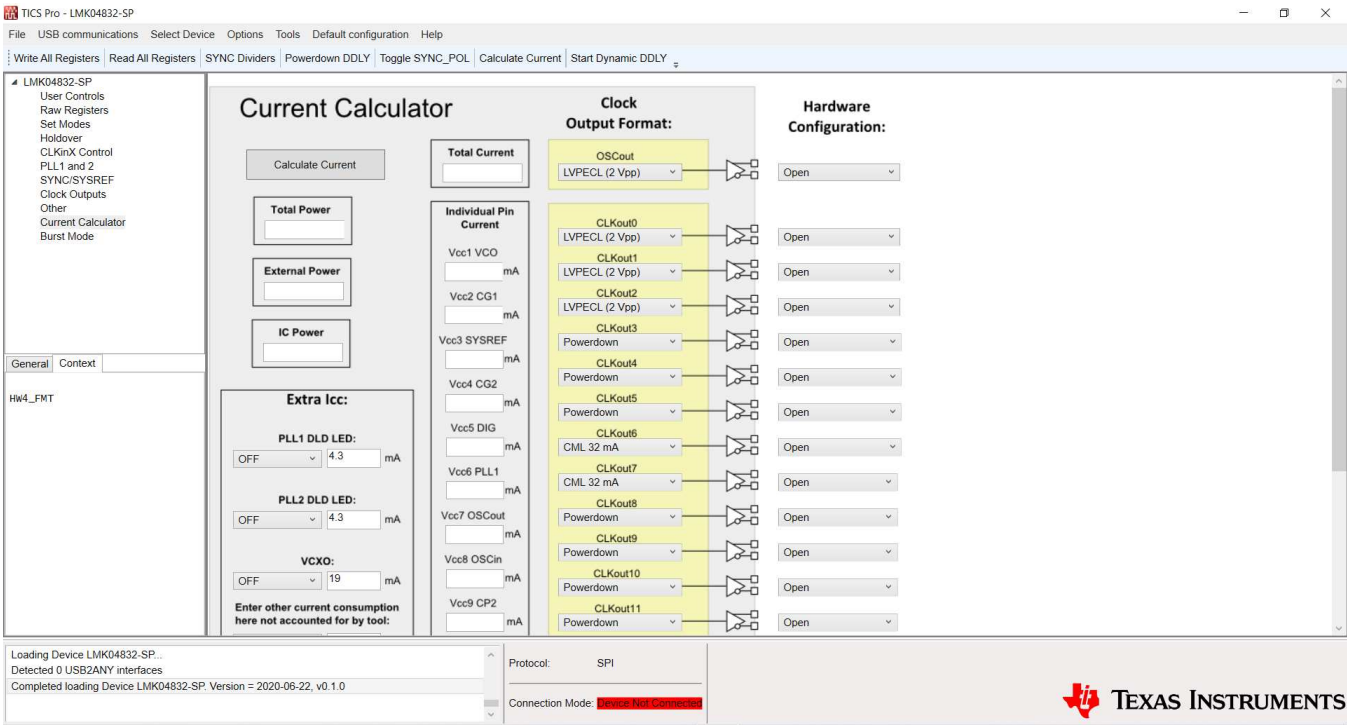

Figure 23. TICS Pro - Current Calculator Page

A.12 Burst Page

The **Burst** page allows the user to program sequences of register programming or pin control.

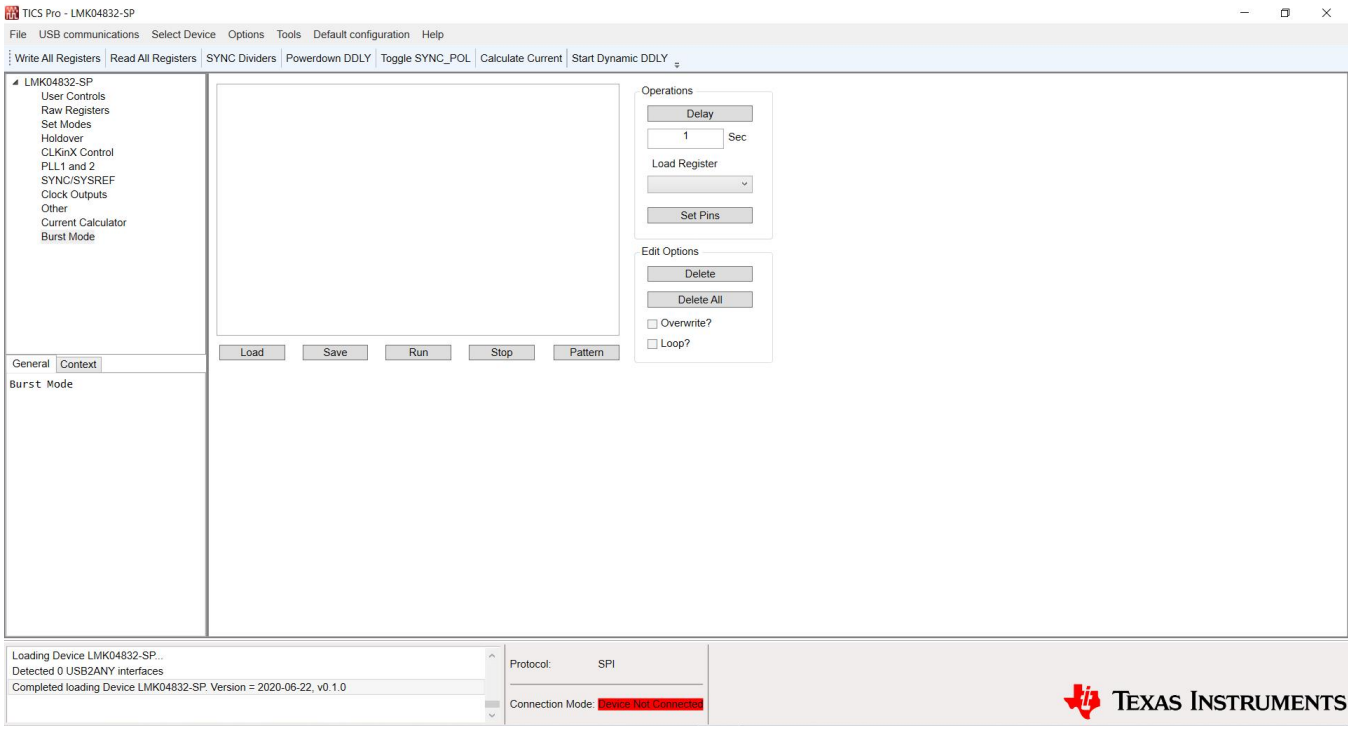

Figure 24. TICS Pro - Burst Page

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