LMK04208

User's Guide

Literature Number: SNAU200
September 2016

Contents

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LMK04208 User's Guide

1 Introduction

This user's guide describes how to set up and operate the LMK04208 evaluation module (EVM). The LMK04208 is the industry's highest performance clock conditioner with JEDEC JESD204B support.

2 Evaluation Board Kit Contents

The evaluation board kit includes what is shown in Table 1.

Table 1. EVM Contents

SV601293	-001
Evaluation Board	(1) LMK04208 Evaluation Board
USB Communications	(1) USB2ANY

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3 Quick Start

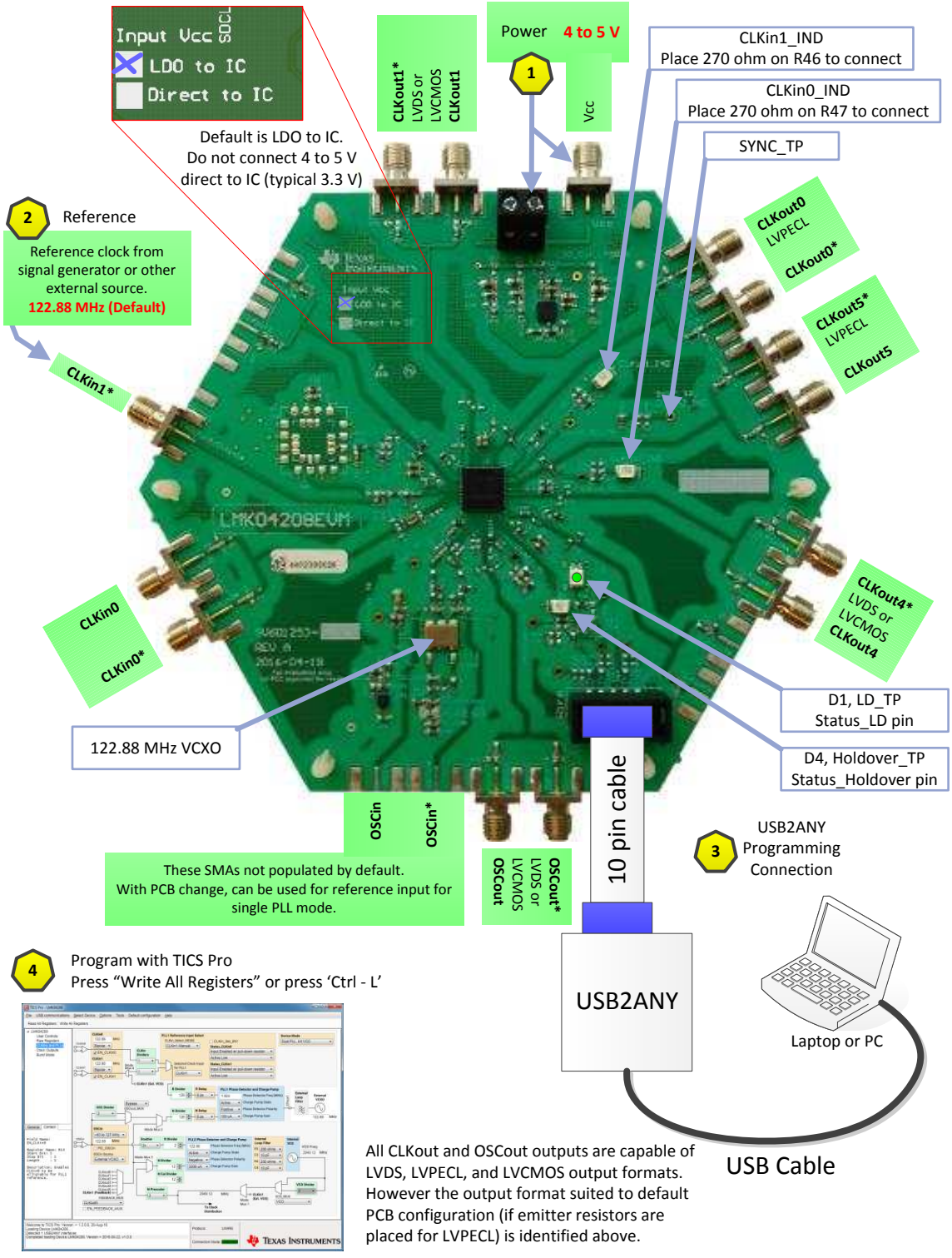

Figure 1. Quick Start Diagram

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3.1 Quick Start Description

The LMK04208 EVM allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Connect a voltage of **4.5** volts to the Vcc SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO. VCXO operates at 3.3 V using onboard LP5900 LDO.
2. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use **122.88 MHz** for default. Exact frequency and input port (CLKin0/CLKin1) depends on programming.
3. Connect uWire (MICROWIRE) header to a computer using USB2ANY.
4. Program the device with TICS Pro. TICS Pro is available for download at: http://www.ti.com/tool/TICS Pro. After starting TICS Pro.
   (a) Choose LMK04208 from the “Select Device" → "Clock Generator/Jitter Cleaner (Dual Loop)” Menu.
   (b) Open the Communication Setup window by click "USB Communications → Interface".
   - Confirm that USB2ANY is selected.
   - Select specific USB2ANY interface to use. click 'Identify' to confirm selected USB2ANY and valid communications to USB2ANY by blinking LED.
   - If LMK04208EVM or USB2ANY available, the software may be run in DemoMode for evaluation and generation of register programming data.
   - Press Close to exit Communication Setup.

   (c) From menu bar click "Default configuration" to select a default mode. For the quick start use, “**CLKin1 122.88 MHz, 122.88 MHz VCXO**”
   (d) Click "Write All Registers" or press **Ctrl-L** to load all registers. Alternatively from menu bar click "USB communications" → "Write All Registers."
5. Measurements may be made at an active CLKout port via its SMA connector. Default configuration configures CLKout4

3.1.1 CLKout Page Description

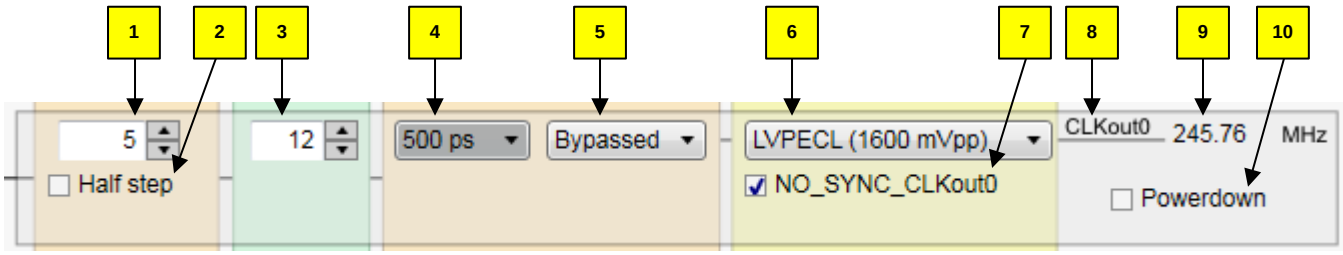

Figure 2. Clock Outputs Page CLKout Path Description Diagram

1. CLKoutX_DDLY for controlling digital delay. Programmed delay value takes effect on SYNC of divider.
2. CLKoutX_HS for finer resolution of digital delay. Advances waveform ½ device clock cycles, -0.5 to digital delay.
3. CLKoutX_DIV, divider for the output channel.
4. CLKoutX_ADLY, Analog delay if enabled with #5.
5. CLKoutX_ADLY_SEL, Analog delay select.
6. CLKoutX_TYPE, clock output format.
7. NO_SYNC_CLKoutX, when checked, output will never be SYNCed or held in SYNC.
8. Clock output identifier.
9. Calculated clock output frequency.
10. CLKoutX_PD, power down the entire CLKoutX group.

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3.1.2 TICS Pro Tips

- Mousing over controls shows help in the "Context" window to bottom left of screen.
- In bottom left of screen is displayed a "General" help for the page. After context help has been displayed, click this tab to view again.
- To enable read back for LMK04208, a 0-Ω resistor must be placed at R59, this shares Status_Holdover for use as read back. R59 is located just below the red D4 Status_Holdover LED.

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4 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO or crystal resonator) for the phase noise of a "dirty" reference clock. The first PLL is typically configured with a narrow loop bandwidth in order to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference.

The loop filters on the LMK04208 evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 100 Hz). Table 2 and Table 3 contain the parameters for PLL1 and PLL2 for using the default VCXO.

TI's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/clockdesigntool.

4.1 PLL1 Loop Filter

Table 2. PLL1 Loop Filter Parameters for VCXO with 8 kHz/V Tuning Sensitivity(1)

PLL1 using 122.88 MHz VCXO (Epson VG-4513CA-122.8800M-GFCT3)			
Loop Bandwidth	20 Hz	**Phase Margin**	50˚
Kφ (Charge Pump)	100 µA	**Tuning Sensitivity (K_{VCO})**	8 kHz/V
Reference Clock Frequency	122.88 MHz	**Phase Detector Freq**	1.024 MHz
PLL Total N	120	**VCXO Frequency**	122.88 MHz (PLL1 feedback and PLL2 reference)
Loop Filter Components	C1_VCXO = 150 nF	C2_VCXO_0603 = 1 µF	R2_VCXO = 22 kΩ

(1) Loop Bandwidth and Phase Margin is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N by device programming will change the loop bandwidth.

4.2 PLL2 Loop Filter

Table 3. PLL2 Loop Filter Parameters using Integrated VCO(1)

PLL2 using internal VCO			
Loop Bandwidth	320 kHz	**Phase Margin**	84˚
Kφ (Charge Pump)	3.2 mA	**Tuning Sensitivity (K_{VCO})**	27 MHz/V
Reference Clock Frequency	122.88 MHz	**Phase Detector Freq**	122.88 MHz
PLL Total N	24	**VCO Frequency**	2949.12 MHz
Loop Filter Components	C1_VCO = 0.022 nF	C2_VCO = 18 nF	Integrated C3 and C4 = 0.01 nF
		R2_VCO = 0.56 kΩ	Integrated R3 and R4 = 200 Ω

(1) Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

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5 Default TICS Pro Modes for the LMK04208

TICS Pro saves the state of the selected LMK04208 device when exiting the software. To ensure a common starting point, the following modes listed in Table 4 may be restored by clicking “Mode” and selecting the appropriate device configuration.

Table 4. Default TICS Pro Modes for the LMK04208

Default TICS Pro Mode	Device Mode	CLKin Frequency	OSCin Frequency
CLKin1 122.88 MHz, OSCin 122.88 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz
CLKin0 122.88 MHz, Dual Loop 0-delay, 122.88 MHz VCXO	Dual PLL 0-delay, Internal VCO	122.88 MHz	122.88 MHz

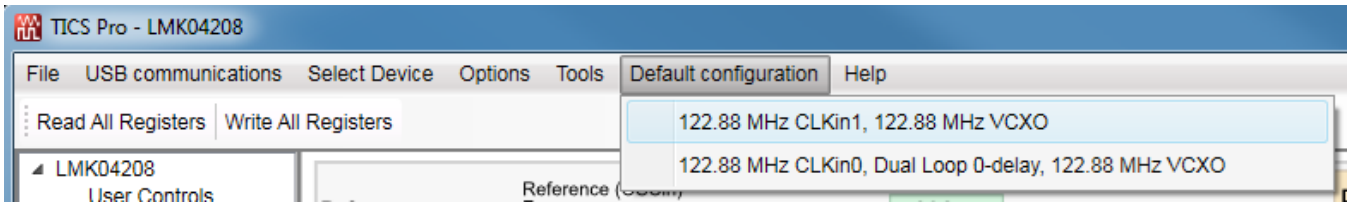

Figure 3. Selecting a Default Mode for the LMK04208 Device

6 Using TICS Pro to Program the LMK04208

This section will demonstrate how to use TICS Pro. Making measurements with the LMK04208 device will serve as an example. For more information on using TICS Pro, refer to Appendix A and TICS Pro instructions, "Help" → "TICS Pro User Manual."

Before proceeding, be sure to follow the instructions in Section 3 to ensure proper connections.

6.1 Start TICS Pro Application

Click “Start” → “Programs” → “Texas Instruments” → “TICS Pro” → “TICS Pro”

The TICS Pro program is installed by default to the TICS Pro application group.

6.2 Select Device

Click “Select Device" → "Clock Generator/Jitter Cleaner (Dual Loop)" → "LMK04208”

Upon start, TICS Pro will load the last used device. To load a different device, click “Select Device” from the menu bar, then select the subgroup and finally, the device to load. For this example, the LMK04208 is chosen.

6.3 Setup and Confirm Communications

If not already plugged in, connect USB2ANY interface. Click "USB communications" → "Interface"

Ensure USB2ANY is selected in the Communication Setup window. Press the Identify button to confirm desired USB2ANY is selected by observing blinking LED. Other instances of TICS Pro can be used at the same time, but if a USB2ANY is used in one application, in cannot be used in the second and may not show up.

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6.4 Restoring a Default Mode

Click “Mode” → “CLKin1 122.88 MHz, 122.88 MHz VCXO”; then press Ctrl+L.

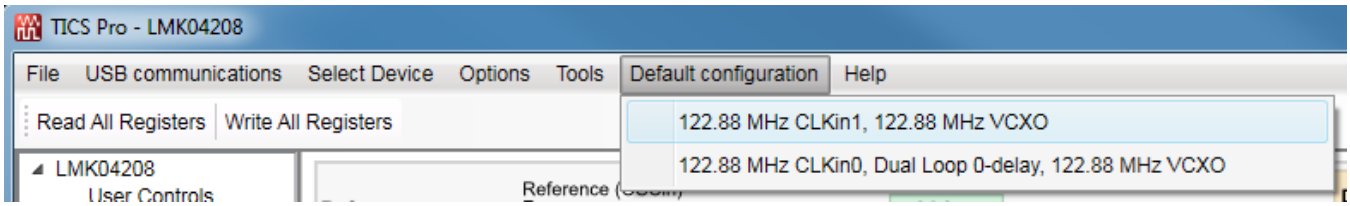

Figure 4. Setting the Default Mode for LMK04208

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when TICS Pro is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.

6.5 Program/Load Device

Provided the communication settings are correct, press the “Ctrl+L” shortcut or click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK04208 file.

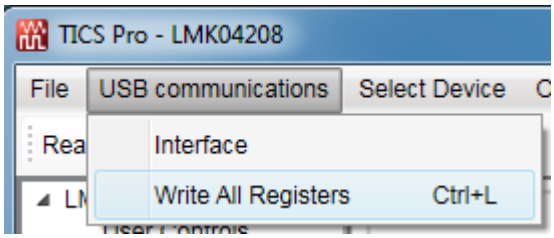

Figure 5. Loading the Device

Once the device has been initially loaded, TICS Pro will automatically program changed registers so it is not necessary to reload the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoUpdate.”

Because a default mode will be restored in the next step, this step isn’t really needed but included to emphasize the importance of pressing “Ctrl+L” to load the device at least once after starting TICS Pro, restoring a mode, or restoring a saved setup using the File menu.

See TICS Pro instructions by clicking "Help" → "TICS Pro User Manual." This contains information on troubleshooting communications.

6.6 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D1 will illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes LD_MUX = PLL1 & PLL2 DLD and LD_TYPE = Output (Push-Pull).

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6.7 Enable Clock Outputs

While the LMK04208 offers programmable clock output buffer formats, the evaluation board is shipped with pre-configured output terminations to match the default buffer type for each output.

To measure Phase noise at one of the clock outputs, for example CLKout0:

1. Click on the Clock Outputs page,
2. Uncheck “Powerdown” in the Clock output box to enable the channel. (10)
3. Set the following as needed:
   (a) Digital Delay value (1)
   (b) Clock Divider value (3)
   (c) Analog Delay Select and Analog Delay Value, if desired (4 and 5). Analog delay will add to noise floor of output.

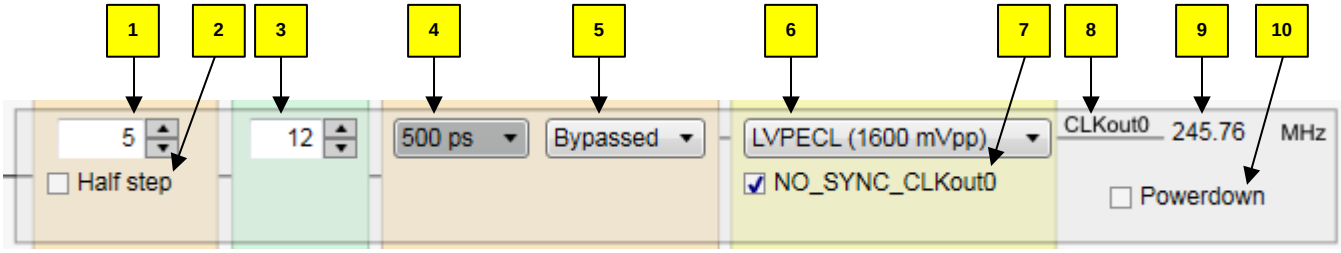

Figure 6. Setting Digital Delay, Clock Divider, Analog Delay and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-Ω input as follows.
   (a) For LVDS:
      (i) A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   (b) For LVPECL:
      (i) A balun can be used, or
      (ii) One side of the LVPECL signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

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7 Evaluation Board Inputs and Outputs

Table 5 contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable TICS Pro programming controls are noted for convenience.

Table 5. Description of Evaluation Board Inputs and Outputs

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="9">Populated:
CLKout0, CLKout0*,
CLKout1, CLKout1*,
CLKout4, CLKout4*,
CLKout5, CLKout5*</td><td rowspan="10">Analog,
Output</td><td colspan="2">Clock outputs with programmable output buffers.</td></tr>
<tr><td colspan="2">Default output terminations on the evaluation board are shown below:</td></tr>
<tr><td>Clock Output</td><td>Default Board Termination</td></tr>
<tr><td>CLKout0</td><td>240 Ω emitter resistor, LVPECL</td></tr>
<tr><td>CLKout1</td><td>open, LVDS/LVCMOS</td></tr>
<tr><td>CLKout2</td><td>240 Ω emitter resistor, LVPECL</td></tr>
<tr><td>CLKout3</td><td>240 Ω emitter resistor, LVPECL</td></tr>
<tr><td>CLKout4</td><td>open, LVDS/LVCMOS</td></tr>
<tr><td>CLKout5</td><td>240 Ω emitter resistor, LVPECL</td></tr>
<tr><td>Not Populated:
CLKout2, CLKout2*,
CLKout3, CLKout3*</td><td colspan="2">Each CLKout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The output buffer type can be selected in TICS Pro on the Clock Outputs page via the CLKoutX_TYPE control.
All clock outputs are AC-coupled to allow safe testing with RF test equipment.
If an output is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is NOT recommended to use Norm/Norm or Inv/Inv mode.</td></tr>
<tr><td rowspan="4">Populated:
OSCout, OSCout*</td><td rowspan="4">Analog,
Output</td><td colspan="2">Buffered output of OSCin port.</td></tr>
<tr><td colspan="2">The output terminations on the evaluation board are shown below.:</td></tr>
<tr><td>OSC Output</td><td>Default Board Termination</td></tr>
<tr><td>OSCout</td><td>open, LVDS/LVCMOS</td></tr>
<tr><td>Populated:
Vcc</td><td>Power,
Input</td><td colspan="2">Main power supply input for the evaluation board.
The LMK04208 contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.
On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See the schematics in section Section 9 for more details.
Apply power to either Vcc SMA or J1, but not both.</td></tr>
<tr><td>Populated:
J1</td><td>Power,
Input</td><td colspan="2">Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND).
Apply power to either Vcc SMA or J1, but not both.</td></tr>
<tr><td>Not Populated:
VccVCXO/Aux</td><td>Power,
Input</td><td colspan="2">Optional Vcc input to power the VCXO circuit if separated voltage rails are needed. The VccVCXO/Aux input can power these circuits directly or supply the on-board LDO regulators. 0 Ω resistor options provide flexibility to route power.
This connector is on the bottom of the PCB.</td></tr>
</table>

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Table 5. Description of Evaluation Board Inputs and Outputs (continued)

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION
Populated: CLKin0, CLKin0*, FBCLKin*/CLKin1*	Analog, Input	**Reference Clock Inputs for PLL1 (CLKin0, CLKin1)** CLKin0/CLKin0* is configured by default for a differential reference clock input from a 50-ohm source. FBCLKin*/CLKin1* is configured by default for a single-ended reference clock input from a 50-ohm source using a 3 dB pad for termination which is recommended for high speed inputs. The unused input pin (FBCLKin/CLKin1) is connected to GND with a 0.1 µF. CLKin1 is the default reference clock input selected in TICS Pro. The clock input selection mode can be programmed on the **CLKins and PLLs** page via the Clock Inputs control.
		CLKin1 as External Feedback Input (FBCLKin) for 0-Delay CLKin1 is shared for use with FBCLKin as an external feedback clock input to PLL1 for 0-delay mode.
		CLKin1 as Fin for external VCO or Clock Distribution mode CLKin1 be used as an RF Input (Fin) for External VCO for PLL2 or for an input in Clock Distribution mode.
Not Populated: OSCin, OSCin*	Analog, Input	OSCin is the feedback clock input to PLL1 and reference clock input to PLL2. The onboard VCXO drives OSCin by default for dual loop operation. By default the differential output of the LVPECL VCXO (U8) or the single-ended output of the onboard VCXO (U2) drives the OSCin input of the device. When using a single ended VCXO the OSCin* port is driven and the non-inverting OSCin input of the device is connected to GND with 0.1 µF. An external VCXO may be optionally attached via these SMA connectors with minor modification to the components going to the OSCin/OSCin* pins of device. This is useful if the VCXO footprint does not accommodate the desired VCXO device or if the user desires to use the LMK04208 in single loop mode. It is also necessary to connect the Vtune input of the VCXO to the CPout1. A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 µF. Refer to the LMK04802 datasheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications (literature number SNAS684).
Test point: VTUNE1_TP	Analog, Input	Tuning voltage monitor for the loop filter for PLL1.
Test point: VTUNE2_TP	Analog, Input	Tuning voltage monitor for the loop filter for PLL2.
Test points: DATA CLK LE	CMOS, Input	10-pin header for MICROWIRE™ programming interface and programmable logic I/O pins for the LMK04208.
Populated: uWire		10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04208. The programmable logic I/O signals accessible through this header include: SYNC, Status_LD, Status_Holdover, Status_CLKin0, and Status_CLKin1. These logic I/O signals also have dedicated SMAs and test points.
Test point: LD_TP	CMOS, Input/Output	Programmable status output pin. By default, set to output the digital lock detect status signal for PLL1 & PLL2 DLD. In the default TICS Pro modes, LED D1 will illuminate green when PLL1 and PLL2 lock is detected by the LMK04208 (output is high) and turn off when lock is lost (output is low).
Status_LD pin 33		The status output signal for the Status_LD pin can be selected on the **User Controls** page via the LD_MUX and LD_TYPE controls. **For debugging purposes, it is suggested to set LD_MUX/Status_LD to output PLL1 DLD and HOLDOVER_MUX/Status_Holdover to output PLL2 DLD individually. In holdover mode PLL1 DLD will normally be low but may flicker high momentarily.**

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Table 5. Description of Evaluation Board Inputs and Outputs (continued)

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>Test point: Holdover_TP</td><td>CMOS, Input/Output</td><td>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL2.
In the default TICS Pro modes, LED D4 will illuminate red when Holdover mode is engaged (output is high) and turn off when holdover is disengaged (output is low).</td></tr>
<tr><td>Status_Holdover pin 27</td><td></td><td>The status output signal for the Status_Holdover pin can be selected on the User Controls page via the HOLDOVER_MUX and HOLDOVER_TYPE controls.
For debugging purposes, it is suggested to set LD_MUX/Status_LD to output PLL1 DLD and HOLDOVER_MUX/Status_Holdover to output PLL2 DLD individually. In holdover mode PLL1 DLD will normally be low but may flicker high momentarily.</td></tr>
<tr><td rowspan="6">Test points: CLKin0_SEL_TP CLKin1_SEL_TP</td><td rowspan="6">CMOS, Input/Output</td><td>Programmable status I/O pins. By default, set as input pins for controlling input clock switching of CLKin0 and CLKin1 if Pin Select mode is enabled by CLKin_Select_MODE.
These inputs will not be functional because CLKin_SEL_MODE is set to 0 (CLKin0 Manual) by default in the User Controls page in TICS Pro. To enable input clock switching, CLKin_SEL_MODE must be 3 and Status_CLKinX_TYPE must be 0 to 2 (pin enabled as an input).</td></tr>
<tr><td>Input Clock Switching – Pin Select Mode
When CLKin_Select_MODE is 3 and CLKin_Sel_INV = 0, the Status_CLKinX pins select which clock input is active as follows:</td></tr>
<tr><td>
<table>
<tr><th>Status_CLKin1</th><th>Status_CLKin0</th><th>Active Clock</th></tr>
<tr><td>0</td><td>0</td><td>CLKin0</td></tr>
<tr><td>0</td><td>1</td><td>CLKin1</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Holdover</td></tr>
</table>
</td></tr>
<tr><td>Test point: SYNC_TP</td><td>CMOS, Input/Output</td><td>Programmable status I/O pin. By default, set as an input pin for synchronizing the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.
A physical SYNC pin transition may be emulated by toggling the SYNC_POL_INV bit.</td></tr>
<tr><td>Populated: SYNC</td><td></td><td>SYNC pin can hold outputs in a low state, depending on system configuration (NO_SYNC_CLKoutX bits). SYNC_POL_INV adjusts for active low or active high control.
A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the User Controls page in TICS Pro.</td></tr>
</table>

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8 Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50-Ω inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it is recommended to use phase-matched, 50-Ω cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

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9 Schematics

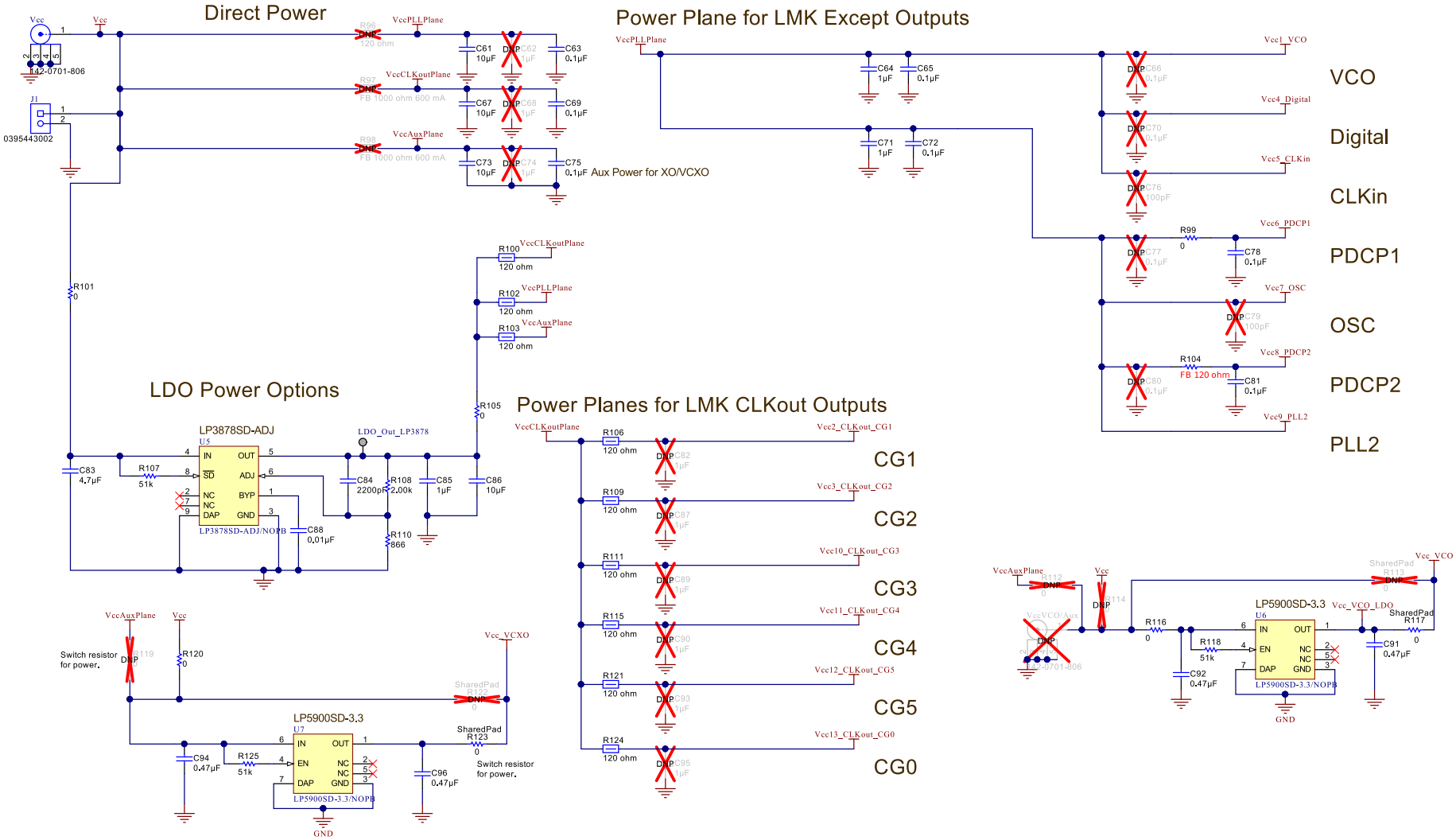

Figure 7. Power Supply

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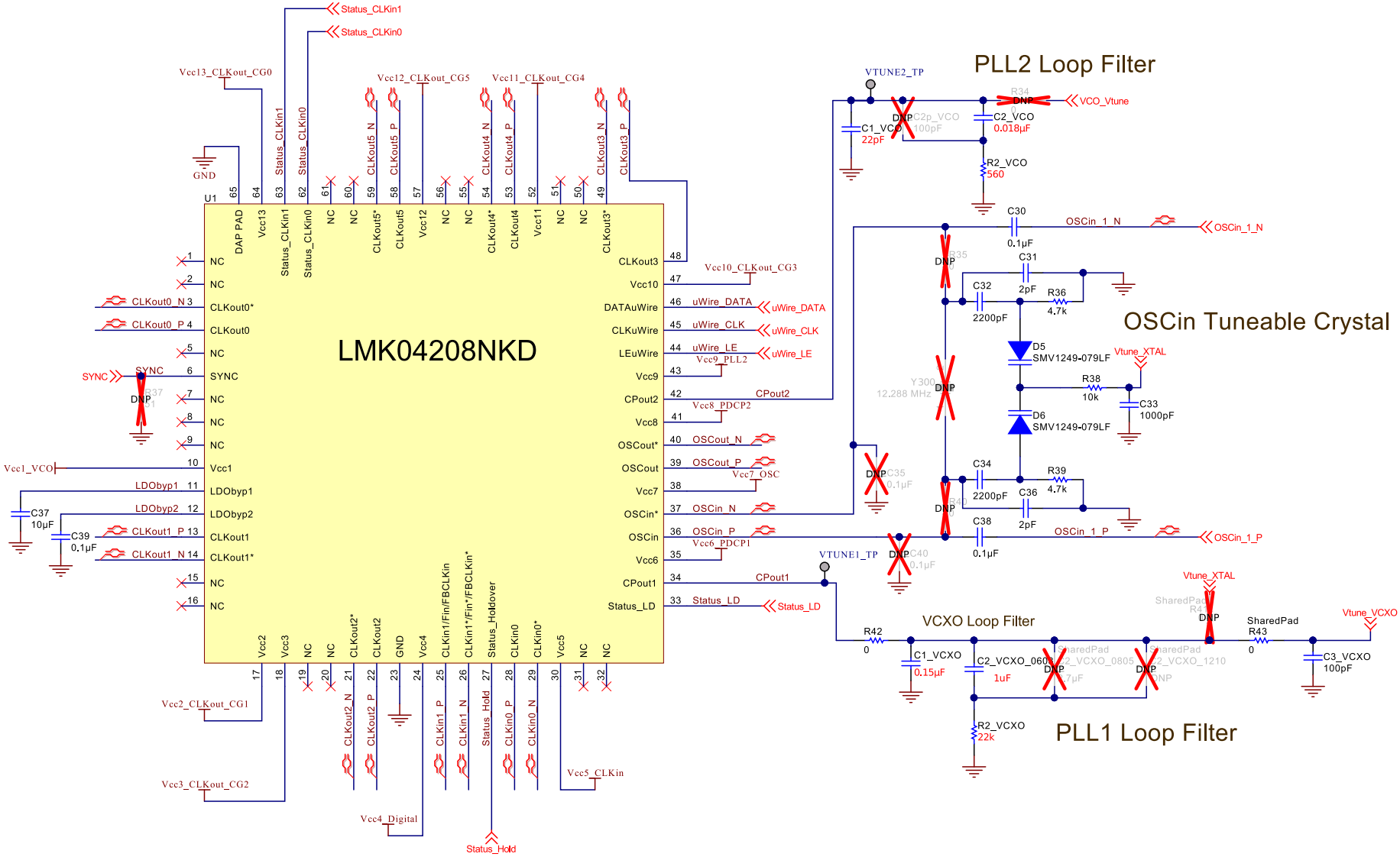

Figure 8. LMK04208

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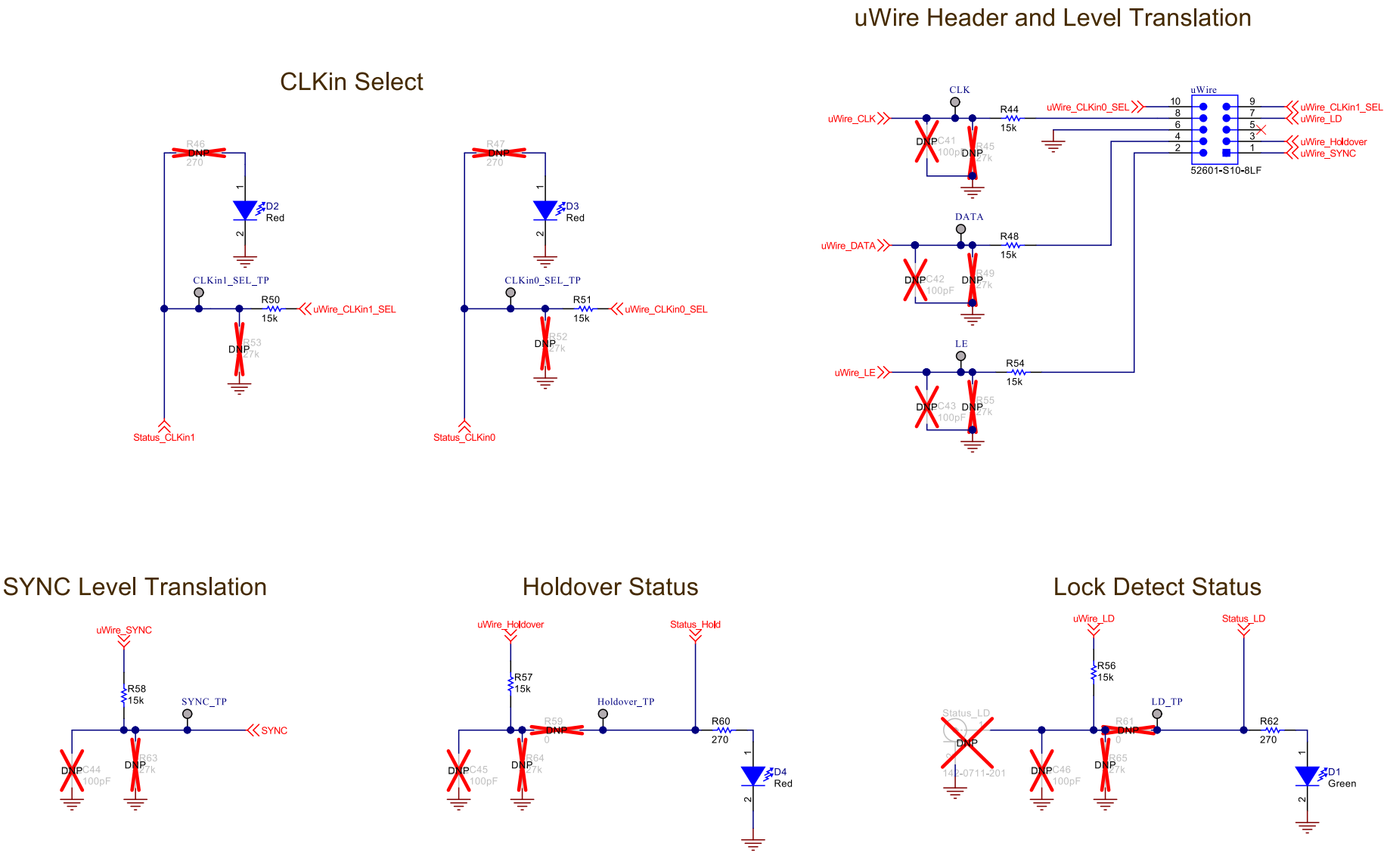

Figure 9. Digital

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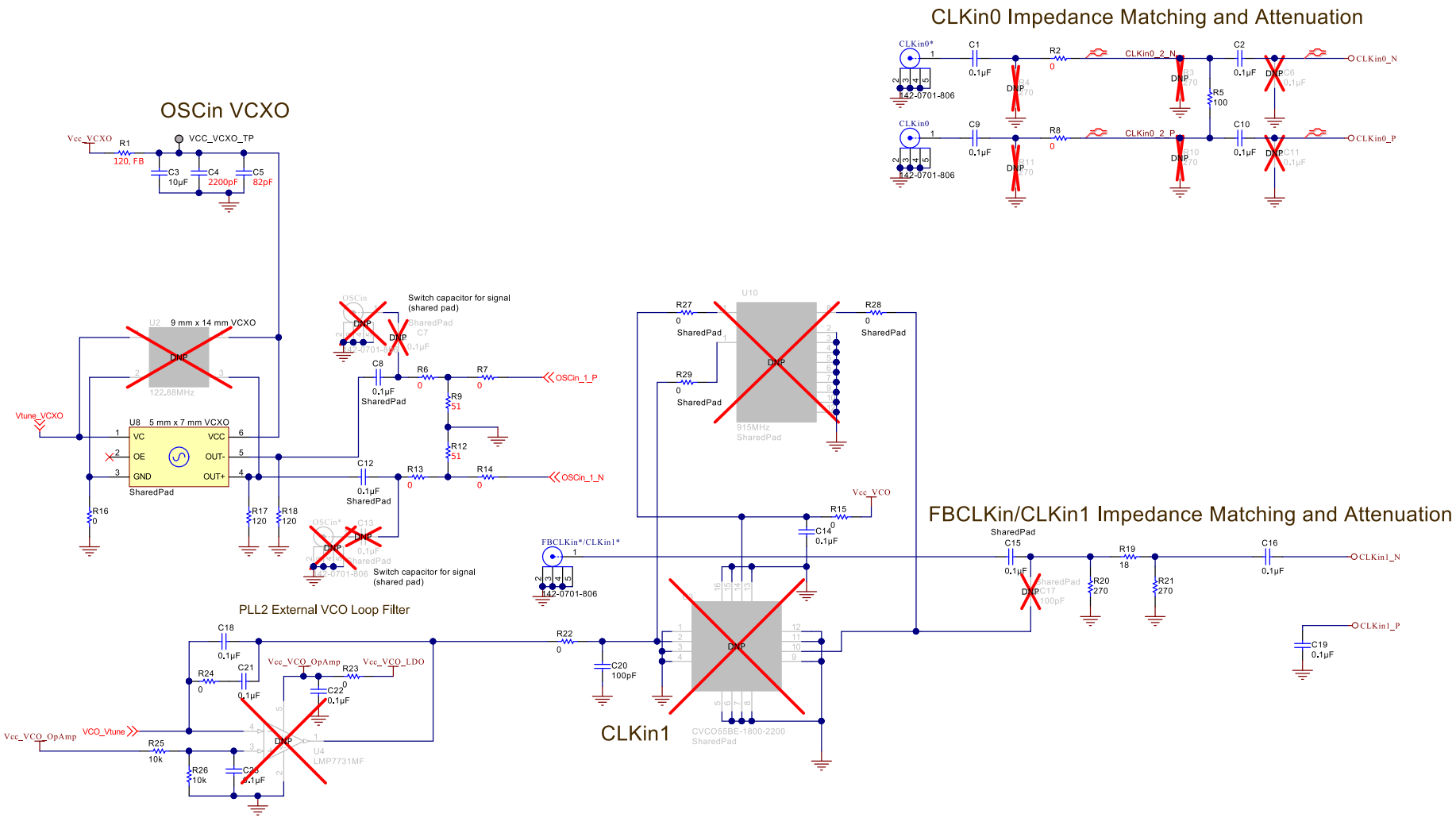

Figure 10. Inputs

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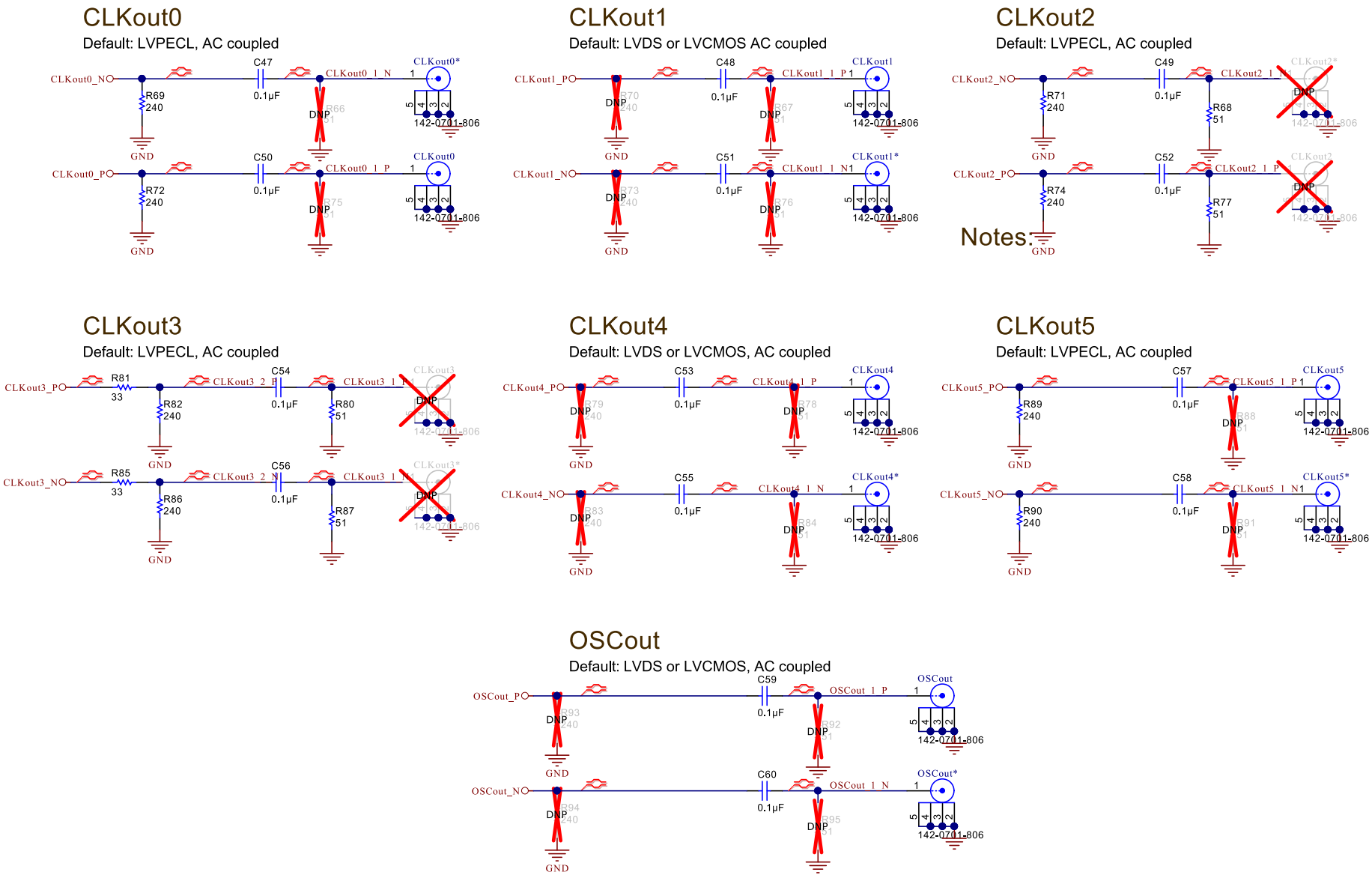

Figure 11. Clock Outputs

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10 Bill of Materials

Table 6. LMK04208EVM BOM

Item	Designator	Qty	Description	PartNumber	Manufacturer
1	!PCB	1	Printed Circuit Board	SV601293	Any
2	C1, C2, C8, C9, C12, C14, C18, C21, C23	9	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	C0603C104K4RACTU	Kemet
3	C1_VCO	1	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	C0603C220J5GACTU	Kemet
4	C1_VCXO	1	CAP, CERM, 0.15 µF, 25 V, +80/-20%, Y5V, 0603	C0603C154Z3VACTU	Kemet
5	C2_VCO	1	CAP, CERM, 0.018 µF, 100 V, +/- 10%, X7R, 0603	C0603C183K1RACTU	Kemet
6	C2_VCXO_0603	1	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	C0603C105K3RACTU	Kemet
7	C3	1	CAP, CERM, 10µF, 10V, +/-20%, X5R, 0805	C0805C106M8PACTU	Kemet
8	C3_VCXO, C20	2	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	C0603C101J5GACTU	Kemet
9	C4, C32, C34	3	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	C0603C222K5RACTU	Kemet
10	C5	1	CAP, CERM, 82pF, 50V, +/-10%, C0G/NP0, 0603	C0603C820K5GACTU	Kemet
11	C10, C15, C16, C19, C30, C38, C39, C47, C48, C49, C50, C51, C52, C53, C54, C55, C57, C58, C59, C60, C63, C69, C78, C81	24	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	C0603C104J3RACTU	Kemet
12	C22	1	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	C0603C104K4RACTU	Kemet
13	C31, C36	2	CAP, CERM, 2pF, 50V, +/-12.5%, C0G/NP0, 0603	C0603C209C5GACTU	Kemet
14	C33	1	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	C0603C102J5GACTU	Kemet
15	C37, C61, C67, C73, C86	5	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	C0805C106K8PACTU	Kemet
16	C56, C65, C72, C75	4	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	C0603C104K3RACTU	Kemet
17	C64, C71	2	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	C0603C105K8PACTU	Kemet
18	C83	1	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	C0603C475K8PACTU	Kemet
19	C84	1	CAP, CERM, 2200pF, 100V, +/-5%, X7R, 0603	06031C222JAT2A	AVX
20	C85	1	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	C1608X7R1C105K080AC	TDK
21	C88	1	CAP, CERM, 0.01 µF, 25 V, +/- 5%, C0G/NP0, 0603	C0603H103J3GACTU	Kemet
22	C91, C92, C94, C96	4	CAP, CERM, 0.47uF, 25V, +/-10%, X7R, 0603	GRM188R71E474KA12D	MuRata
23	CLKin0, CLKin0*, CLKout0, CLKout0*, CLKout1, CLKout1*, CLKout4, CLKout4*, CLKout5, CLKout5*, FBCLKin*/CLKin1*, OSCout, OSCout*, Vcc	14	Connector, End launch SMA, 50 ohm, SMT	142-0701-806	Emerson Network Power
24	D1	1	LED, Green, SMD	SML-LX2832GC-TR	Lumex
25	D2, D3, D4	3	LED, Red, SMD	SML-LX2832IC-TR	Lumex

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Table 6. LMK04208EVM BOM (continued)

Item	Designator	Qty	Description	PartNumber	Manufacturer
26	D5, D6	2	Hyperabrupt Junction Tuning Varactor, SOD-523	SMV1249-079LF	Skyworks Solutions
27	FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
28	J1	1	Terminal Block, 5.08mm, 2x1, TH	0395443002	Molex
29	LBL1	1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	THT-13-457-10	Brady
30	R1	1	FB, 120 ohm, 500 mA, 0603	BLM18AG121SN1D	Murata
31	R2, R8, R15, R16, R22, R23, R24, R42, R43, R99, R101, R105, R116, R117, R120, R123	16	RES, 0 ohm, 5%, 0.1W, 0603	CRCW06030000Z0EA	Vishay-Dale
32	R2_VCO	1	RES, 560, 5%, 0.1 W, 0603	CRCW0603560RJNEA	Vishay-Dale
33	R2_VCXO	1	RES, 22 k, 5%, 0.1 W, 0603	CRCW060322K0JNEA	Vishay-Dale
34	R5	1	RES, 100 ohm, 5%, 0.1W, 0603	CRCW0603100RJNEA	Vishay-Dale
35	R6, R7, R13, R14	4	RES, 0, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
36	R9, R12	2	RES, 51, 5%, 0.1 W, 0603	CRCW060351R0JNEA	Vishay-Dale
37	R17, R18	2	RES, 120 ohm, 5%, 0.1W, 0603	CRCW0603120RJNEA	Vishay-Dale
38	R19	1	RES, 18 ohm, 5%, 0.1W, 0603	CRCW060318R0JNEA	Vishay-Dale
39	R20, R21, R60, R62	4	RES, 270 ohm, 5%, 0.1W, 0603	CRCW0603270RJNEA	Vishay-Dale
40	R25, R26, R38	3	RES, 10k ohm, 5%, 0.1W, 0603	CRCW060310K0JNEA	Vishay-Dale
41	R27, R28, R29	3	RES, 0, 5%, 0.063 W, 0402	CRCW04020000Z0ED	Vishay-Dale
42	R36, R39	2	RES, 4.7k ohm, 5%, 0.1W, 0603	CRCW06034K70JNEA	Vishay-Dale
43	R44, R48, R50, R51, R54, R56, R57, R58	8	RES, 15k ohm, 5%, 0.1W, 0603	CRCW060315K0JNEA	Vishay-Dale
44	R68, R77, R80, R87	4	RES, 51 ohm, 5%, 0.1W, 0603	CRCW060351R0JNEA	Vishay-Dale
45	R69, R71, R72, R74, R82, R86, R89, R90	8	RES, 240 ohm, 5%, 0.1W, 0603	CRCW0603240RJNEA	Vishay-Dale
46	R81, R85	2	RES, 33 ohm, 5%, 0.1W, 0603	CRCW060333R0JNEA	Vishay-Dale
47	R100, R102, R103, R106, R109, R111, R115, R121, R124	9	Ferrite Bead, 120 ohm @ 100 MHz, 0.5 A, 0603	BLM18AG121SN1D	Murata
48	R104	1	Ferrite	BLM18AG121SN1D	Murata
49	R107, R118, R125	3	RES, 51k ohm, 5%, 0.1W, 0603	CRCW060351K0JNEA	Vishay-Dale
50	R108	1	RES, 2.00k ohm, 1%, 0.1W, 0603	CRCW06032K00FKEA	Vishay-Dale
51	R110	1	RES, 866 ohm, 1%, 0.1W, 0603	CRCW0603866RFKEA	Vishay-Dale
52	S1, S2, S3, S4, S5, S6	6	HEX STANDOFF SPACER, 9.53 mm	TCBS-6-01	Richco Plastics
53	U1	1	Low-Noise Clock Jitter Cleaner with Dual Loop PLLs, NKD0064A	LMK04208NKDR	Texas Instruments
54	U5	1	Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	LP3878SD-ADJ/NOPB	Texas Instruments
55	U6, U7	2	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	LP5900SD-3.3/NOPB	Texas Instruments
56	U8	1	OSC, 122.88 MHz, 3.3 Vdc, SMD	VG-4513CA 122.8800M-GFCT3	Epson
57	uWire	1	Header (shrouded), 100mil, 5x2, Gold, SMT	52601-S10-8LF	FCI

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TICS Pro Usage

TICS Pro is used to program the evaluation board with the USB2ANY adapter. TICS Pro is available for download at: http://www.ti.com/tool/ticspro-sw.

The following shows screenshots from the application for the LMK04208 along with some comments for use of the displayed screen.

A.1 Communication Setup Window

The Communication Setup dialog is opened by selecting "USB communications" → "Interface." The user may select the USB2ANY that will be used to program the device on the evaluation board. If multiple USB2ANYs are connected to the same PC, identify the target device by clicking the Identify button - the selected USB2ANY will briefly blink the onboard LED.

If no USB2ANY + LMK04208 is available, selecting DemoMode will allow the application to be used and generate programming configurations.

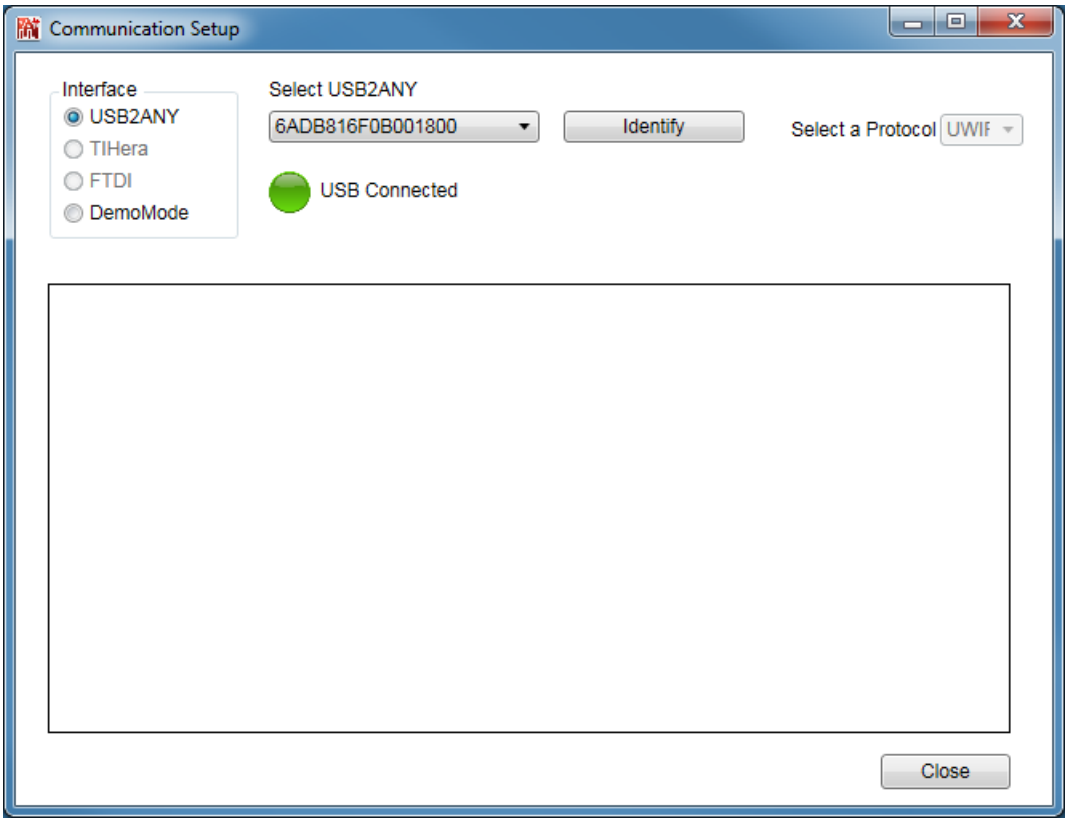

Figure 12. Communication Setup Dialog

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A.2 CLKins and PLLs Page

The CLKins and PLL page allows the user to change select device operation mode, select clock input and PLL operational frequencies.

The OSCin Source control doesn't control an actual register but unlinks the VCXO frequency from OSCin to allow for single PLL operation of PLL2.

Likewise the "selected clock input for PLL1" combobox allows the user to select which input clock to use for frequency calculations, this is important for Pin Select and Auto CLKin Select modes.

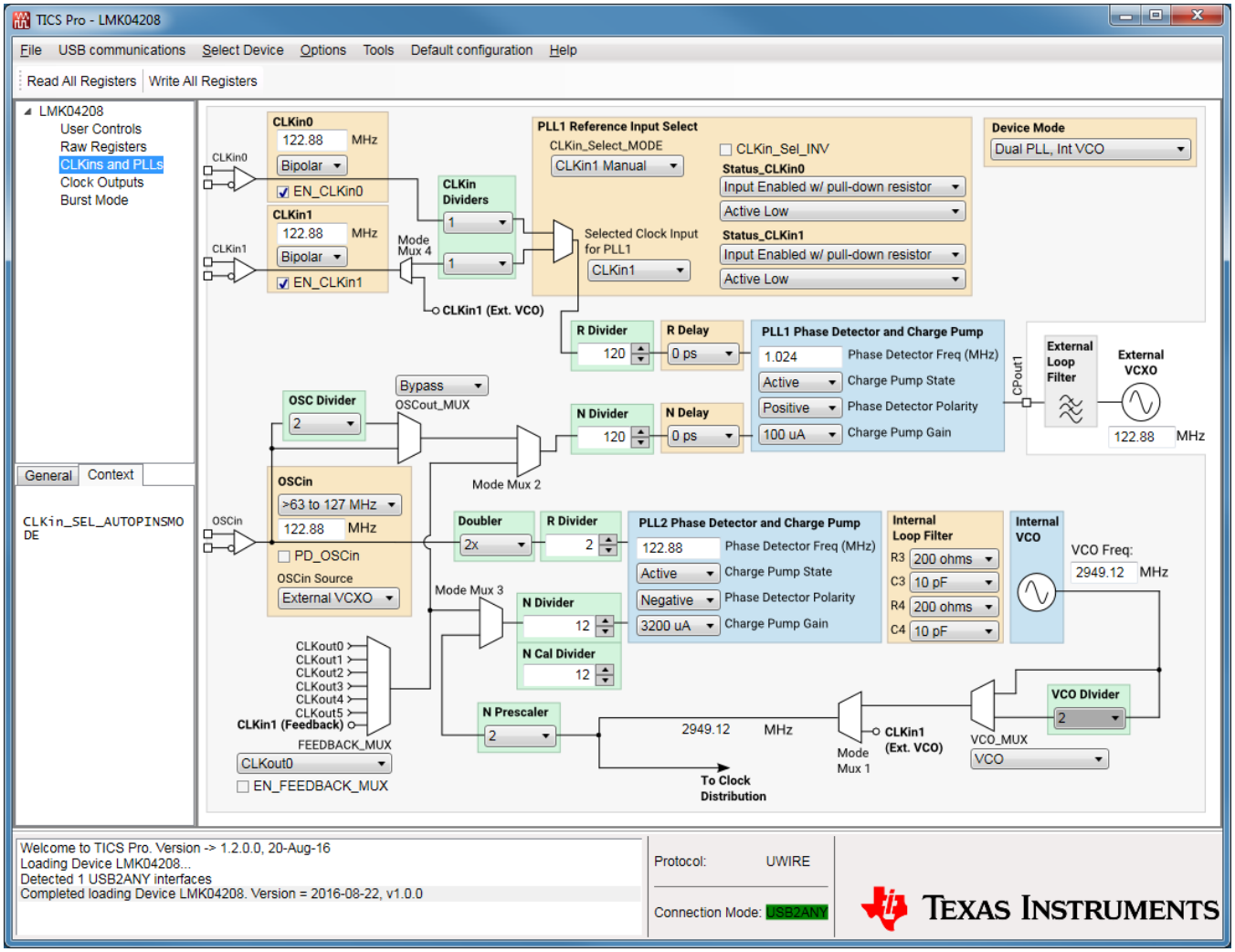

Figure 13. CLKins and PLLs page

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A.3 Clock Outputs Page

The **Clock Distribution** page allows the user to control the output channel blocks.

If a 0-delay mode is being used, changing the clock output frequency (divider or source) in the feedback path may impact PLL lock.

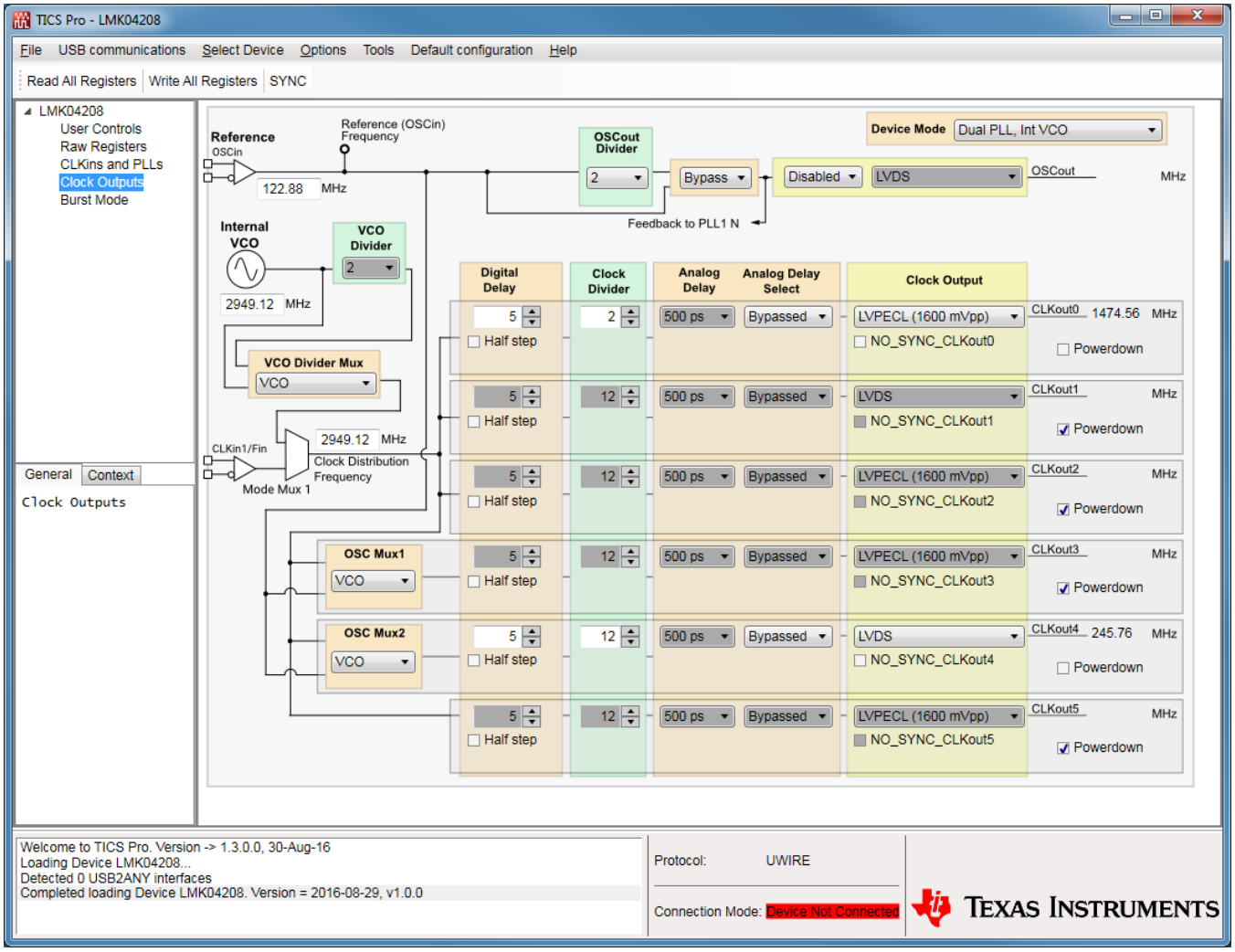

Figure 14. Clock Outputs Page

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A.4 User Controls Page

The **User Controls** page allows the user to program bits not available on other pages. Of note is the LD_MUX and HOLDOVER_MUX registers for controlling the status outputs. These allow the user to set the status outputs to display PLL1 or PLL2 digital lock detect. Other common settings are PLLX R/2 or PLLX N/2 to troubleshoot PLL locking issues. This displays half the frequency at the phase detector from the R or N path. Unexpected frequencies from either of these nodes will help to determine if the lock issue is associated with reference or feedback path.

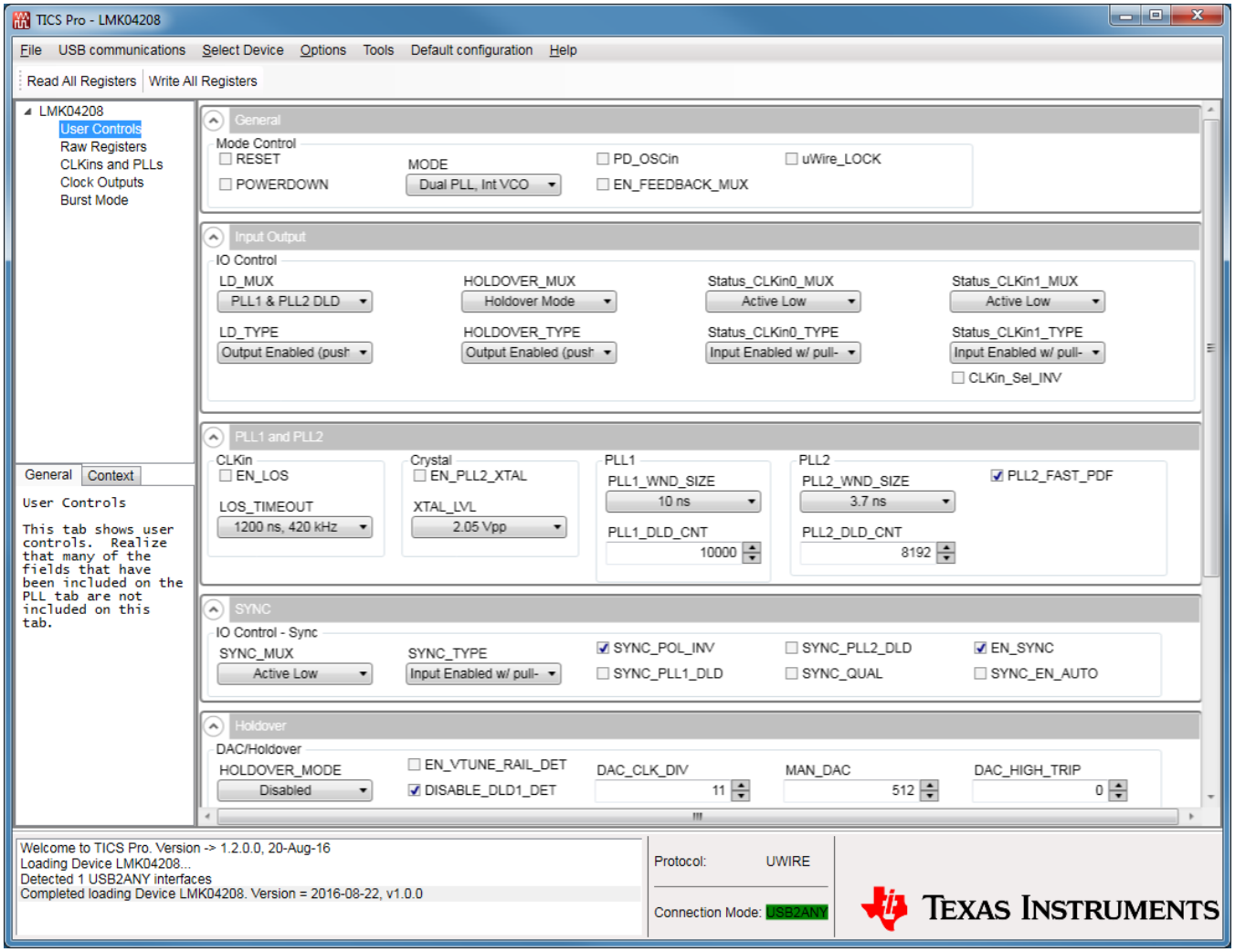

Figure 15. User Controls page

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A.5 Raw Registers Page

The **Raw Registers** page allows the user to see and directly change the bit field being used to program the device.

Export Register Map or "File" → "Export Hex Register Values" will dump the registers to a simple txt file format which can then be used by the customer's application for programming the configured LMK04208 mode.

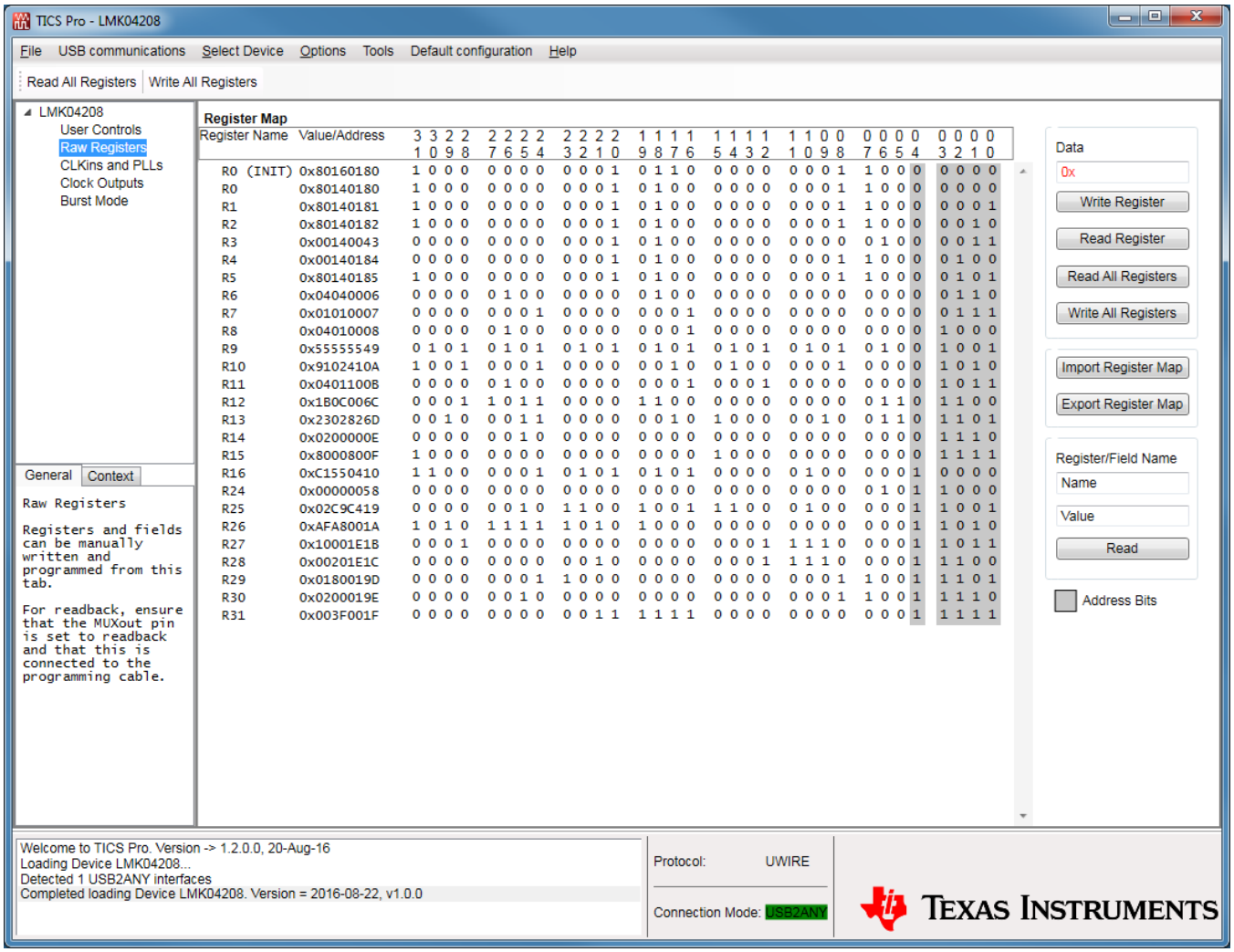

Figure 16. Raw Registers Page

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A.6 Burst Mode Page

The **Burst Mode** page allows the user to create sequences or loops of register programming for test purposes.

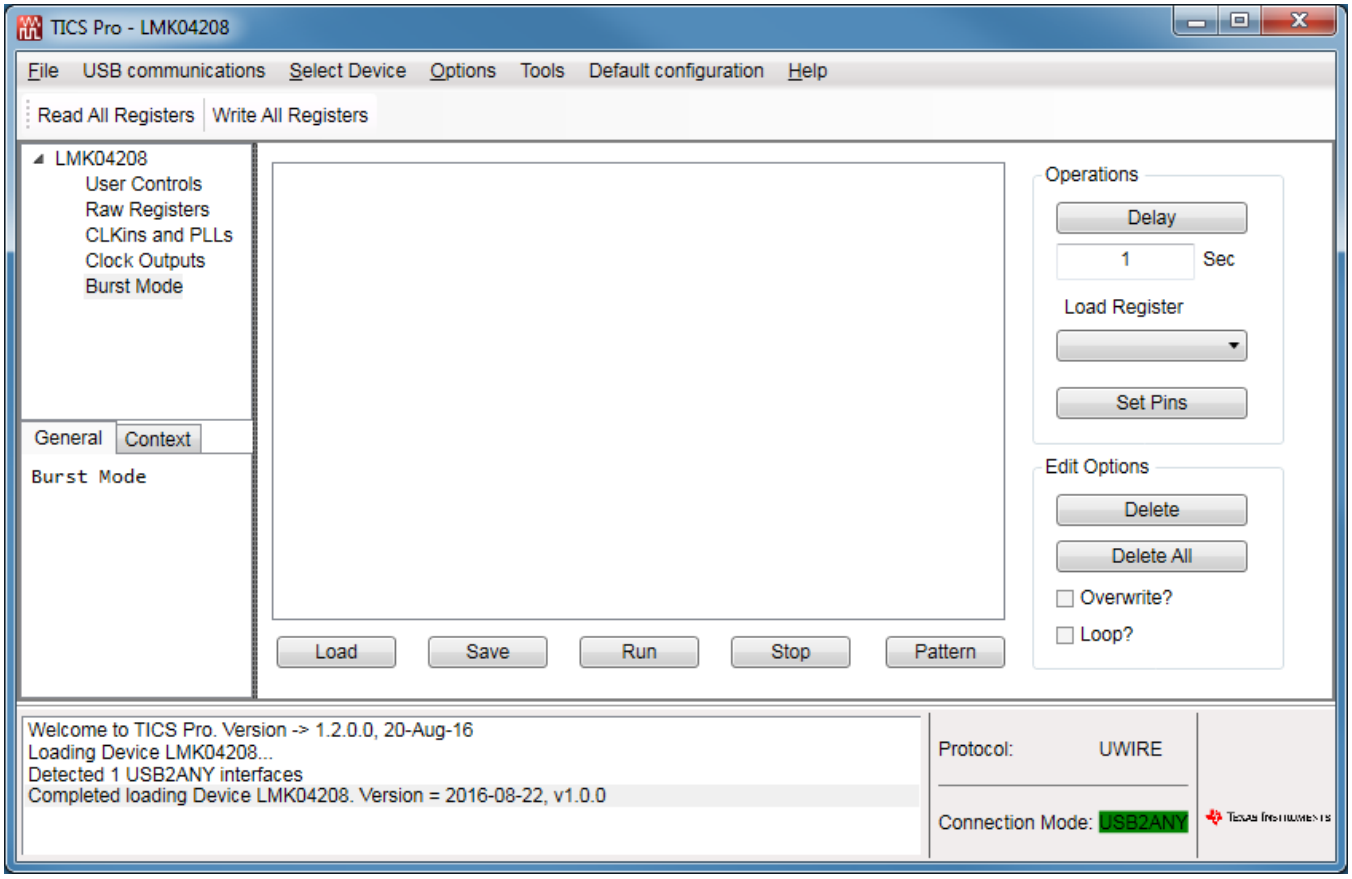

Figure 17. Burst Mode Page

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Typical Phase Noise Performance Plots

The LMK04208's dual PLL architecture achieves ultra low jitter and phase noise by allowing the external VCXO or Crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in the best overall noise and jitter performance.

Table 7 lists the test conditions used for output clock phase noise measurements with the VG-4513CA-122.8800M-GFCT3 Epson VCXO.

Table 7. LMK04208 Test Conditions

PARAMETER	VALUE
PLL1 Reference clock input	CLKin1* single-ended input, CLKin1 AC-coupled to GND
PLL1 Reference Clock frequency	122.88 MHz
PLL1 Phase detector frequency	1024 kHz
PLL1 Charge Pump Gain	100 µA
VCXO frequency	122.88 MHz
PLL2 phase detector frequency	122.88 MHz
PLL2 Charge Pump Gain	3.2 mA
PLL2 REF2X mode	Enabled

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B.1 VCXO Phase Noise 122.88 MHz

The phase noise of the reference is masked by the phase noise of this VCXO by using a narrow loop bandwidth for PLL1 while retaining the frequency accuracy of the reference clock input. This VCXO sets the reference noise to PLL2. Figure 18 shows the open loop typical phase noise performance of the VG-4513CA-122.8800M-GFCT3 Epson VCXO and CVHD-950-122.88 Crystek VCXO.

120 ohm em refers to the emitter resistors of the AC coupled LVPECL output are 120 Ω.

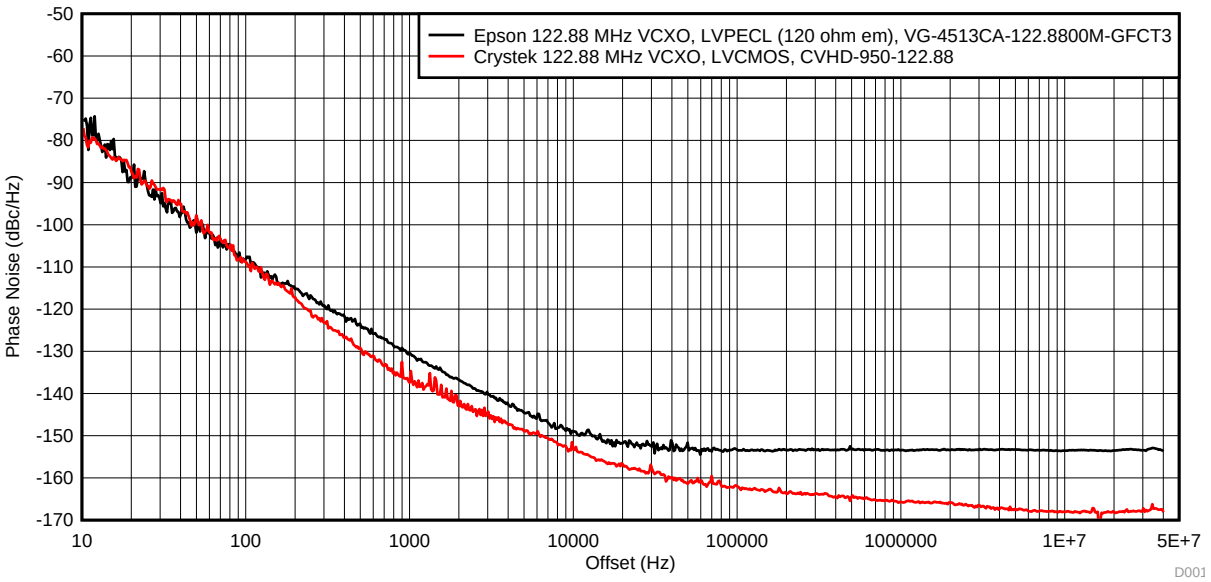

Figure 18. VCXO Phase Noise at 122.88 MHz

Table 8. VCXO Phase Noise at 122.88 MHz (dBc/Hz)

Offset	Epson	Crystek
10 Hz	-74.1	-76.6
100 Hz	-108.2	-108.9
1 kHz	-130.4	-137.4
10 kHz	-148.9	-153.3
100 kHz	-153.3	-162.0
1 MHz	-153.4	-165.7
5 MHz	-153.3	-167.5
10 MHz	-153.6	-168.1
20 MHz	-153.5	-168.0
40 MHz	-153.7	-168.1

Table 9. VCXO Jitter at 122.88 MHz (fs RMS)

Offset	Epson	Crystek
100 Hz to 20 MHz	185.6	60.5
12 kHz to 20 MHz	174.6	35

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B.2 Clock Output Phase Noise Measurements

The LMK04208 features programmable LVDS, LVPECL, and LVCMOS output modes. Below is a phase noise measurement of CLKout0 for LVPECL and CLKout4 for LVDS and LVCMOS outputs. When measured single ended (SE) the unmeasured output is terminated using a 50-Ω termination. Balun measurements are made using the Prodyn BIB-100G balun. Measurements are provided for 245.75 MHz and 2949.12 MHz. The default populated VG-4513CA-122.8800M-GFCT3 Epson VCXO is used for measurements. The note 240 ohm em refers to the emitter resistors of the AC coupled LVPECL output are 240 Ω.

B.2.1 CLKout 245.76 MHz

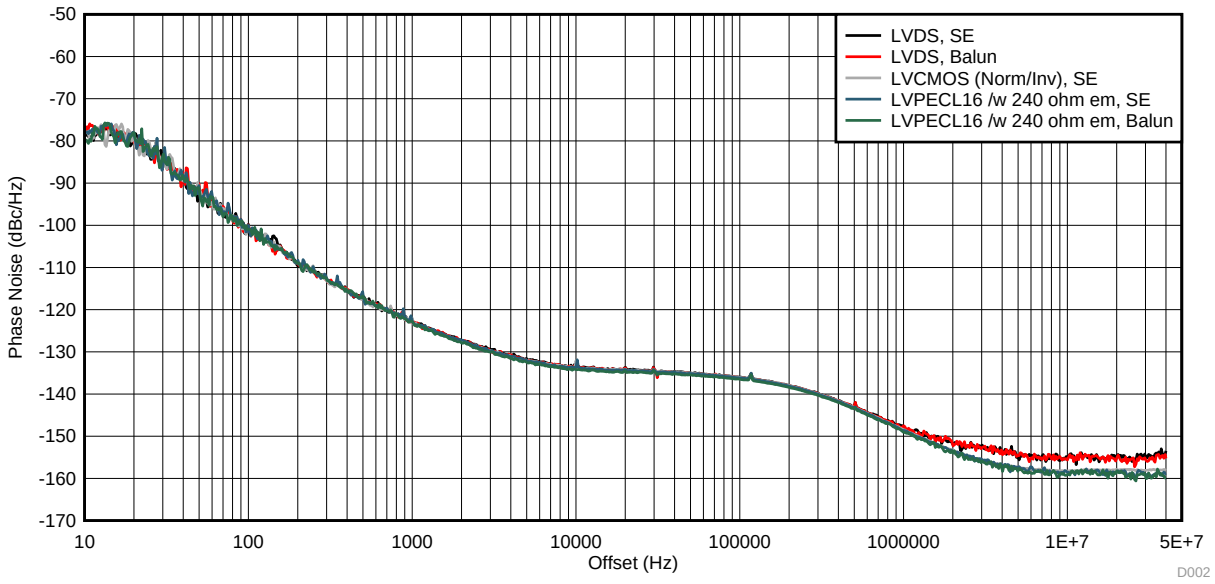

Figure 19. LMK04208 245.76 MHz, Divide-by-12

Table 10. 245.76 MHz Clock Output Phase Noise (dBc/Hz)

Offset	LVDS, SE	LVDS, Balun	LVCMOS (Norm/Inv), SE	LVPECL16 /w 240 ohm em, SE	LVPECL16 /w 240 ohm em, Balun
10 Hz	-78.3	-77.3	-77.2	-77.7	-79.1
100 Hz	-99.8	-99.9	-101	-100.0	-100.9
1 kHz	-122.7	-122.9	-122.0	-122.7	-122.8
10 kHz	-133.5	-133.6	-132.1	-133.7	-134.2
100 kHz	-136.0	-136.1	-136.0	-136.2	-136.5
1 MHz	-147.6	-147.5	-148.4	-148.7	-149.1
5 MHz	-155.0	-154.5	-157.4	-157.3	-158.0
10 MHz	-154.8	-155.6	-158.2	-158.6	-159.1
20 MHz	-155.1	-155.5	-157.9	-158.5	-158.5
40 MHz	-153.5	-155.2	-158.1	-158.8	-159.9

Table 11. 245.76 MHz Clock Output Jitter (fs RMS)

Offset	LVDS, SE	LVDS, Balun	LVCMOS (Norm/Inv), SE	LVPECL16 /w 240 ohm em, SE	LVPECL16 /w 240 ohm em, Balun
100 Hz to 20 MHz	139.3	136.5	126.3	125.5	121.7
12 kHz to 20 MHz	117.1	116.1	103.4	101.4	97.7

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B.2.2 CLKout 2949.12 MHz

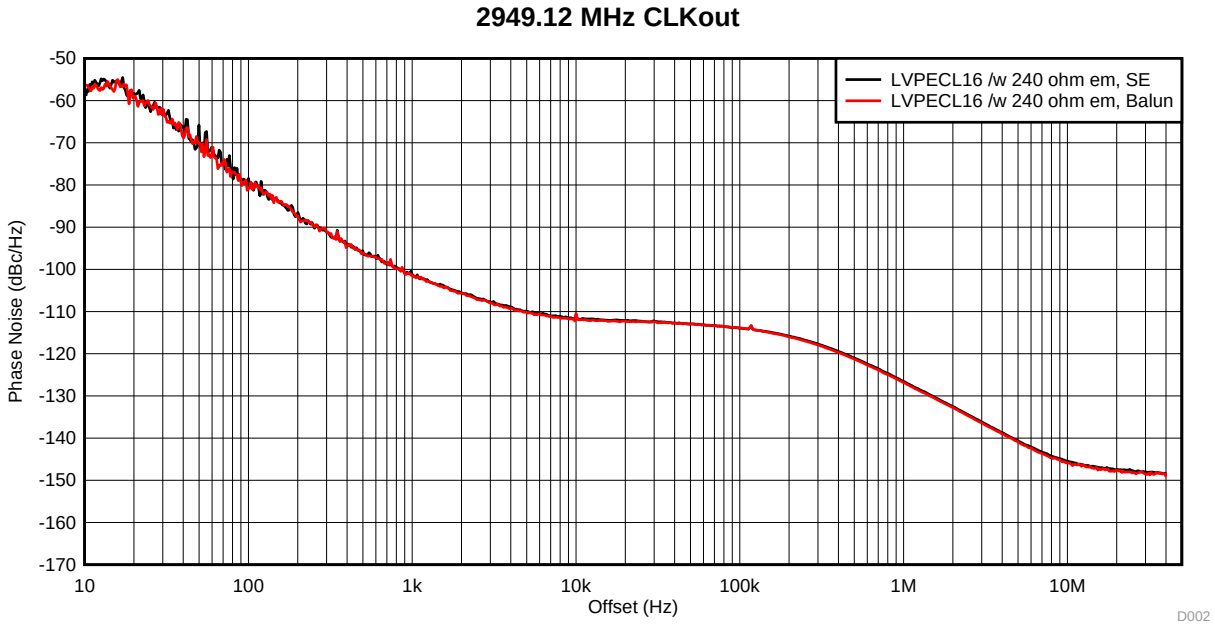

Figure 20. LMK04208, 2949.12 MHz, Divide-by-1

Table 12. 2949.12 MHz Clock Output Phase Noise (dBc/Hz)

Offset	LVPECL16 /w 240 ohm em, SE	LVPECL16 /w 240 ohm em, Balun
10 Hz	-58.4	-55.7
100 Hz	-78.4	-80.8
1 kHz	-101.2	-101.3
10 kHz	-110.8	-110.4
100 kHz	-114.0	-113.9
1 MHz	-126.6	-126.8
5 MHz	-140.7	-141.0
10 MHz	-145.4	-145.8
20 MHz	-147.4	-147.7
40 MHz	-148.5	-149.2

Table 13. 2949.12 MHz Clock Output Jitter (fs RMS)

Offset	LVPECL16 /w 240 ohm em, SE	LVPECL16 /w 240 ohm em, Balun
100 Hz to 20 MHz	122.7	121
12 kHz to 20 MHz	98.2	96.4

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3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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