Application Note

Combining More than Two Signals for Better Noise

Dean Banerjee

ABSTRACT

One approach to improving phase noise is to combine multiple signals. If two signals are combined, then there is a theoretical 3dB improvement in phase noise. However, in some situations, this makes sense to combine more than two signals not only for better noise, but better resistance to phase differences. This document explores combining more than two sources, combining circuits that can be used, theoretical benefits, and impact of phase error.

Table of Contents

Trademarks

1 Introduction

When phase noise performance is critical and one PLL synthesizer does not work, one approach is to combine multiple synthesizers. *Combining Two LMX2820 Synthesizer Outputs for Improved Phase Noise* gives an good analysis of combining two signals for better phase noise and demonstrates the theoretical and measured 3dB benefit as well as shows the impact if the signals are not in phase. Also, combining N synthesizers can yield a 10×log(N) theoretical benefit, but there are questions of how to buffer or split the input signal, how to combine multiple outputs, and how much phase error is tolerable (for more than two devices).

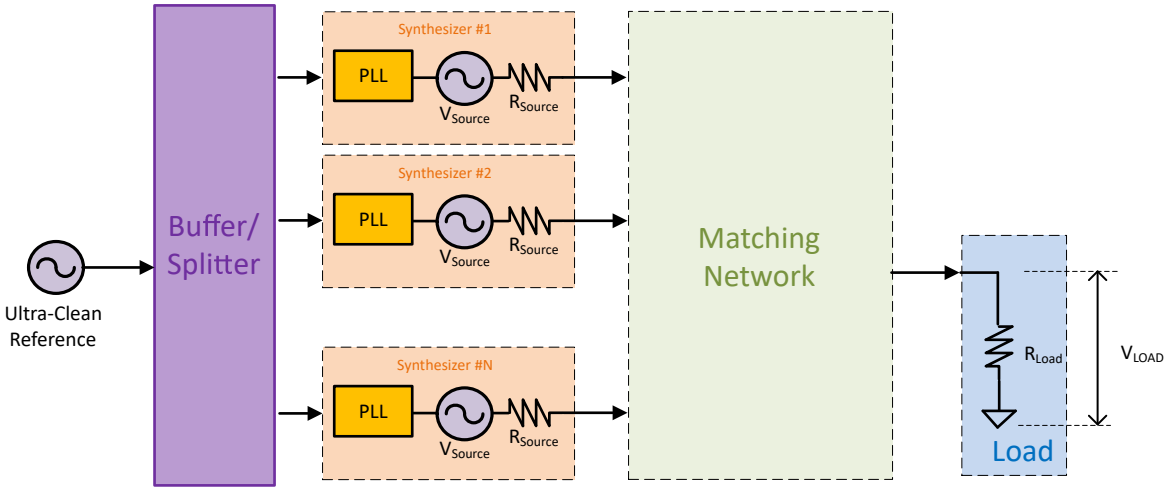

Figure 1-1. General Method of Combining N Frequency Synthesizers

Figure 1-1 shows the general method of combing multiple synthesizers for better phase noise. The assumption is that one starts with one ultra-clean source that is lower phase noise than the synthesizes and buffers. For the purpose of this article, the assumption is to be noiseless. Forward from this reference, there is a need to distribute this reference to the synthesizers, and combing the synthesizers to a single output to the load. There are considerations of noise, skew, and matching that are discussed in this article. Especially at higher frequencies, there is importance in knowing how much phase error is tolerable and how this varies with the number of synthesizers. Although calibration routines and programmable delays can adjust the phases, these require calibration and can add noise.

2 Creating Multiple Copies of the Input Signal

2.1 Skew and Slew Rate Considerations

Any skew introduced by the buffering can add to whatever skew is introduced by the differences in propagation delays of the synthesizers. The impact of the total skew is discussed later, but from a high level is desirable to be much less than that from the synthesizer. For many PLLs, the phase noise is dependent on the slew rate and if the slew rate is not sufficient, then the PLL phase noise can be degraded.

2.2 Buffers vs. Resistive Splitters

The resistive splitter potentially offers tighter skew and also does not add phase noise. However, the problem is that if there are too many synthesizers to drive, this can degrade the slew rate and thus the PLL noise. The buffer is a good design for the slew rate, but this can introduce skew and also the buffer noise can go to the output. The treatment of the buffer noise is tricky. The noise from the input to the buffer is common to all sources and therefore goes straight to the output. The noise from different outputs of the same buffer is uncorrelated, which means that this phase noise is reduced. Buffer data sheets typically do not separate the noise into that due from the input and that from the output, but if we assume that they are equal, then this can mean that we can assume that the input buffer is 3dB better than the total noise floor as well as the output buffer being 3dB better than the total noise floor.

2.3 Phase Noise Considerations With Buffers

Assuming a noiseless input source, we want the buffer noise to be lower than that of the PLL. For the PLL, this noise gets reduced when multiple synthesizers are combined together. For the buffer, only the output state noise gets reduced by the combining, but the input stage goes straight to the output. Table 2-1 shows an analysis with just one source to show the challenge of finding a buffer with adequate phase noise.

Table 2-1. Buffer Phase Noise Comparison

Frequency	LMX2820 PLL	LMK12C104 Buffer	LMK12D104 Buffer	LMX1204 Buffer
Skew	Prop. Delay Variation: 60ps (typ)	Output-Output Skew: 50ps (max)	Output-Output Skew: 20ps (max)	Output-Output Skew: 1ps (typ) 15ps (max)
10MHz	-166	-170	-163.0	x
50MHz	-159	-170	-162.7	x
100MHz	-156	-170	-161.6	x
250MHz	-152	-168	-160.2	x
500MHz	-146	x	-159.1	-161
1GHz	-143	x	-158.1	-161

The PLL noise floor can be calculated by taking the PLL figure of merit and adding $10\times\log(f_{PD})$. f_{PD} is the phase detector frequency, which is equal to the input frequency, provided the phase detector goes that high. If not, then this is degraded. For Table 2-1, a PLL figure of merit of -236dBc/Hz was assumed and the maximum phase detector frequency is 400MHz, so this is why the phase noise degrades at a faster rate after 250MHz. There is also the 1/f noise of the PLL that needs to be compared to that of the buffer. Keep in mind that this is for a single synthesizer, combining the synthesizers makes the noise requirement more stringent for the buffer.

3 Considerations with Combining Outputs

3.1 Isolation Between Sources

Multiple sources that are connected together and running at the same frequency have a tendency to fight each other. The amount of isolation depends on the device, but adding more resistance, buffering, or using off the shelf combiners can help with this. One way to think of isolation is the voltage that source A can develop across the source output impedance of source B.

The approaches here use inductor or resistive networks for matching but if there are issues in some systems that require more matching, then an off the shelf combiner can be used. However, this increases cost and size and also can put restrictions on what number of synthesizers to combine.

3.2 Single-Ended vs. Differential Outputs

In most cases, this is much easier to combine single ended signals than differential signals, the assumption is that the signals are single ended. If the device outputs a differential signal, this can be converted with a balun, or just one side can be used and the complimentary side disregarded

3.3 Losses Due to Combining

When the process of combining signals introduces the same amount of loss to both the desired signal and noise, then this does not impact the phase noise. For instance, a resistive pad can decrease the signal and noise by both 6dB, but this does not degrade the phase noise. As multiple signals are being combined, this is acceptable to have some loss as there can also be gain due to the increased number of synthesizers.

However, if signal power is lost due phase misalignment, this can decrease the power of the desired signal, but not decrease the power of the noise. So in this case, this can result in a degradation in phase noise.

4 Resistive Method for Combining Multiple Signals

4.1 General Case Where Source Output Impedance can be Different Than Load Impedance

Figure 4-1 shows a general approach of combining multiple sources to drive a single load. The assumption is that all the sources are the same amplitude and output impedance and the output impedance of a single source is equal to the load.

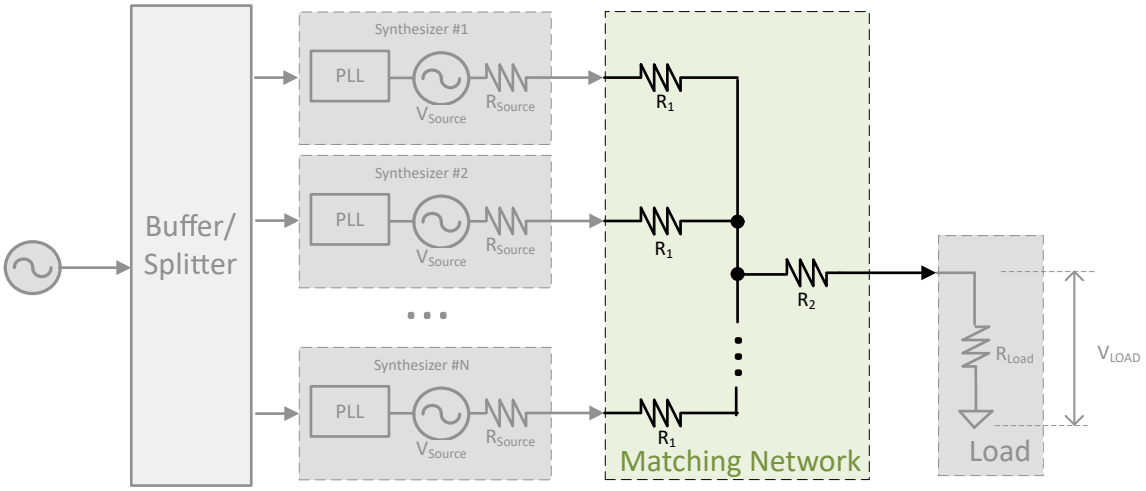

Figure 4-1. General Resistive Matching Network

The value of the matching resistor can be calculated as follows (*Appendix A*):

$$R_1 = R_{Source} \times \left(\frac{2 \times R_{Load} \times N \times (N-1)}{N^2 \times R_{Load} - R_{Source}} - 1 \right) \quad (1)$$

$$R_2 = R_{Load} \times \left(1 - \frac{2 \times R_{Source} \times (N-1)}{N^2 \times R_{Load} - R_{Source}} \right) \quad (2)$$

This matching is possible provided that:

$$\frac{R_{Load}}{R_{Source}} \geq \frac{2 \times N - 1}{N^2} \quad (3)$$

For the purpose of analysis, a useful quantity to know the equivalent resistance of the load in parallel with N-1 sources.

$$R_{eq} = \frac{(R_1 + R_{Source}) \times (R_2 + R_{Load})}{R_1 + R_{Source} + (N-1) \times (R_2 + R_{Load})} \quad (4)$$

From this the relative power can be calculated.

$$P_{Relative} = 20 \times log \left[\frac{N \times R_{eq} \times (R_{Load} + R_{Source})}{(R_{eq} + R_{Load} + R_{Source}) \times (R_2 + R_{Load})} \right] \quad (5)$$

The isolation between source A and source B can be defined as the voltage that source A produces across the source impedance of source B. This can be expressed in dB.

$$Isolation = 20 \times log \left[\frac{R_{Source} \times R_{eq}}{(R_{eq} + R_1 + R_{Source}) \times (R_1 + R_{Source})} \right] \quad (6)$$

4.2 Special Case Where Source and Load Impedance are the Same

If the source and load resistances are the same, then Equation 1, Equation 2, and simplify to:

$$R_1 = R_2 = R_{Match} = R_{Source} \times \frac{N-1}{N+1} \quad (7)$$

$$P_{Relaive} = 0 \quad (8)$$

In the case that there are two sources, Figure 4-2 shows a common way that this can be combined.

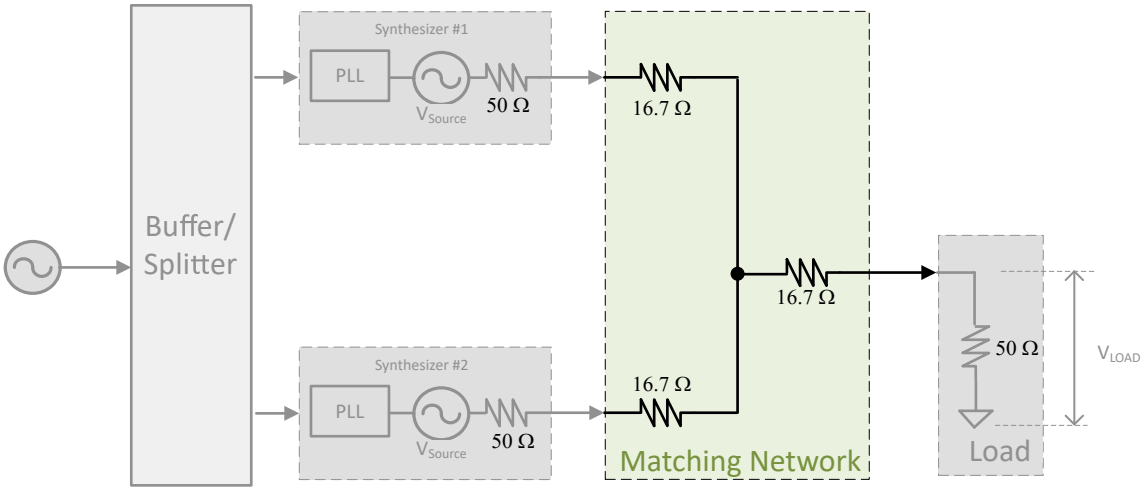

Figure 4-2. Combination of Two 50Ω Sources

Three sources can be combined as well in this manner.

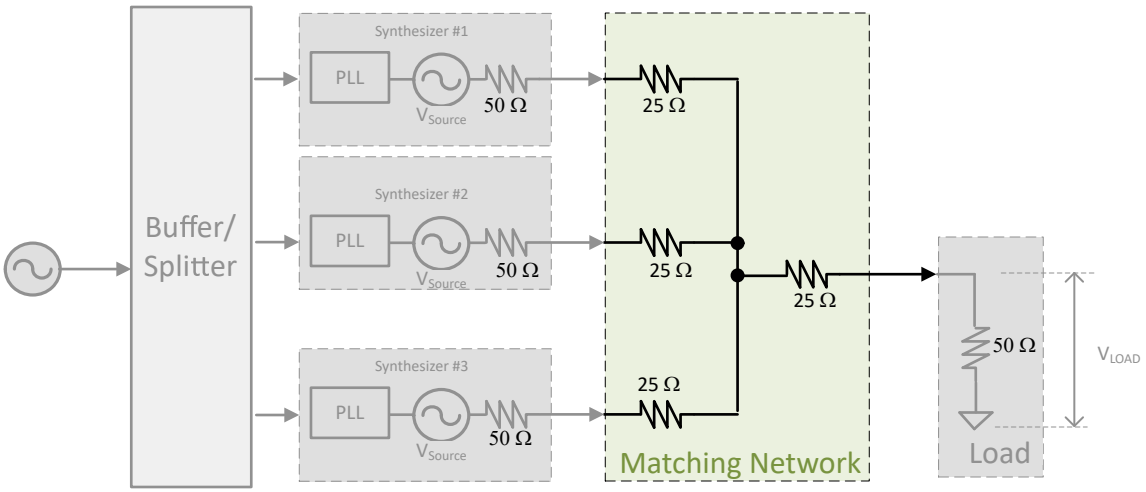

Figure 4-3. Combination of Three 50Ω Sources

4.3 Increasing R1 to Improve Isolation

To improve isolation, one approach is to visualize adding a series resistance, R_{ISO} to each source and then do calculations as before, but use an increased source resistance of (R_{Source}+R_{ISO}) . The extreme case is to to make the maximum choice for R_{ISO} that satisfies Equation 3.

$$R_{ISO} = \frac{N^2}{2 \times N - 1} \times R_{Load} - R_{Source} \quad (9)$$

When this choice is made, the other components can be solved for:

$$R_1 = N \times R_{Load} - R_{Source} \quad (10)$$

$$R_2 = 0 \quad (11)$$

In the case that the source and load impedance are the same, this choice yields very similar power or perhaps a fraction of a dB higher. The concern can be though that the trace impedance needs to be matched to something much different than 50Ω. In Figure 4-4, the trace needs to technically be 66.7Ω between these resistances. Figure 4-5. In this case, the calculated power is about 0.7dB lower, but the isolation between sources is improved by about 8dB.

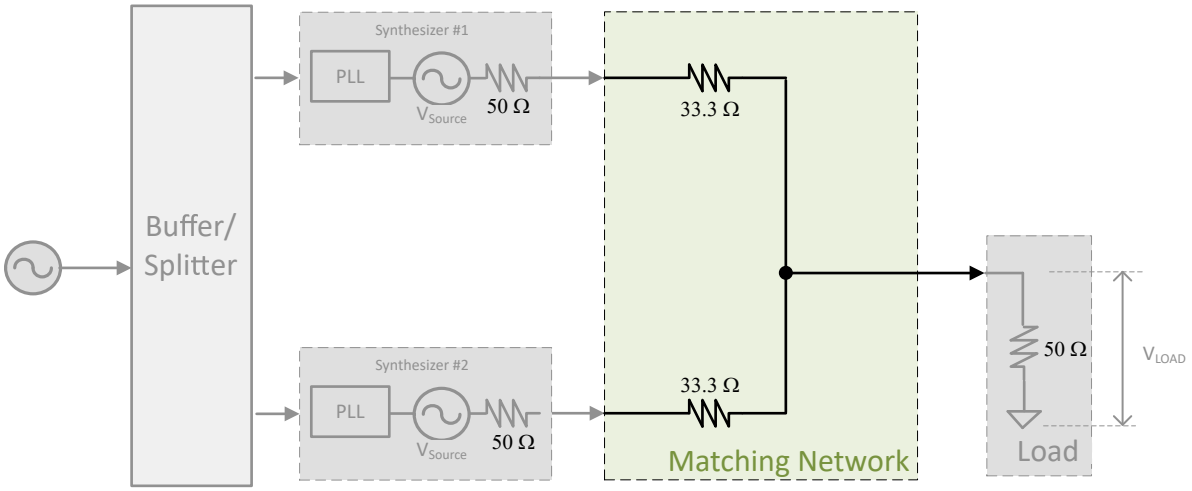

Figure 4-4. Combination of Two Sources With Added Isolation

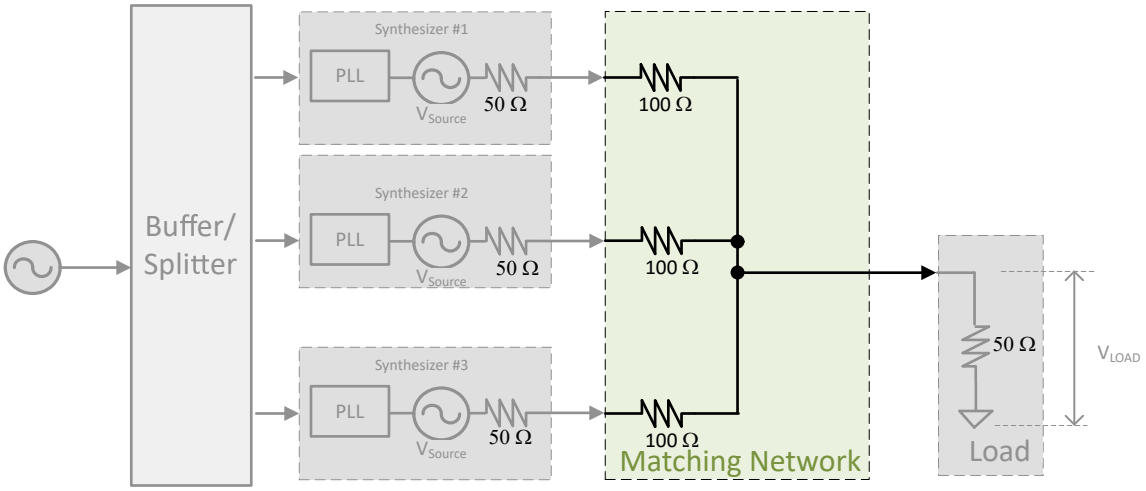

Figure 4-5. Combination of Three Sources With Added Isolation

For the case of three sources, adding the isolation resistance theoretically delivers the exact same power, but improves isolation by 10dB. However, matching of trace impedance is something to take into consideration as this has changed the matching far from a 50Ω system.

5 Impedance Matching With Reactive Circuit

The resistive matching circuit is simple and provides a good match. However, the circuit sacrifices output power. By using an inductor and capacitor, a match can be provided that gives theoretically 6dB higher output power. However, at high frequencies, one needs to be aware of non-designed for behaviors of inductors and capacitors.

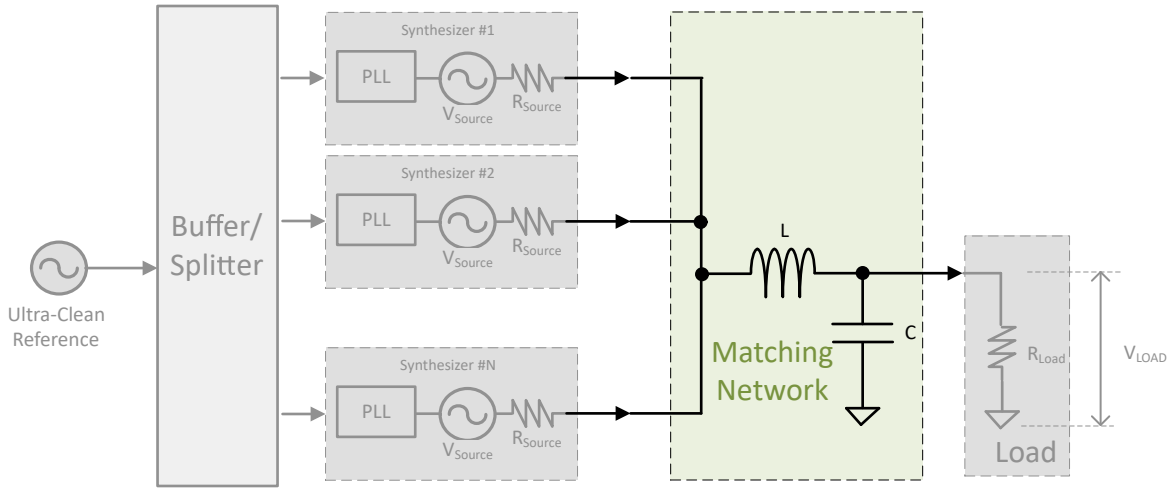

Figure 5-1. Reactive Matching Circuit

The value of L and C can be calculated (*Appendix B*) as follows:

$$L = \frac{j \times \frac{Q \times R_{Source}}{N}}{2\pi \times f \times j} = \frac{R_{Source} \times Q}{2\pi \times f \times N} \quad (12)$$

$$C = \frac{-j}{2\pi \times f \times X_C} = \frac{Q}{R_{Load} \times 2\pi \times f} \quad (13)$$

These work provided the following restriction is satisfied.

$$\frac{R_{Source}}{N} < R_{Load} \quad (14)$$

Directly shorting the outputs together can create some concerns about isolation between the sources. To alleviate this concern, one can add a series resistance and recalculate R_{Source} including this resistance. However, this approach does sacrifice some power.

6 Loss Due to Phase Error

Phase between the signals results in loss of power. Appendix C shows that the worst case combination of N signals with a worst case phase error ϕ that is limited to less than 180 degrees is:

$$Loss = \begin{cases} 10 \times log\left[\frac{1+\cos\phi}{2}\right] & N\ even \\ 10 \times log\left[\frac{1}{n^2} + \left(1 - \frac{1}{n^2}\right)\left(\frac{1+cos(\phi)}{2}\right)\right] & N\ odd \end{cases} \quad (15)$$

From this, the observation is that an odd number of signals has higher resistance to phase error.

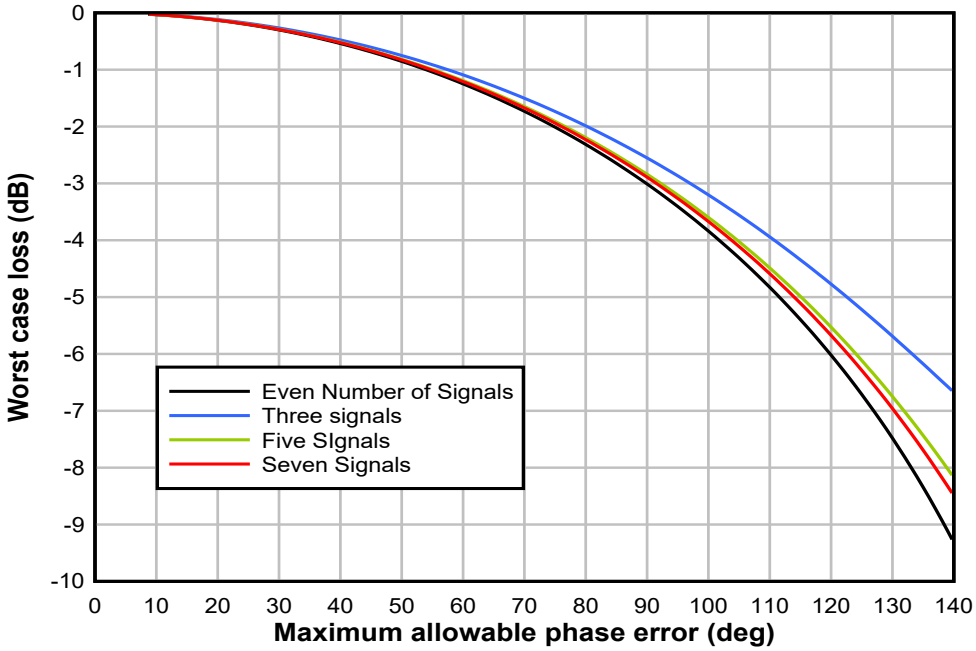

Figure 6-1. Loss Due to Phase Error

7 Phase Noise Improvement by Combining Multiple Signals

7.1 Theoretical Improvement for Multiple Signals Designed for in Phase

Consider first the case of combining two synthesizers that are designed for in phase and the same amplitude. In this case, the voltage can double, increasing the output power by 6dB. However, the noise of these two synthesizers is not correlated, so that the noise power increases only 3dB. This leads to a theoretical improvement in phase noise is 3dB. Even if there are losses in the combining, such as in the case of a resistive circuit, this applies to the output power and noise power equally, so the phase noise improvement is still 3dB. One consideration is that the input reference clock needs to be sufficiently clean. As the noise of this reference clock is common to both synthesizers, this actually increases 6dB with the noise power. Also, this method improves the noise due to the synthesizer, but not the reference clock. To generalize this result, when N signals in phase are combined, the theoretical improvement in phase noise is 10×log(N)

7.2 Combining Multiple Signals With a Phase Error

When a phase error is present, this decreases the signal power, but not the noise power. If this is added to the theoretical noise improvement, then the result for phase noise improvement accounting for phase error can be found..

$$L(n) = \begin{cases} 10 \times log(n) + 10 \times log\left(\frac{1+cos(\phi)}{2}\right) & n\ even \\ 10 \times log(n) + 10 \times log\left[\frac{1}{n^2} + \left(1 - \frac{1}{n^2}\right)\left(\frac{1+cos(\phi)}{2}\right)\right] & n\ odd \end{cases} \quad (16)$$

Figure 7-1 shows the improvement for combining multiple signals. Note that the combination of an odd number of synthesizers, especially three, seems to give a higher immunity to larger phase errors.

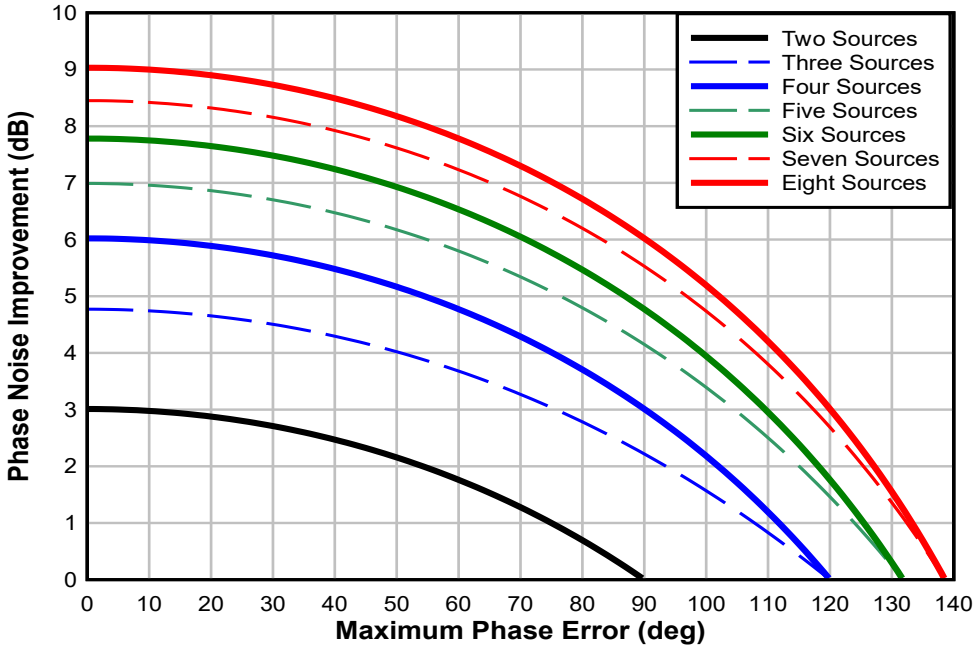

Figure 7-1. Phase Noise Improvement for Combining Multiple Signals

8 Summary

Combining multiple signal sources to get better phase noise is a valid approach to use when there is room to allow for increased cost, board area, and power. Although two sources are often used, this process can be scaled to a larger number of sources as well.

9 References

1. Texas Instruments, *Combining Two LMX2820 Synthesizer Outputs for Improved Phase Noise* , application note.
2. Texas Instruments, *Multiple PLL Combination Reference Design for <40-fs Jitter (100-Hz to 100-MHz)*. design guide.

A Appendix: Calculations for Resistive Matching Network

The two key constraints are:

1. Impedance as seen looking out from the load is equal to the load impedance
2. Impedance as seen looking out from any source is equal to that source output impedance

To simplify this, first introduce these two variables, x and y.

$$x = R_1 + R_{Source} \tag{17}$$

$$y = R_2 + R_{Load} \tag{18}$$

Now realizing that the combination of N things in parallel has an impedance that is equal to the original impedance divided by N and using the above two definitions yields the following key equations:

$$R_{Load} = R_2 + \frac{x}{N} \tag{19}$$

$$R_{Source} = R_1 + \left(\frac{x}{N-1}\right) \left|\right| (y) = R_1 + \frac{x \times y}{x + (n-1) \times y} \tag{20}$$

These equations can be rearranged as follows:

$$\frac{x}{N} + y = 2 \times R_{Load} \tag{21}$$

$$\frac{x \times y}{x + (n-1) \times y} + x = 2 \times R_{Source} \tag{22}$$

Equation Equation 22 can be simplified to

$$2 \times N \times R_{Load} \times x = 2 \times R_{Source} \times (2 \times N \times R_{Load} - y) \tag{23}$$

Equations Equation 21 and Equation 23 can be combined to get

$$x = \frac{2 \times R_{Source} \times R_{Load} \times N \times (N-1)}{N^2 \times R_{Load} - R_{Source}} \tag{24}$$

Equations (11), (12), (18), and (19) can be combined to get the values for R1 and R2

$$R1 = R_{Source} \times \left(\frac{2 \times R_{Load} \times N \times (N-1)}{N^2 \times R_{Load} - R_{Source}} - 1\right) \tag{25}$$

$$R2 = R_{Load} \times \left(1 - \frac{2 \times R_{Source} \times (N-1)}{N^2 \times R_{Load} - R_{Source}}\right) \tag{26}$$

By setting the following condition, this can make sure that R2 >=0, which also makes sure R1 >=0

$$\frac{R_{Load}}{R_{Source}} = \frac{2 \times N - 1}{N^2} \tag{27}$$

In many cases, the sources and load impedance are the same. In such cases, equations Equation 25 and Equation 26 simplify to:

$$R_1 = R_2 = R_{Match} \times \left(\frac{N-1}{N+1}\right) \tag{28}$$

B Appendix: Calculations for Reactive Matching Network

Introduce the following terms:

$$X_L = 2\pi \times f \times j \times L \tag{29}$$

$$X_C = -j \times \frac{1}{2\pi \times f \times C} \tag{30}$$

$$z = X_L + \frac{R_{Source}}{N} \tag{31}$$

The impedance as looking into and out of the load needs to be the same.

$$R_{Load} = z \left|\right| X_C = \frac{z \times X_C}{z + X_C} \tag{32}$$

This equation can be rearranged as:

$$z = \frac{X_C \times R_{Load}}{X_C - R_{Load}} \tag{33}$$

The impedance as looking out from inductor needs to be equal to the impedance looking in

$$2 \times \frac{R_{Source}}{N} = z + R_{Load} \left|\right| X_C = z + \frac{R_{Load} \times X_C}{R_{Load} + X_C} \tag{34}$$

Combine these equations to get

$$2 \times \frac{R_{Source}}{N} = \frac{R_{Load} \times X_C}{X_C - R_{Load}} + \frac{R_L \times X_C}{X_C + R_{Load}} = \frac{2 \times R_{Load} \times {X_C}^2}{{X_C}^2 - {R_{Load}}^2} \tag{35}$$

Defile the following term:

$$Q = \sqrt{\frac{N \times R_{Load}}{R_S} - 1} \tag{36}$$

Being very careful to get the correct root and get the correct branch. For example, realize that these equations can be combined as

$$\text{i.e. } \sqrt{\frac{1}{-1}} = -j \neq j \tag{37}$$

Keeping this in mind, these equations can be combined as

$$X_C = -j \times \frac{R_{Load}}{\sqrt{\frac{N \times R_{Load}}{R_S} - 1}} = -j \times \frac{R_{Load}}{Q} \tag{38}$$

Substituting this back into the values for x and y yield:

$$\frac{\left(-j \times \frac{R_{Load}}{Q}\right) \times R_{Load}}{\left(-j \times \frac{R_{Load}}{Q}\right) - R_{Load}} = X_{Load} + \frac{R_{Source}}{N} \tag{39}$$

This can be simplified to say:

$$X_L = \frac{\left(-j \times \frac{R_{Load}}{Q}\right) \times R_{Load}}{\left(-j \times \frac{R_{Load}}{Q}\right) - R_{Load}} - \frac{R_{Source}}{N} = \frac{j \times Q \times R_{Load} + R_{Load}}{Q^2 + 1} - \frac{R_{Source}}{N} = \frac{j \times Q \times R_{Load} + R_{Load}}{\frac{N \times R_{Load}}{R_{Source}}} - \frac{R_{Source}}{N} \quad (40)$$
$$= j \times \frac{Q \times R_{Source}}{N}$$

Finally, the values for the inductance and capacitance can be found:

$$L = \frac{j \times \frac{Q \times R_{Source}}{N}}{2\pi \times f \times j} = \frac{R_{Source} \times Q}{2\pi \times f \times N} \quad (41)$$

$$C = \frac{-j}{2\pi \times f \times X_C} = \frac{Q}{R_{Load} \times 2\pi \times f} \quad (42)$$

C Appendix: Calculation of Loss Due to Phase Error

Start by thinking about adding two vectors of equal magnitude. The first vector is at angle of zero degrees and the second is at angle of ϕ. The vector is therefore:

<1+cos ϕ, sin ϕ>

The magnitude can be calculated to be:

$$\|\langle 1+cos\,\phi,\ sin\,\phi\rangle\| = \sqrt{(1+cos\,\phi)^2+(sin\,\phi)^2} = 2\times\sqrt{1+cos\,\phi} \tag{43}$$

If not intuitive that the angle of the resultant vector is, then this becomes more apparent by recognizing the angle as calculated by this vector relates to the half angle formula for tangent.

$$tan\,\frac{\phi}{2} = \frac{sin\,\phi}{1+cos\,\phi} \tag{44}$$

Furthermore, this needs to be intuitive that if one combines an even number of vectors, the angle does not change and the magnitude can be:

$$\frac{N}{2}\times 2\times\sqrt{1+cos\,\phi} = N\times\sqrt{1+cos\,\phi} \tag{45}$$

If there is an odd number of vectors, then add all but the last one and this formula is known. Clearly if the last vector was at angle f/2, then this can give the most power, so without loss of generality, this can be at zero degrees for the worst case. So in the case of an odd number of vectors, the magnitude can be:

$$\left\|\left\langle 1+\frac{N-1}{2}+\frac{N-1}{2}\times cos\,\phi,\frac{N-1}{2}\times sin\,\phi\right\rangle\right\| = \sqrt{\left(1+\frac{N-1}{2}+\frac{N-1}{2}\times cos\,\phi\right)^2+\left(\frac{N-1}{2}\times sin\,\phi\right)^2} \tag{46}$$
$$=\sqrt{\frac{N^2+1}{2}+\frac{N^2-1}{2}\times cos\,\phi}$$

Of interest is the loss in power compared to the designed for combination of N signals and this can be calculated as:

$$Loss = \begin{cases} 10\times log\left[\frac{1+cos\,\phi}{2}\right] & N\ even \\ 10\times log\left[\frac{1}{n^2}+\left(1-\frac{1}{n^2}\right)\left(\frac{1+cos(\phi)}{2}\right)\right] & N\ odd \end{cases} \tag{47}$$

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