Application Note

Termination Guidelines for Differential and Single-Ended Signals

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ABSTRACT

Output signals must be terminated to generate a toggling voltage signal that has a particular voltage swing and DC bias. When properly terminated, the transmission line (trace) impedance is maintained. Impedance matching is necessary to prevent reflections, overshoot, undershoot, and ringing at the outputs. Care must be taken with the PCB layout design as the trace width, trace gap, and stack-up all contribute to the trace impedance. This application note describes the general guidelines and steps required to terminate differential and single-ended signals. Layout techiniques are not covered in this application note.

Table of Contents

List of Figures

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1 Introduction

Table 1-1 lists the definition for each abbreviation and/or key terminology used in the document.

Table 1-1. Terminology Used Throughout Application Note

TERM	DEFINITION
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVDS	Low Voltage Differential Signaling
HCSL	High Speed Current Steering Logic
LP-HCSL	Low Power High Speed Current Steering Logic
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
P and N	Complimentary pair of a differential signal. P is the non-inverted signal and N is the inverted signal.
Single-ended	One input or output signal (such as LVCMOS)
Differential	A pair of "P" and "N" input or output signals (such as LVPECL)
PCB	Printed circuit board
Z_O	Transmission line impedance, characteristic impedance, PCB trace impedance(1)
VCM	Common-mode voltage, where VCM = (P + N) /2, the average of the P and N signal
VIH	Input high voltage level
VIL	Input low voltage level
VOH	Ouput high voltage level
VOL	Output low voltage level
VID	Single-ended input voltage swing level (amplitude), where VID = VIH − VIL
VOD	Single-ended output voltage swing level (amplitude), where VOD = VOH −VOL
V_{PP}	Differential peak-to-peak voltage, where V_{PP} = 2 × VID or 2 × VOD
VDD or V_{CC}	Supply voltage
IBIS	Input/Output Buffer Information Specification

(1) This application note uses the impedance value of 50-ohms for single-ended traces and 100-ohms for differential in the examples.

2 General Termination Guidelines

The steps to properly terminate a signal can be broken into three sequential sections:

1. Identify the Driver and Receiver Requirements
2. Determine the Termination Type
3. Review the recommended termination for a Differential or Single-Ended signal

2.1 Identify the Driver and Receiver Requirements

The first step is to gather the details listed in Table 2-1 for both the clock driver and the receiver. Each signal type has a voltage swing, common-mode voltage (for differential), and trace impedance requirement. Each signal type can vary across product family and vendor. Therefore, read the *Electrical Characteristics* table for every clock driver and receiver data sheet prior to starting the design.

Table 2-1. Termination Requirements for Single-Ended and Differential Signals

PARAMETER	PURPOSE OF KNOWING	EXAMPLES(1)
Signal type	To know what termination to use for the driver and receiver	• LVPECL • LVDS • HCSL • LVCMOS
Voltage swing	To meet receiver requirements	• VID • VOD • V_{PP}
Common-mode voltage (differential signals only)	To meet receiver requirements(2)	• VCM • V_{ICM} (input VCM) • V_{OCM} (output VCM)
Impedance	To maintain signal integrity and minimize reflections, overshoot, undershoot, and ringing	• Z_O = 50Ω, single-ended • Z_O = 100Ω, differential

(1) Common examples used to define and refer to the parameter in the industry.
(2) Receivers must be presented with a signal that is biased to the specified DC bias level (common-mode voltage) for proper operation. Some receivers have a self-biasing input feature that enables automatic biasing. See the device data sheet to confirm the requirements.

2.2 Determine the Coupling Type

After identifying the signal requirements, the next step is to identify the coupling type. Refer to the DC-coupled and AC-coupled sections to determine which coupling type to use.

2.2.1 DC-Coupled Signal

Outputs are typically DC-coupled in the following cases:

- The receiver data sheet specifies a DC-coupled input signal.
- The common-mode voltage and voltage swing of the driver match the receiver input specifications.
  - No need for AC-coupling capacitors.
- The outputs are low frequency, such as 1PPS.
  - Signal distortion and/or attenuaton can occur with low frequency signal that pass through an AC-coupling capacitor. The degraded signal can violate the receiver input specification.
- The outputs are SYSREF operating in pulser (one-shot) mode.
  - Signal distortion and/or attenuaton can occur with a pulsed signal that passes through an AC-coupling capacitor. The degraded signal can violate the receiver input specification.
- Fast rise times are of high importance.
  - Rise times are reduced when AC-coupling capacitors are introuced in the signal path.

DC-coupled outputs can be terminated on either the driver or receiver side. High speed differential signals (such as LVDS) are load terminated which means termination is typically near the receiver. However, termination placement generally does not matter as long as the impedance of the signal matches the transmission line impedance.

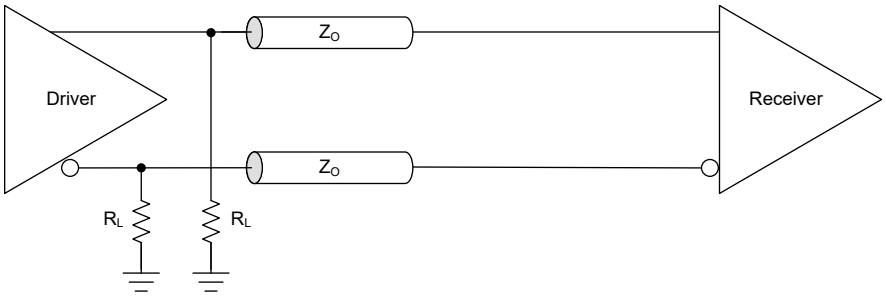

Figure 2-1. Example of DC-Coupled Termination on the Driver Side

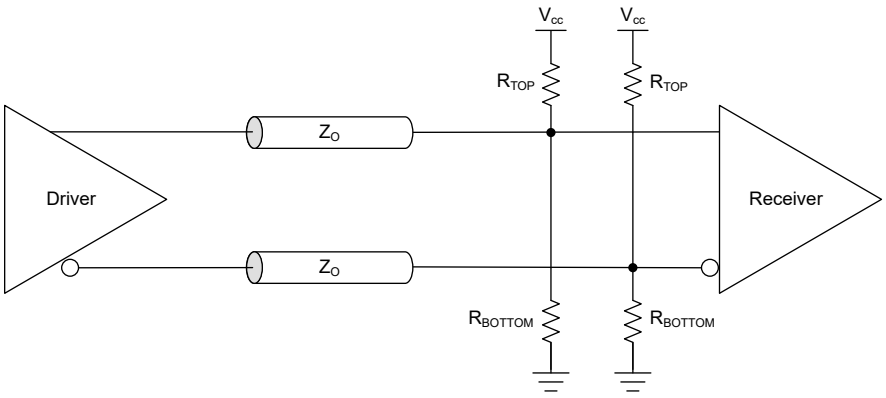

Figure 2-2. Example of DC-Coupled Termination on the Receiver Side

2.2.2 AC-Coupled Signal

Outputs are typically AC-coupled in the following cases:

- The receiver data sheet specifies an AC-coupled input signal.
  - In this case, the receiver has an internal DC biasing network that must be used. The external AC-coupling capacitor placed in series with the input signal "clears" or separates the DC bias from the driver to avoid conflict with the internal bias from the receiver.
- The common-mode voltage of the driver does not match the receiver input specifications.
  - AC-coupling capacitors must be used to reconfigure the DC bias. Use an external or internal biasing network.

AC-coupled outputs can require termination on both the driver and receiver side depending on the signal type. The termination structure is broken down into three steps as illustrated and explained in Figure 2-3.

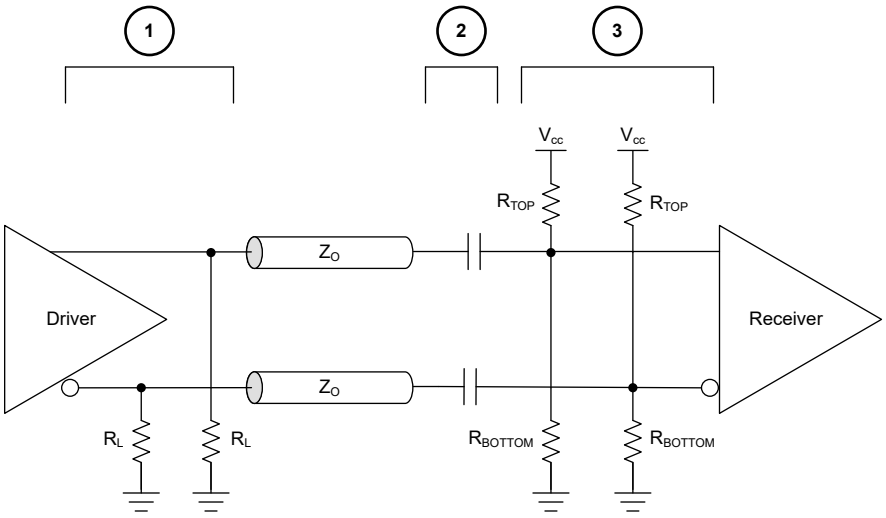

Figure 2-3. Example of AC-Coupled Termination Using Three Steps

1. Terminate on the driver side if the driver requires a DC return path to ground. This step is optional if the receiver is internally terminated and biased.
2. Add AC-coupling capacitors (typically 0.1uF) after the driver termination and before the receiver termination to shift (or "clear") the DC bias from one level to another. The AC-coupling capacitor isolates the DC offset in the signal allowing only the AC signal to pass through.
3. Terminate on the receiver side to reconfigure the common-mode voltage to the receiver specification. This step is optional if the receiver is internally terminated and biased.

3 Differential

A differential signal consists of a complementary pair of toggling voltages across two wires. If the driver common-mode voltage does not match the receiver specification, see to Setting the Common-Mode Voltage (Thevenin Termination). See the following sections for guidance on terminating differential signals.

3.1 Setting the Common-Mode Voltage (Thevenin Termination)

When the driver VCM and the receiver VCM do not match, translation is required and the VCM must be reconfigured to meet the receiver specification. Use the *Thevenin* termination to adjust the common-mode voltage of differential outputs.

The Thevenin equivalent circuit consists of a resistor network, as shown in Figure 3-1. Impedance matching occurs when the two resistors are configured using Equation 1 and Equation 2. A signal with Thevenin termnation is less susceptible to signal degradation because the circuit can provide additional current and reduce the driver load. However, a Thevenin termination can increase the power consumption as a result. For power-sensitive designs, use a Y-bias termination instead.

$$Z_O = \frac{R_{TOP} \times R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \approx 50\Omega \quad (1)$$

$$V_{TERM} = V_{CC} \times \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad (2)$$

Where,

- Z_O is the characteristic impedance (such as 50Ω single-ended).
- R_{TOP} is the resistor pulled-up to the supply.
- R_{BOTTOM} is the resistor pulled-down to ground.
- V_{TERM} is the termination voltage (typically the common-mode voltage).
- V_{CC} is the supply voltage (such as 3.3V).

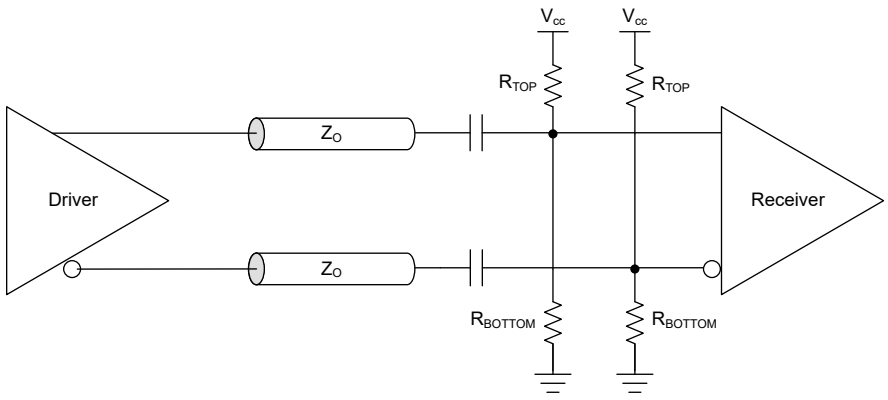

Figure 3-1. Thevenin Termination for AC-Coupled Outputs

3.2 LVPECL

3.2.1 DC-Coupled LVPECL

For DC-coupled LVPECL signals, proper output termination is required to fulfill three requirements: to provide a DC return path, to keep the impedance matched, and to maintain the common-mode voltage.

General Guidelines:

DC Return Path

LVPECL outputs are based on open-emitters as described in *Section 3.1.1 LVPECL Output Stage* of the SLLA120 application note. A current return path to ground (such as pull-down resistors) is required to complete the circuit from the output stage and get a signal at the outputs.

Common-Mode Voltage

The traditional LVPECL output stage has a VCM of V_{CC} – 1.3V, as listed in Table 3-1.

Table 3-1. Output VCM for Traditional LVPECL

V_{CC} [V]	OUTPUT VCM [V]
3.3	2
2.5	1.2\

Termination resistors (which are equal to the trace impedance) are pulled up to Vcc – 2V to produce an LVPECL output current of about 15mA. Keep the termination voltage less than the VCM of the LVPECL output driver to maintain the output driver stage in proper operation. More details on the LVPECL input and output stage design are found in the SLLA120 application note.

Impedance Matching

The transmission line impedance is impacted by the resistor network. If care is not taken to match the impedance and only the DC path is provided, then the outputs can experience significant overshoot, undershoot, and/or reflections. Use IBIS models to simulate the signal integrity through software such as HyperLynx. The following figures show IBIS simulations between an LVPECL driver and LVPECL receiver.

Figure 3-3 provides the oscilliscope simulated result when the output driver is better terminated. The DC return path is provided and impedance is matched.

Figure 3-2 provides the oscilloscope simulated result when the output driver is poorly terminated. The DC return path is provided but the impedance is mismatched.

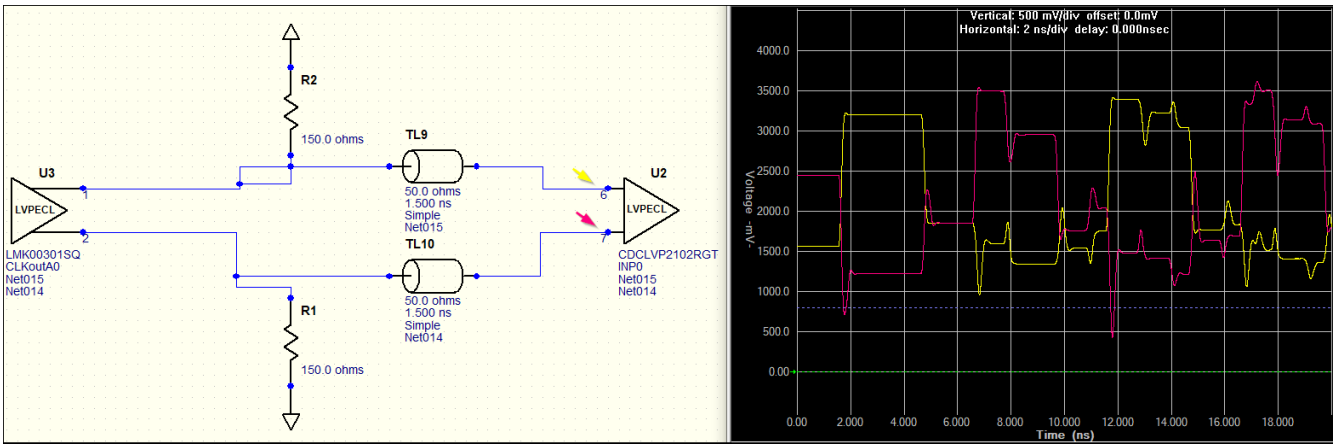

Figure 3-2. HyperLynx LVPECL Simulation with Poor Termination

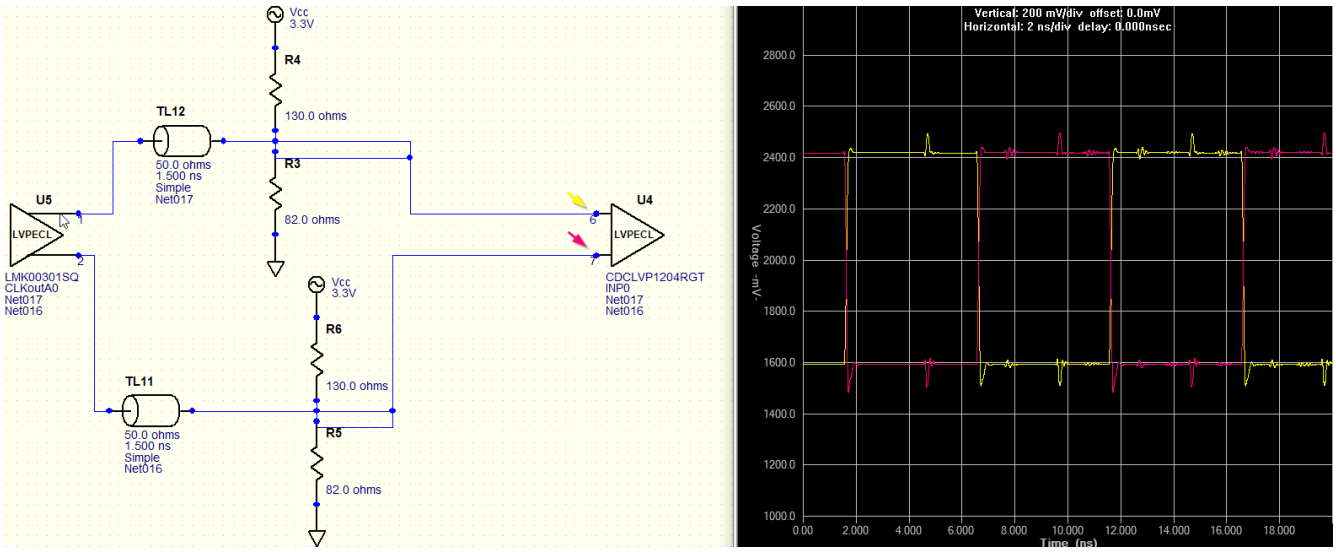

Figure 3-3. HyperLynx LVPECL Simulation with Better Termination

DC-Coupled LVPECL to LVPECL Using a Traditional Termination

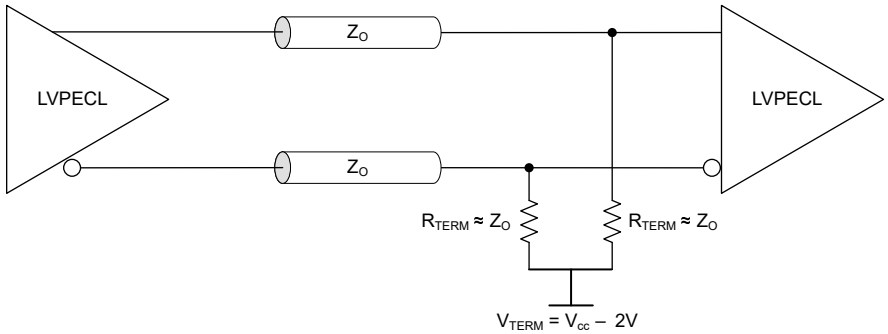

Figure 3-4. Traditional LVPECL Termination

DC-Coupled LVPECL to LVPECL Using a Thevenin Termination

When an external supply voltage of Vcc – 2V is not readily available, use a Thevenin termination instead. Use other resistor networks methods, such as π (PI) and Y-bias, to terminate without a supply voltage connection.

Example Termination

Configure the resistor network to have a bias voltage of VCC – 2V (to allow margin) and provide 50Ω impedance matching.

$$Z_O = \frac{R_{TOP} \times R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} = \frac{130\Omega \times 82\Omega}{130\Omega + 82\Omega} \approx 50\Omega \quad (3)$$

If R_{TOP} = 130Ω and R_{BOTTOM} = 82Ω, then:

$$V_{TERM} = V_{CC} \times \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} = \frac{3.3V \times 82\Omega}{130\Omega + 82\Omega} \approx 1.3V \quad (4)$$

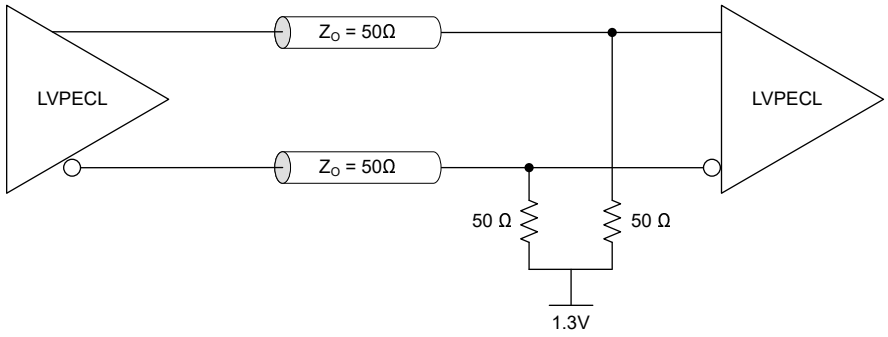

Figure 3-5. DC-Coupled LVPECL to LVPECL Using a Traditional Termination

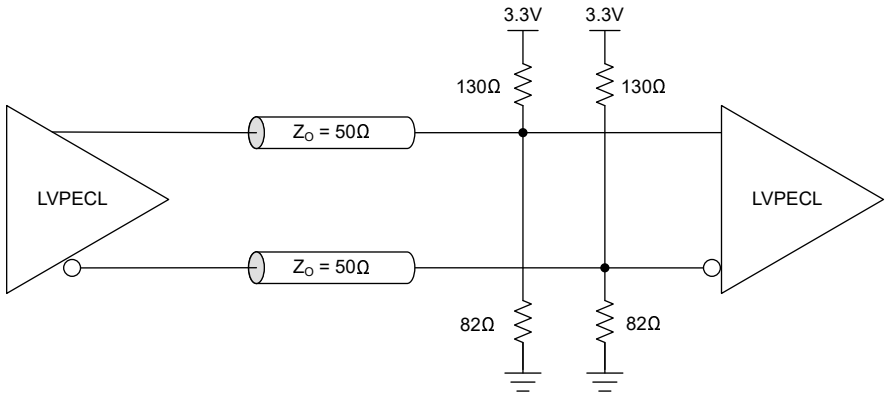

Figure 3-6. DC-Coupled LVPECL to LVPECL Using a Thevenin Termination

3.2.2 AC-Coupled LVPECL

Apply AC-coupling capacitors to the LVPECL output when interfacing with non-LVPECL receivers and/or to reconfigure the VCM.

Example Termination

For a traditional LVPECL driver, a DC return path is required. Place emitter resistors (140 to 220Ω, typically 150Ω) to ground on the driver side to maintain the current path. Then, add AC-coupling capacitors to separate the DC bias from the driver. Use a Thevenin termination to provide a new bias voltage that is less than V_{CC} – 1.3V. The bias voltage activates the gates of the emitter-follower pair from the LVPECL input stage. See *Section 3.1.2 Input Stage for Devices Using LVPECL Drivers* in*Interfacing Between LVPECL, VML, CML and LVDS Levels*.

AC-Coupled LVPECL to LVPECL

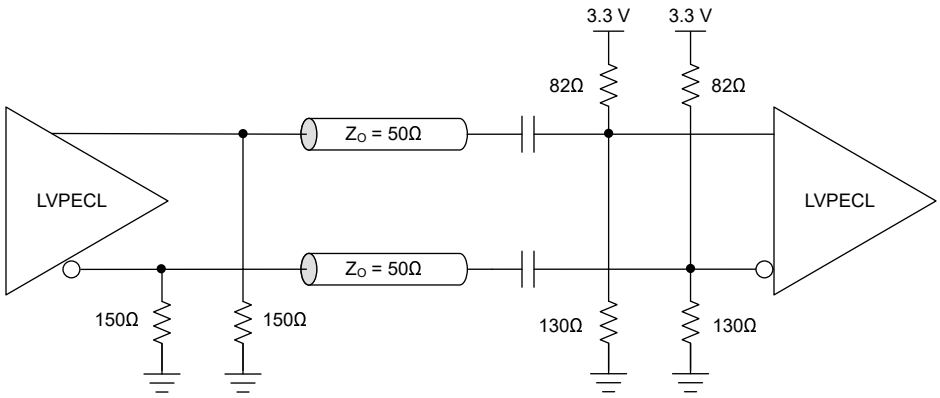

Figure 3-7. AC-Coupled LVPECL to LVPECL Using a Thevenin Termination

AC-Coupled *AC-LVPECL* to LVPECL

For *AC-LVPECL* type outputs (as seen in LMK05318B), termination before the AC-coupling capacitors is not required because the driver is internally biased and terminated. The capacitors can be placed on the receiver or driver side. Do not DC-couple the signal unless the output VCM meets the receiver specification.

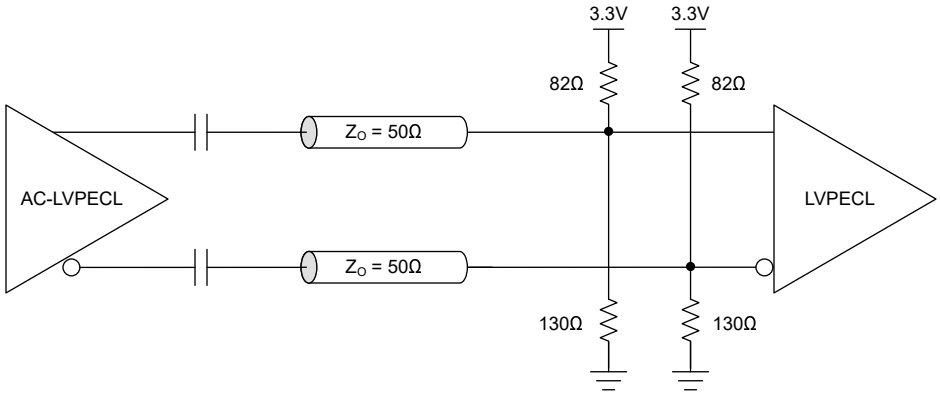

Figure 3-8. AC-Coupled *AC-LVPECL* to LVPECL Using a Thevenin Termination

3.3 LVDS

3.3.1 DC-Coupled LVDS

Traditional LVDS uses a current-mode driver to source 3.5mA and generate a toggling voltage across a differential termination. The signal seen by the receiver has a 350mV voltage swing (VOD) and 1.2V common-mode (VCM).

General Guidelines

- Terminate the LVDS driver with a differential resistor (typically 100Ω) across the output P and N signals.
- Place the differential resistor on the receiver side as close to the input pins as possible.

Example Termination

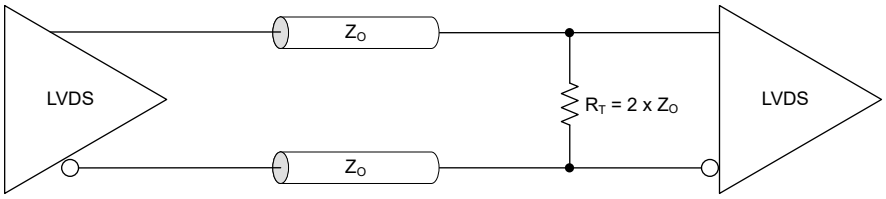

Figure 3-9. Traditional LVDS Termination

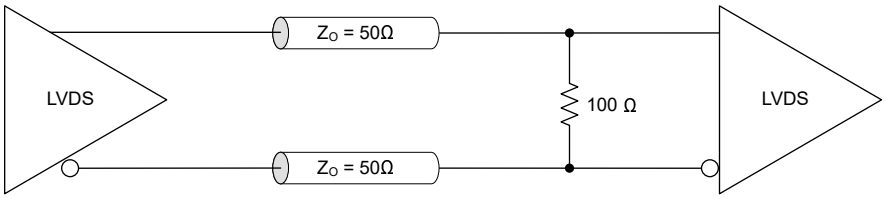

Figure 3-10. DC-Coupled LVDS to LVDS

3.3.2 AC-Coupled LVDS

Apply AC-coupling capacitors to the LVDS output when interfacing with non-LVDS receivers and to reconfigure the VCM. Provide the necessary differential termination required by the LVDS driver. Example termination is explained in the following sections.

AC-Coupled LVDS to LVPECL

For LVDS to LVPECL translation, terminate after the AC-coupling capacitors to set the common-mode voltage to VCC − 1.3V. Such resistor network provides the 100Ω differential termination required by the LVDS driver.

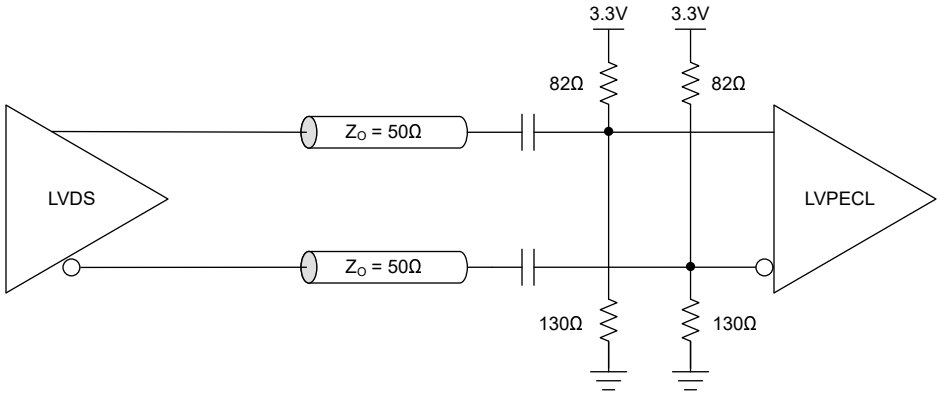

Figure 3-11. AC-Coupled LVDS to LVPECL

AC-Coupled LVDS to HCSL

For LVDS to HCSL translation, use a resistor network after the capacitors to set the common-mode voltage to 350mV. The termination on the receiver side must provide the 100Ω differential termination required by the LVDS driver.

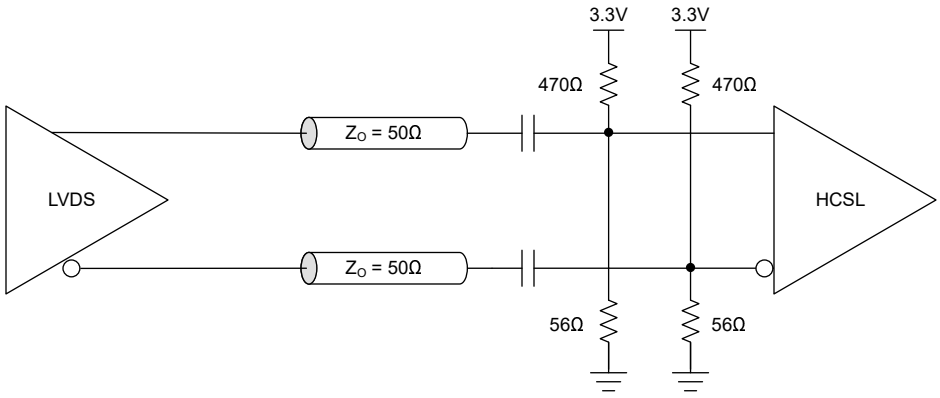

Figure 3-12. AC-Coupled LVDS to HCSL

AC-Coupled LVDS to LP-HCSL

For LVDS to LP-HCSL translation, terminate the LVDS driver before the AC-coupling capacitors and directly route the AC-coupled outputs to the LP-HCSL receiver.

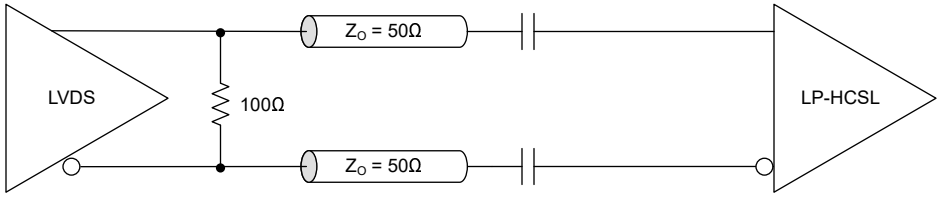

Figure 3-13. AC-Coupled LVDS to LP-HCSL

AC-Coupled LVDS to LVDS With Internal Biasing

For LVDS to drivers with internal biasing, terminate the LVDS driver before the AC-coupling capacitors. Some clock receivers which follow this termination scheme are LMK0482x and LMK04832 are receivers which have internal biasing and require this method.

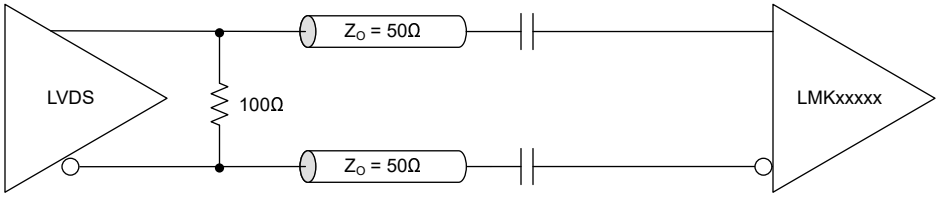

Figure 3-14. AC-Coupled LVDS to LVDS With Internal Biasing

AC-Coupled LVDS to LVDS With Internal Biasing and Termination

For LVDS to drivers with internal termination and biasing, only the AC-coupling capacitors are required. Some clock receivers which follow this termination scheme are LMK05318B, LMK5B family (such as LMK5B33216), and LMKCA family (such as LMK5C33216A). Note that the input buffer register must be configured to *internal 100Ω differential termination*.

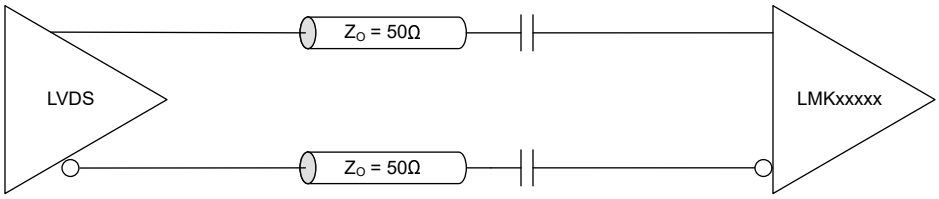

Figure 3-15. AC-Coupled LVDS to LVDS with Internal Biasing and Termination

AC-Coupled LVDS to Receivers With A Biasing Pin

For receivers with a biasing pin (such as the V_{AC_REF} pin), follow the recommended termination from the data sheet. A 0.1uF capacitor to ground can be required depending on the receiver. Some clock receivers which follow this termination scheme are the LMK1Dxxxx family (such as LMK1D1208) and CDCLVPxxxx family (such as CDCLVP1208). Note that the LMK1Dxxx family also supports DC-coupled inputs with external 100Ω differential termination, but the V_{AC_REF} pin must be left floating.

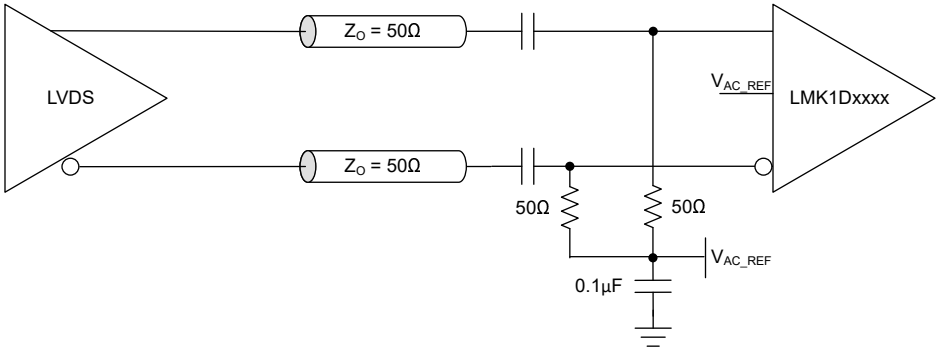

Figure 3-16. AC-Coupled LVDS to LMK1Dxxxx

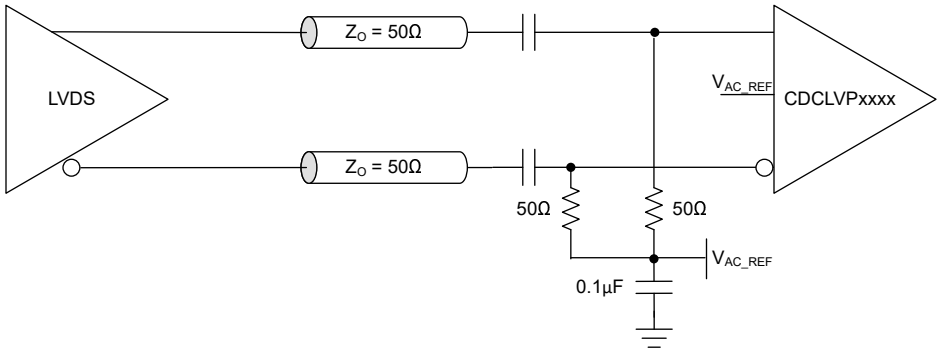

Figure 3-17. AC-Coupled LVDS to CDCLVPxxxx

AC-Coupled *AC-LVDS* to LVDS

For *AC-LVDS* type outputs (as seen in LMK05318B), termination before the AC-coupling capacitors is not required because the driver is internally biased and terminated. The capacitors can be placed on the receiver or driver side. Do not DC-couple the signal unless the output VCM meets the receiver specification.

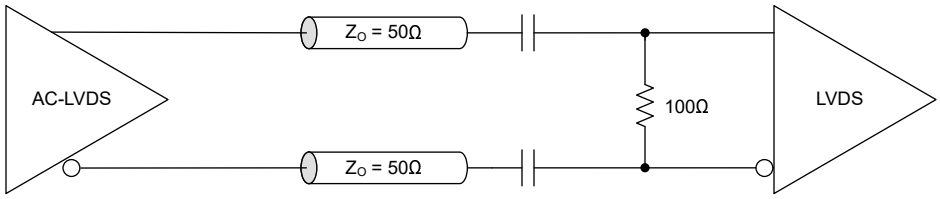

Figure 3-18. AC-Coupled *AC-LVDS* to LVDS

3.4 HSDS

3.4.1 DC-Coupled HSDS

HSDS is similar to LVDS except the HSDS signal has a larger voltage swing. For certain drivers, termination is not required to get a proper output clock but signal integrity can be distorted without proper termination. Some clock receivers which follow this termination scheme are the LMK5B family (such as LMK5B33216) and LMKCA family (such as LMK5C33216A). The LMK5B and LMK5CA families have register-configurable VOD and VCM settings.

General Guidelines

- Terminate the HSDS driver with a differential resistor (typically 100Ω) across the output P and N signals.
- Place the differential resistor on the receiver side as close to the input pins as possible.

Example Termination

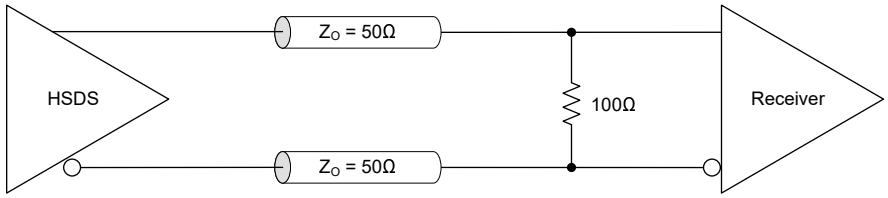

Figure 3-19. DC-Coupled HSDS to Generic Receiver

3.4.2 AC-Coupled HSDS

Apply AC-coupling capacitors to the HSDS output when interfacing with non-HSDS receivers and/or to reconfigure the VCM. If the driver supports adjustable voltage swing, configure the register settings to meet the receiver specification.

Example Termination

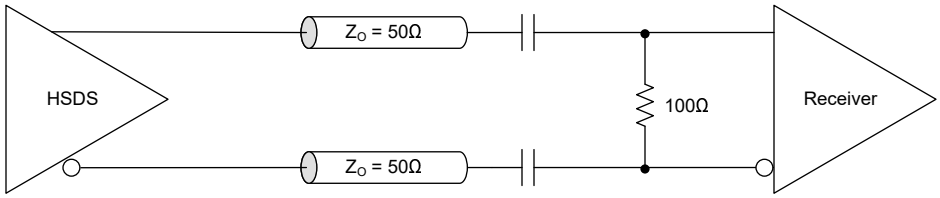

Figure 3-20. AC-Coupled HSDS to Generic Receiver With Internal Biasing (Differential Termination)

AC-Coupled HSDS to Generic Receiver With Internal Biasing (Single-Ended Termination)

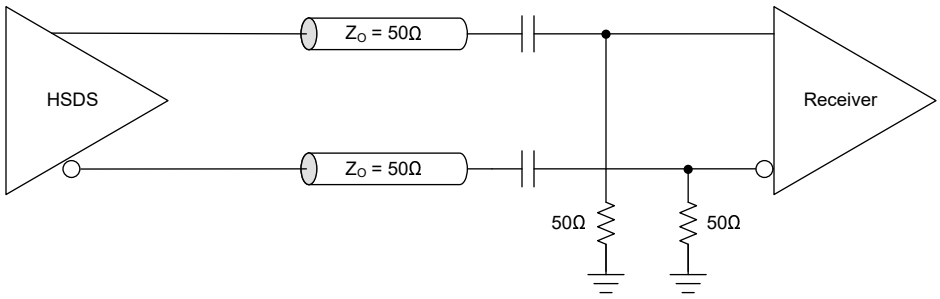

Figure 3-21. AC-Coupled HSDS to Generic Receiver With Internal Biasing (Single-Ended Termination)

3.5 HCSL

3.5.1 DC-Coupled HCSL

General Guidelines

Traditional HCSL uses a current-mode driver to source 15mA from an open-emitter output. HCSL outputs must drive into resistive loads to provide a DC return path and generate a switching signal. Placing a 50Ω resistor to ground on each P and N leg sets the output swing to 750mV and the common-mode voltage to 350mV.

- Terminate the HCSL driver with a 50Ω resistor to ground on each of the P and N outputs.
- Series resistors (R_S) can be placed close to the the output pins to correct overshoot and reduce the output slew rate. The value of R_S is determined by the transmission line impedance and the internal output impedance of the driver. Fulfill the equation to maintain impedance-matched outputs:
  - $Z_O = R_O + R_S$
- When R_O is unknown, set R_S = 0Ω in the initial design. R_S can be adjusted for impedance matching after testing the signal integrity of the PCB. The typically used R_S values are listed:

Table 3-2. Typical Series Termination for HCSL

Z_O (SINGLE-ENDED) [Ω]	Z_O (DIFFERENTIAL) [Ω]	R_O [Ω]	R_S [Ω]
50	100	17	33
42.5	85	15.5	27

Example Termination

DC-Coupled HCSL to HCSL

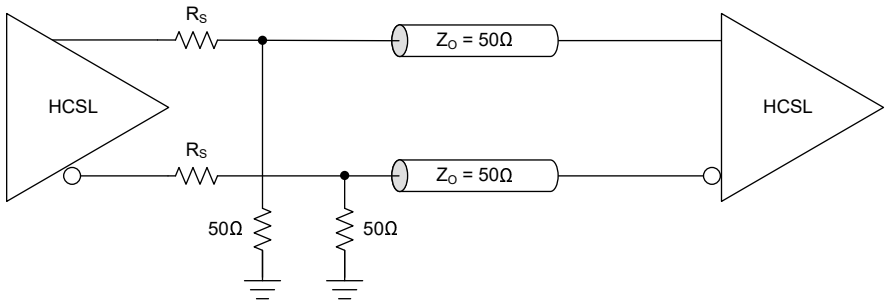

Figure 3-22. DC-Coupled HCSL to HCSL

When interfacing with an LP-HCSL receiver, follow the same guidelines as DC-coupled HCSL receivers.

DC-Coupled HCSL to LP-HCSL

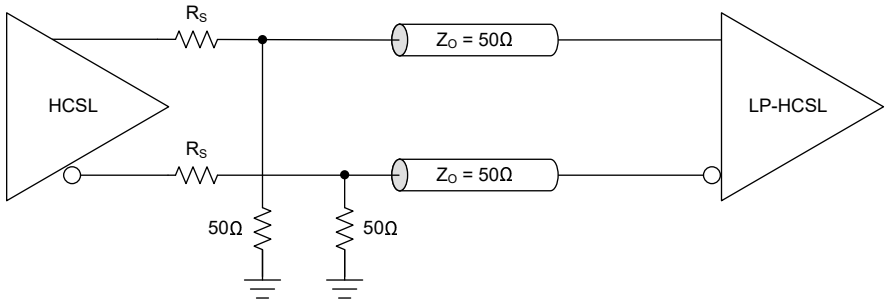

Figure 3-23. DC-Coupled HCSL to LP-HCSL

3.5.2 AC-Coupled HCSL

Apply AC-coupling capacitors to the HCSL output when interfacing with non-HCSL receivers or to reconfigure the VCM.

External Termination

AC-Coupled HCSL to LVPECL

For HCSL to LVPECL translation, place the resistors to ground before the AC-coupling capacitors to provide the DC return path for the HCSL driver. Use a resistor network after the capacitors to set the common-mode voltage to V_{CC} – 1.3V for the LVPECL receiver.

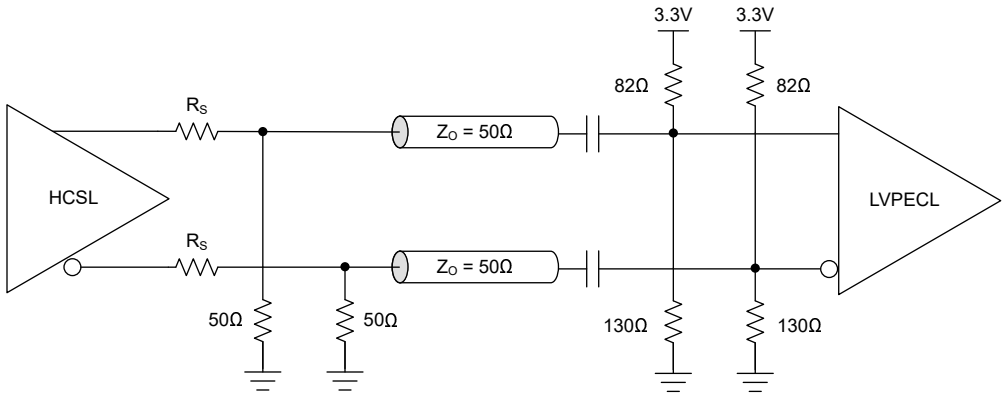

Figure 3-24. AC-coupled HCSL to LVPECL

AC-Coupled HCSL to LVDS With External Termination and Internal Biasing

For translation with an LVDS receiver that accepts the VCM of an HCSL output and/or has internal biasing, terminate the HCSL driver with resistors to ground and the LVDS receiver with a differential resistor.

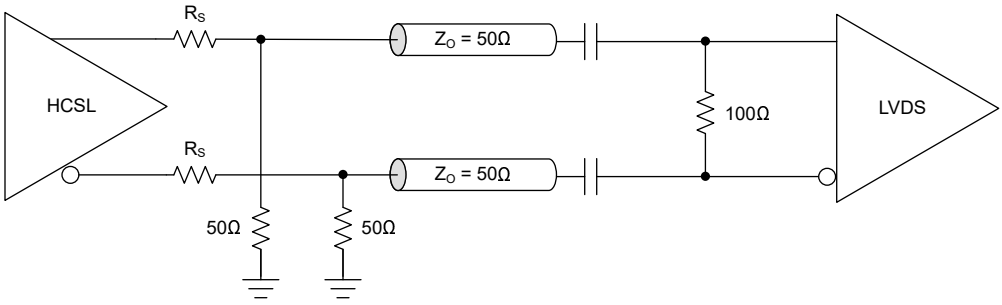

Figure 3-25. AC-Coupled HCSL to LVDS with External Termination and Internal Biasing

AC-Couple HCSL to LVDS With External Termination and Biasing

For translation with an LVDS receiver that is not internally biased, terminate the HCSL driver with resistors to ground and reconfigure the common-mode voltage to 1.2V using a resistor network.

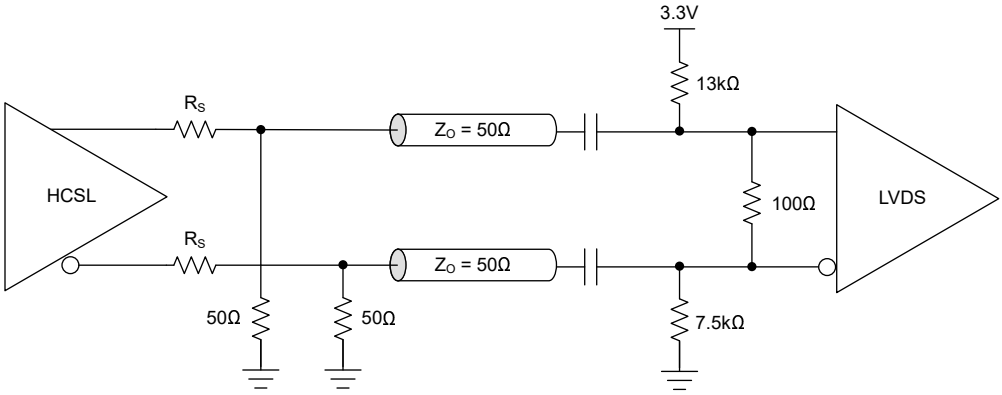

Figure 3-26. AC-Coupled HCSL to LVDS with External Termination and Biasing

AC-Coupled HCSL to LVDS With Internal Termination and Biasing

For translation with an LVDS receiver that is biased and terminated, only terminate the HCSL driver with resistors to ground.

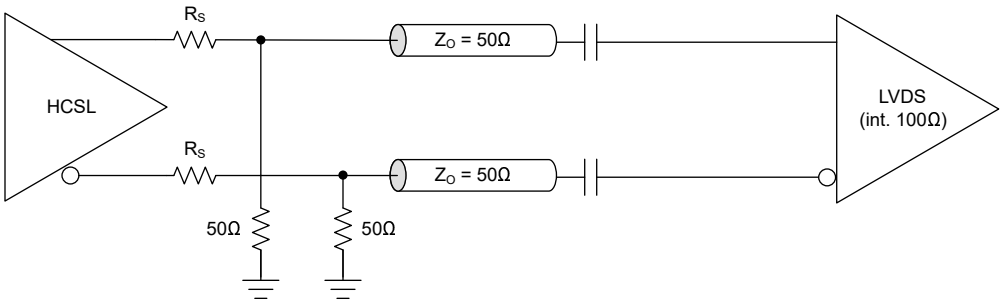

Figure 3-27. AC-Coupled HCSL to LVDS with Internal Termination and Biasing

3.6 LP-HCSL

3.6.1 DC-Coupled LP-HCSL

LP-HCSL is similar to HCSL through the same swing (750mV) and common-mode (350mV) specifications. LP-HCSL is different from HCSL through the type of driver architecture used. LP-HCSL uses a push-pull voltage driver instead of a current-mode. As a result, external termination is not required for LP-HCSL signals and the outputs must drive into capacitve loads. LP-HCSL signals also use newer technology newer technology which have low power consumption (about 4mA).

General guidelines:

- Series resistors (R_S) can be placed close to the the output pins to correct overshoot and reduce the output slew rate. The value of R_S is determined by the transmission line impedance and the internal output impedance of the driver. Fulfill the equation to maintain impedance-matched outputs:
  - $Z_O = R_O + R_S$
- When R_O is unknown, set R_S = 0Ω in the initial design. R_S can be adjusted for impedance matching after testing the signal integrity of the PCB. The typically used R_S values are listed:

Table 3-3. Typical Series Termination for LP-HCSL

Z_O (SINGLE-ENDED) [Ω]	Z_O (DIFFERENTIAL) [Ω]	R_O [Ω]	R_S [Ω]
50	100	17	33
42.5	85	15.5	27

Example termination:

- **DC-Coupled LP-HCSL to LP-HCSL**

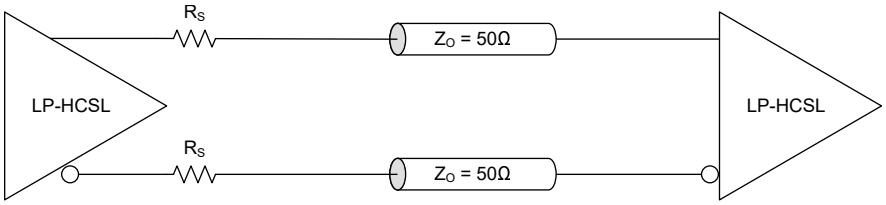

Figure 3-28. DC-Coupled LP-HCSL to LP-HCSL

- **DC-Coupled LP-HCSL to HCSL**

  Follow the same guidelines as interfacing with DC-coupled LP-HCSL to LP-HCSL receivers.

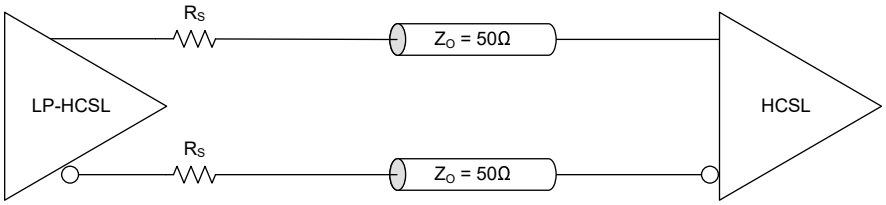

Figure 3-29. DC-Coupled LP-HCSL to HCSL

3.6.2 AC-Coupled LP-HCSL

Apply AC-coupling capacitors to the LP-HCSL output when interfacing with non LP-HCSL receivers and/or to reconfigure the VCM.

The examples in AC-Coupled HCSL can be used for AC-coupled LP-HCSL termination, **but omit the 50Ω resistors to ground before the AC-coupling capacitors** as the resistors are not required for LP-HCSL.

Example termination:

- **AC-Coupled LP-HCSL to LP-HCSL**

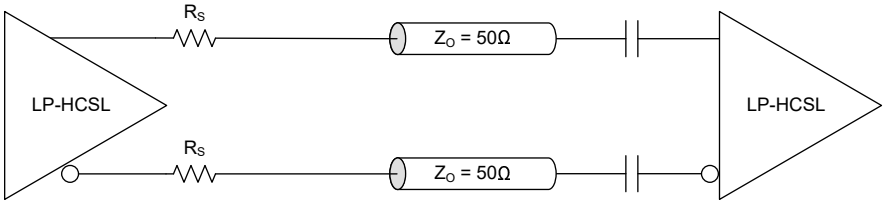

Figure 3-30. AC-Coupled LP-HCSL to LP-HCSL

4 Single-Ended

A single-ended signal consists of a toggling voltage across one wire as the signal and another wire as the reference (ground) voltage. Refer to the following sections for guidance on terminating single-ended sginals.

4.1 LVCMOS

4.1.1 DC-Coupled LVCMOS (Series Termination)

LVCMOS drivers are typically source-terminated and internally biased to mid-level of VOH (or VOH/2), where VOH tends to be near VDD and VOL near 0V.

General Guidelines

- Avoid placing resistors to ground on the CMOS outputs to prevent high current consumption. If pull-downs are used to reduce the voltage swing, confirm the current limit of the output driver is not violated. Check the driver data sheet.
- A series resistor (R_S) can be placed in the case the output impedance (R_O) does not match the required transmission line impedance (Z_O).
- Place R_S as close to the output pins as possible to match the impedance, correct the overshoot, and reduce the output slew rate. Fulfill the equation to maintain impedance-matched outputs:
  - $Z_O = R_O + R_S$
- When R_O is unknown, set R_S = 0Ω in the initial design. R_S can be adjusted for impedance matching after testing the signal integrity of the PCB.

Example Termination:

DC-Coupled LVCMOS to LVCMOS

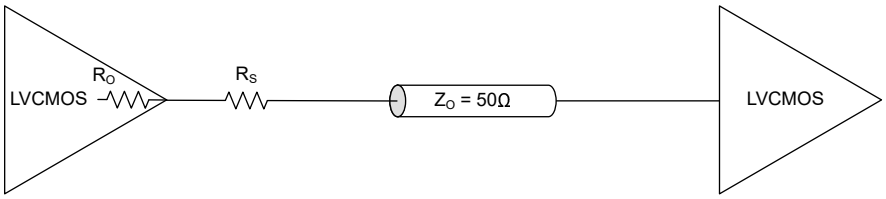

Figure 4-1. DC-Coupled LVCMOS to LVCMOS

4.1.2 AC-Coupled LVCMOS (Series Termination)

When source-terminated, LVCMOS drivers outputs can be simply AC-coupled. Configure R_S as needed.

Example Termination:

AC-Coupled LVCMOS to LVCMOS

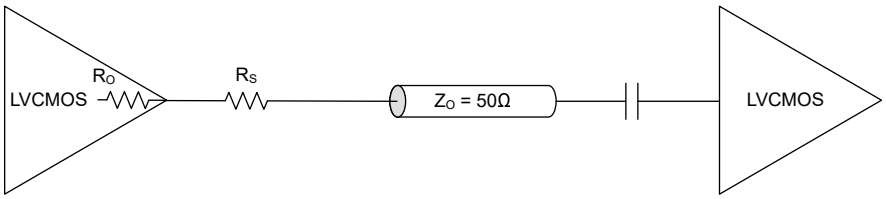

Figure 4-2. AC-Coupled CMOS to CMOS

4.2 Differential P or N

One side of a differential signal (either P or N) can be used for a single-ended receiver. However, the differential signal must be properly terminated and meet the receiver VIH and VIL specification.

4.2.1 DC-Coupled Differential P or N

General Guidelines

- Terminate the differential driver as explained in the Differential section.
- Provide a DC return path for the differential driver, if required.
- Confirm that the single-ended output voltage swing (VOD) meets the single-ended receiver requirements.
- Use IBIS models to simulate the signal integrity and translation between the differential and single-ended receiver.

DC-Coupled LVPECL to Two Single-Ended Receivers Using a Thevenin Termination

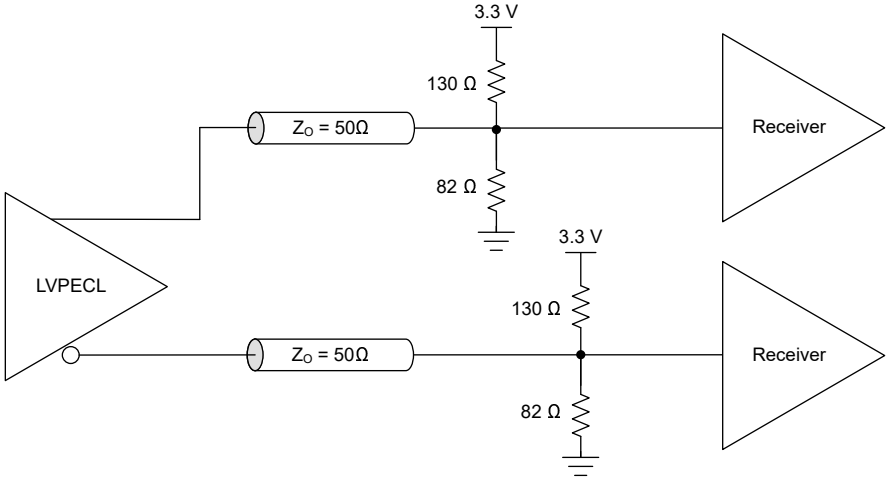

Figure 4-3. DC-Coupled LVPECL to Two Single-Ended Receivers Using a Thevenin Termination

DC-Coupled LVPECL to One Single-Ended Receiver Using a Thevenin Termination

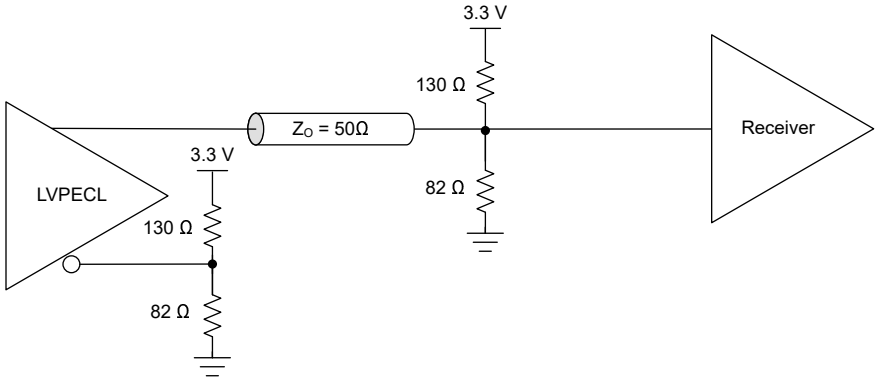

Figure 4-4. DC-Coupled LVPECL to One Single-Ended Receiver Using a Thevenin Termination

DC-Coupled LVDS to One Single-Ended Receiver

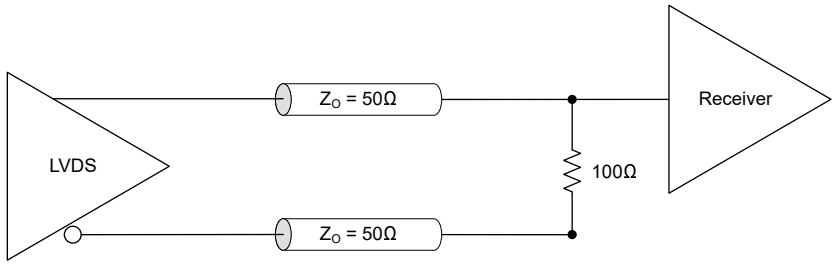

Figure 4-5. DC-Coupled LVDS to One Single-Ended Receiver

DC-Coupled HCSL to Two Single-Ended Receivers

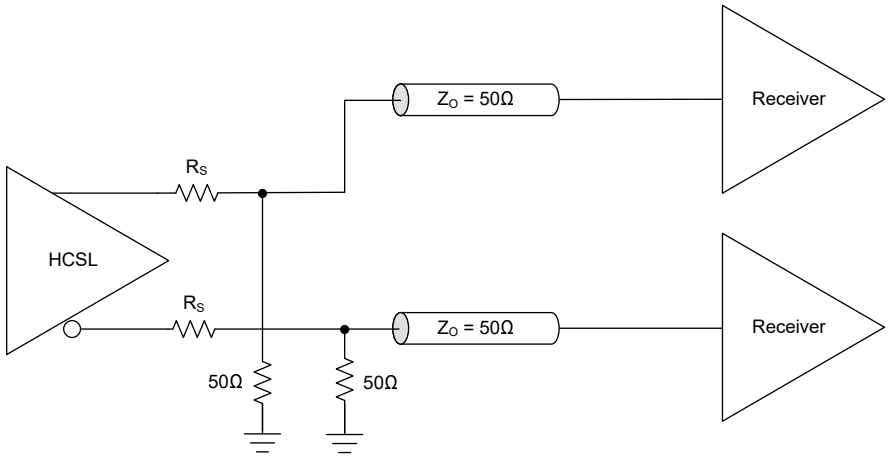

Figure 4-6. DC-Coupled HCSL to Two Single-Ended Receivers

DC-Coupled HCSL to One Single-Ended Receiver

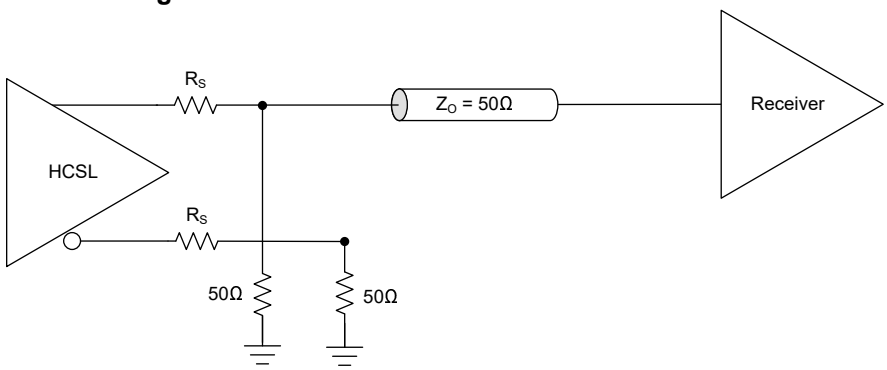

Figure 4-7. DC-Coupled HCSL to One Single-Ended Receiver

DC-Coupled LP-HCSL to Two Single-Ended Receivers

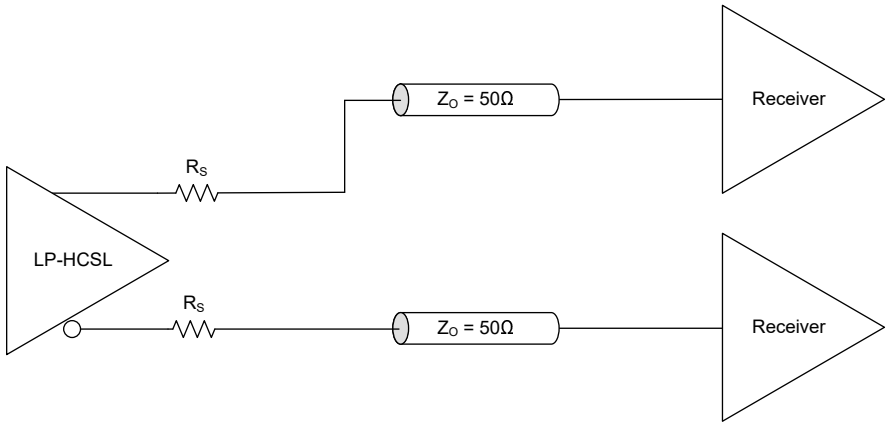

Figure 4-8. DC-Coupled LP-HCSL to Two Single-Ended Receivers

DC-Coupled LP-HCSL to One Single-Ended Receiver

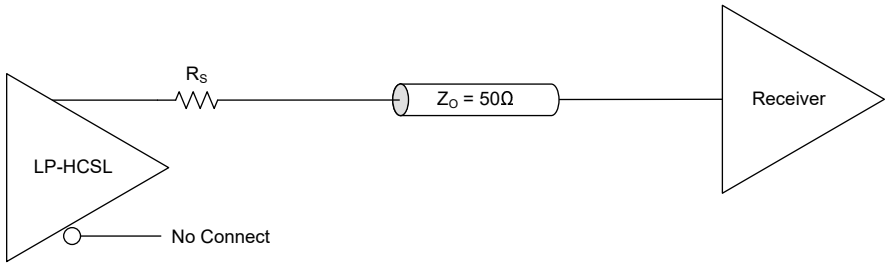

Figure 4-9. DC-Coupled LP-HCSL to One Single-Ended Receiver

5 Summary

Termination can be made simple by referring to the steps listed in the General Termination Guidelines. Follow the driver and receiver specifications and maintain impedance-matched signals for proper signal integrity. Use the Thevenin Equivalent termination with AC-coupled outputs to translate between two signal types and reconfigure the common-mode voltage. Consider the figures from Differential and Single-Ended as examples when designing the signal path.

6 References

- Texas Instruments, *Interfacing Between LVPECL, VML, CML, and LVDS Levels*, application note.
- Texas Instruments, *LMK04828*, product page.
- Texas Instruments, *LMK04832*, product page.
- Texas Instruments, *LMK05318B*, product page.
- Texas Instruments, *LMK5B33216*, product page.
- Texas Instruments, *LMK5C33216A*, product page.
- Texas Instruments, *LMK1D1208*, product page.
- Texas Instruments, *CDCLVP1208*, product page.

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