Total Ionizing Dose (TID) and Single Event Effects (SEE) Test Report

TEXAS INSTRUMENTS

Low Drop Out (LDO) Regulator

TPS7H1101-SP QMLV

SMD#: 5962-1320201VXC

Date: January 10, 2014
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TPS7H1101-SP Product Description

The TPS7H1101-SP is a low dropout (LDO) linear regulator that uses a PMOS pass element. The benefits of this approach is very low dropout, and performance, at higher temperatures and during Single Event Effects (SEE). The TPS7H1101-SP operates over a wide range of input voltage, from 1.5 V to 7 Volts, enabling very low noise regulation in application transitions from 6V-IN to 5 V-OUT, and 1.5 V-IN to 1.2 V-OUT with excellent Power Supply Rejection Ratio (PSRR). It also features a Power Good output for easy power sequencing, and a programmable Current Limit, and Soft Start. The part is available in a 16 pin ceramic flat pack QMLV certified under SMD # 5962-1320201VXC as shown below.

QMLV Qualified
Ceramic Flat Pack
5962-1320201VXC

Radiation Executive Test Summary

The TPS7H1101-SP has been radiation tested against Total Ionizing Dose (TID) and Single Event Effects (SEE). This report presents details on the tests performed. In summary the device is very rugged to these effects as shown below:

- **Total Dose (TID) Tolerance > 100kRAD(Si) @ 100RAD(si)/sec. dose rate**
- **ELDRS free to > 100kRAD(Si) @ 10mRAD(si)/sec. dose rate**
- **Single Event Latchup (SEL) Immune to LET > 85MeV-cm^2/mg @ 125^{o}C**
- **SEB and SEGR Immune to LET > 85MeV-cm^2/mg @ 25^{o}C**
- **SET/SEFI Onset > 40MeV-cm2/mg* (Proton Immune)**
- **QMLV 5962-1320201VXC available now.**
- **RHA 5962R1320201VXC – Pending (1Q2014)**

*** Threshold for SET/SEFI detection was set to a +\- 2% change of Vout**

TPS7H1101-SP QMLV Radiation Report

1.0. TID Overview and Background

It is well known that ionizing radiation can cause parametric degradation and ultimately functional failures in electronic devices. There are two dominant mechanisms associated with these effects, the generation of hole traps and interface states. Both of these mechanisms contribute to the overall MOS transistor Vt shifts. First order effects are typically seen in the thick field isolation region and second order effects in the gate region, under Total Irradiated Dose (TID) exposure. These mechanisms occur due to electron-hole pair production from ionization radiation and their transport and trapping in the dielectric and silicon interface regions. These mechanisms, know as hole traps, "Vot" and interface traps "Vit" have been studied for many years and are well documented. It is also well know that annealing of the these mechanisms can occur over time and may be accelerated by temperature. Figure 1. is a general summary of these effects. The effects are greatly dependent dielectric thickness of the particular process technology node and also device component construction.

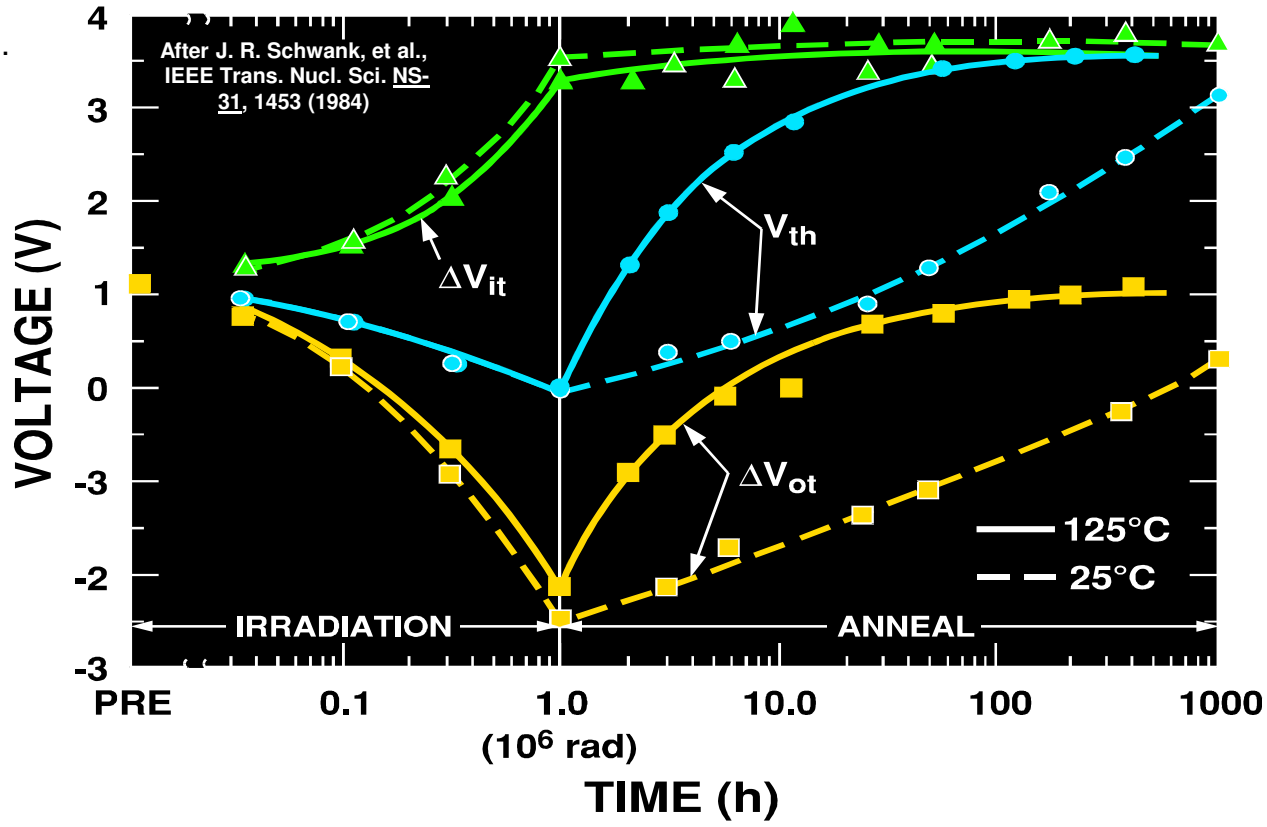


Figure 1. Vot / Vit Generation and Time/ Temperature Annealing

Accumulation of hole traps is typically the primary mechanism for increased leakage and failures in MOS semiconductor devices. MOS Semiconductor devices are typically less dependent on the generation of interface traps, but the ratio of these two mechanisms do play a role in overall time dependent device behavior, and are typically very process and structure dependent. The anneal rate of hole traps (either deep or shallow) of a particular device is also process and structure dependent. Some semiconductor processes exhibit quick anneal rates, while others may anneal at a low rates. Activation energy plays an important role in these recombination rates, i.e. annealing of hole traps, as show by elevated temperatures in figure 1. On the other hand interface (electron or H) traps do not anneal easily and can accumulate over time. Because of accelerated testing, both hole traps and interface generation rates may not correlate to the actual intended radiation mission environment. In a space environment the where TID rates are typically less than 0.01mRad/sec, giving way to unexpected results compared to accelerated exposure. MIL-STD-883, method 1019 covers both annealing , and rebound effects (accelerated anneal) with a 168 hour 100^{o}C post electrical test. Interface state generation is of prime importance for bipolar devices, being one of the major factors in Enhanced Low Dose Rate Sensitivity (ELDRS) of these device. Bipolar structures are affected primarily by interface states and secondary by hole traps in the base oxide. Both of these mechanisms play a role in device behavior. Both again are very process and structure dependent.

The TPS7H1101-SP has been evaluated for TID tolerance. High dose Rate (HDR) exposure was performed on biased and unbiased devices in a Co60 gamma cell at TI SVA facility in Santa Clara California. Figure 2. illustrates a picture of the Gamma Cell 220 used for the exposure. The un-attenuated dose rate of this cell is 100 RAD/sec.

The test matrix of devices is included in Appendix A. After exposure. The devices were packed in dry ice (per MIL-STD-883H Method 1019.9 section 3.10.) and returned to TI Dallas for a full post radiation electrical evaluation on Automated Test Equipment (ATE).

Test conditions for HDR are shown in Figure 3. Measurements include pre-radiation quiescent current, V_{in}, and load regulation values. Post radiation measurements were taken within 30 minutes of removal of the devices from the dry ice container. The devices were allowed to reach room temperature prior to electrical post radiation measurements. At the 50kRAD TID level, a ~ 6mV V_{out} delta was observed, while a ~ 10mV V_{out} delta was observed at the 100kRAD level.

Figure 2. TI SVA Gamma Cell

	Pre radiation			Post Radiation		
				100Krad		
Board # 3	Q current	6.92ma		Q current	7.23ma	
	Line Reg	Vin	Vout	Line Reg	Vin	Vout
		2.05438	1.78163		2	1.7942
		7.03638	1.78156		7	1.7926
	Load Reg	Vin	Vout	Load	Load Reg	Vin	Vout	Load
		2	1.78158	0		2	1.7885	0
		2	1.78161	1.0026		2	1.7876	1
		2	1.78187	2.0032		2	1.7874	2
				50Krad		
Board # 8	Q current	6.88ma		7.21ma		
	Line Reg	Vin	Vout	Line Reg	Vin	Vout
		2.0398	1.77628		2	1.783
		7.02298	1.77608		7	1.7827
	Load Reg	Vin	Vout	Load	Load Reg	Vin	Vout	Load
		2	1.77618	0		2	1.7828	0
		2	1.77622	1.0026		2	1.7827	1
		2	1.7762	2.0036		2	1.7825	2

Figure 3. Pre and Post TID electrical measurements

2.0. Low Dose Rate TID Introduction and Overview

Because the TPS7H1101-SP is a BiCMOS technology containing bipolar devices, it must be checked for low dose rate TID exposure response, to determine if these devices exhibit Enhanced Low Dose Rate Sensitivity (ELDRS). As mentioned previously, bipolar devices are often sensitive to interface and hole traps occurring in the base oxide and base emitter junction interface region as shown in figure 4.

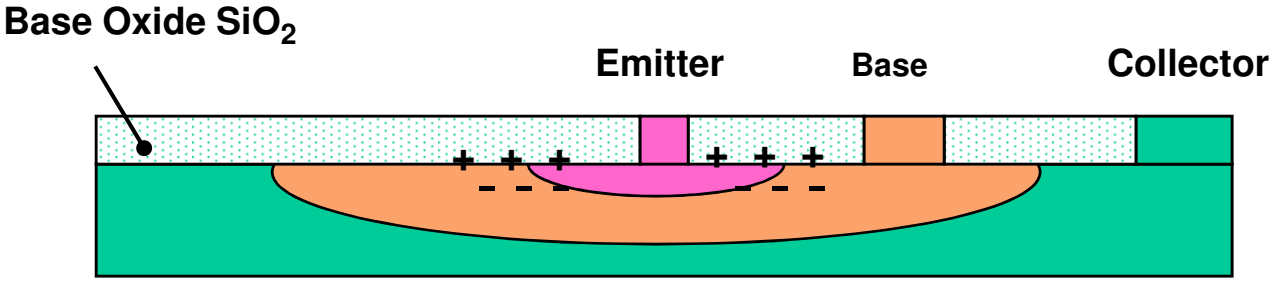


Figure 4. Bipolar structure and TID effects

The TPS7H1101-SP Low Drop Out Regulator (LDO) is manufactured in TI's 7th generation Linear BiCMOS (LBC7) process technology. Over 99.9% of the design utilizes the CMOS components from the component library in the LBC7 process. The device incorporates only three bipolar transistors that are used in the design of the band gap reference and a 4th device used for current shutdown. As previously mentioned Per Mil-Std-883H, method 1019.9, a BiCMOS technology should be checked for Low Dose Rate (LDR) Total Ionizing Dose (TID) exposure response. The purpose of this test is to determine if there are time dependent effects to dose rate, in particular to low dose rates, in such application as Space where charge yield is low.

The charge yield or generation rates of hole and interface traps both contribute to overall "effective" Hfe or transistor gain reduction in bipolar transistors. Interface trap generation is often the dominate mechanism effecting bipolar transistor gain. Interface state generation is primarily caused by the proton transport mechanism or the release of trapped hydrogen in the device from processing, particularly in oxide layers. The generation of these interface states are greatly enhanced at low dose rates due to a low concentration of hole traps at the interface that typically repel positive charged hydrogen under high dose rate exposure. The test for low dose rate sensitivity is described in method 1019.9, and is performed at 10mRAD(si)/sec. A rate that is still much higher than actual space dose rates, but is much closer than High Dose Rates (HDR) or the accelerated rates of 50-300RAD/sec called out in Condition A of MIL-STD-883H, 1019.9. This is then compared to HDR for any substantial differences with LDR results.

The facility and Radiation Source used for LDR exposure was Radiation Assured Devices' Longmire Laboratories, Colorado Springs, CO. Co60 (GB-150) low dose rate source, shown in figure 5. Dosimetry is performed by an Air Ionization Chamber (AIC) traceable to NIST. RAD's dosimetry has been audited by DSCC and RAD has been awarded Laboratory Suitability for MIL-STD-750 and MIL-STD-883 TM 1019.

The dose rate is obtained by positioning the device-under-test at a fixed distance from the gamma cell. The dose rate for this irradiator varies from approximately 50rad(Si)/s close to the rods down to <1mrad(Si)/s at a distance of approximately 4-meters.

Figure 5. Low Dose Rate Source

As mentioned above, the TPS7H1101-SP contains only four bipolar transistors in the entire design. Three of these devices form an on-chip band gap voltage reference. A design that is commonly used across the semiconductor industry. A schematic implementation of the band gap used in the TPS7H1101-SP is shown in figure 6.

The fourth bipolar transistor is used in the current shutdown circuit. The schematic of the current shutdown is shown in Figure 7. As current increases in the resistor string, the voltage drop eventually is large enough for forward bias the base emitter junction of the NPN current shutdown circuit. This circuit is not transistor gain sensitive, and hence, robust to TID effects..

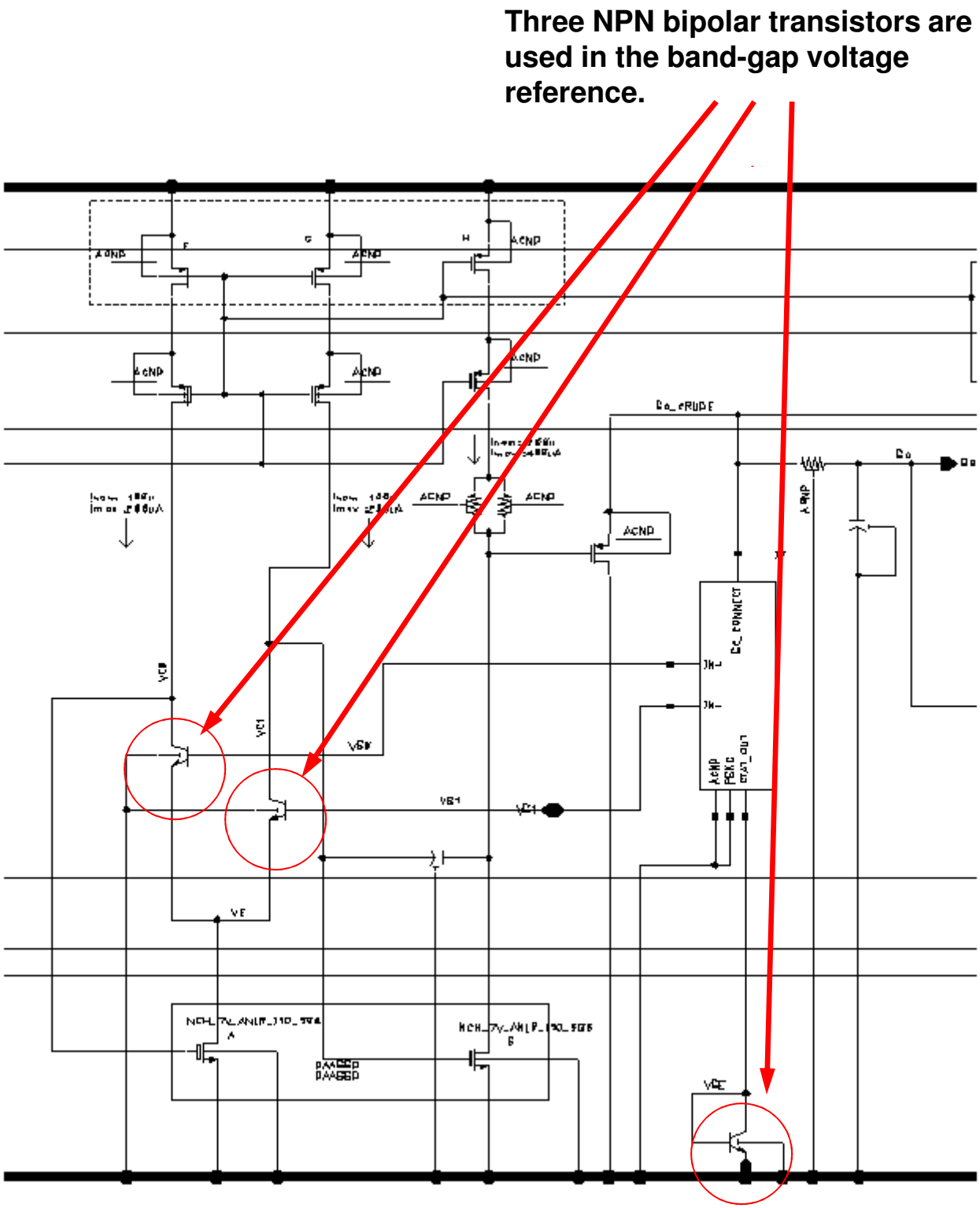


Figure 6. Schematic of LDO Bipolar Band gap Voltage Reference

As shown in figure 7, the resistor ladder , Rlad, is across the base emitter junction of the NPN current shutdown transistor. As current increases in the resistor ladder, at a set current point, the voltage drop becomes large enough to turn on the NPN transistor. i.e. forward bias the base-emitter junction. This transistor acts like a switch and triggers the Schmitt buffer, providing a logic like output . The output of the Schmitt buffer causes shutdown of the LDO, and if a proper load is sensed, the LDO will restart. The transistor in this switch configuration is not gain sensitive and therefore robust against TID effects.

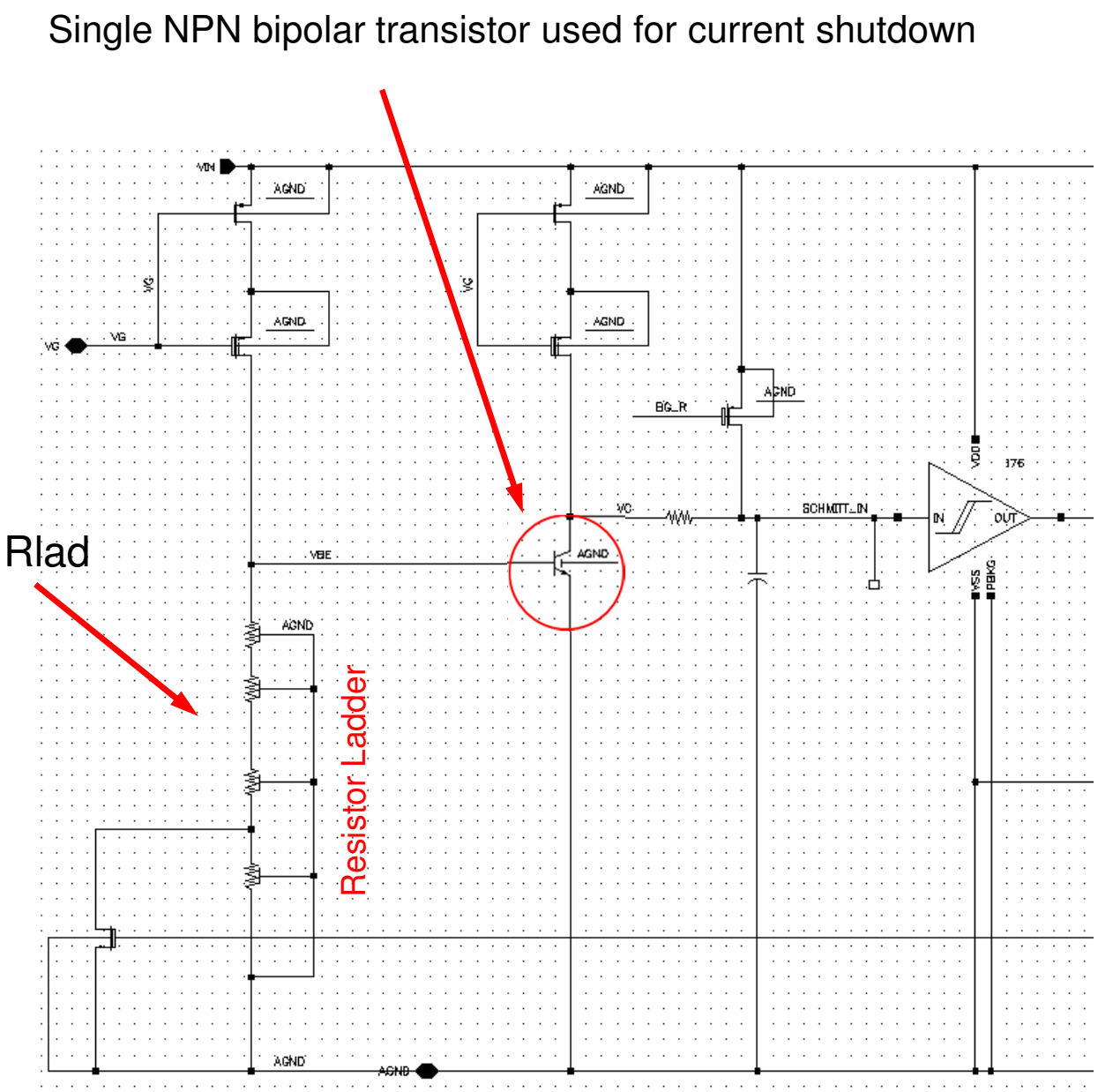


Figure 7. Schematic of LDO current shutdown

Low dose rate (LDR) and high dose rate (HDR) testing was performed on a previous silicon revision of the TPS7H1101-SP LDO regulator. Devices were exposed to TID of levels, 10, 20, 30, 40, 50kRAD(si) and checked for both high dose and low dose rate sensitivity at the exposure rate of 50 RAD/(si)sec. and 10mRAD(si)/sec. respectively. No noticeable difference was observed between the High Dose Rate (HDR) and the Low Dose Rate (LDR) data. This initial look ahead radiation testing was used to determine if any changes were needed to the final silicon design. The band gap design did not change from the initial to the final device release.

Qualification TID testing was also performed for final product qualification and has been completed on the LDO. This TID testing includes HDR, LDR in both biased and unbiased configurations to levels of 50-100kRAD(si). The results are shown in figures 4-9 under various Vin and Vout conditions. It should be noted that the observed delta between the 5 configurations in both biased and unbiased conditions after HDR and LDR showed little change. All units used in the radiation qualification exposure were from the same wafer lot, used the same production packaging, and went through burn-in prior to TID exposure. Post radiation accelerated anneal showed no potential long term effects.

It should be noted that any change in the band gap characteristics will cause an output voltage change, or Vout voltage change. Also any circuit behavior changes would also alter the regulation of the regulator. No noticeable changes were observed after the above HDR and LDR data logs. The NPN transistors used in this design, showed no sensitivity to TID dose rate.

In conclusion the device does not exhibit ELDRS, and is targeted to be released as a 100kRAD(si) RHA product in 1Q2014.

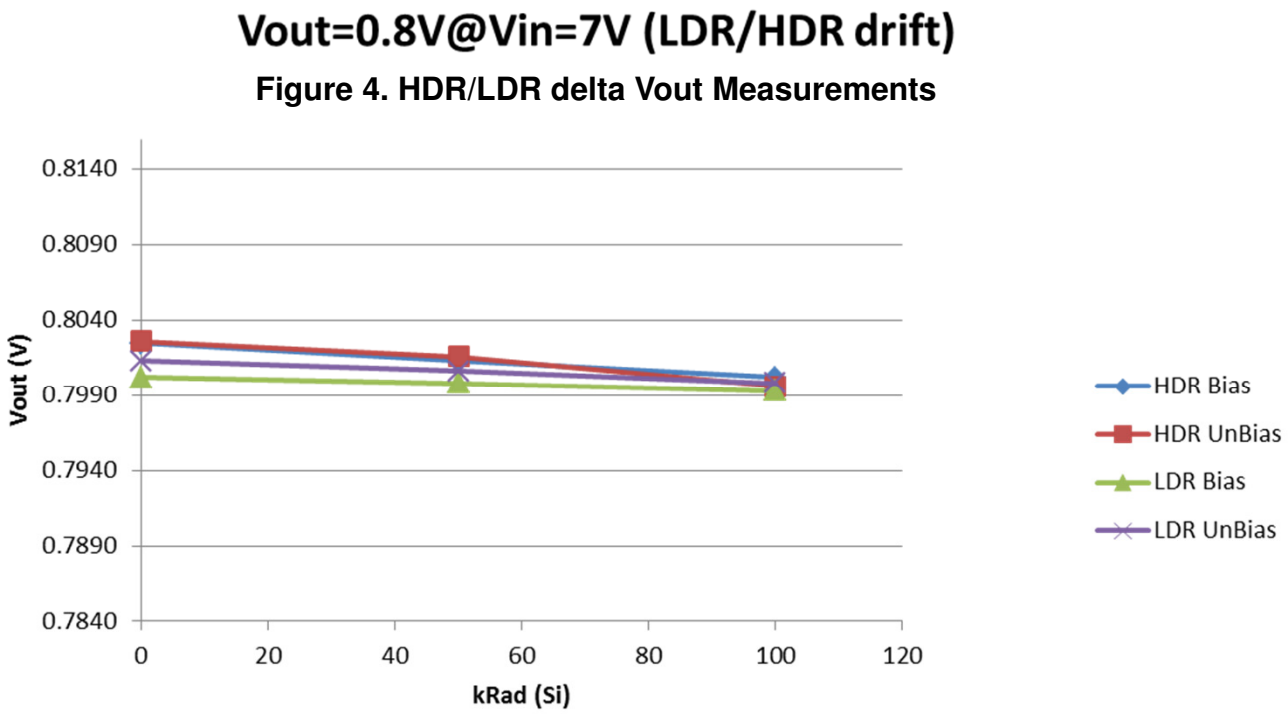


Figure 4. HDR/LDR delta Vout Measurements

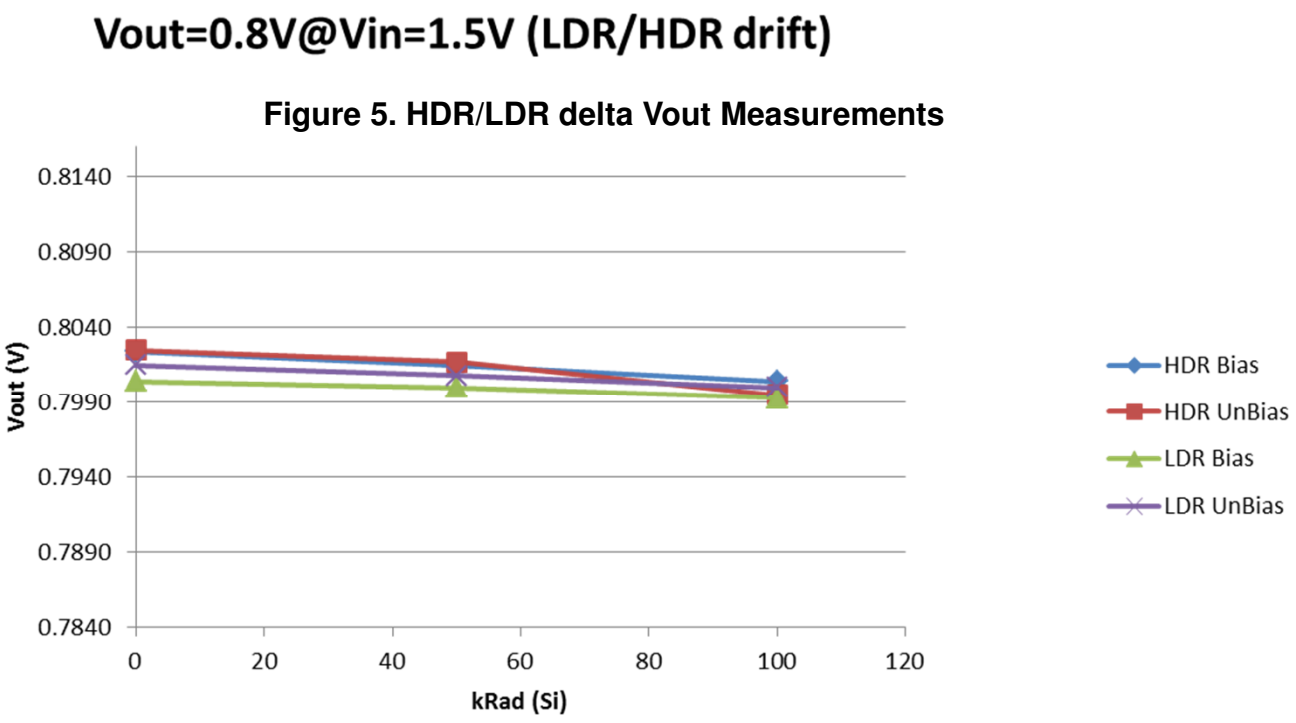
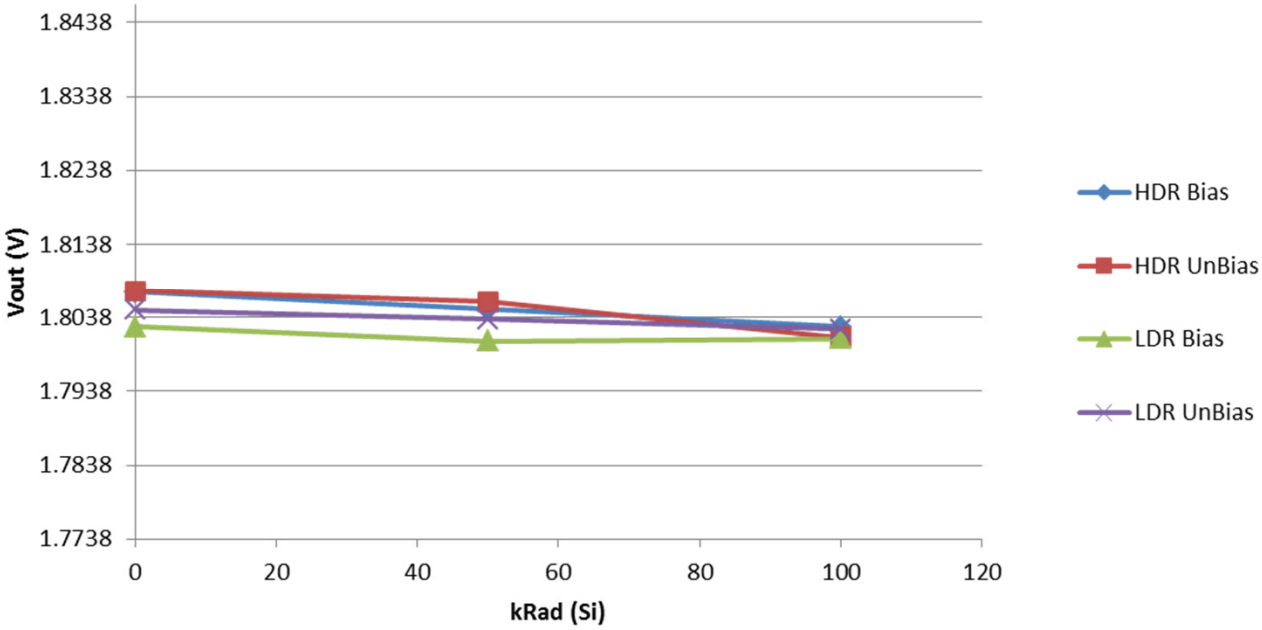


Figure 5. HDR/LDR delta Vout Measurements

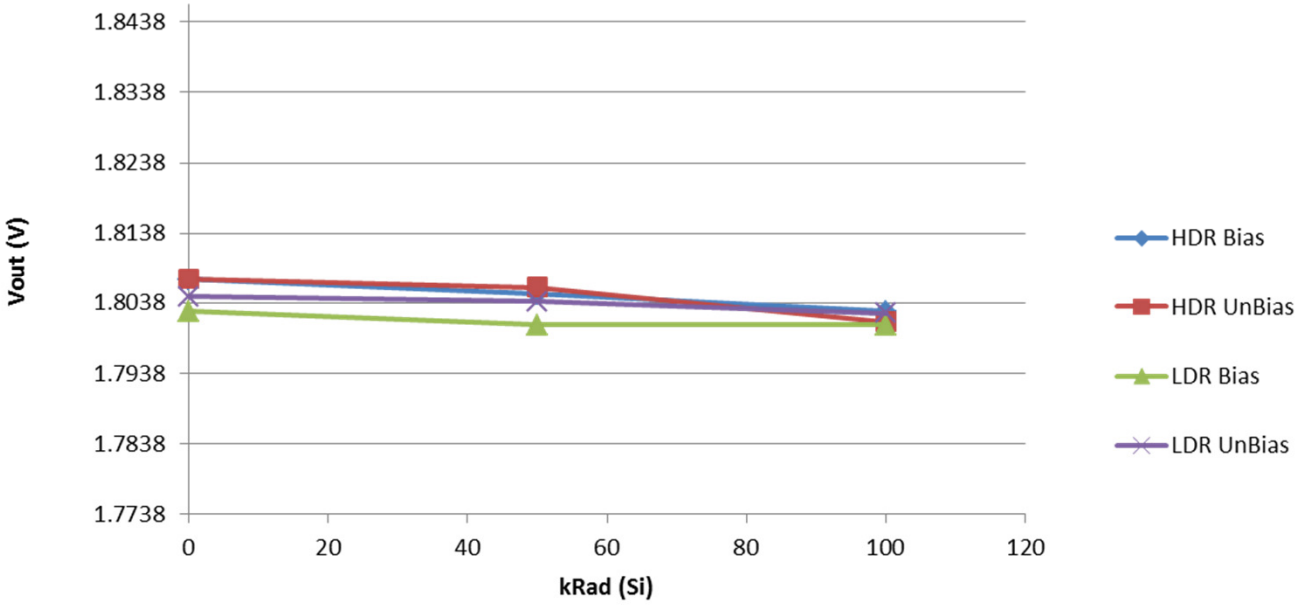
Vout=1.8V@Vin=2.0V (LDR/HDR drift)

Figure 6. HDR/LDR delta Vout Measurements



Vout=1.8V@Vin=7V (LDR/HDR drift)

Figure 7. HDR/LDR delta Vout Measurements



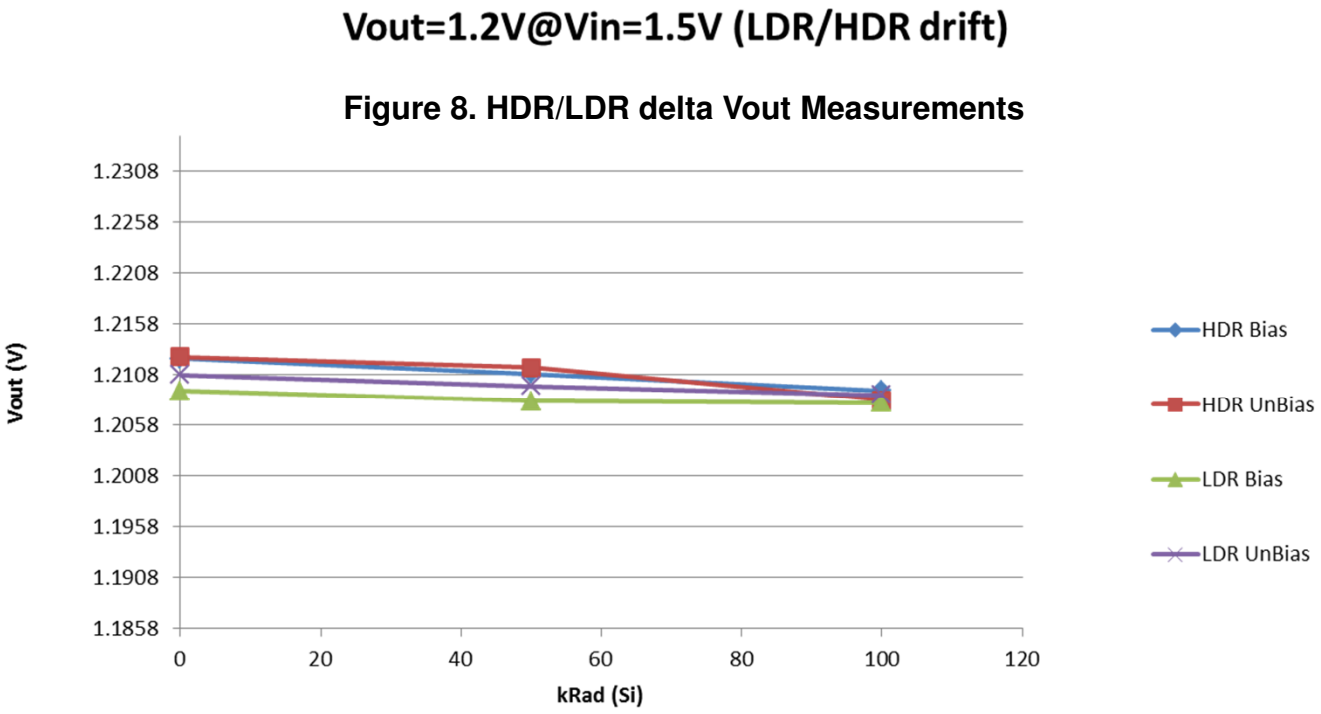


Figure 8. HDR/LDR delta Vout Measurements

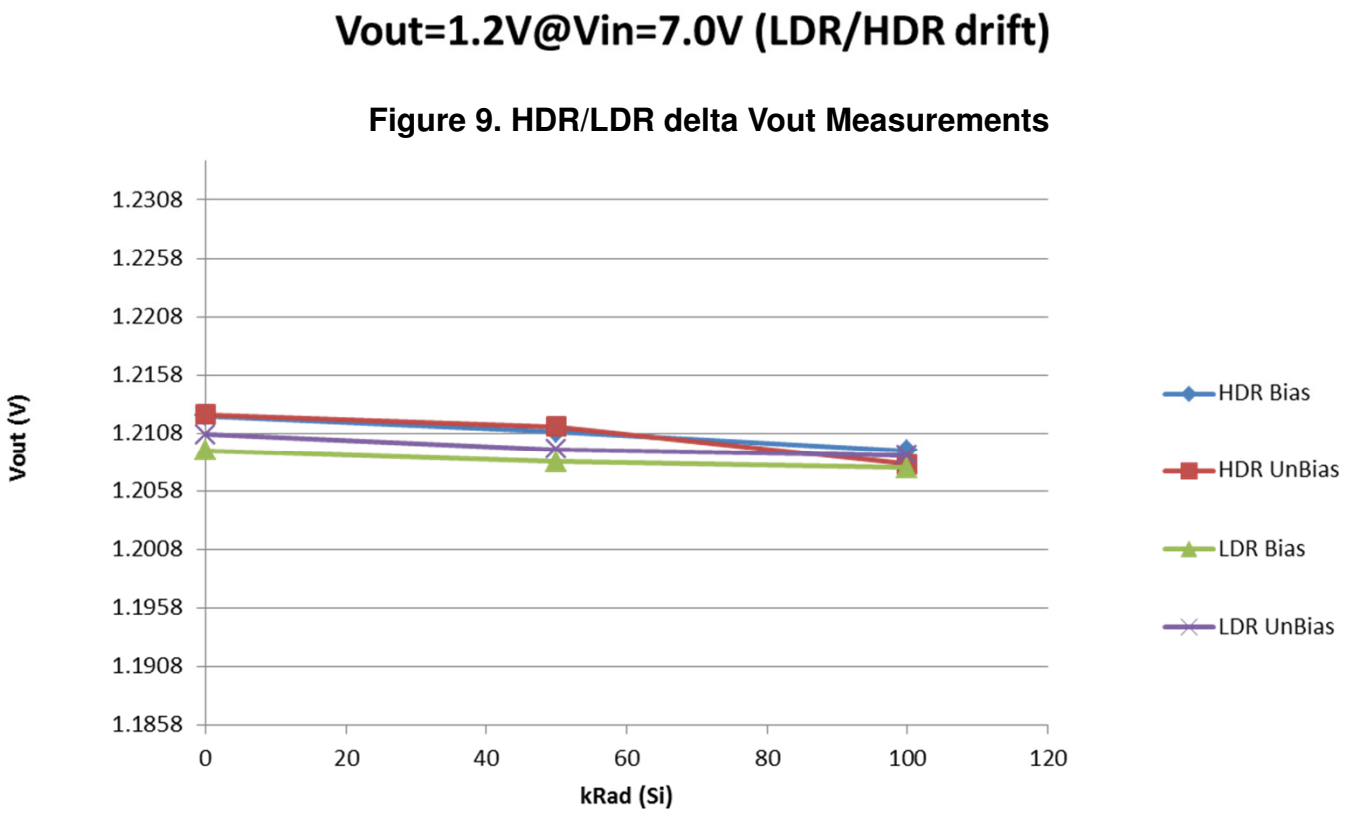


Figure 9. HDR/LDR delta Vout Measurements

3.0 Single Event Effects Testing

Single Event Effects comprises a large group of terms and effects from single or multiple particle events such as those from Neutrons, Protons, and Heavy Ions. Circuit test conditions must be adjusted for various test conditions, along with particle energy, mass, flux, and fluence.

Two separate Heavy ion tests have been completed on the TPS7H1101-SP, one on December 3, 2012, and the second one that took place on November 11, 2013. Both were conducted at the TAMU Cyclotron. The test board used during both tests is shown below in Figure 10.

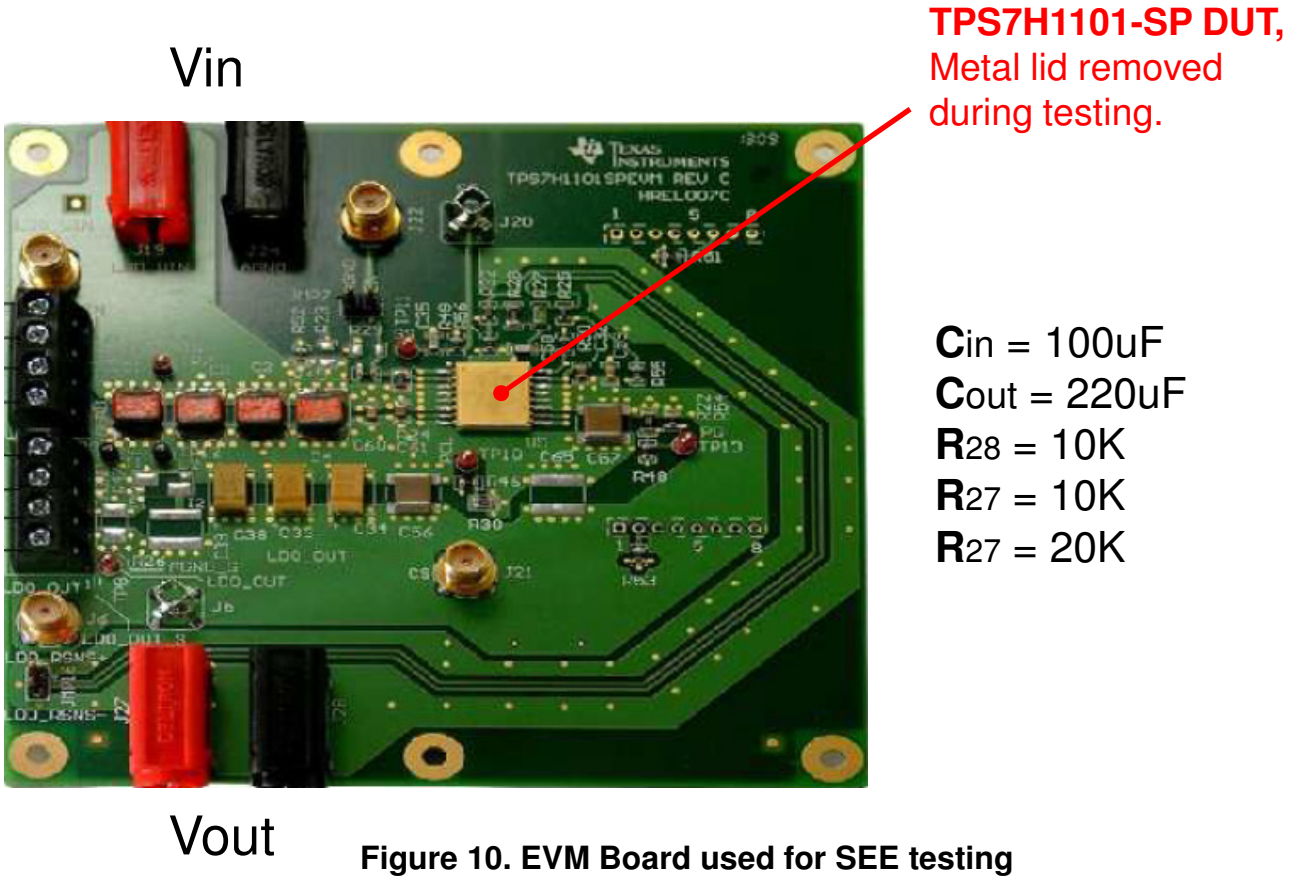


Figure 10. EVM Board used for SEE testing

The complete EValuation Module (EVM) is attached as appendix A, including schematics. Input capacitor to the LDO was an onboard total of 100uF, while the output capacitance of the LDO was 220uF. The output voltage was set by changing out R27. With R27 set at 10K the output voltage was 1.2Volts, and with R27 set at 20K, the output voltage was 1.8 Volts. The feedback/voltage set divider can be found in Appendix A.

3.1 Single Event Effects Testing (1st round)

The TPS7H1101-SP was evaluated against Heavy Ion exposure from the Texas A&M University 88-inch Cyclotron on December 3, 2012. A 15 MeV/amu beam line was used with the ions shown in table 1. The LET show below was an effective LET measurement from the beam line equipment. Zero degree " incident" and 45 degree angles were used to vary the effective LET on the three selected ions in Table 1. Available beam characteristics are show in Figure 11.

Ion	Total Energy (MeV)	LET (MeV-cm²/mg)	Range in Si (µm)
^{84}Kr	1259	28.2	170
^{129}Xe	1934	52.1	156
^{165}Ho	2475	69.8	112

Table 1. Heavy ion selection

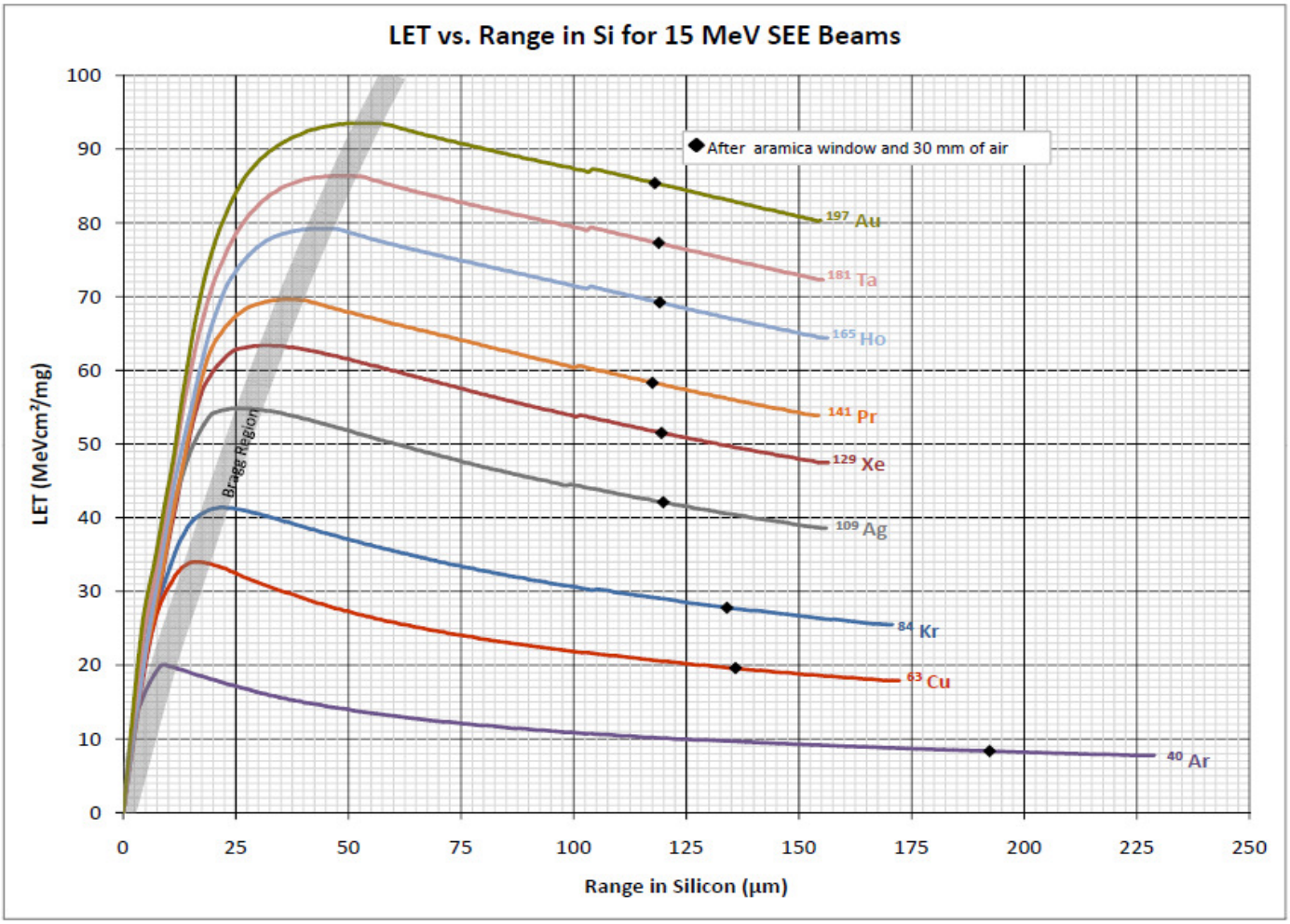


Figure 11. TAMU Cyclotron 15 A MeV Beam Characteristics

3.2 Single Event Effects Run Log

The TPS7H1101-SP Heavy Ion Run Log is show in Table 2. LET ion values range from ~ 28 MeV-cm^2/mg to 100 MeV-cm^2/mg. SET events were defined as V_{out} changes of >10%, while SEFI events were determined by a logic level transition of the Power Good (PG) signal.

ION LET	Device	Temp (deg C)	VIN	VOUT	FLUX	FLUENCE	LOAD	Looked at	Events	Xsection
Kr (28.2 MeV)	1	27	1.5	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (28.2 MeV)	1	27	1.5	1.2	1.00E+04	1.00E+06	430mA	PG	0	0.00E+00
Kr (28.2 MeV)	1	27	3	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (28.2 MeV)	1	27	5	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (28.2 MeV)	1	27	6	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (39.9 MeV)	1	27	1.5	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (39.9 MeV)	1	27	6	1.2	1.00E+04	1.00E+06	430mA	VOUT	0	0.00E+00
Kr (39.9 MeV)	5	27	3	1.8	1.00E+04	1.00E+06	2.5 A	VOUT	0	0.00E+00
Kr (39.9 MeV)	5	27	4	1.8	1.00E+04	1.00E+06	2.5 A	VOUT	0	0.00E+00
Kr (39.9 MeV)	4	27	7	5	1.00E+04	1.00E+06	2.86 A	VOUT	0	0.00E+00
Kr (39.9 MeV)	4	27	5.5	5	1.00E+04	1.00E+06	2.86 A	VOUT	0	0.00E+00
Xe(73.7 MeV)	4	27	7	5	1.00E+04	1.00E+06	2.86 A	VOUT	0	0.00E+00
Xe(73.7 MeV)	4	27	7	5	1.00E+04	1.00E+06	2.86 A	VOUT	0	0.00E+00
Xe(73.7 MeV)	4	27	5.6	5	1.00E+04	1.00E+06	2.86 A	VOUT	0	0.00E+00
Xe(73.7 MeV)	3	27	2	1.2	1.00E+04	1.00E+06	2.5 A	VOUT	2	2.00E-06
Xe(73.7 MeV)	3	27	2	1.2	1.00E+04	1.00E+06	2.5 A	PG	1	1.00E-06
Xe(73.7 MeV)	3	27	1.5	1.2	1.00E+04	1.00E+06	2.5 A	VOUT	8	8.00E-06
Xe(73.7 MeV)	3	27	2	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	34	3.40E-06
Xe(73.7 MeV)	3	27	2.5	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	24	2.40E-06
Xe(73.7 MeV)	3	27	3	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	17	1.70E-06
Xe(52.1 MeV)	3	27	1.5	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	6	6.00E-07
Xe(52.1 MeV)	3	27	2	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	12	1.20E-06
Xe(52.1 MeV)	3	27	2.5	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	7	7.00E-07
Xe(52.1 MeV)	3	27	3	1.2	1.00E+05	1.00E+07	2.5 A	VOUT	4	4.00E-07
Ho (98.9 MeV)	3	27	1.5	1.2	1.00E+05	1.00E+07	2.5 A	PG	92	9.20E-06
Ho (98.9 MeV)	3	27	1.5	1.2	1.00E+04	1.00E+06	2.5 A	VOUT	58	5.80E-05
Ho (69.8 MeV)	3	27	1.5	1.2	1.00E+04	1.00E+06	2.5 A	VOUT	4	4.00E-06
Ho (98.9 MeV)	3	27	7	1.2	1.00E+04	1.00E+06	0	VOUT	5	5.00E-06
Ho (98.9 MeV)	3	27	7	1.2	1.00E+05	1.00E+07	0	VOUT	20	2.00E-06
Ho (98.9 MeV)	3	27	7	1.2	1.00E+05	1.00E+07	0	PG	11	1.10E-06
Ho (98.9 MeV)	3	125	7	1.2	1.00E+05	1.00E+07	0	PG	0	0.00E+00
Ho (98.9 MeV)	3	125	1.5	1.2	1.00E+04	1.76E+06	2.5 A	VOUT	38	2.16E-05
Ho (98.9 MeV)	4	27	7	5	1.00E+04	1.00E+06	2.9 A	VOUT	0	0.00E+00

Table 2. Heavy Run Log

Numbers in red were adjusted based on data from the captured plots.

The TPS7H1101-SP was SEE tested under various V_{in} and V_{out} conditions, as well as load conditions of 0A – 3A load. The external filter capacitor value used was 220uF. SEL and SEB testing included maximum input voltage of 7V @ room and at 125°C, as well as high and low V_{out} values. Total fluence for each of these runs reached 1E7 ions/cm^2 using ^{165}Ho ion at a 45 degree angle, providing an effective LET ~ 100 MeV-cm^2/mg

No SET or SEFI's were observed at LET $\leq$ 40 MeV-cm^2/mg. The first observable event was using ^{129}Xe with an effective LET ~ 52 MeV-cm^2/mg. Onset LET is somewhere between 40 and 52 MeV-cm^2/mg. This suggests the device is immune to a LEO proton environment.

Figure 12 is a cross section plot of SET and SEFI events combined. The saturated cross section approaches 1.0E-04 cm^2. Figure 13 illustrates a SET event, where a V_{out} change of > 10% occurs causing the trigger of the Power Good signal. Figure 13 illustrates a SEFI event triggering a soft start event.

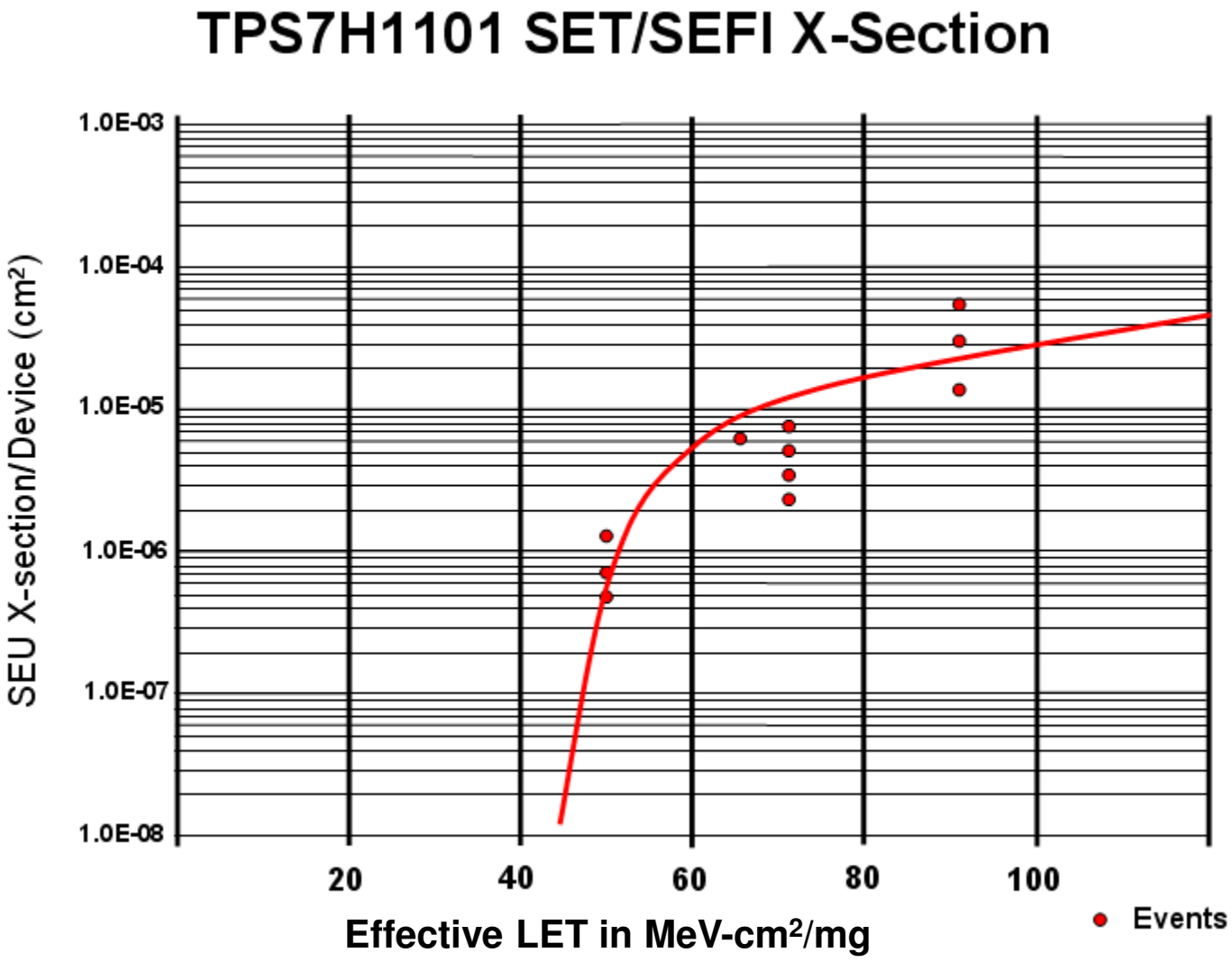


Figure 12. Weibull Cross Section Fit

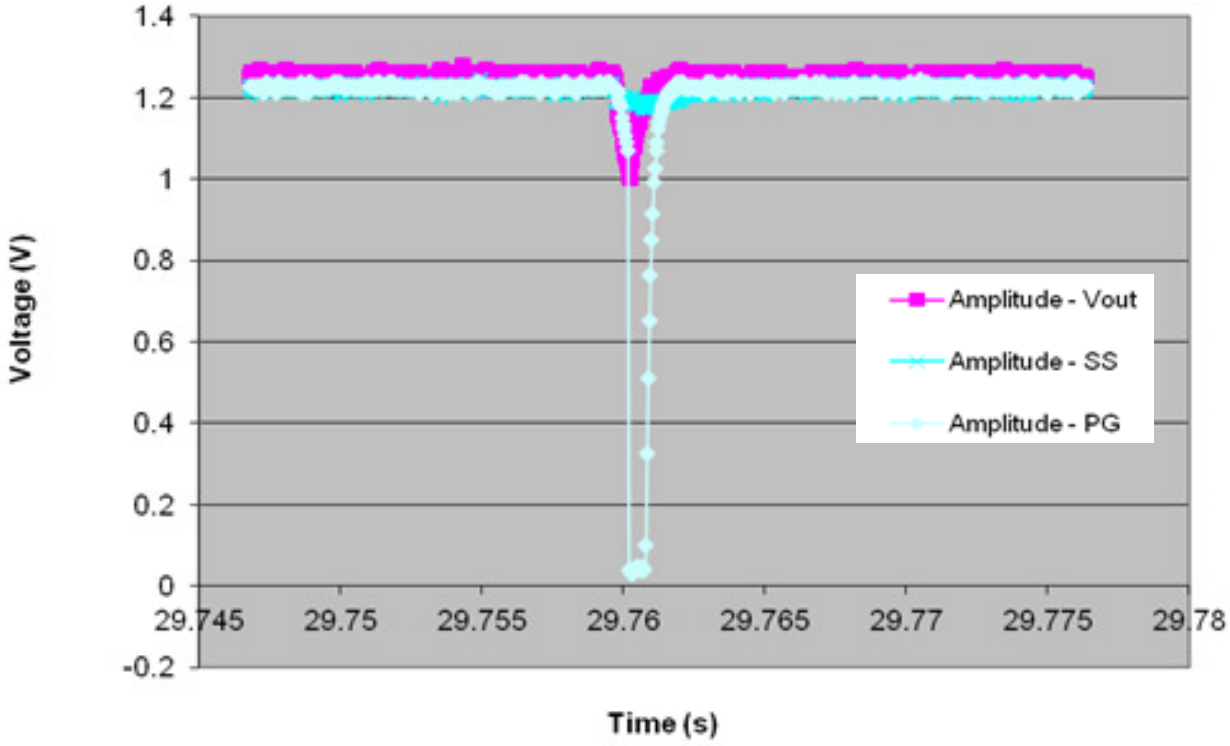


Figure 12. SET causing Power Good Signal Transition

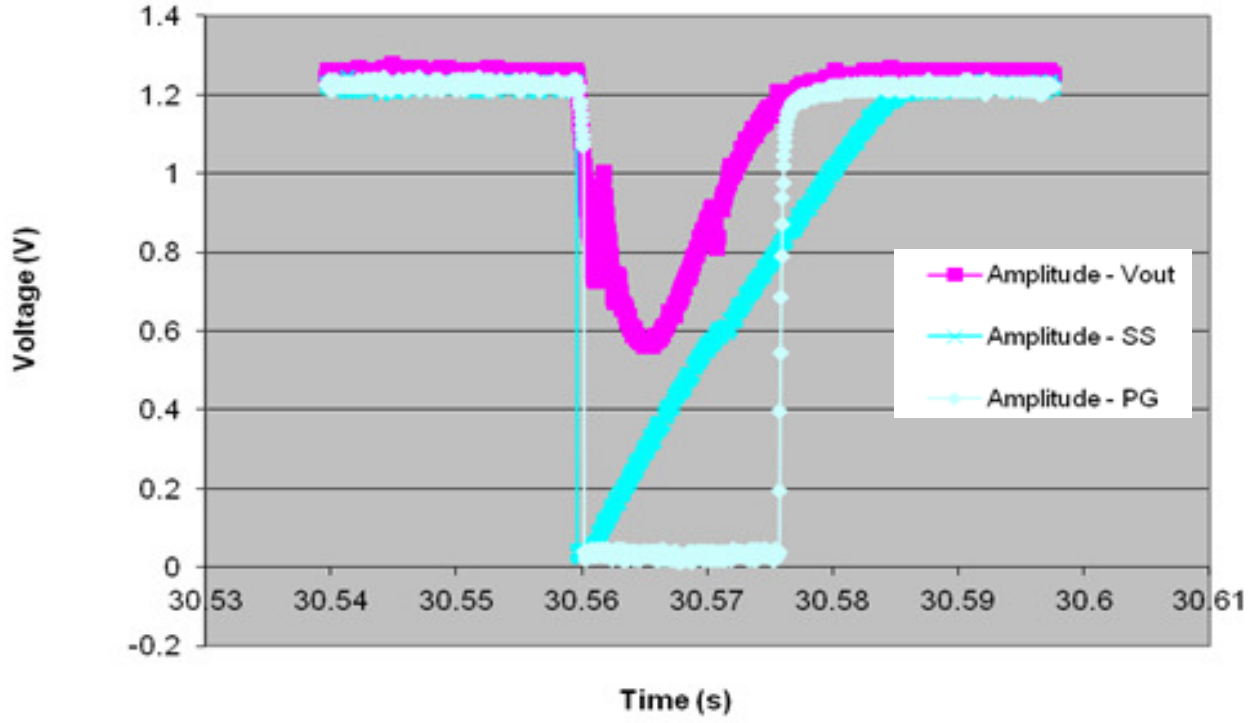


Figure 13. SEFI Producing Soft Start event

4.0 Single Event Effects (2nd round)

The TPS7H1101-SP was evaluated against Heavy Ion exposure from the Texas A&M University 88-inch Cyclotron on November 11, 2013 to collect additional heavy ion data around the onset threshold of 40 MeV-cm^2/mg. The trigger point for detecting upsets was lowered to 5% and 2% of Vout rather than 10%, and any positive transients of Vout was monitored. There were no upsets observed below the 40 MeV-cm^2/mg onset threshold at either a 2% or 5% change of Vout.

The 15 MeV/amu beam line was used with the ions shown in table 3. The LET show below was an effective LET measurement from the beam line equipment. Zero degree " incident" and 45 degree angles were used to vary the effective LET on the two selected ions in Table 3.

Ion	Total Energy (MeV)	LET (MeV-cm^2/mg)	Range in Si (µm)
^{84}Kr	1259	28.8	170
^{197}Au	2954	86.3	155

Table 3. Heavy ion selection

The run log of the November 11th 2013 is shown in Table 4. ^{84}Kr was used at a 45 degree angle and produced an effective LET of 40.7 MeV-cm^2/mg. No trigger events were detected at this LET. A ^{197}Au ion was used at the beginning of the test to determine the proper operation of the setup, and did correlate to the previous TAMU tests.

TEST	Run	Time	Distance	Temp	Ion/LET	Beam Angle	Flux	Fluence	Vin	Vout	Load	Events	Notes
SEU	62	7:00	30mm	25	Au/82MeV	0	1.00E+04	1.00E+06	1.5V	1.2V	2.9A	22	Trigger 5% of Vout, capture SS/PG/Vout
SEU	64	7:26	30mm	25	Kr/40 MeV	45	1.00E+04	1.00E+06	1.5V	1.2V	3A	0	Trigger 5% of Vout, capture SS/PG/Vout
SEU	65	7:29	30mm	25	Kr/40 MeV	45	1.00E+04	1.00E+06	1.5V	1.2V	3A	0	Trigger 2% of Vout, capture SS/PG/Vout
SEU	66	7:34	30mm	25	Kr/40 MeV	45	1.00E+04	1.00E+06	1.5V	1.2V	3A	0	Trigger PG (50%), capture SS/PG/Vout

Table 4 Heavy ion selection

5.0 Summary

During the 1st round of SEE testing It was determined that there were no upsets on Vout with the Vout threshold trigger set at +\- 10% delta Vout at or below the onset threshold of 40.7 MeV-cm^2/mg. No trigger events were detected at this LET, which verified previous SET testing that showed no upsets at a LET of $\leq$ 40.7 MeV-cm^2/mg.

During the 2nd round of SEE testing the output was again checked for any positive going SET events. (This is where the output will go higher than the set point of Vout.) No positive going transients were observed. The detection trigger point of Vout was set to +\-5% and then +\- 2% delta Vout. No observed SET/SEFI 's were observed at or below the onset threshold of 40.7Mev-cm^2/mg. At higher LET's only negative going SET/SEFI events were observed. (a droop in Vout)

In order to upset high, the gate of the PMOS pass element during SET must be pulled down. The design uses an asymmetrical gate driver for the PMOS pass element. i.e. The driver can source a lot more current than it is able to sink. If you pull down the input of the gate driver there is a time constant associated with slewing or drawing down the gate charge of the pass element. This time is dictated by a fixed pull down current source and the overall gate capacitance of the pass element (I/C = dV/dt). The time needed to discharge significant gate charge (the voltage) is much greater than the time duration of our modeled critical charge produced for a LET of 85 MeV-cm^2/mg. This means that the charge injection associated with a heavy ion strike producing a LET of 85 MeV-cm^2/mg is of insufficient time duration to cause a significant droop on the gate voltage (not enough charge is removed from the equivalent gate capacitance). A strike on the output of the gate driver also meets a similar fate as there is simply not enough charge removed from the gate capacitance to cause a SET. This is the reason we don't see SET events going high during Single Event testing.

It should be noted though, that large inductive loads may produce a back EMF that will push the output of the LDO high. The LDO has limited current sink capabilities, nor crowbar capability when the output is forced higher than the Vout set point. The LDO is ideally suited for radiation applications such as Medical and Industrial X-Ray, nuclear power plants, high altitude avionics, and space.

Appendix A

TPS7H1101SPEVM User's Guide

Contents

List of Figures

1 INTRODUCTION

This user's guide describes the characteristics, operation, and use of the TPS7H1101SP evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS7H1101SP ultra-low Dropout LDO regulator. It is rated for 3-A ultra low-dropout (LDO) voltage regulator. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the EVM.

1.1 Related Documentation

1. TPS7H1x01 Datasheet (SLVSAS4)

2 BACKGROUND

The TPS7H1101SPEVM helps designers evaluate the operation and performance of the TPS7H1101SP ultra low drop out regulator.

Table 1. Summary of Performance

TEST CONDITIONS	OUTPUT CURRENT RANGE
V_{IN} = 1.5 V to 7 V	Max 3 A

The evaluation module is designed to provide access to the features of the TPS7H1101. Some modifications can be made to this module to test performance at different input and output voltages, current and switching frequency. Please contact TI Field Applications Group for advice on these matters.

3 SAFETY

3.1 Eye Protection

Safety glasses are to be worn while performing all testing on the EVM.

3.2 General Risks

This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.

3.3 Electrostatic Discharge

ESD precautions must be followed while handling electronic assemblies.

3.4 Thermal/Shock Hazards

Precautions should be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

4 APPAREL

- Electrostatic smock
- Electrostatic gloves or finger cots
- Safety glasses
- Ground ESD wrist strap

5 EQUIPMENT

5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 7-V at 5-A or higher is required.

5.2 Load #1

Electronic load, i.e. Chroma 63640-80-80 module along with 63600-2 DC electronic load Mainframe or Decade Resistor Box.

5.3 Meters

Four (4) Fluke 75, (equivalent or better) or two (2) equivalent voltage meters and two (2) equivalent current meters.

The current meters must be able to measure 5 A current. Note: Shunt along with DVM can be used to monitor output current.

5.4 Oscilloscope

An Tektronix Oscilloscope, i.e. DPO 7104CCurrent Probe Tektronix TCP202 or equivalent.

6 BOARD LAYOUT

6.1 EVM Layout Flexibility

The EVM is layed out to provide flexibility for the customer evaluation thus providing test points and or cold nose probes to monitor various critical nodes of the design as highlighted in the schematic.

Additionally, placeholder is provided thus one can add esr in series with the output capacitor (R47 in series with C39) thus making it easier to evaluate performance with increased capacitor esr.

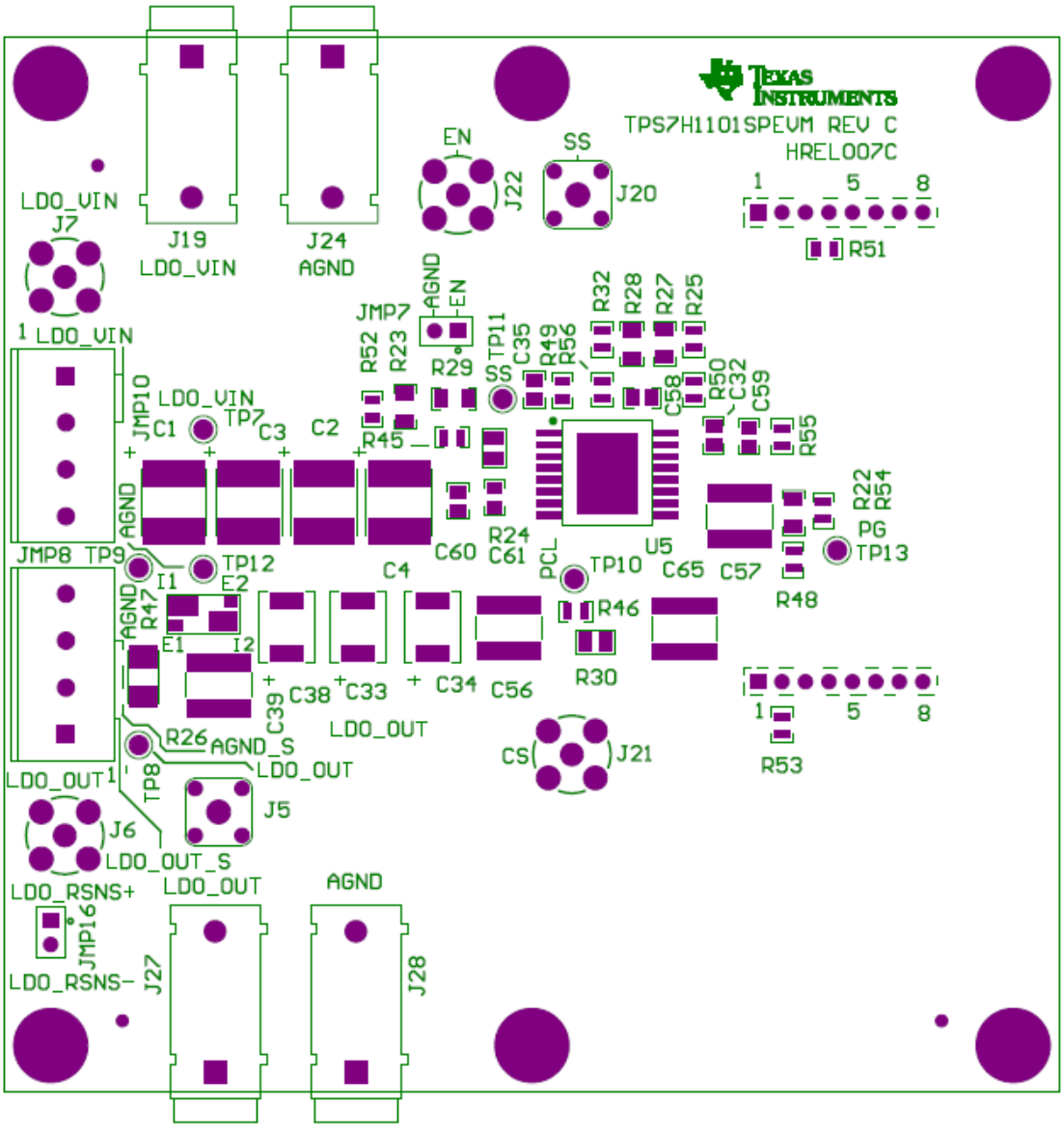


Figure 1. Component Placement (Top Side)

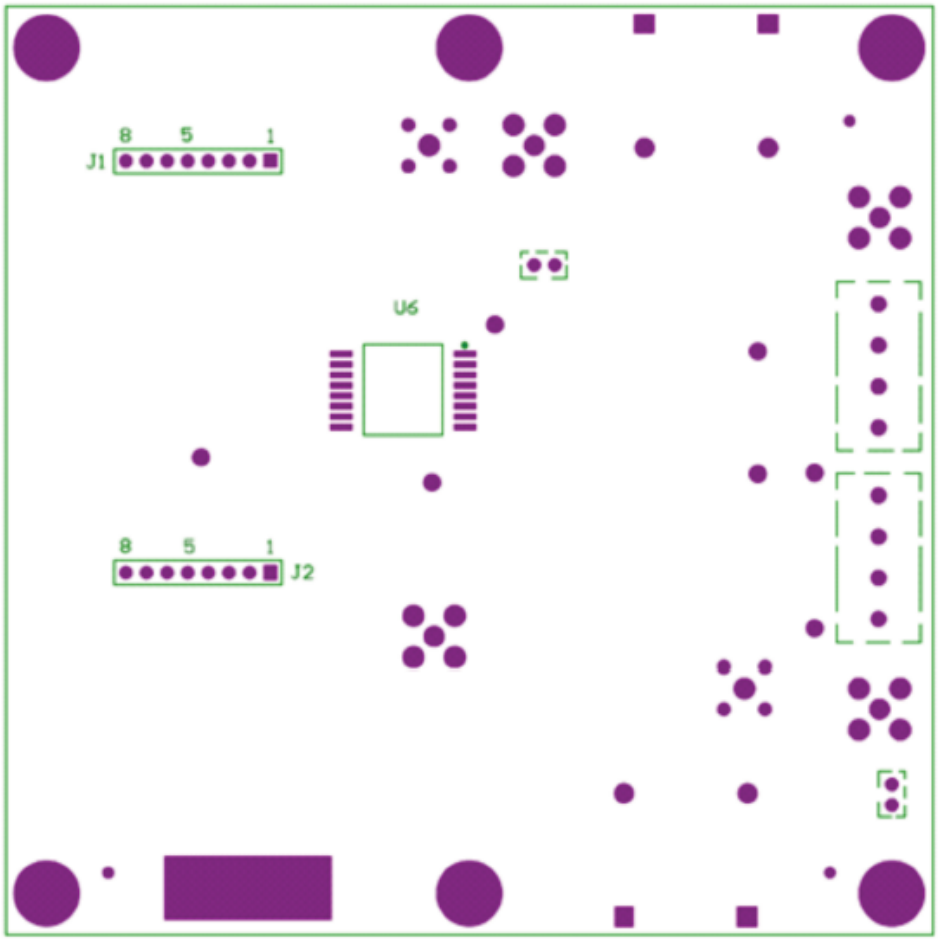


Figure 2. Component Placement (Bottom Side)

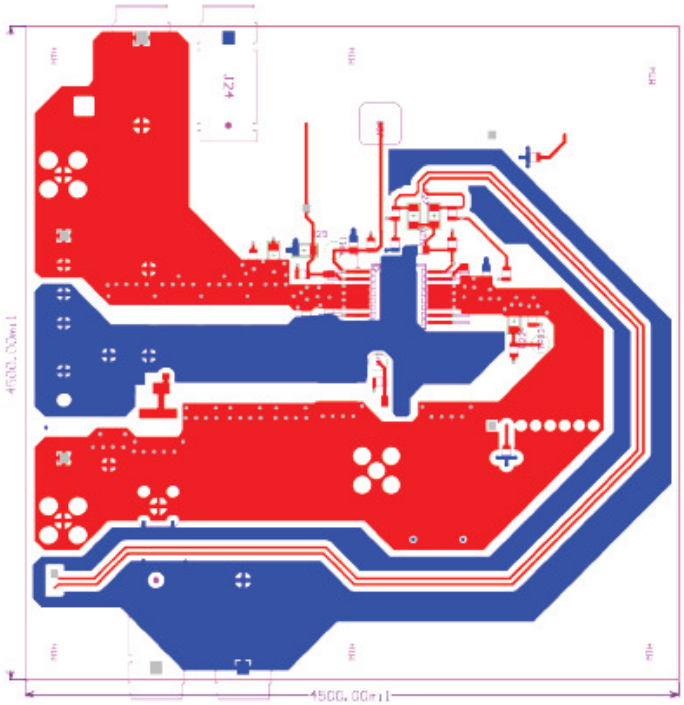


Figure 3. PCB Layout (Top Layer)

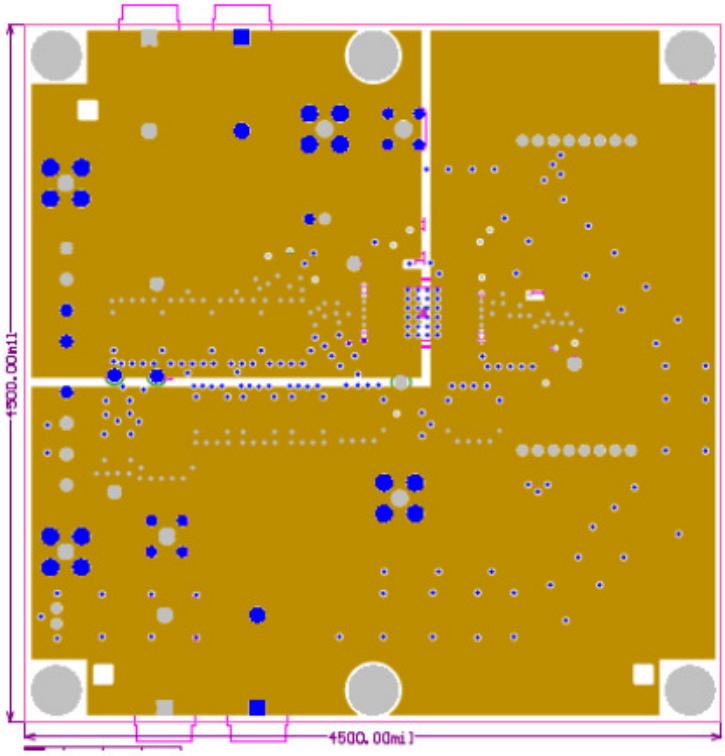


Figure 4. Board Layout - Second Layer (Mid Layer 1)

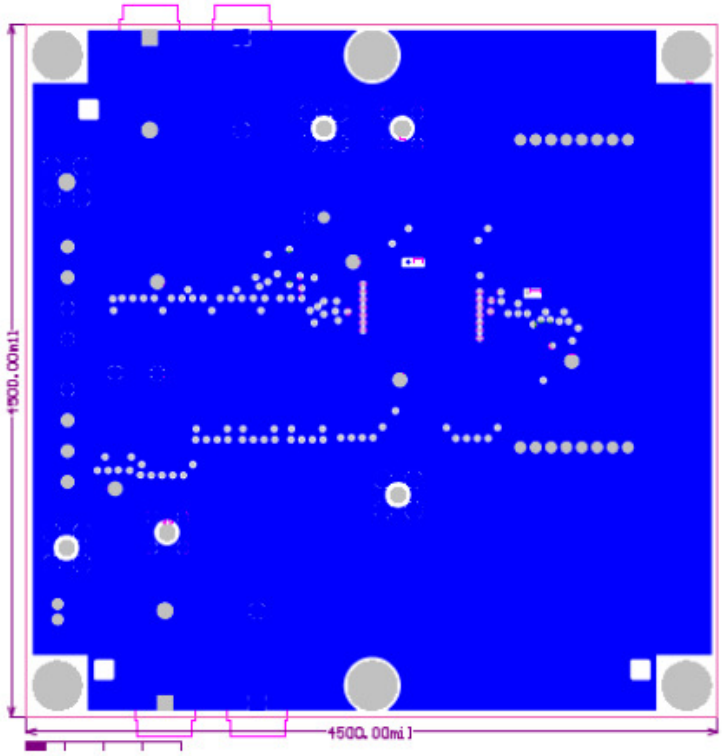


Figure 5. Board Layout - Third Layer (Mid Layer 2)

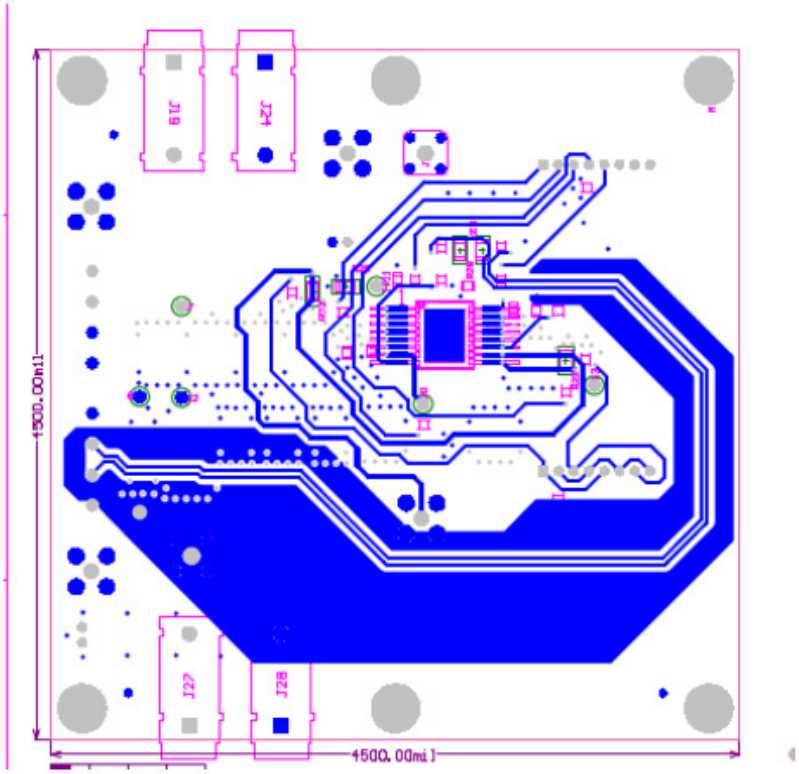


Figure 6. Board Layout - Fourth Layer (Bottom Layer)

7 BENCH TEST SETUP CONDITIONS

7.1 Headers Description and Jumper Placement

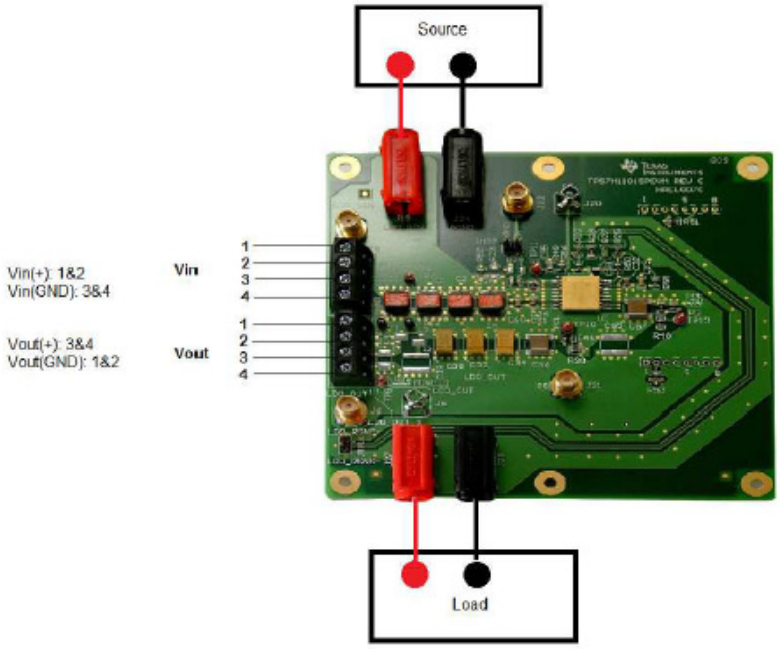


Figure 7. Headers Description and Jumper Placement

7.2 Testing

Table 2. Power Connectors

NO.	FUNCTION
J19	V_{IN} input voltage connector (see for V_{IN} range)
J24	V_{IN} input voltage connector to ground
J27	V_{OUT} output voltage connector
J28	V_{OUT} output connector to ground
J7	Vin_SMA
J22	EN_SMA
J20	SS_Probe
J5	LDO_OUT_Probe
TP8	LDO Vout measure point (+)
TP9	LDO Vout measure point (GND)
J6	LDO_OUT_SMA
TP7	LDO Vin measure point (+)
TP12	LDO Vin measure point (GND)
TP10	PCL
J21	CS_SMA
TP13	PGOOD
TP11	SS
JMP10	V_{IN} alternative connection: 1,2 (+) and 3,4 (GND)
JMP8	V_{OUT} alternative connection 3,4 (+) and 1,2 (GND)

8 POWER-UP PROCEDURE

Table 3. Test Results

	V_{OUTMIN}	V_{OUTMAX}	CURRENT LIMIT	CURRENT FEEDBACK	
V_{OUT} = 1.8 V	1.76 V	1.836 V	< 3.8 A	< 1.9 A	OUTPUT SET POINT
I_{OUT} = 3 A	1.8166 V		3.5 A		CURRENT LIMIT

8.1 I_{OUT} and V_{OUT} Measurements

1. Make sure all power supplies in workstation are OFF.
2. Locate connectors J19 and J24.
3. Connect V_{IN}(+) to J19 and V(GND) to J24. Set it to 2.3 V.
4. Locate measure points TP7 and TP12.
5. Connect voltmeter: V_{IN}(+) to TP7 and V(GND) to TP12.
6. Locate connectors J27 and J28 and connect load here (be aware of polarities).
7. Locate measure points TP8 and TP9.
8. Connect voltmeter: V_{OUT}(+) to TP8 and V(GND) to TP9.
9. Output voltage should be per Table 1. This is done by setting R27 = 19.8 kΩ and R28 = 10 kΩ. V_{OUT} can be determined by equation highlighted below or per equation 1 in the datasheet.

$$V_{OUT} = \frac{(R_{27} + R_{28}) \bullet V_{REF}}{R_{28}} \quad (1)$$

Where V_{REF} = 0.605 V.

8.2 Output Current Limiting

A resistor value R30 connected from PCL pin to GND determines the output current limit set point based on Equation 2.

Maximum programmable current limit is 3800 mA.

$$R_{pcl} = R_{30} = \frac{CSR(V_{ref})}{PCL_{cl} - 0.0216} \quad (2)$$

Where V_{REF} = 0.605 V, PCL_{cl} = programmabe current limit (A), CSR = Current sense ratio (typical value = 47394).

CSR between I_{cs} pin and I_{OUT} can be measured as shown in Figure 8.

- Make sure all power supplies in workstation are OFF.
- Connect V_{IN}(+) to J19 & V(GND) to J24 and set it to 2.3 V.
- Set V_{OUT} to 1.8V. (R27 = 19.8 kΩ and R28 = 10 kΩ)
- Connect load as previously instructed, set it to zero.
- Increase I_{load} (steps of 0.100 A are suggested) until V_{load} starts to drop.
- Current limit trip point < 3.8 A (1101SP).

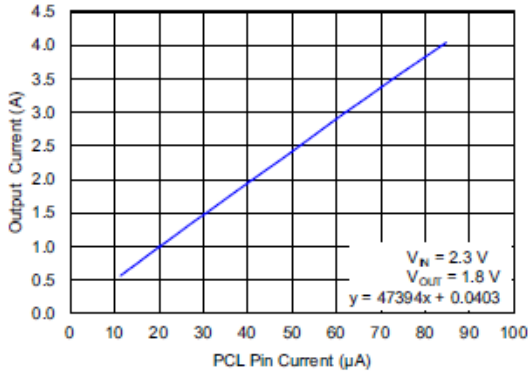


Figure 8. I_{OUT} (A) vs I_{PCL} (A)

8.3 High Side Current Sense

Monitoring the voltage at the CS pin will indicate voltage proportional to the output current. Figure 9 shows typical curve V_{CS} vs I_{OUT} for Vin = 2.28 V and R23 = 3.65 kΩ. A resistor connected from current sense (CS) pin to V_{IN} indicates voltage proportional to the output current.

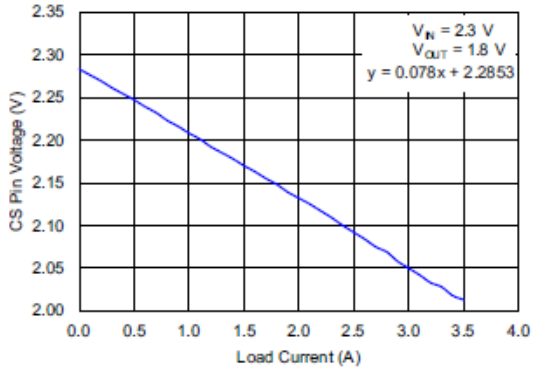


Figure 9. V_{CS} (V) vs I_{OUT} (A)

Monitoring current in CS pin (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMosFET and the current sense Mosfet as shown in Figure 10.

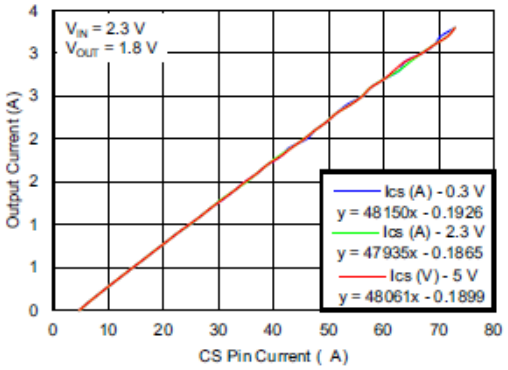


Figure 10. I_{OUT} (A) vs I_{CS} (A)

8.4 Current Foldback

1. When current sense (CS) pin is held high, foldback current limit is enabled. Shorting CS low will disable the foldback current limit.
2. With foldback current limit enabled, when current limit trip point is activated,

   (a) Output voltage will drop low

   (b) output current will fold back to approx. 50% of the current limit trip point. This results in minimizing the power loss under fault conditions.

8.5 Power Good

Power good pin is an open drain connection, connect it high via pull up resistor to external voltage source. Power Good pin indicates the status of the output voltage.

8.6 Dropout Voltage

Drop out voltage (V_{DO}) is the difference between the input voltage and output voltage needed to maintain regulation. V_{DO} vs I_{OUT} is highlighted in Figure 11.

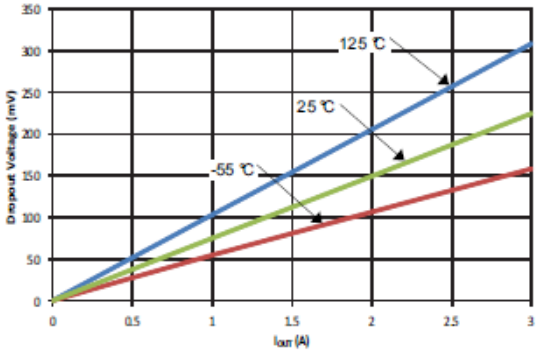


Figure 11. V_{DO} vs I_{OUT}

8.7 Transient Response

Waveforms below indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot / undershoot

Channel 2: Step load in current

Channel 3: Input voltage

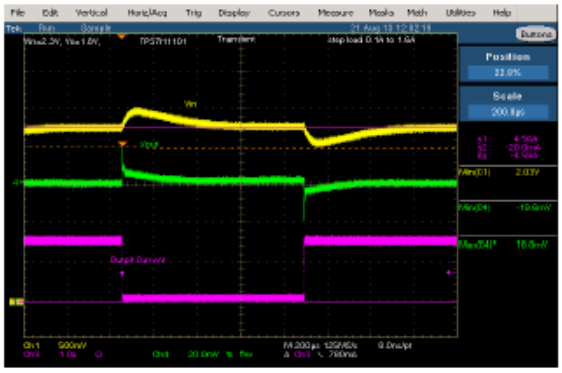


Figure 12. Load Transient Response: Step Load 0.1 A to 1.6 mA

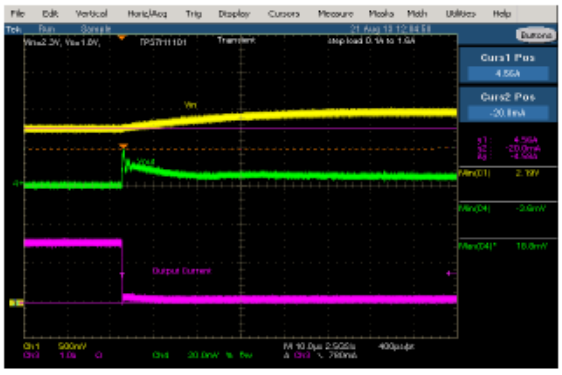


Figure 13. Expanded View Overshoot

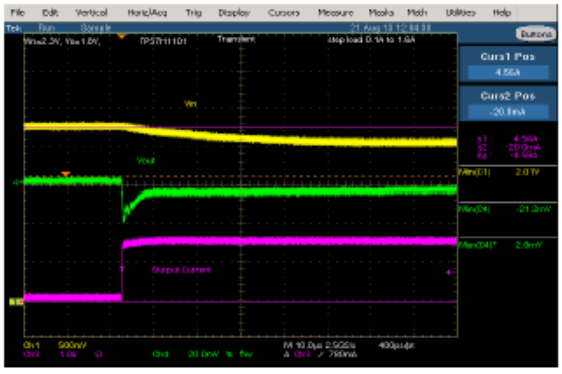


Figure 14. Expanded View Undershoot

8.8 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled.

- In parallel mode CS pin of LDO#1 must be connected to PCL pin of LDO#2 via a series resistor (3.75 kΩ) and CS pin of LDO#2 must be connected to PCL pin of LDO#1 via series resistor (3.75 kΩ).
- In parallel configuration R30 (resistor from PCL to GND) and R23 (resistor from CS pin to V_{IN}) must be left open (unpopulated).

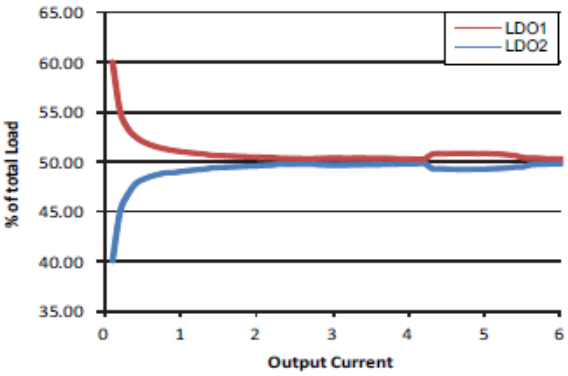


Figure 15. Current Sharing LDO_1 and LDO_2

8.9 Soft-Start

Connecting a capacitor on CS pin to GND (C_{35}) slows down the output voltage ramp rate. The soft-start capacitor will charge up to 1.2 V.

$$C_{35} = \frac{t_{ss} \bullet I_{ss}}{V_{REF}} \quad (3)$$

Where:

t_{ss} = Soft-start time

I_{ss} = 2.5 µA

V_{REF} = 0.605 V

8.10 Enable/Disable

EVM can be disabled via pulling the enable pin low via shorting JMP7-1 (Enable) to JMP7-2 (GND). Enable pin is tied high to V_{IN} via R24 (20 kΩ) resistor, thus keeping the EVM enabled.

Alternately, EVM can also be disabled via pulling SS pin (U6 pin 1) low via an external circuit comprising of 2N7002 MOSFET as shown in Figure 16. A high signal at the gate of Q100 will discharge the SS pin and disable the device.

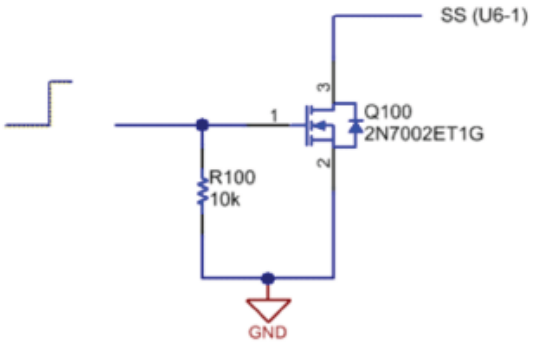


Figure 16. Disabling the LDO via Soft-Start Pin

8.11 Turn-Off

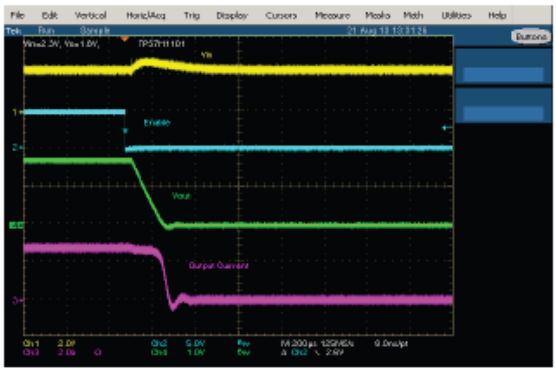


Figure 17. Turn-Off

8.12 Output Noise

Output noise is measured using HP3495A. For details on the setup see "Output Noise Measurement Setup" document. Plots below shows noise in μV/√Hz vs Frequency.

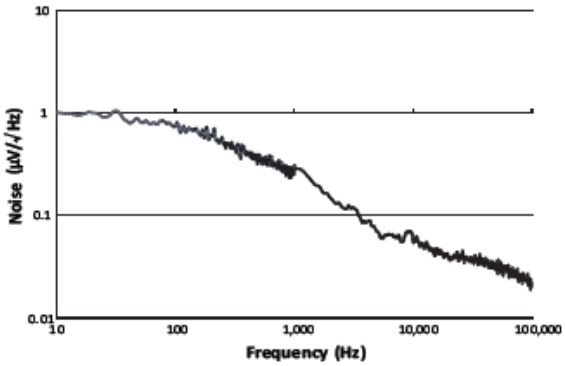


Figure 18. RMS Noise (10 Hz - 100 kHz) = 20.33 μVrms, V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A.

9 SCHEMATIC AND BILL OF MATERIALS

The following pages contain the TPS7H1101HTEVM schematic and bill of materials.

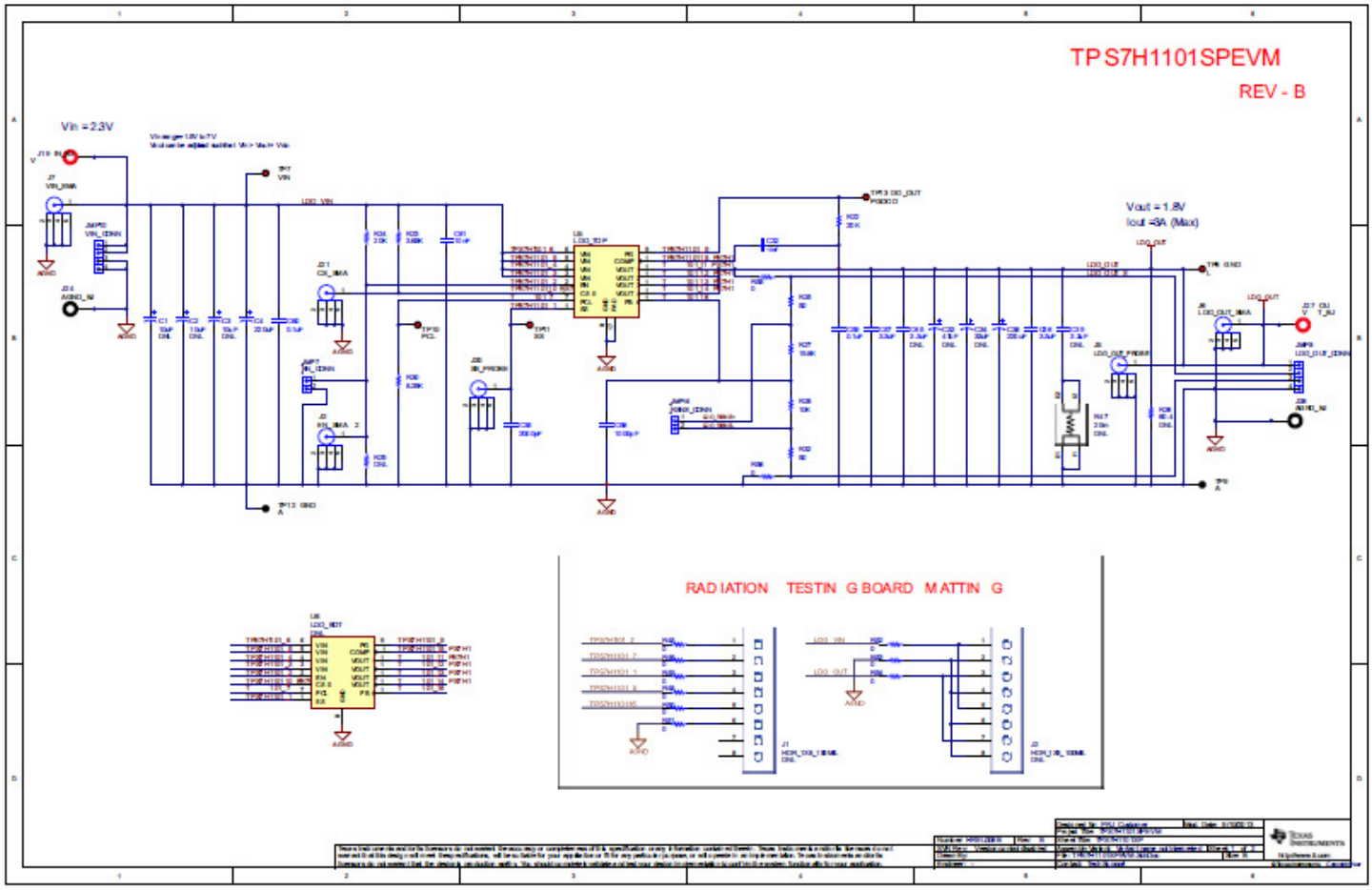


Figure 19. TPS7H1101SPEVM Schematic

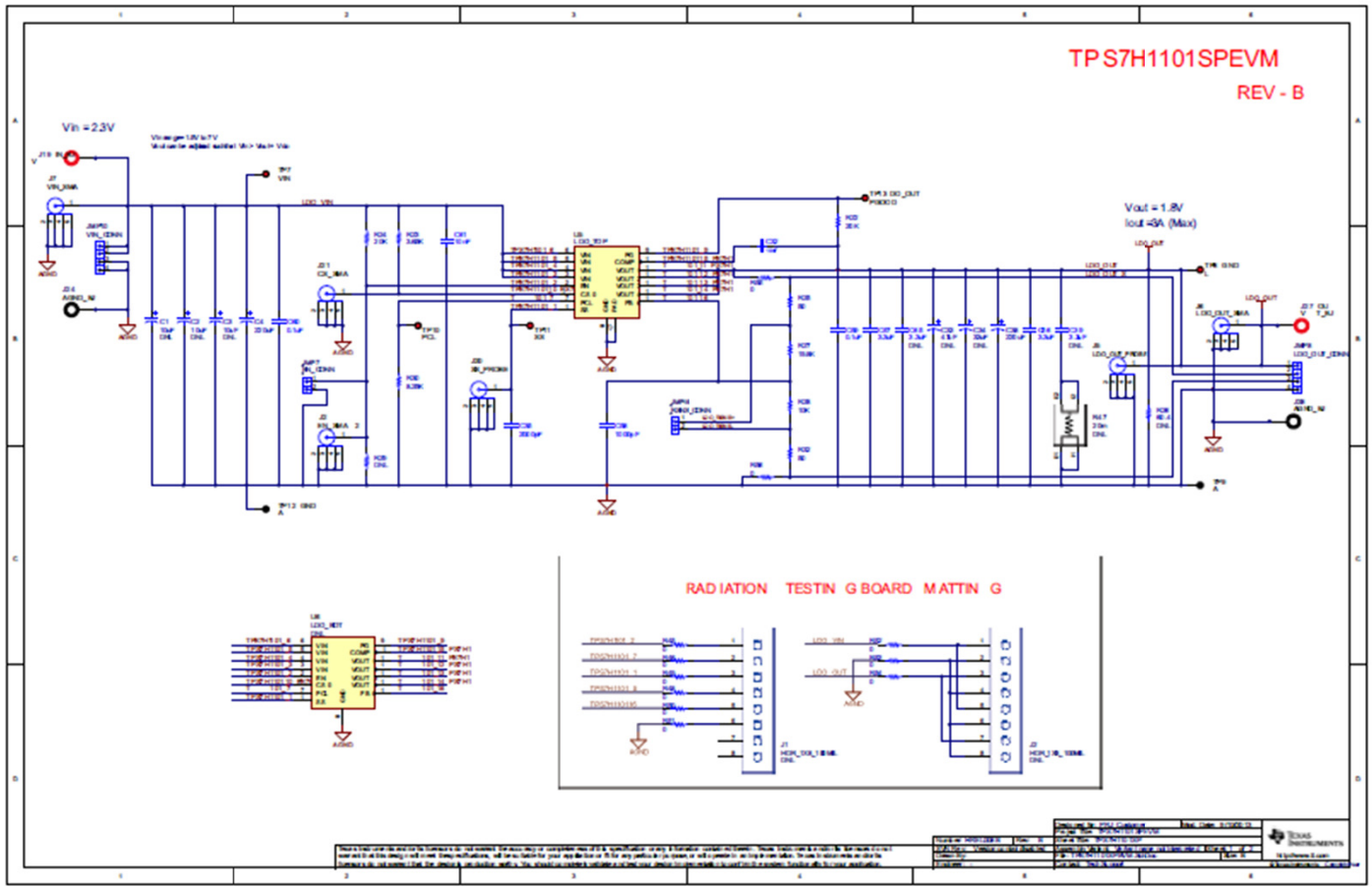


Figure 19. TPS7H1101SPEVM Schematic

Table 4. TPS7H1101SPEVM Bill of Materials

Item No.	Qty	Designator	Value	Footprint	Manufacturer	Part No.	Description
1	1	C4	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
2	2	C32,C61	10nF	0805	Kemet	C0805C103K3RACTU	CAP CER 10000PF 25V 10% X7R 0805
3	1	C35	2000pF	0805	Kemet	C0805C202J3GACTU	CAP CER 2000PF 25V 5% NP0 0805
4	1	C38	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
5	2	C56,C57	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
6	1	C58	1000pF	0805	Kemet	C0805C102J3GACTU	CAP CER 1000PF 25V 5% NP0 0805
7	2	C59,C60	0.1uF	0805	Kemet	C0805C104K3RACTU	CAP CER 0.1UF 25V 10% X7R 0805
8	1	J5			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
9	1	J6			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
10	1	J7			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
11	1	J19			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
12	1	J27			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
13	1	J20			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
14	1	J21			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
15	1	J22			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
16	2	J24,J28			DEM Manufacturing	571-0100	Standard Banana Jack, insulated, 10A, black
17	1	JMP7		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
18	1	JMP8		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
19	1	JMP10		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
20	1	JMP16		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
21	1	R22	20kΩ	1206	Stackpole	RNCP1206FTD20K0	RES 20K OHM 1/2W 1% 1206 SMD
22	1	R23	3.65kΩ	1206	Panasonic	ERJ-8ENF3651V	RES 3.65k, 1/4W, 1%, 100ppm/C 1206
23	1	R24	20kΩ	0805	Stackpole	RNCP0805FTD20K0	RES 20K OHM 1/4W 1% 0805 SMD
24	2	R25,R32	50Ω	0603	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
25	1	R27	19.8kΩ	1206	Stackpole	RNCF1206BTE19K8	RES 19.8K OHM 1/8W 0.1% 1206
26	1	R28	10kΩ	1206	Stackpole	RNCS1206BKE10K0	RES 1/8W 10K OHM 0.1% 1206
27	1	R30	49.9kΩ	0805	Stackpole	RMCF0805FT49K9	RES 49.9K OHM 1/8W 1% 0805 SMD
28	11	R45,R46,R48, R49,R50,R51, R52,R53,R54, R55,R56	0Ω	0603	Panasonic	ERJ-3GEY0R00V	RES 0.0 OHM 1/10W 0603 SMD
29	1	TP7			Keystone	5000	Test Point, TH, Miniature, Red
30	1	TP8			Keystone	5000	Test Point, TH, Miniature, Red
31	2	TP9,TP12			Keystone	5001	Test Point, TH, Miniature, Black
32	1	TP10			Keystone	5000	Test Point, TH, Miniature, Red
33	1	TP11			Keystone	5000	Test Point, TH, Miniature, Red
34	1	TP13			Keystone	5000	Test Point, TH, Miniature, Red

Table 4. TPS7H1101SPEVM Bill of Materials (continued)

Item No.	Qty	Designator	Value	Footprint	Manufacturer	Part No.	Description
35	1	U6		CFP (HKS)	Texas Instruments	TPS7H1201SHKS	IC installed as lid down at the back of the board
36	4				Keystone	2029K-ND	Standoffs
37	4				Pencom	4-40X1/4PH-PN-MS-SS	Screws for standoffs
38	1		HREL008		Any	HREL008	PCB
39	1				Brady	THT-13-457-10	Label on the EVM under TI logo = TPS7H1201HTEVM
							HREL008-001
40	0	C1,C2,C3	10uF	7260-38_1	Vishay	T95R106K050LSAL	CAP TANT 10UF 50V 10% 2824
41	0	C33	47uF	7260-38	Kemet	T491X476M035AT	CAP TANT 47UF 35V 20% 2917
42	0	C34	33uF	7260-38	Kemet	T491X336K035AT	CAP TANT 33UF 35V 10% 2917
43	0	C39,C65	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
44	0	J1,J2	HDR_1X8_100MIL	HDR_1X8_BCS	SAMTEC	BCS-108-F-S-TE	SKT 8 POS 2.54mm Solder ST Thru-Hole
45	0	R29	DNL	1206	TBD	TBD	TBD
46	0	R26	60.4Ω	2010	Rohm	MCR50JZHF60R4	RES 60.4 OHM 1/2W 1% 2010 SMD
47	0	R47	20mΩ	RES_Y14870R02000B0R	VISHAY	Y14870R02000B0R	Current sensing chip resistor, 20m OHM, 0.1%
48	0	U5		CFP (HKR)	Texas Instruments	TPS7H1101SHKR	IC installed as lid up at the top of the board

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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