e-book

An Engineer’s Guide to Low EMI in DC/DC Regulators

An overview of EMI management and mitigation techniques for DC/DC regulators

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Introduction

There's an inescapable requirement in most power-supply applications to reduce electromagnetic interference (EMI), so system designers must explore all avenues to reduce both conducted and radiated emissions. EMI is an increasingly vexing issue in a product's design and qualification cycle, and compliance with electromagnetic compatibility standards – for example, Comité International Spécial des Perturbations Radioélectriques (CISPR) 32 for multimedia equipment [1] and CISPR 25 for automotive applications [2] – is vitally important, as the efforts required to achieve compliance affect both product development costs and time to market.

Although the emergence of faster-switching power devices for DC/DC regulators provides an opportunity for increased switching frequencies and smaller sizes, the higher switch voltage and current slew rates (dv/dt and di/dt) that occur during switching transitions often exacerbate EMI, causing problems in the overall system. For example, the high switching speed of gallium nitride power devices can result in a 10-dB increase in EMI at high frequencies [3].

This e-book delves into EMI in significant detail, with an emphasis on conducted EMI specifically, to provide an understanding from both theoretical and practical standpoints. The content focuses largely on the management and mitigation of conducted emissions from DC/DC regulators, as the mitigation of conducted EMI generally supports better radiated EMI performance.

It will explain EMI propagation modes; the effects of circuit parasitics during power switching and associated EMI behaviors; and, lastly, EMI mitigation techniques for both isolated and nonisolated designs. The e-book includes presentations of several DC/DC circuits that highlight both system-level and integrated circuit-specific features used to avoid the majority of EMI problems.

About the author

Timothy Hegarty is a senior member of technical staff (SMTS) at Texas Instruments. With over 25 years of power-management engineering experience, he has written numerous articles, conference papers, seminars, application notes and white papers. His technical interests include EMI/EMC in power electronics systems, high-efficiency and high-power-density power conversion, and circuit topologies for power electronics.

Timothy Hegarty

Applications engineer, Buck Switching Regulators, Texas Instruments

Common terms

AE	Auxiliary or associated equipment
AF	Antenna factor
AL	Attenuator loss factor
ALSE	Absorber-lined shielded enclosure
AMN, AN	Artificial mains network, artificial network
ANSI C63.4	American National Standards Institute
AVG	Average
BB	Broadband
BCM	Boundary conduction mode
CCM	Continuous conduction mode
CE Mark	Conformité Européene
CE, RE	Conducted emissions, radiated emissions
CENELEC	Comité Européene de Normalisation Électrotechnique
CISPR	Comité International Spécial des Perturbations Radioélectriques, an International Electrotechnical Commission (IEC) technical committee
CM, DM	Common mode, differential mode
CMRR	Common mode rejection ratio
CL	Capacitor-inductor
CS, RS	Conducted susceptibility, radiated susceptibility
DCM	Discontinuous conduction mode
DoC	Declaration of conformity
DRHA	Double ridge horn antenna
dBµV, dBµA	0 dBµV = 1 µV, 20 dBµA = 10 µA
EM	Electromagnetic
EMI	Electromagnetic interference
EMC	Electromagnetic compatibility
EPC	Equivalent parallel capacitance
EUT	Equipment under test
dv/dt	Voltage rate of change
di/dt	Current rate of change
EN	European norm
EN 55022	European standard, a modified derivative of CISPR 22 prepared by the Comité Européen de Normalisation Électrotechnique (CENELEC) and ratified by the European Union (EU)
ESA	Electronic subassembly
ESL	Equivalent series inductance
ESR	Equivalent series resistance
EU	European Union
EUT	Equipment under test
FCC Part 15	Federal Communications Commission; Part 15 subpart B applies to unintentional radiators
FCOL	Flip chip on lead
FFT	Fast Fourier transform

FM	Frequency modulation
GaN	Gallium nitride
GLONAS	Global navigaton satellite system
IC	Integrated circuit
IEC	International Electrotechnical Commission
ITE	Information technology equipment
LC	Inductor-capacitor
LLC	Inductor-inductor-capacitor
LISN	Line impedance stabilization network
MOSFET	Metal oxide semiconductor field effect transistor
NB	Narrowband
OATS	Open-area test site
UNECE	United Nations Economic Commission for Europe
PCB	Printed circuit board
PE, GW	Protective earth, green wire (both refer to earth or chassis ground)
PGND	Power ground
PK	Peak
PSR	Power supply rejection
QP	Quasi-peak
RBW	Resolution bandwidth (of the EMI receiver/spectrum analyzer)
RC	Resistor-capacitor
RF	Radio frequency
RLC	Resistor inductor capacitor
RM	Rectangular modulus (magnetic core)
SA	Spectrum analyzer
SAC, FAR	Semi-anechoic chamber, fully anechoic room
SGND	Signal ground, secondary ground
SEPIC	Single-ended primary inductance converter
SiC	Silicon carbide
SRF	Self-resonant frequency
SSFM	Spread spectrum frequency modulation
SW	Shortwave

Table 1. *Common acronyms, abbreviations and units related to EMI and EMC.*

1. Standards requirements and measurement techniques

Electromagnetic energy, whether intentionally or unintentionally generated, results in electromagnetic interference (EMI) with other equipment. Commercial products are designed to minimize the amount of electromagnetic energy produced during normal operation.

Numerous governing bodies throughout the world regulate the permissible level of conducted and radiated EMI generated by an end product. Applicable measurement techniques quantify such emissions so that you can take appropriate steps to achieve regulatory compliance.

While electromagnetic compatibility (EMC) requirements generally pertain to complete systems measured on AC power lines (and signal lines), a DC/DC regulator is a subcomponent for which no specified EMC limits exist. However, you can perform pre-compliance testing to determine whether EMI will be an issue.

This chapter:

- Reviews relevant standards for both industrial and automotive end equipment.
- Explains associated measurement techniques.
- Describes a measurement system setup that includes a line impedance stabilization network (LISN) and an EMI receiver.
- Presents a practical measurement system from a pre-compliance lab testing environment.

EMC regulatory specifications

EMC refers to the ability of a system or its constituent components to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment. Because the effects of interference can pose severe consequences, EMC is a frequent subject of national and international regulation [4].

Within the European Union (EU), power-supply products marketed for multimedia markets have used the European Norm (EN) 55022/Comité International Spécial des Perturbations Radioélectriques (CISPR) 22 product standard [5] to show conformance for both conducted and radiated emissions, with the conducted emissions (CE) declaration of conformity (DoC) for external power supplies referencing this standard to show conformance with the EU's EMC directive 2014/30/EU [6].

Products designed for North American markets have complied with limits established by the Federal Communications Commission Part 15. International Electrotechnical Commission (IEC) 61000-6-3 and IEC 61000-6-4 generic EMC standards apply to light industrial and industrial environments, respectively [7], [8].

For emissions, however, the EN 55032 product standard replaces and becomes an amalgamation of EN 55022 (information technology equipment), EN 55013 (broadcast receivers and associated equipment) and EN 55103-1 (audio and studio equipment). This new standard becomes effective as a harmonized emission standard in compliance with the EMC directive. More specifically, any product previously tested under EN 55022 that ships into the EU after March 2, 2017, must now meet the requirements of EN 55032.

As the EN 55022 standard is withdrawn and replaced by EN 55032, power-supply manufacturers and vendors need to update their DoC to the new standard in order to affix a valid CE marking logo. **Figure 1** shows the EN 55022/32 Class A and Class B limits for conducted emissions with quasi-peak (QP) and average (AVG) signal detectors over the applicable frequency range of 150 kHz to 30 MHz.

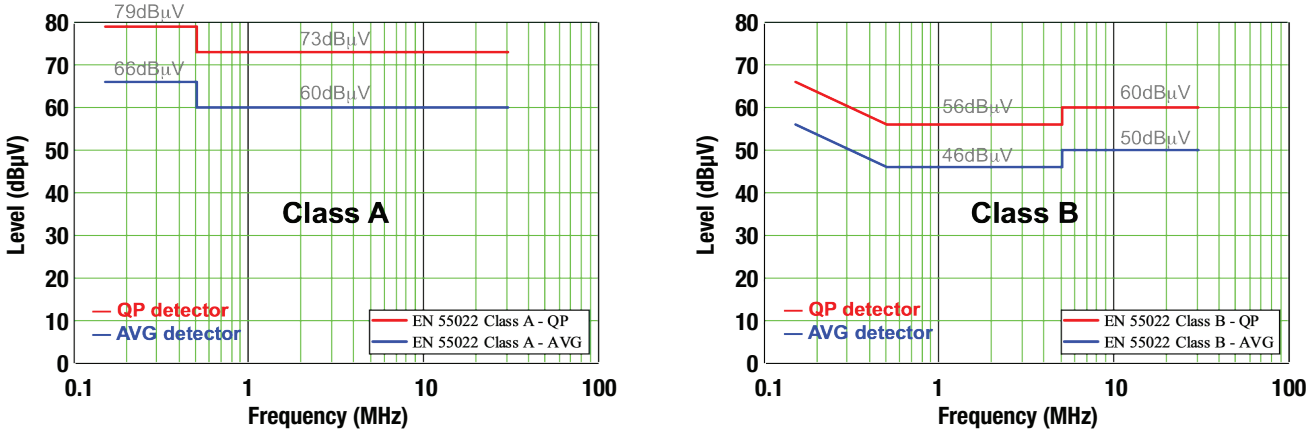


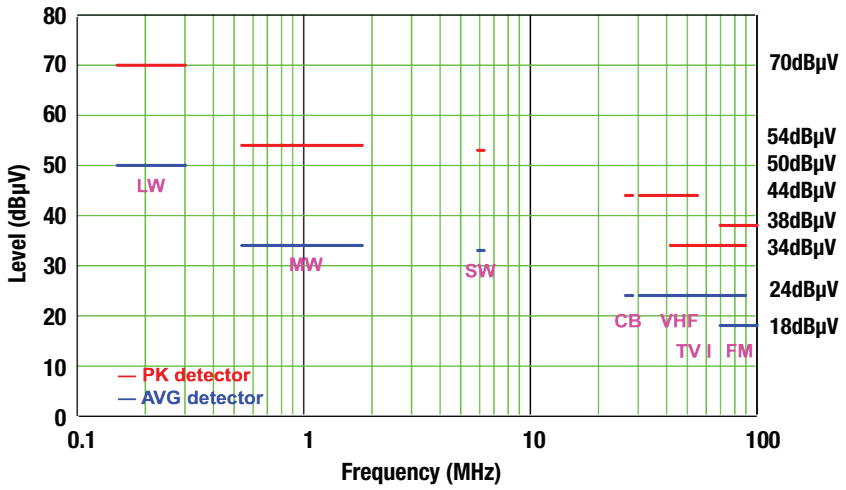
Figure 1. *EN 55022 Class A and Class B conducted emission limits with QP and AVG detectors.*

In terms of automotive end equipment, the main impetus for EMC compliance in the future will surely be autonomous vehicles supported by intervehicle communications. The CISPR 25 specification for the "protection of onboard receivers" already has challenging limits for conducted emissions, particularly in the FM band (76 MHz to 108 MHz).

From a regulatory standpoint, United Nations Economic Commission for Europe regulation No. 10 [7], [10], having replaced the EU's Automotive EMC Directive 2004/104/EC in November 2014, requires manufacturers to gain type approval for all vehicles, electronic subassemblies, components and separate technical units.

Conducted emissions for CISPR 25 testing are measured over a frequency range of 150 kHz to 108 MHz in specific frequency bands. More specifically, the regulated frequency ranges are dispersed across AM broadcast, FM broadcast and mobile service bands, as displayed in the graphic and tabular formats in **Figure 2**. This figure also plots the relevant limit lines for Class 5, the most stringent requirements in CISPR 25.

Even though higher noise spikes may be allowed in the gaps between the frequency bands, automotive manufacturers may choose to extend these frequency ranges according to their particular in-house EMC requirements [11]. Often based on international IEC standards, these requirements change only a few parameters of different tests or limits, with the essence of the requirements remaining the same.



	Band	Frequency (MHz)	PK (dBµV)	QP (dBµV)	AVG (dBµV)
Broadcast	LW	0.15 - 0.3	70	57	50
	MW	0.53 - 1.8	54	41	34
	SW	5.9 - 6.2	53	40	33
	FM	76 - 108	38	25	18
	TV Band I	41 - 88	34	–	24
Mobile Services	CB	26 - 28	44	31	24
	VHF	30 - 54 68 - 87	44 38	31 25	24 18

Figure 2. *CISPR 25 Class 5 conducted emission limits.*

Measuring conducted EMI

A LISN measures conducted emissions from the equipment under test (EUT). The LISN is an interface inserted at the measurement point between the EMI source and the power source to ensure the repeatability and comparability of EMI measurements [12], [13]. **Figure 3** shows a functional equivalent circuit (not a complete schematic) of a standard 50-µH LISN defined by CISPR 16-1-2 [14] or American National Standards Institute (ANSI) C63.4 [15] standards.

The LISN provides:

- A stable and calibrated source impedance in a given frequency range.
- Isolation of the EUT and measuring equipment from the input power source in that frequency range.
- A safe and suitable connection to the measuring equipment.
- Separate measurement of total noise levels in both lines, designated as L and N in Figure 3.

In short, it's possible to achieve reproducible results using a defined test setup with a known source impedance. Note that a LISN may contain one or more individual LISN circuits.

The LISN in principle is a π-filter network. Through a low-pass LC filter, the EUT connects to the input power lines L and N, as shown in Figure 3. The value of the LISN inductor is based on the anticipated inductance of the power line for the intended installation of the product.

CISPR 16 and ANSI C63.4 specify a 50-µH inductor for the LISN, a value that tallies with the inductance of a power-distribution wiring system running for approximately 50 m in a telecommunications installation. In contrast, CISPR 25 specifies a 5-µH LISN to correspond with the approximate inductance of an automotive wiring harness.

The LISN presents a well-defined impedance to the noise emission signal. The LISN manufacturer normally provides a calibration plot indicating the nominal impedance over the designated measurement frequency range. The allowable tolerance according to CISPR 16-1-2 is ±20% amplitude and a ±11.5-degree phase.

For measurements with an EMI receiver or spectrum analyzer, the noise signal is available from a high-pass filter network (as shown in Figure 3) with a 0.1-µF coupling capacitor and 1-kΩ discharge resistor that parallels with a 50-Ω termination at the measurement port. **Figure 4** shows a simulated impedance plot of a (50 µH + 5 Ω) || 50-Ω LISN over a frequency range from 150 kHz to 30 MHz.

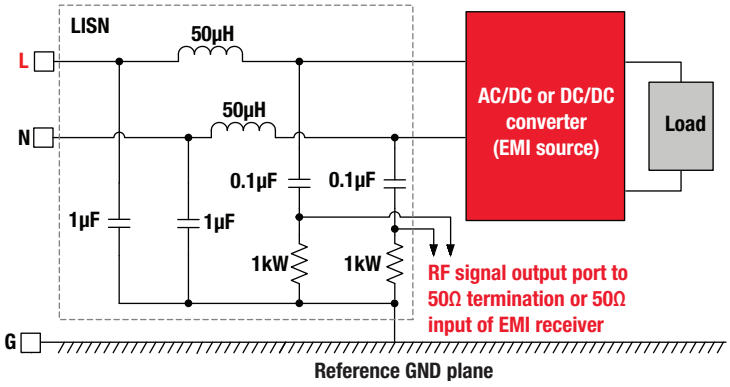


Figure 3. *Conducted emissions measurement with a V-type LISN.*

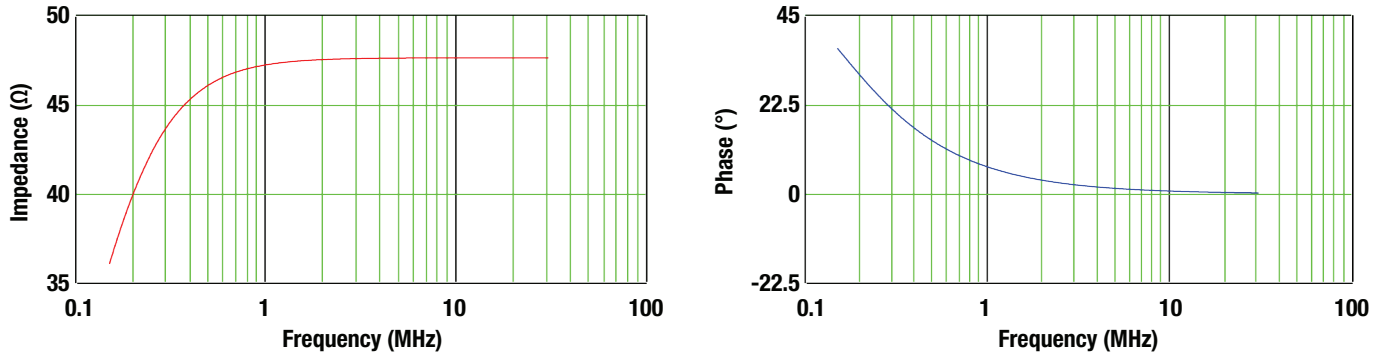


Figure 4. *Nominal impedance characteristic of a 50-Ω, 50-µH LISN at the measurement port over the regulated frequency range from 150 kHz to 30 MHz.*

CISPR 25 test setup for automotive applications

Figure 5 shows the conducted emissions test setup recommended by CISPR 25. This standard defines the disposition of the system under test and the measurement protocols and equipment. The LISN is designated here as an artificial network (AN) by the CISPR 25 specification. The EUT is remotely grounded when the vehicle power return line is longer than 200 mm, and two ANs are required: one for the positive supply line and one for the power return line. Conversely, if the vehicle power return line is 200 mm or shorter, the EUT is locally grounded and the positive supply requires only one AN.

The AN(s) are mounted directly on the reference ground plane, with the AN case(s) bonded to the ground plane. The power-supply return also connects to the ground plane between the power supply and the AN(s). Connecting the EMI receiver on the measuring port of the corresponding AN ensures a successful measurement of the conducted emissions on each power line. Meanwhile, a 50-Ω load terminates the measuring port of the AN inserted in the other power line.

Figure 6 shows a CISPR 25 conducted emissions test chamber for pre-compliance testing [13]. The LISNs are the blue boxes on the right side; a lithium-ion car battery is located behind them, and the DC/DC regulator EUT is located on the insulating material to the left. To test at a specific source voltage – for example, 13.5 V – a variable voltage supply is fed through the bulkhead from outside the test chamber, with measurements taken on both the line (hot) and return (ground) sides through their respective LISNs.

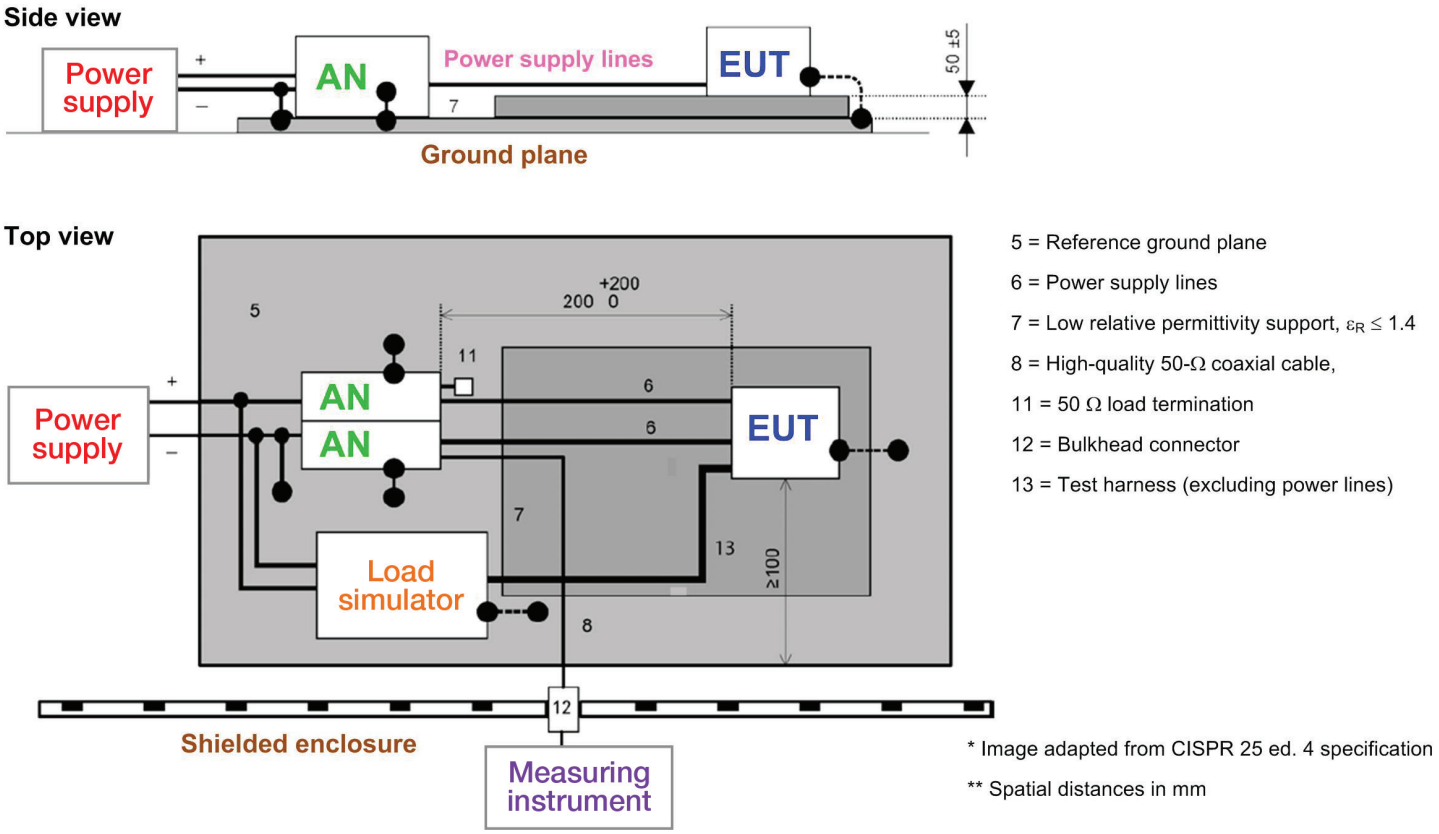


Figure 5. *General overview of CISPR 25 conducted EMI test setup (voltage method).*

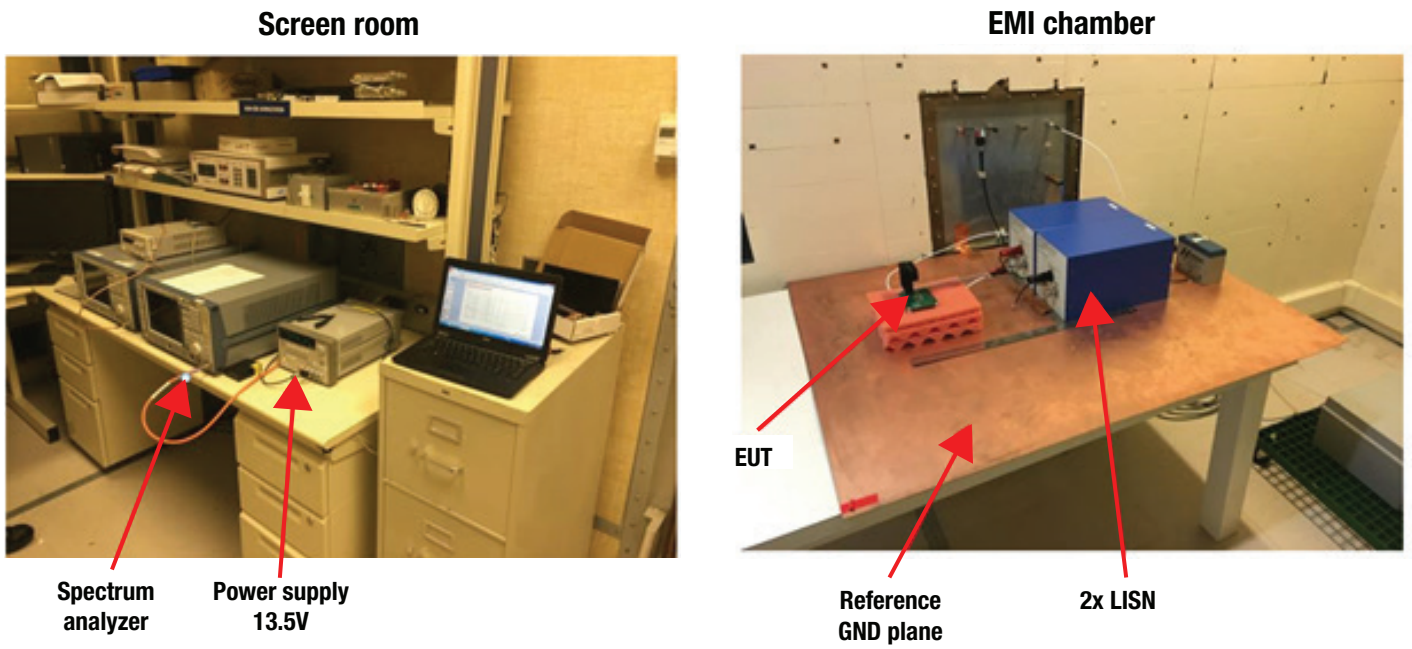


Figure 6. CISPR 25 conducted EMI test setup using two single-pole LISNs and a copper ground plane.

Figure 7 shows a typical CISPR 25 conducted EMI scan with yellow and blue denoting the peak and AVG measurements, respectively. You can see that the DC/DC regulator operates quietly and the conducted emissions are much below stringent Class 5 limits. This measurement technique changes above 30 MHz, as the EMI receiver's resolution bandwidth adjusts from 9 kHz to 120 kHz, resulting in a change in the measurement noise floor.

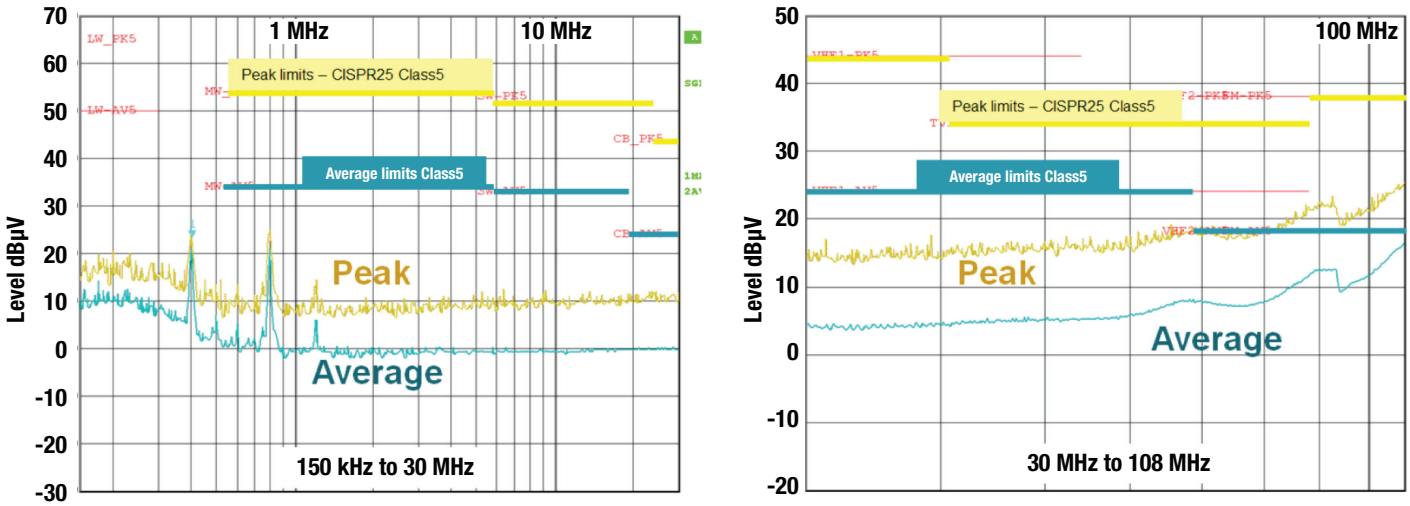


Figure 7. Typical CISPR 25 conducted EMI measurements.

2. Noise propagation and filtering

A high switching frequency is a major catalyst for size reduction in the advancement of power conversion technology. It is thus essential to understand the electromagnetic interference (EMI) characteristics of high-frequency switching regulators, since the required EMI filter necessary for regulatory compliance typically occupies a significant portion of the overall system footprint and volume. Understanding sources and propagation paths for both differential-mode (DM) and common-mode (CM) conducted emissions noise components enables further insight into DC/DC regulator conducted EMI behavior.

This chapter:

- Describes DM and CM noise separation from the total noise measurement.
- Explains conducted EMI propagation modes, including capacitive (electric field) and inductive (magnetic field [H-field]) coupling related to high transient voltage (dv/dt) and transient current (di/dt) switching.
- Describes the relevant propagation paths for DM and CM currents in various power-stage topologies.
- Emphasizes the separation of DM and CM emissions during EMI testing to help recognize and troubleshoot the relevant EMI source and streamline the EMI filter design process.
- Presents a case study highlighting the CM EMI signature associated with an automotive synchronous boost converter.

DM and CM conducted disturbances

DM and CM signals represent two forms of conducted emissions. DM currents are generally known as symmetrical mode signals or transverse signals, whereas CM currents are also known as asymmetrical mode or longitudinal signals. **Figure 1** shows a representation of DM and CM current paths in synchronous buck and boost DC/DC topologies. Y-capacitors C_{Y1} and C_{Y2} connected from positive and negative supply lines to GND conveniently complete the CM current propagation path [16].

DM conducted noise

DM noise current, I_{DM}, is caused by the intrinsic regulator switching action and flows in opposite directions in the positive and return power lines, labeled L1 and L2 in Figure 1. DM emissions are “current driven” and associated with di/dt, H-fields and low impedance. DM noise generally flows in a small loop area, with a close and compact return path.

As an example, a buck regulator in continuous conduction mode draws a trapezoidal-shaped current rich in harmonics. These harmonics present as noise on the power lines. The buck regulator’s input capacitor, designated C_{IN} in Figure 1. helps supply these higher-order current harmonics, but because of the capacitor’s parasitic nonidealities – equivalent series inductance (ESL) and equivalent series resistance – some harmonics inevitably appear in the supply current as DM noise, even after adding a practical EMI input filter stage.

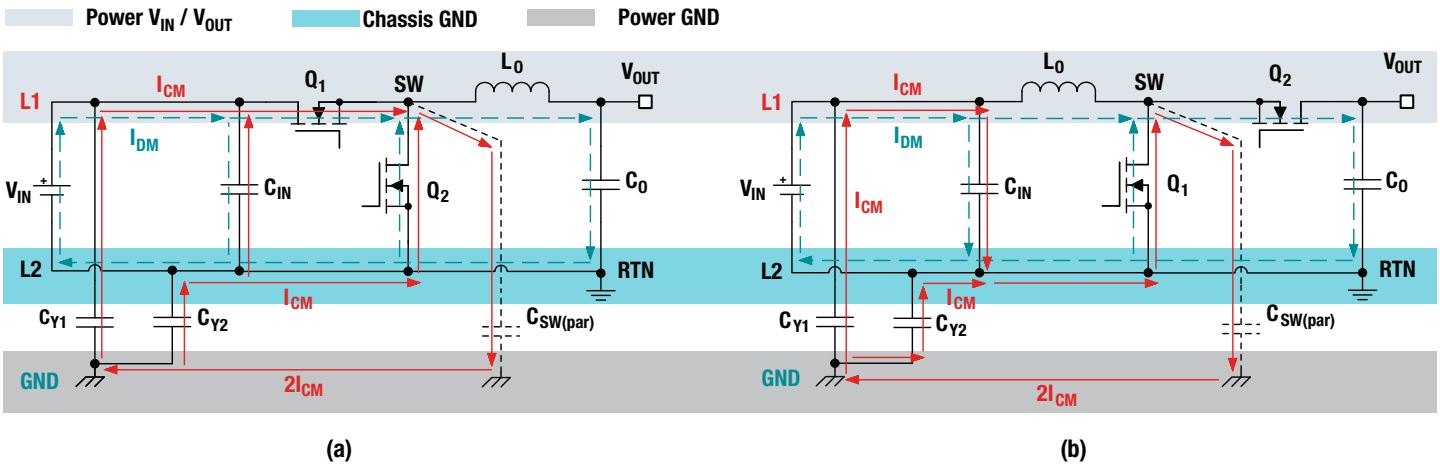


Figure 1. *Synchronous buck (a) and boost (b) converter DM and CM conducted noise paths.*

CM conducted noise

On the other hand, CM noise current, I_{CM}, flows in the earth GND wire and returns through both the L1 and L2 power lines. CM emissions are “voltage driven” and associated with a high slew-rate dv/dt, electric fields and high impedance. In the case of a nonisolated DC/DC switching regulator, the CM noise is mainly caused by the high dv/dt at the switch node, causing a displacement current that couples to the GND system through the parasitic capacitance associated with the metal-oxide semiconductor field-effect transistor (MOSFET) case, heat sink and switch node trace. Coupling capacitance associated with long cabling from a regulator’s input or output may also represent a CM noise path.

The CM current in Figure 1 is depicted as returning through the Y-capacitors of the input EMI filter, C_{Y1} and C_{Y2}. The alternative return path is through the 50-Ω measuring impedance of the line impedance stabilization network (LISN) setup (discussed in Chapter 1), and is obviously undesirable. Even though CM current is considerably less in magnitude than DM current, it is more difficult to deal with, as it typically flows in a large conducting loop area, thus acting as an antenna and representing a possible mechanism for increased radiated EMI.

Figure 2 shows the DM and CM conduction paths for a Fly-Buck (isolated buck) regulator. A CM current flows to the secondary side through the lumped interwinding capacitance of transformer T1 (designated C_{PS} in Figure 2) and returns through the earth GND connection. Figure 2b shows the simplified equivalent circuit for CM propagation.

In practical converters, these component parasitics all influence the voltage and current waveforms, as well as the CM noise:

- MOSFET output capacitance (C_{OSS}).
- Rectifier diode junction capacitance (C_D).
- Equivalent parallel capacitance of the main inductor winding.
- ESL of the input and output capacitors.

Chapter 3 has more details about capacitance.

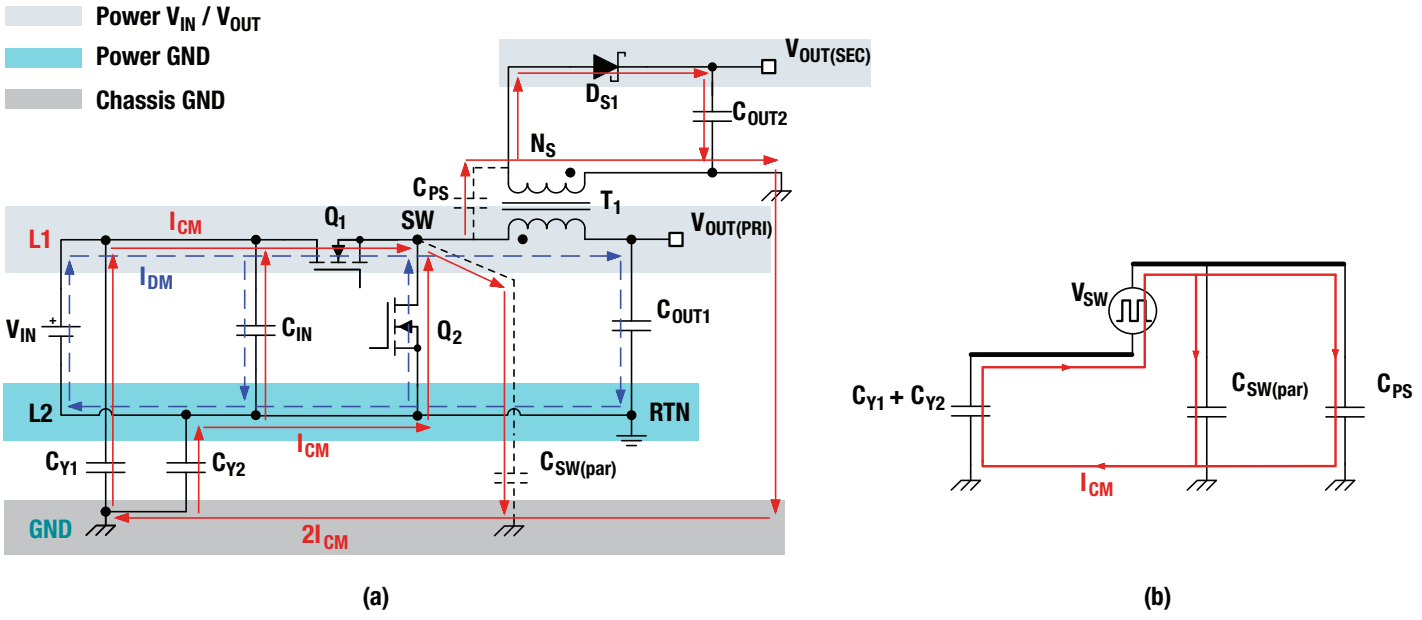


Figure 2. *Fly-Buck isolated regulator DM and CM conducted noise propagation paths (a); CM equivalent circuit (b).*

Noise source and propagation paths

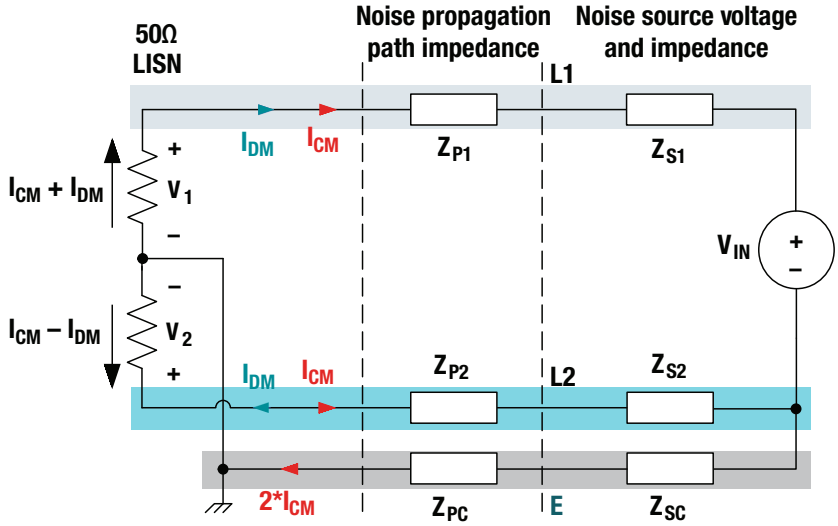
As outlined in Chapter 1, DC/DC regulator conducted emissions over a regulatory bandwidth of 150 kHz to 30 MHz for CISPR 32, and an even wider 150-kHz to 108-MHz frequency range for CISPR 25, are measured with respect to the total noise voltage or "unsymmetric" disturbance relative to earth GND across a 50-Ω LISN resistor for each power line [16].

Figure 3 models the phenomenon of EMI noise generation, propagation and measurement [16]. The noise source voltage is denoted as V_N and the noise source and propagation path impedances are Z_S and Z_P, respectively. The high-frequency equivalent circuit of the LISN and EMI receiver is simply two 50-Ω resistors.

Figure 3 also illustrates the respective DM and CM noise voltages, V_{DM} and V_{CM}, derived from the total noise voltage of each power line, V_1 and V_2. The DM or "symmetric" voltage component is defined as half the vector difference of V_1 and V_2, whereas the CM or "asymmetric" voltage component is half the vector sum of V_1 and V_2 [17]. Note the possible 6-dB discrepancy in the common definition of V_{DM} provided here vis-à-vis what the CISPR 16 standard specifies.

The CM noise source impedance is mostly capacitive and Z_{CM} decreases with frequency. Meanwhile, the DM noise source impedance is typically resistive and inductive, whereby Z_{DM} increases with frequency.

One way to reduce the level of conducted noise is to ensure that the noise source itself generates less noise. For the noise propagation path, the goal is to modify the impedance by filtering or other means to reduce the corresponding current flow. For example, CM noise reduction in a buck or boost converter entails decreasing the switch node dv/dt (the noise source), increasing impedance by decreasing the parasitic capacitance to GND, or filtering using Y-capacitors or a CM choke (or both). Chapters 5 and 6 will include a detailed classification of EMI mitigation techniques.



$$|V_{Total}| = |V_1| = |50\cdot(I_{CM} + I_{DM})$$

or

$$|V_{Total}| = |V_2| = |50\cdot(I_{CM} - I_{DM})$$

DM noise voltage: $$|V_{DM}| = \left|\frac{V_1 - V_2}{2}\right| = |50\cdot I_{DM}|$$

CM noise voltage: $$|V_{CM}| = \left|\frac{V_1 + V_2}{2}\right| = |50\cdot I_{CM}|$$

Figure 3. Conducted EMI emission model showing noise-source voltage, noise propagation path and LISN equivalent circuit.

DM and CM EMI filtering

Passive EMI filtering is the most common approach to EMI noise mitigation. As the name suggests, these filters use only passive components. The design of such filters for use in power electronics is particularly challenging, since the filters terminate with varying noise-source (switching converter) and load (power line) impedances [17], [18].

Figure 4a shows a conventional π-stage EMI input filter, as well as rectification and transient voltage clamping functions for EMC protection for a DC/DC regulator supplied by a DC or AC input. Figure 4 also includes the LISN high-frequency equivalent circuit from Chapter 1.

The two CM windings of a typical EMI filter are coupled, and the CM inductances of the two windings are L_{CM1} and L_{CM2}. The DM inductances L_{DM1} and L_{DM2} are the leakage inductances of the two coupled CM windings and may also include discrete DM inductors. C_{X1} and C_{X2} are DM filter capacitors and C_{Y1} and C_{Y2} are CM filter capacitors.

The EMI filter decouples into its equivalent DM and CM equivalent circuits to simplify its design, enabling analysis of the DM and CM attenuation of the filter, respectively. Decoupling is based on the assumption that the EMI filter has perfectly symmetrical circuit structures. In a symmetrical filter implementation, assume that component values $L_{CM1} = L_{CM2} = L_{CM}$, $C_{Y1} = C_{Y2} = C_Y$ and $L_{DM1} = L_{DM2} = L_{DM}$. Assume that the printed circuit board layout is perfectly symmetric. Figures 4b and 4c derive the DM and CM equivalent circuits, respectively [19].

Strictly speaking, however, perfect symmetry cannot apply in a practical case, so the DM and CM filters cannot totally decouple. As a result, DM noise can transform into CM noise and vice versa due to asymmetries. In general, unbalance associated with both converter noise sources and EMI filter parameters can result in such mode transformations [20].

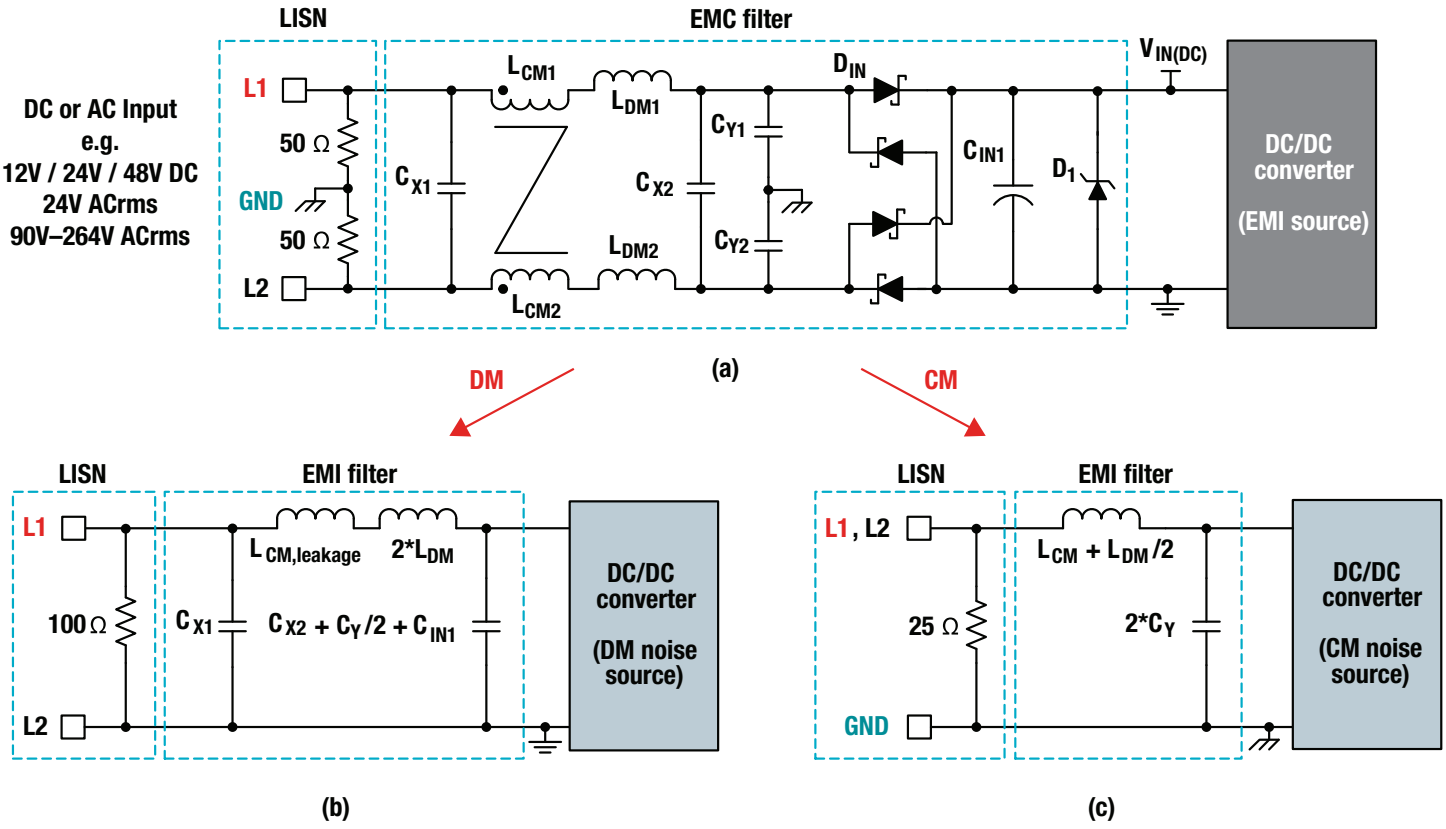


Figure 4. *Conventional EMC input filter (a), including equivalent circuits for DM (b) and CM (c) filter sections.*

DM and CM noise separation

Initial measurements of conducted EMI often reveal insufficient EMI filter attenuation. For proper EMI filter design, it is imperative to individually investigate the DM and CM noise-voltage components of the conducted emissions generated by the equipment under test. Treating DM and CM separately helps in the recognition and troubleshooting of the relevant EMI source and streamlines the EMI filter design process.

As highlighted in the previous section, the EMI filter employs essentially different filter components to suppress both DM and CM emissions. Within this context, one common approach for a diagnostic inspection is to separate the conducted noise into its DM and CM noise voltages.

Figure 5 presents passive and active realizations of a DM and CM separator circuit that facilitate direct and simultaneous measurement of DM and CM emissions.

The passive separator circuit [19] in Figure 5a uses wideband radio-frequency transformers, such as Coilcraft's SWB1010 series, with a characteristic impedance (Z_O) of 50 Ω and 100 Ω for T_1 and T_2, respectively, to achieve acceptable separation capabilities over the frequency range of the EMI sweep. A 50-Ω resistor in series with the input impedance of the spectrum analyzer at the DM output port achieves a divide-by-two function according to the expression for V_{DM} provided in Figure 3.

Figure 5b presents an active separator circuit using low-noise, high-bandwidth operational amplifiers [21]. U_1 and U_2 realize an ideal input impedance matrix for the LISN outputs, while U_3 and U_4 provide the CM and DM voltages, respectively. L_{CM} is a CM line filter, such as the Würth Elektronik 744222, at the input to differential amplifier U4 that increases the CM rejection ratio of the DM result (common-mode rejection ratio → −∞ dB) and minimizes CM/DM cross-coupling.

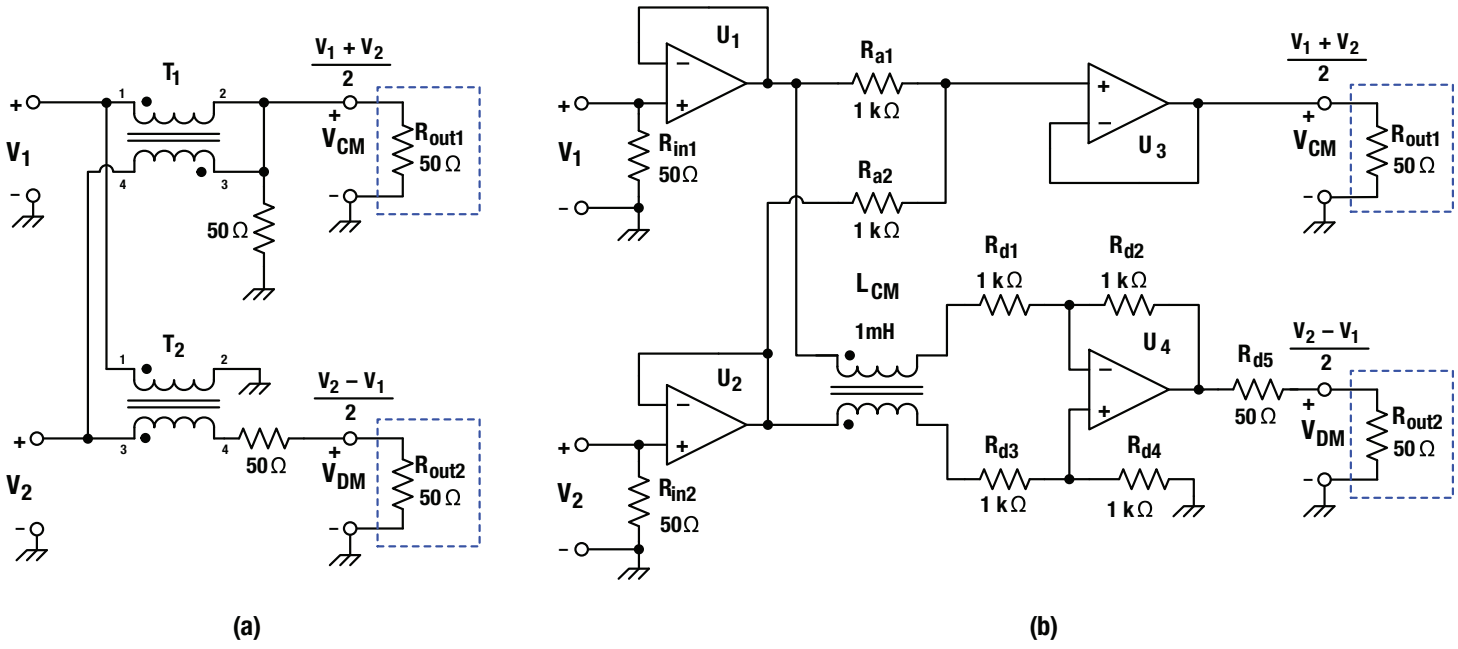


Figure 5. *Passive (a) and active (b) circuit realizations for DM and CM noise separation.*

Practical circuit example – automotive synchronous boost regulator

Consider the synchronous boost regulator shown in **Figure 6**. This circuit is common in automotive applications as a pre-boost regulator to maintain the battery-voltage supply during cold-crank or transient undervoltage conditions [22].

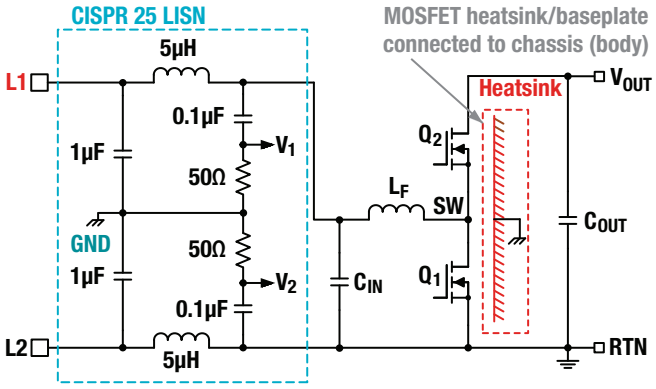


Figure 6. *Automotive synchronous boost regulator with 50-Ω/5-µH LISN for CISPR 25 EMI testing.*

A MOSFET heat sink is directly attached to the vehicle's chassis GND to improve the regulator's thermal performance and reliability, but at the expense of CM EMI performance. The schematic in Figure 6 includes the boost converter together with two CISPR 25-recommended LISN circuits connected at the L1 and L2 input lines.

To consider the boost regulator CM noise propagation paths, **Figure 7** replaces MOSFETs Q_1 and Q_2 with their equivalent AC voltage and current sources [23]. Figure 7 also depicts the parasitic component elements associated with boost inductor L_F, input capacitor C_{IN} and output capacitor C_{OUT}. In particular, C_{RL-GND} is the parasitic capacitance from load circuit to chassis GND, including contributions from long load lines and cabling as well as the downstream load configuration (for example, an isolated converter with a secondary-side output grounded to a chassis, or a motor-drive system load with a large metallic case bonded to a chassis).

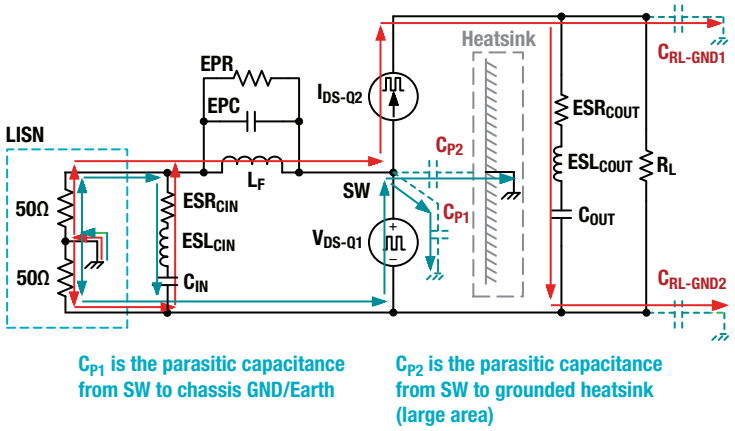


Figure 7. *High-frequency equivalent circuit for a synchronous boost topology with LISN. Only the CM current paths that flow in LISN are relevant for CM emission measurements.*

The drain-to-source switching (switch node) voltage rising and falling edges represent the dominant CM noise source. C_{P1} and C_{P2} represent the effective parasitic capacitances from SW to chassis and SW to heat sink, respectively. **Figure 8** shows the simplified CM noise equivalent circuit if the switch-node capacitive electric-field coupling is the dominant CM propagation path.

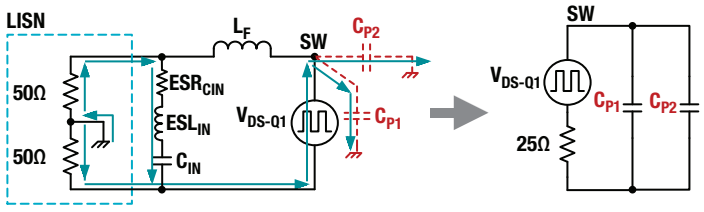


Figure 8. *Simplified CM equivalent circuit derived from Figure 7 for the synchronous boost circuit with LISN connected.*

3. Understanding power-stage parasitics

Gallium nitride power stages [28], [31], [32] notwithstanding, synchronous buck converters generally switch at frequencies under 3 MHz but generate broadband noise and electromagnetic interference (EMI) to 1 GHz and above. Their fast-switching voltages and currents are a major source of EMI. In fact, the high-frequency spectral content of the device switching waveforms is an alternative way to obtain an indication of EMI generation potential and points to a trade-off of EMI versus switching loss.

Being aware of the key converter switching loops from the schematic and making a diligent effort to minimize these loop areas during printed circuit board (PCB) converter layout design will inevitably abate parasitic inductance and related magnetic field (H-field) coupling, leading to lower conducted and radiated EMI. In general, a compact, optimized power-stage layout not only lowers EMI for easier regulatory compliance, but also increases efficiency and reduces overall solution costs.

This chapter:

- Provides a comprehensive illustration of inductive and capacitive parasitic elements for a buck-regulator circuit that affect not only EMI performance but also switching losses.
- Explores how an understanding of the contribution of responsible circuit parasitics is the first step toward minimizing them and reducing the overall EMI signature.

Examining critical loops with high slew-rate currents

In translating a power-supply schematic to a board layout, one essential step is to pinpoint the high slew-rate current (high transient current [di/dt]) loops, with an eye to identifying the layout-induced parasitic or stray inductances that cause excessive noise, ringing, overshoot and ground bounce. The power-stage schematic in **Figure 1** shows a synchronous buck controller driving high- and low-side metal-oxide semiconductor field-effect transistors (MOSFETs) designated Q_1 and Q_2, respectively.

Consider the turn-on transition of Q_1. Supplied by the input capacitor C_{IN}, Q_1's drain current increases rapidly to the inductor current level while the current flowing from Q_2's source to drain drops to zero. The loop shaded in red of the MOSFETs and input capacitor, labeled "1" in Figure 1, is the buck regulator's high-frequency commutating power loop, or "hot" loop [24], [25]. The power loop carries high-frequency currents of relatively large amplitude and di/dt, particularly during MOSFET switching.

Labels "2" and "3" in Figure 1 mark the gate loops for the power MOSFETs: loop 2 represents the high-side MOSFET's gate-drive circuit supplied by the bootstrap capacitor, C_{BOOT}, and loop 3 corresponds to the low-side MOSFET's gate driver supplied by V_{CC}. Solid and dashed lines delineate the turn-on and turn-off gate-current paths in each case, respectively.

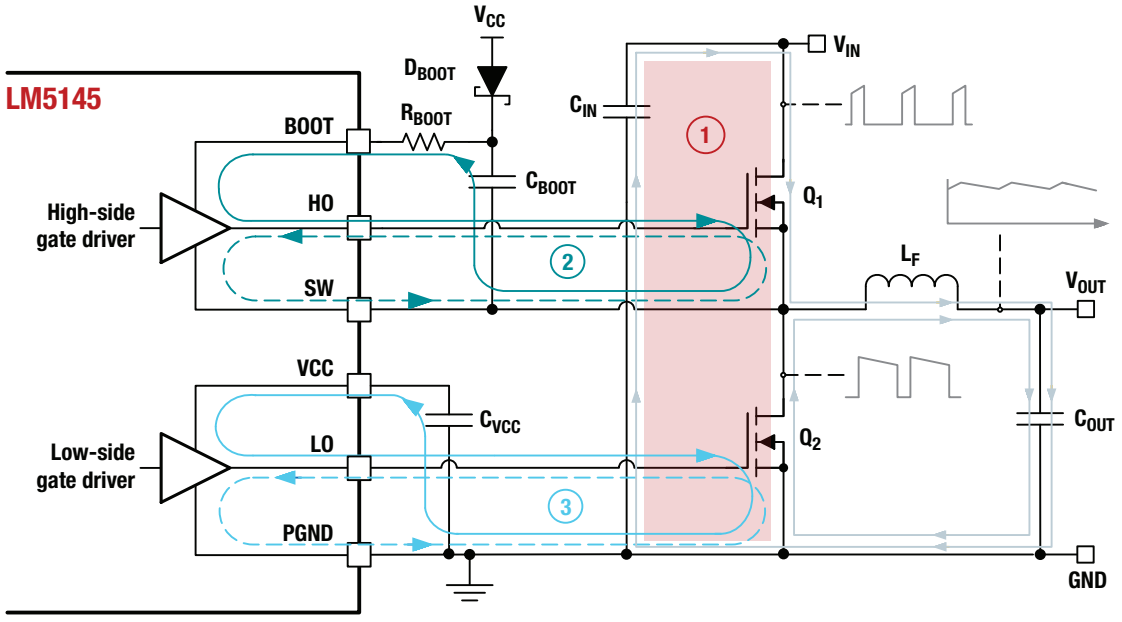


Figure 1. *Critical high-frequency switching loops with high slew-rate currents.*

Parasitic components and radiated EMI

EMI problems typically entail three elements: source, victim and coupling mechanism. The source refers to a noise generator with high transient voltages, di/dt or both, and the victim corresponds to a susceptible circuit (or the EMI measurement equipment). Coupling mechanisms can be categorized into conductive and nonconductive coupling. Nonconductive coupling can be electric field (e-field) coupling, H-field coupling or a combination of both, which is known as far-field electromagnetic radiation. Near-field coupling occurs as a result of parasitic inductances and capacitances and may have a decisive and significant effect on a regulator's EMI performance.

Power-stage parasitic inductances

Power MOSFET switching behavior and the consequences for waveform ringing and EMI correlate with the partial inductances [26] of the power-loop and gate-drive circuits. **Figure 2** provides a comprehensive illustration of the parasitic elements arising from component placement, device package and PCB layout routing that affect synchronous buck regulator EMI performance.

The effective high-frequency power-loop inductance, L_{LOOP}, is a sum of the total drain inductance, L_D, and common-source inductance, L_S, resulting from the equivalent series inductance (ESL) of the input capacitor and PCB traces and the package inductances of the power MOSFETs. As expected, L_{LOOP} is highly related to the layout geometry of the input capacitor-MOSFET loop, denoted by the red shaded area in Figure 1 [27], [28], [29].

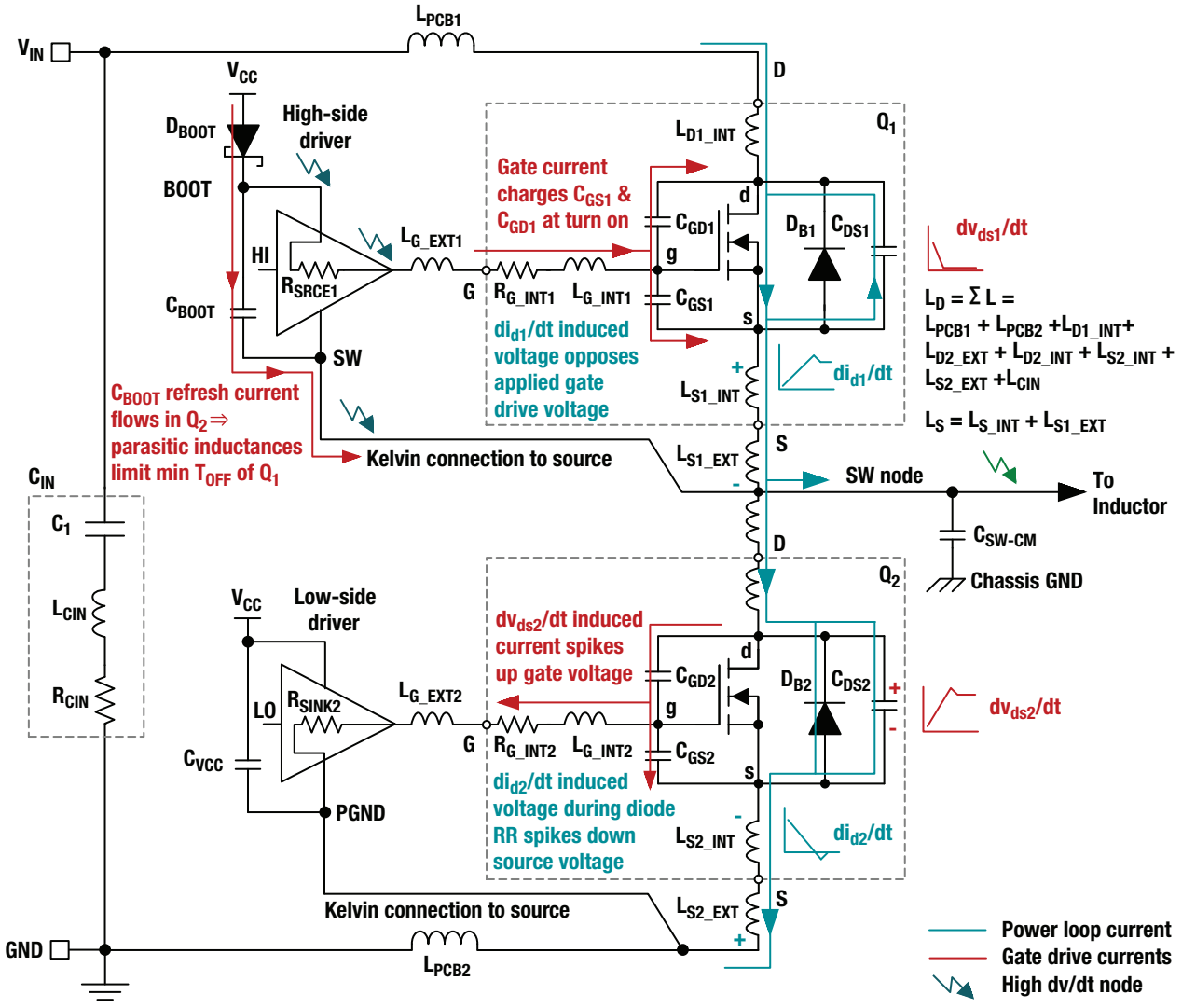


Figure 2. *Buck power-stage and gate driver "hidden schematic" inclusive of inductive and capacitive parasitic elements.*

Meanwhile, the self-inductance, L_G, of the gate loop includes lumped contributions from the MOSFET package and PCB trace routing. An inspection of Figure 2 reveals that the common-source inductance of the high-side MOSFET Q_1 exists mutually in both the power and gate loops. The common-source inductance of Q_1 reduces the di/dt in the power loop because it creates an opposing feedback voltage effect that impedes the rise and fall times of the MOSFET's gate-source voltage. However, it has the detrimental effect of increasing switching loss and is thus undesirable [30], [31].

Power-stage parasitic capacitances

Equation 1 expresses the power MOSFET input, output and reverse-transfer capacitances that affect EMI and switching behaviors as a function of the terminal capacitances shown in Figure 2. Such parasitic capacitances demand high-amplitude, high-frequency currents during MOSFET switching transitions.

$$\begin{aligned} C_{ISS} &= C_{GS} + C_{GD} \\ C_{OSS} &= C_{DS} + C_{GD} \\ C_{RSS} &= C_{GD} \end{aligned} \quad (1)$$

Equation 2's approximation shows a highly nonlinear voltage dependency for C_{OSS}. **Equation 3** gives the effective charge, Q_{OSS}, at a particular input voltage, where $C_{OSS\text{-}TR}$ is the time-related effective output capacitance as defined in the data sheets of some newer power FET devices [32].

$$C_{OSS}(V_{DS}) \approx C_{OSS,ref}\sqrt{\frac{V_{DS,ref}}{V_{DS}}} \quad (2)$$

$$Q_{OSS}(V_{IN}) = \int_0^{V_{IN}} C_{OSS}(v)dv = V_{IN} \bullet C_{OSS\text{-}TR}(V_{IN}) \quad (3)$$

Another critical parameter from Figure 2 is the reverse-recovery charge of body diode D_{B2}, designated as Q_{RR}, causing a significant spike in the current of Q_1 during turn-on. Q_{RR} depends on many parameters, including diode forward current before recovery, current transition speed and die temperature. In general, MOSFET Q_{OSS} and body diode Q_{RR} present several challenges to both analysis and measurement. The leading-edge current spikes during turn-on of Q_1 to charge C_{OSS2} of Q_2 and supply Q_{RR2} to recover body diode D_{B2} have similar profiles, and the two are often conflated.

EMI frequency ranges and coupling modes

Table 1 delineates the three loosely defined frequency ranges over which a switch-mode power regulator excites and propagates EMI [27]. During power MOSFET switching, when the slew rate of the commutating current can exceed 5 A/ns, a 3-nH parasitic inductance results in a voltage overshoot of 15 V. Furthermore, the current in the power loop with fast switching edges – and possible leading-edge ringing related to body diode reverse recovery and MOSFET C_{OSS} charging – is rich in harmonic content, posing a severe threat of H-field coupling and consequently increased conducted and radiated EMI.

Converter noise type		Dominant converter noise source	EMI frequency range	Conducted and radiated emissions
1	Low-frequency noise	Switching frequency harmonics	150 kHz to 50 MHz	Conducted
2	Broadband noise	MOSFET voltage and current rise and fall times, resonant ringing	50 MHz to 200 MHz	Both
3	High-frequency noise	Body diode reverse recovery	Above 200 MHz	Radiated

Table 1. *Switching converter noise sources and general EMI frequency classifications.*

The three dominant noise-coupling paths are conducted noise through the DC input lines, H-field coupling from the power loop and inductor, and e-field coupling from the switch-node copper surface [29].

Converter switching waveform analytical modeling

As highlighted in Chapter 2, the switch-node voltage rising and falling edges represent the dominant source of common-mode noise and e-field coupling in nonisolated converters. In EMI analysis, the upper bound or "spectral envelope" of the harmonic content of the noise emissions of a power converter, as opposed to the amplitudes of individual harmonic components, is of most interest to designers. Simplified analytical models of switching waveforms enable you to readily establish the influence of time-domain waveform parameters on the resulting frequency spectrum.

To get an idea of the harmonic frequency spectral envelope pertaining to the switch-node voltage, Figure 3 approximates the time-domain waveform. Each segment is characterized by its amplitude (V_{IN}), duty cycle (D), rise and fall times (t_R and t_F), and pulse width (t_1), defined between the midpoints of the rising and falling edges.

Fourier analysis reveals that the harmonic amplitude envelope is a double-sinc function with corner frequencies of f_1 and f_2, depending on the pulse width and rise and fall times of the time-domain waveform [33]. You can apply a similar treatment for the input current waveforms of the buck switching cell. The applicable frequency component(s) from the measured voltage and current waveforms can represent a ringing characteristic at the edges on the switch voltage and current waveforms (arising from parasitic loop inductance and body diode reverse recovery, respectively).

In general, inductance L_{LOOP} increases the MOSFET drain-to-source peak voltage spike. It also exacerbates switch-node voltage ringing, affecting broadband EMI in the 50-MHz to 200-MHz range. Clearly, then, it is vital to minimize the effective loop length and enclosed area of the power loop. Not only does this reduce parasitic inductance, but H-field self-cancellation can help reduce the magnetically coupled radiated energy emanating from what effectively is a loop antenna structure.

Conducted noise coupling appears on the regulator input side based on the ratio of loop inductance and input capacitor ESL. Reducing L_{LOOP} increases the input filter attenuation requirement. Fortunately, the noise conducted to the output is minimal if the buck output inductor has a high self-resonant frequency. In other words, the inductor should have a low effective parallel capacitance to obtain a high transfer impedance from switch node to V_{OUT} nets. The output noise is additionally filtered by low-impedance output capacitor(s).

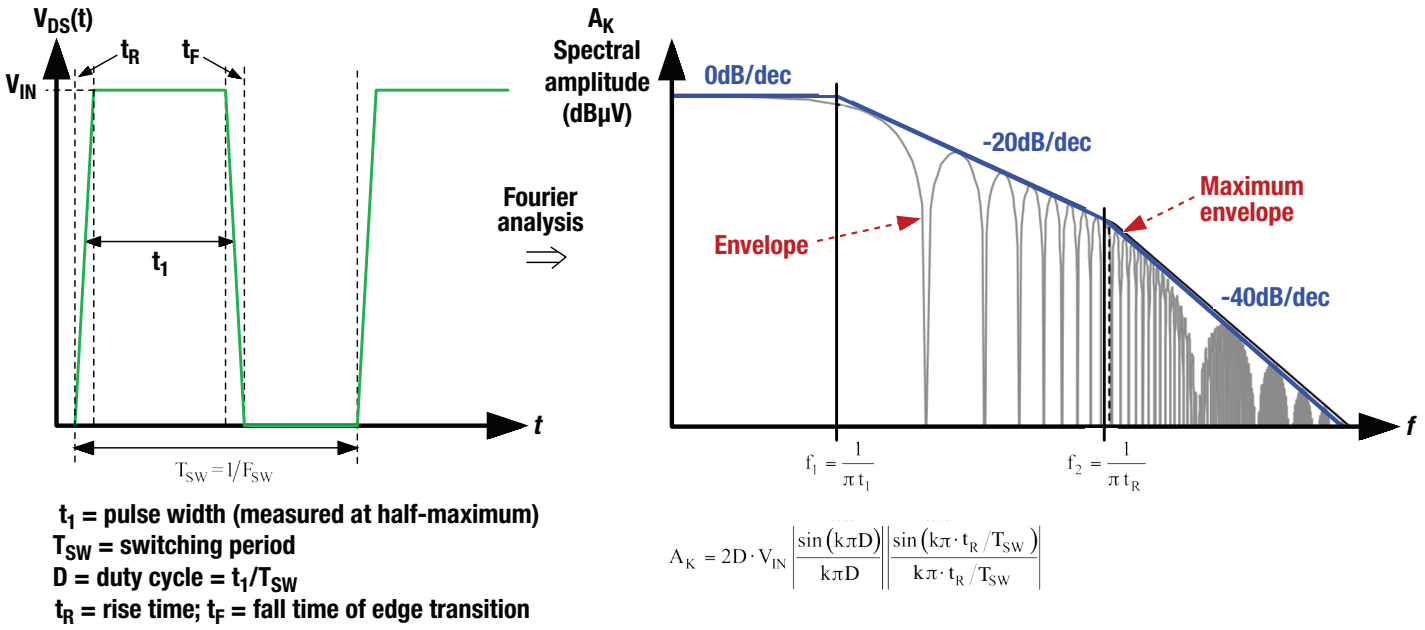


Figure 3. *Switch-node voltage trapezoidal waveform and its spectral envelope impacted by pulse width and rise and fall times.*

Equivalent resonant circuits

Looking at the synchronous buck regulator time-domain switch-node voltage waveform in **Figure 4,** the parasitic energy transferred during MOSFET switching excites a resistor-inductor-capacitor (RLC) resonance. Simplified equivalent circuits analyze the switching behavior when Q_1 turns on and off. Switch-node voltage overshoot above V_{IN} and undershoot below GND are evident during the rising and falling edges of the voltage waveform, respectively.

The oscillation amplitude depends on the distribution of partial inductances within the loop, and the effective AC resistance of the loop damps the subsequent ringing. Not only does this contribute to voltage stress of the MOSFETs and gate drivers, it also correlates to the frequency at which broadband radiated EMI is centered.

Rising-edge voltage overshoot indicates a ringing period of 6.25 ns in Figure 4, corresponding to a resonant frequency of 160 MHz. A near-field H-probe placed directly over the switching loop area can also identify this frequency component. Computational EM field simulation tools can derive the partial loop inductance values associated with the high-frequency resonance and radiated emission. However, a simpler technique involves measuring resonant period T_{Ring1}, and knowing C_{OSS2} at the input voltage operating point from the MOSFET's data sheet, **Equation 4** calculates the total loop inductance:

$$\sum L_{LOOP} = \frac{T_{Ring1}^2}{4\pi^2 C_{OSS2}} \quad (4)$$

Two important aspects are the resonant frequency and the loss or damping factor, α, inherent to the resonance. The main design goal is to push the resonant frequency as high as possible by minimizing the loop inductance. This decreases the total stored reactive energy and lowers the resonant switch-node voltage peak overshoot. Also, the damping factor increases at higher frequencies due to the skin effect, increasing the effective value of R_{LOOP}.

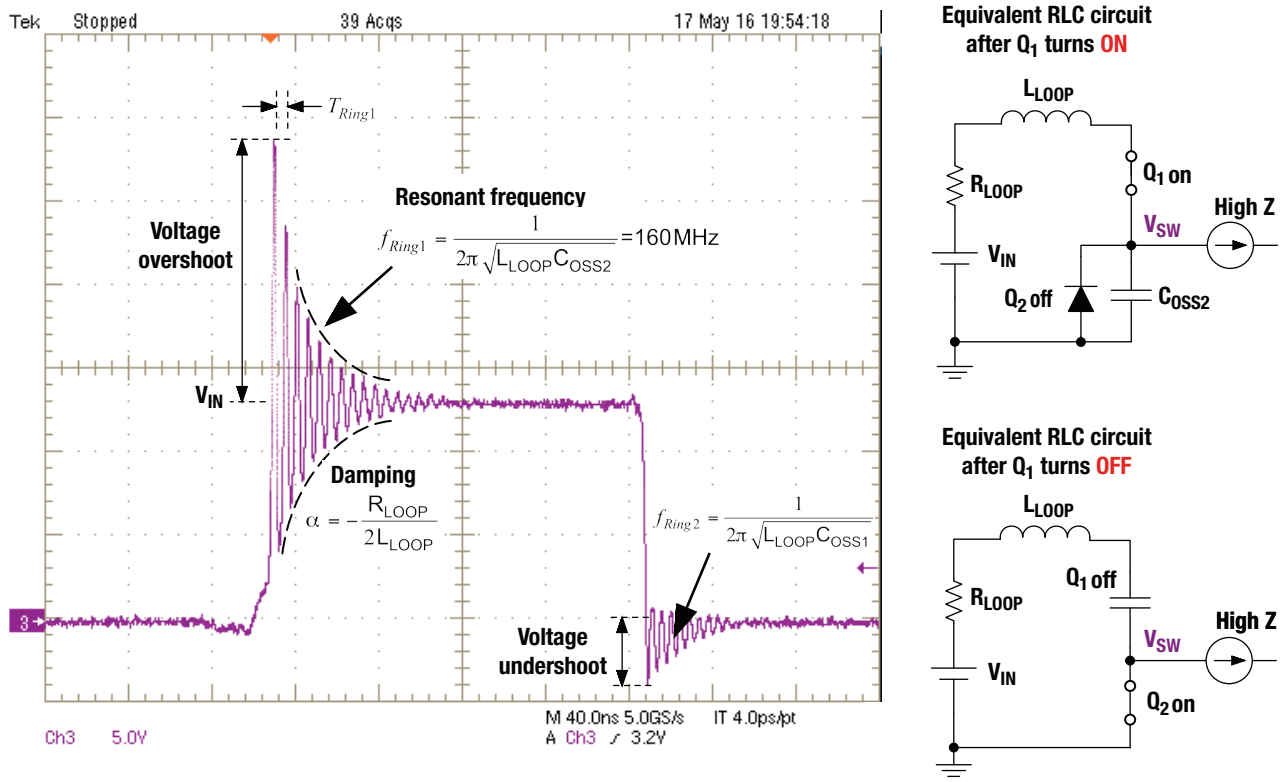


Figure 4. *Synchronous buck switch-node voltage waveform and equivalent RLC circuits during MOSFET turn-on and turn-off switching transitions.*

4. Radiated emissions

Radiated electromagnetic interference (EMI) is a dynamic and situational problem that depends on parasitic effects [34], circuit layout and component placement within the power converter itself, and the overall system in which it operates. Thus, the issue of radiated EMI is typically more challenging and complex from the design engineer's perspective, particularly when multiple DC/DC power stages are located on the system board.

Radiated emissions affect a power converter's EMI signature at high frequencies [41]. The upper frequency for radiated tests extends to 1 GHz and higher (depending on the specification) – much higher than for conducted emissions. Radiated emissions measurements, while not as straightforward as conducted emissions tests, are necessary for compliance testing and can easily become a bottleneck in a product's development process.

For automotive applications, the cable bundle is often the dominant radiating structure at low frequencies given its length. The measured radiated emissions profile largely comprises common-mode current in the attached cables, which is driven by electric near-field coupling between the printed circuit board and the cables.

This chapter:

- Offers some perspective on radiated emissions from switching power converters, particularly those intended for applications in the automotive and industrial sectors.
- Explains the basic mechanisms for radiated EMI, as well as the measurement requirements, frequency ranges and applicable limits.
- Presents radiated EMI measurement setups and results for two DC/DC buck converters.

Near-field coupling

Figure 1 provides an overview of the fundamental EMI coupling modes between noise source and victim circuits. In particular, inductive or magnetic field (H-field) coupling requires a time-varying, high transient current (di/dt) source and two magnetically coupled loops (or parallel wires with return paths). Capacitive or electric field (e-field) coupling, on the other hand, requires a time-varying, high transient voltage (dv/dt) source and two closely spaced metal plates. Both mechanisms are described as near-field coupling where the noise source and victim circuits are in close proximity and can be measured using near-field sniffer probes.

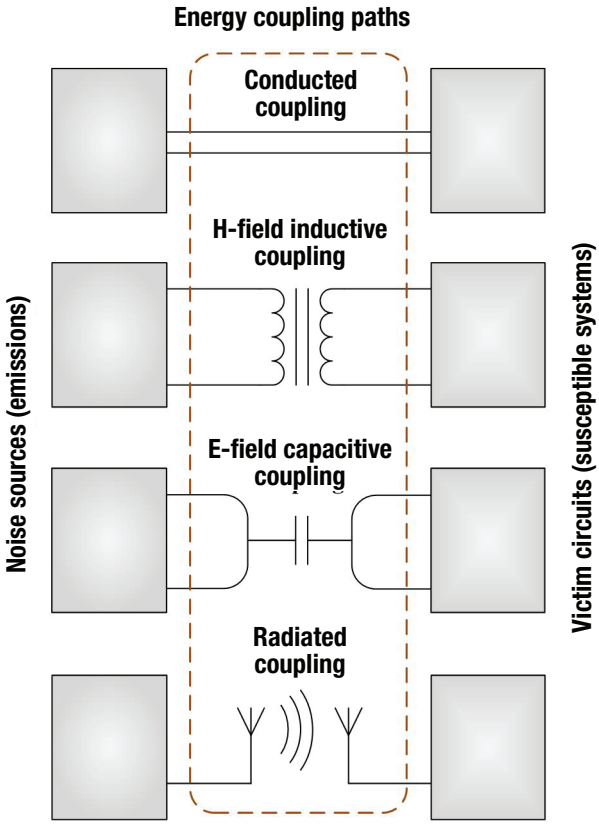


Figure 1. *EMI coupling modes.*

As an example, modern power switches, particularly gallium nitride- and silicon carbide-based transistors, have low output capacitance C_{OSS} and gate charge Q_G, and can switch at extremely high dv/dt and di/dt slew rates. The possibility for H-field and e-field coupling and crosstalk to adjacent circuits is high. However, larger distances between the coupled structures significantly reduce near-field coupling as the mutual inductance or capacitance decreases.

Far-field coupling

A classic electromagnetic (EM) wave propagates as a combination of E and H fields. The structure of the fields near the radiating antenna source is a complex, three-dimensional pattern. Further from the source, the EM wave in the far-field region comprises e-field and H-field components oriented orthogonally to each other and to the direction of propagation. **Figure 2** depicts this plane wave [35], as it represents the primary basis for radiated EMI that is limited by various emissions standards.

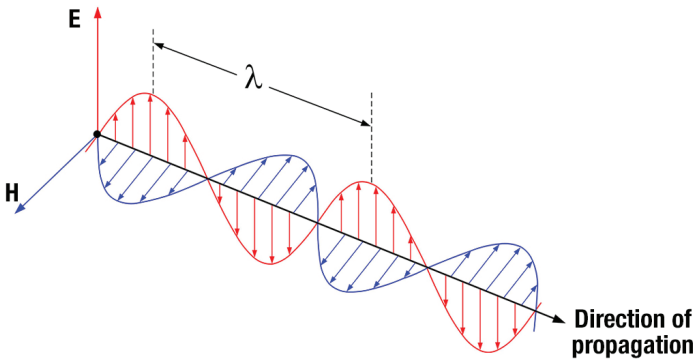


Figure 2. *EM plane-wave propagation.*

The wave impedance, plotted in **Figure 3**, is the ratio of the e-field and H-field strengths. As the E and H components in the far-field region are in phase with each other, the far-field impedance is resistive and given by the plane-wave solution of Maxwell's equations, shown here as **Equation 1**:

$$Z_{W(far\text{-}field)} = \frac{E}{H} = Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} \approx \sqrt{\frac{4\pi\times10^{-7}\ H/m}{\frac{1}{36\pi}\times10^{-9}\ F/m}} \approx 120\pi\,\Omega \approx 377\Omega \quad (1)$$

If λ is the wavelength and f is the frequency of concern, **Equation 2** usually denotes the boundary between the near-field and far-field regions:

$$d_{NF\text{-}FF} = \frac{\lambda}{2\pi} \approx \frac{48}{f\,(MHz)} \quad (2)$$

This boundary, however, is not a precise criterion but is only intended to indicate a general transition region (**Figure 3** delineates λ/16 to 3λ) where the fields evolve from complicated distributions to planar waves.

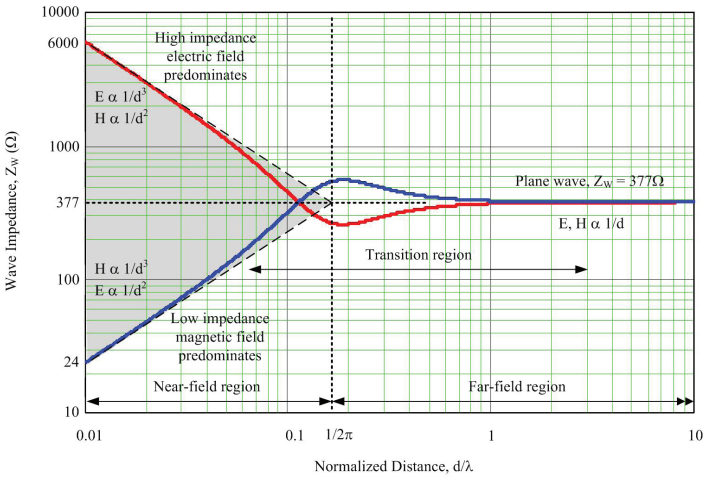


Figure 3. *The wave impedance in near-field and far-field regions from Maxwell's laws.*

Given that most antennas are designed to detect and respond to e-fields, the radiated EM wave is often described as vertically or horizontally polarized, depending on the direction of the e-field. In general, a measuring e-field antenna should be oriented in the same plane as the propagating e-field to detect the maximum field strength. As a result, radiated EMI test standards typically describe measurements with the receiving antenna mounted in both vertical and horizontal polarizations.

Radiated EMI in industrial and multimedia equipment

Table 1 presents the specified Class A and Class B radiated emissions limits from Federal Communications Commission (FCC) Part 15 Subpart B [35] for unintentional radiators. In addition, clause 15.109(g) of the specification allows the use of Comité International Spécial des Perturbations Radioélectriques (CISPR) 22 limits [36] for radiated emissions as given in **Table 2**, using the measurement methods specified in American National Standards Institute (ANSI) C63.4-2014. The use of CISPR limits facilitates harmonization of requirements for the U.S. and Europe. Note that CISPR 32 now replaces CISPR 22, though as of this writing, FCC Part 15 has not yet been updated to reflect this change.

The limits in Tables 1 and 2 assume a CISPR quasi-peak (QP) detector function and a resolution bandwidth (RBW) of 120 kHz for frequencies below 1 GHz. Tables 3 and 4 present limits for frequencies above 1 GHz using peak (PK) and average (AVG) detectors and a receiver RBW of 1 MHz.

For a given measurement distance, Class B limits for residential or domestic applications are generally more restrictive by a 6- to 10-dB margin than Class A limits for commercial or industrial use. Note also that Tables 1 and 2 include an inverse linear distance (1/d) proportionality factor of 20 dB/decade, used per 15.31(f)(1), to normalize limits for 3- and 10-m antenna measurement distances to determine compliance. For example, placing the antenna at 3 m instead of 10 m to stay within the test facility boundaries requires adjusting the limit amplitudes by approximately 10.5 dB.

Frequency range (MHz)	3-m distance		10-m distance	
	Class A (dBµV/m)	Class B[1] (dBµV/m)	Class A[2] (dBµV/m)	Class B (dBµV/m)
30-88	49.6	**40**	**39.1**	29.5
88-216	54	**43.5**	**43.5**	33
216-960	56.9	**46**	**46.4**	35.5

Notes:

[1] Class B limits are specified by the FCC at a distance of 3 m and extrapolated here for 10 m by subtracting 10.5 dB.

[2] Class A limits are specified by the FCC at a distance of 10 m and extrapolated here for 3 m by adding 10.5 dB.

Table 1. *Radiated emissions field strength QP limits per 47 CFR 15.109(a) and (b), 30 MHz to 1 GHz.*

Frequency range (MHz)	3-m distance		10-m distance	
	Class A (dBµV/m)	Class B (dBµV/m)	Class A (dBµV/m)	Class B (dBµV/m)
30-230	50.5	40.5	**40**	**30**
230-1000	57.5	47.5	**47**	**37**

Note:

The limits are specified in CISPR 22 at 10 m and extrapolated here for 3 m by adding 10.5 dB.

Table 2. *Radiated emissions field strength QP limits per 47 CFR 15.109(g)/ CISPR 22/32, 30 MHz to 1 GHz.*

Frequency range (MHz)	Class A (dBµV/m)		Class B (dBµV/m)	
	AVG	PK	AVG	PK
0.96-40	60	80	54	74

Table 3. *Radiated emissions field strength limits at 3 m per 47 CFR 15.109(a) and (b), 1 GHz to 6 GHz.*

Frequency range (MHz)	Class A (dBµV/m)		Class B (dBµV/m)	
	AVG	PK	AVG	PK
1-3	56	76	50	70
3-6	60	80	54	74

Table 4. *Radiated emissions field strength limits at 3 m per 47 CFR 15.109(g), CISPR 22/32, 1 GHz to 6 GHz.*

Figure 4 plots the relevant limit lines for Class A and Class B at a 3-m antenna distance. As an example of an FCC-compliant design, a battery-powered gas-sensor implementation using Bluetooth® Low Energy is available for purchase from Texas Instruments [37]. The FCC Class A compliance reports with radiated emissions test data and plots for this design are available to download for review.

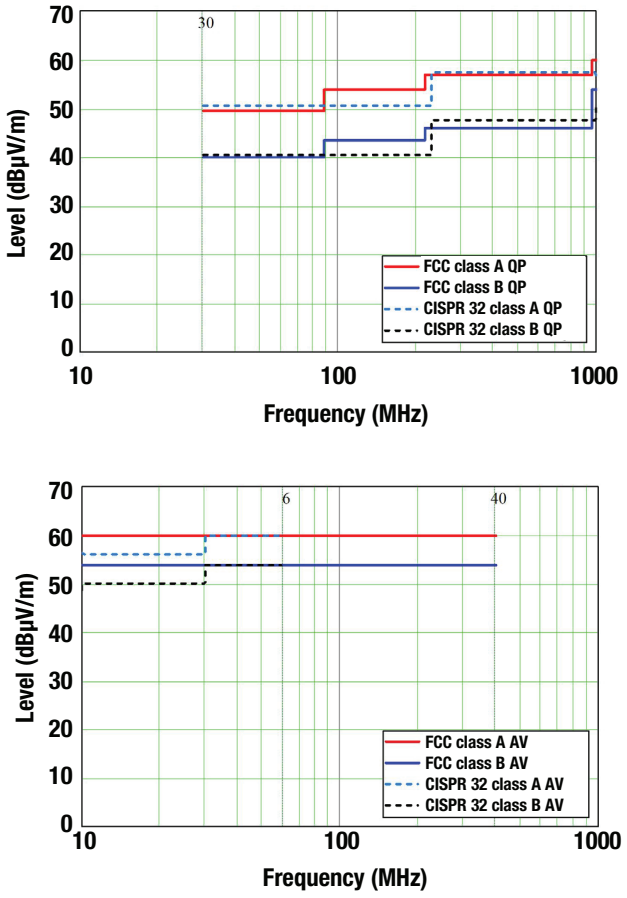


Figure 4. *FCC Part 15 and CISPR 22 radiated limits for Class A and Class B (using QP and AVG detectors below and above 1 GHz, respectively).*

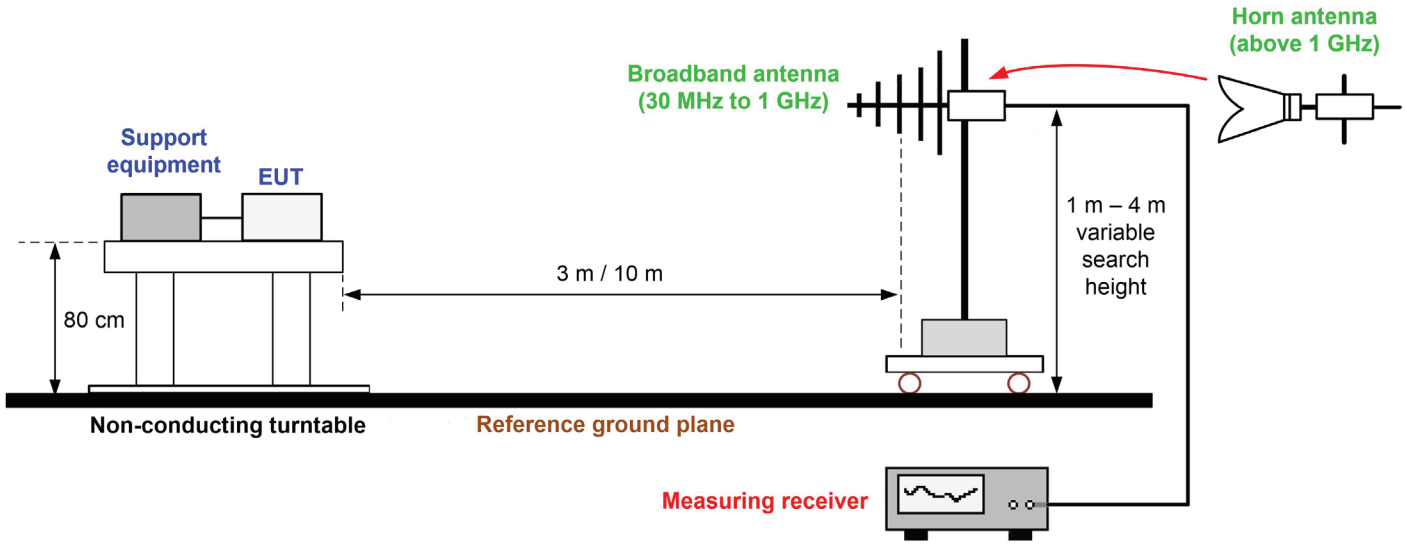


Figure 5. *Radiated emissions measurement setup for FCC Part 15 and CISPR 22/32.*

As **Figure 5** depicts, a radiated EMI test procedure involves placing the equipment under test (EUT) and support equipment on a nonconductive turntable 0.8 cm above the reference ground plane in a semi-anechoic chamber or open area test site, as defined in CISPR 16-1. The EUT is set 3 m away from the receiving antenna, which is mounted on an antenna tower.

A PK detector pre-scan using a calibrated broadband antenna (a combined biconical and log-periodic antenna, or bilog) detects emissions from 30 MHz to 1 GHz with both horizontal and vertical antenna polarizations. Such an exploratory test determines the frequencies of all significant emissions. This is followed by a QP detector check of relevant trouble spots to record the final compliance measurements.

The RBW of the EMI receiver is set at 120 kHz during the test. The antenna is configured for horizontal and vertical polarizations (by rotating it by 90 degrees relative to the ground plane) and adjusted in height between 1 m and 4 m above the ground plane to maximize the field strength reading at each test frequency in consideration of ground-plane reflections. The antenna-to-EUT azimuth also varies during the measurements by rotating the EUT on a turntable 0 to 360 degrees to find the maximum field-strength readings from an EUT directional standpoint. The antenna is in the EUT's far-field region, which corresponds to 15.9 MHz for a 3-m antenna distance.

It's possible to conduct a PK detector pre-scan using a horn antenna for scans above 1 GHz, followed by an AVG detector at frequencies close to the limit. The EMI receiver RBW is set at 1 MHz. A height scan is not required, as the antenna is more directional and reflections from the ground plane and chamber walls are less troublesome. The EUT's emissions at these frequencies are also more directional, however, so the turntable is again rotated through 360 degrees and antenna polarization is oriented for maximum response. According to **Table 5**, the upper range of concern varies with the EUT's highest internal frequency.

EUT highest internal frequency	Upper frequency of measurement range
Below 1.705 MHz	Testing not required
1.705 MHz to 108 MHz	1 GHz
108 MHz to 500 MHz	2 GHz
500 MHz to 1 GHz	5 GHz
Above 1 GHz	Fifth harmonic of highest frequency or 6 GHz (CISPR 22/32) and 40 GHz (FCC Part 15), whichever is lower

Table 5. *Radiated emissions maximum measurement frequency based on the highest frequency of the EUT internal clock source(s).*

Radiated emissions tests measure the electric field strength calibrated in units of decibel microvolts per meter (dBµV/m). The antenna factor (AF) is the ratio of the electric field (in µV/m) present at the plane of the antenna to the voltage measured by the spectrum analyzer or scanning EMI receiver (in dB/µV). In general, it is possible to derive a corrected emission level from **Equation 3**:

$$\text{Emission level (dBµV/m)} = \text{SA reading (dBµV)} + \text{AF (dB/m)} + \text{CL (dB)} + \text{AL (dB)} - \text{AG (dB)} \quad (3)$$

where SA is the spectrum analyzer, CL is the cable loss, AL is the attenuator and radio-frequency limiter loss factor, and AG is the amplifier pre-gain.

Figure 6 shows the radiated emissions test setup photo and results for the Texas Instruments LMR16030 60-V/3-A buck converter [38]. The measurements are taken at a 24-V input, 5-V output at a 3-A load and 400-kHz switching frequency.

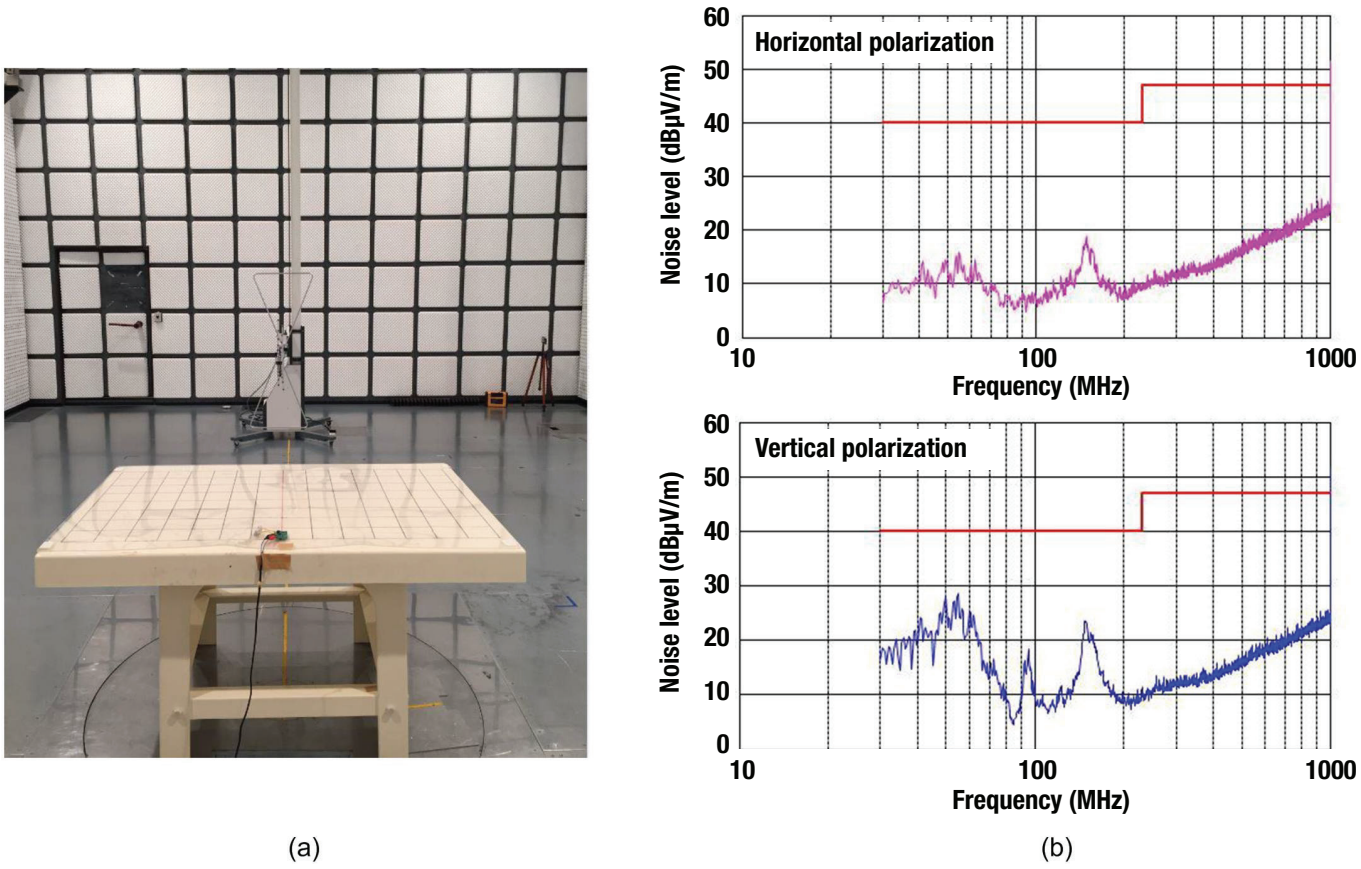


Figure 6. *CISPR 22 radiated EMI test: setup photo (a); radiated EMI results with horizontally and vertically polarized antenna (b).*

Radiated EMI in automotive systems

Although shielded cables reduce interference effects in automotive systems, EMI can efficiently couple to susceptible circuits through crosstalk. And as a consequence of field-to-wire coupling effects, radiated emissions may also imply radiated-immunity problems to signal interconnects in the relatively small volume of a vehicle with densely packed arrangements of power and signal runs in the cable harness. For these reasons, assessing EMI performance is an issue of heightened concern for automotive engineers involved in electric vehicle design and testing.

UNECE regulation 10 and CISPR 25

CISPR 12 and CISPR 25 are international standards containing limits and procedures for the measurement of radio disturbances to protect automotive offboard and onboard receivers, respectively. CISPR 25 [39] in particular applies at the vehicle level and also to any electronic subassemblies intended for the use in vehicles. In contrast to other standards, CISPR 25 is typically used as the basis for product specifications defined by an automotive manufacturer and its suppliers, but is not the basis for regulatory compliance and conformity assessments. That distinction goes to United Nations Economic Commission for Europe (UNECE) Regulation 10 [40] since the discontinuation of the European Union's Automotive EMC Directive.

CISPR 25 defines several methods and limit classes for emission measurements of vehicle components and considers both broadband and narrowband (NB) sources. **Figure 7** shows the Class 5 limits using PK and AVG detectors for components/modules. Measurements are taken apropos receivers in the broadcast and mobile service bands operating within the vehicle. The lowest measurement frequency relates to the European long-wave broadcast band of 150 kHz to 300 kHz, and the highest frequency is 2.5 GHz in consideration of Bluetooth transmissions.

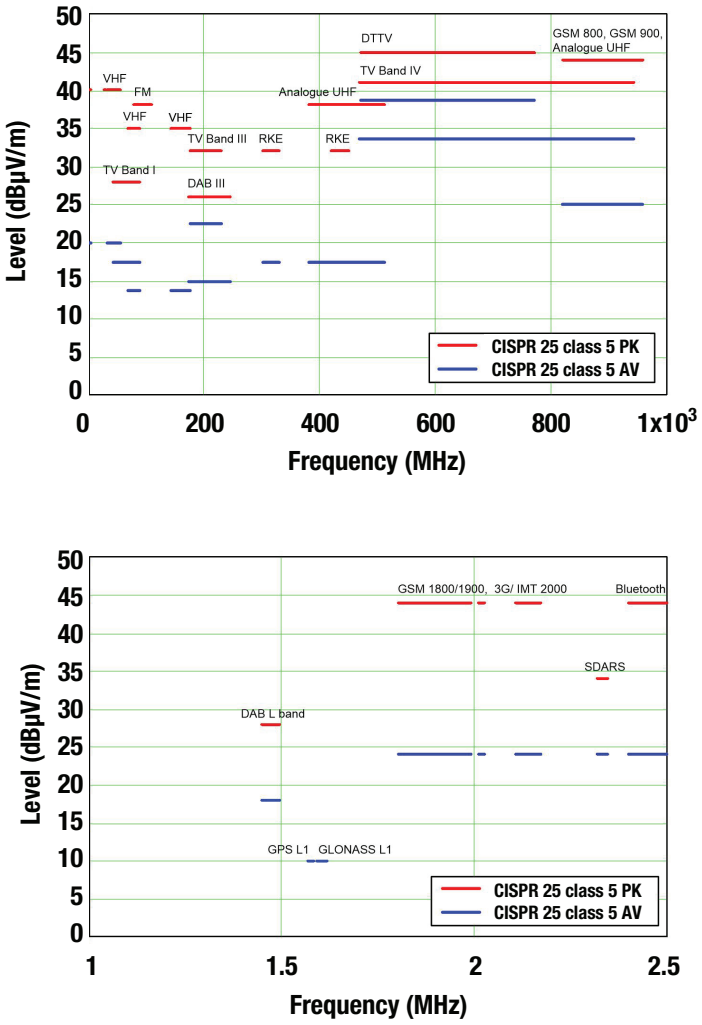


Figure 7. CISPR 25 Class 5 radiated limits for components or modules using the absorber-lined shielded enclosure (ALSE) method with PK and AVG detectors (linear frequency scale).

The scanning receiver's RBW is 9 kHz and 120 kHz for detection below and above 30 MHz, respectively. Exceptions are the GPS L1 civil (1.567 GHz to 1.583 GHz) and Global Navigation Satellite System L1 (1.591 GHz to 1.613 GHz) bands, requiring an RBW of 9 kHz and a maximum step size of 5 kHz to detect applicable NB emissions using only an AVG detector.

Antenna systems for CISPR 25

Measurements are made using linearly polarized electric field antennas with a nominal 50-Ω output impedance. **Table 6** and **Figure 8** show the antennas recommended in CISPR 25 to increase the consistency of results between laboratories.

Frequency range	Recommended antenna	Measurement polarization
150 kHz to 30 MHz	1-m vertical monopole with counterpoise	Vertical only
30 MHz to 300 MHz	Biconical	Horizontal and vertical
200 MHz to 1 GHz	Log-periodic	
30 MHz to 1 GHz	Broadband (bilog)	
1 GHz to 2.5 GHz	Horn or log-periodic	

Table 6. *Recommended electric field antennas per CISPR 25; the biconical and log-periodic antenna overlap in frequency, whereas a bilog antenna covers their respective frequency ranges.*

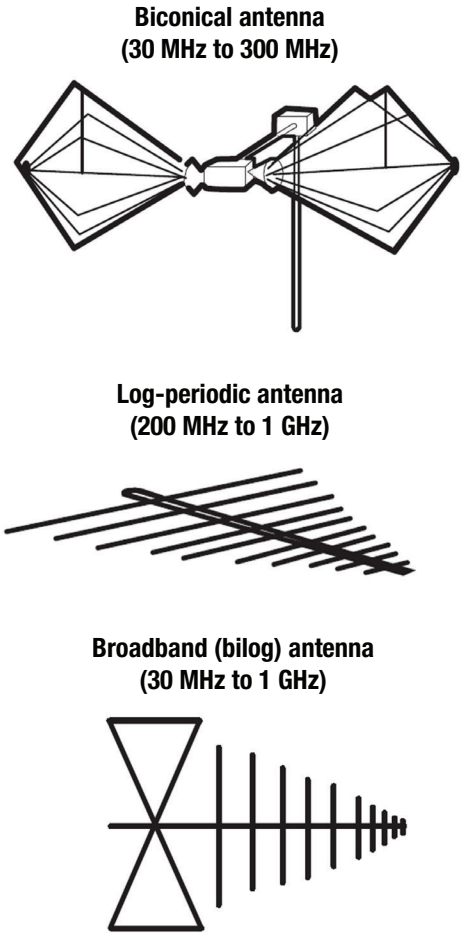


Figure 8. *Measurement antennas per the CISPR 25 specification.*

A passive/active rod monopole antenna with counterpoise is used for low-frequency measurements. Biconical and log-periodic dipole array antennas generally cover the frequency ranges of 30 MHz to 200 MHz and 200 MHz to 1 GHz, respectively. Finally, a dual-ridge horn antenna is common for the 1- to 2.5-GHz range. The broadband bilog antenna is a larger format than the biconical or log-periodic antennas and is sometimes used to cover the frequency range from 30 MHz to 1 GHz.

Radiated EMI tests using ALSE

Figures 9, 10 and **11** depict the typical setups using the CISPR 25 ALSE method, also known as the antenna method, for radiated emission measurements over the frequency ranges specified in Table 6.

The EUT and cable harness are placed on a nonconductive, low relative permittivity material ($\varepsilon_r \leq 1.4$) 50 mm above the ground plane. The length of the harness parallel to the front of the ground plane is 1.5 m, with the total length of the test harness between the EUT and the load simulator not to exceed 2 m. The long segment of the test harness is located parallel to the edge of the ground plane facing the antenna at a distance 100 mm from the edge. The requirements on the ground plane are a minimum width and length of 1 m and 2 m, respectively, or underneath the entire equipment plus 200 mm, whichever is larger. Based on the near- to far-field transition given by Equation 2 and the antenna distance of 1 m, it is important to note that measurements in the EUT's near-field region occur at frequencies below 48 MHz.

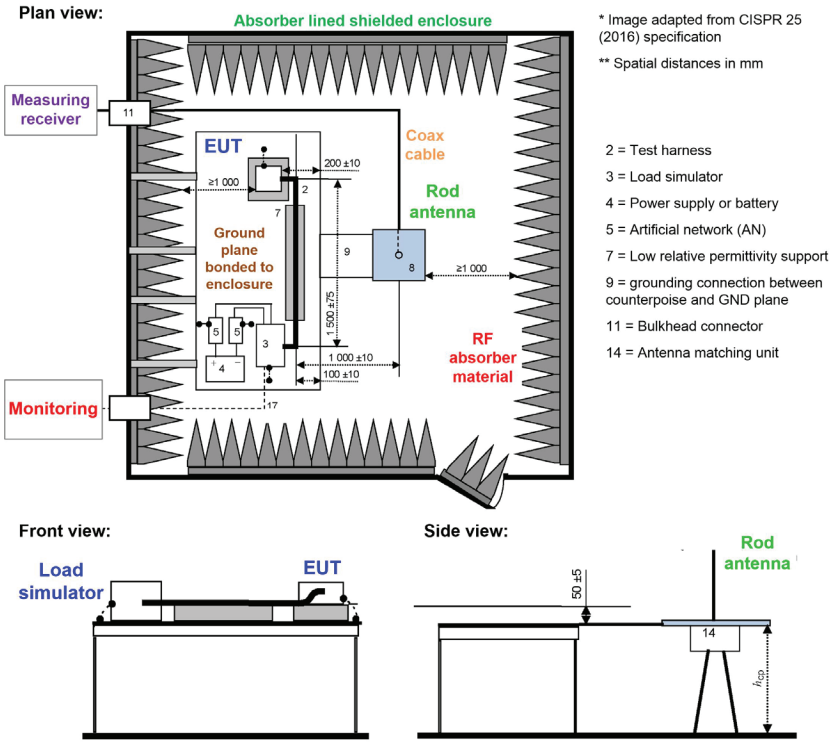


Figure 9. *CISPR 25 radiated emissions measurement setup, monopole rod antenna (150 kHz to 30 MHz).*

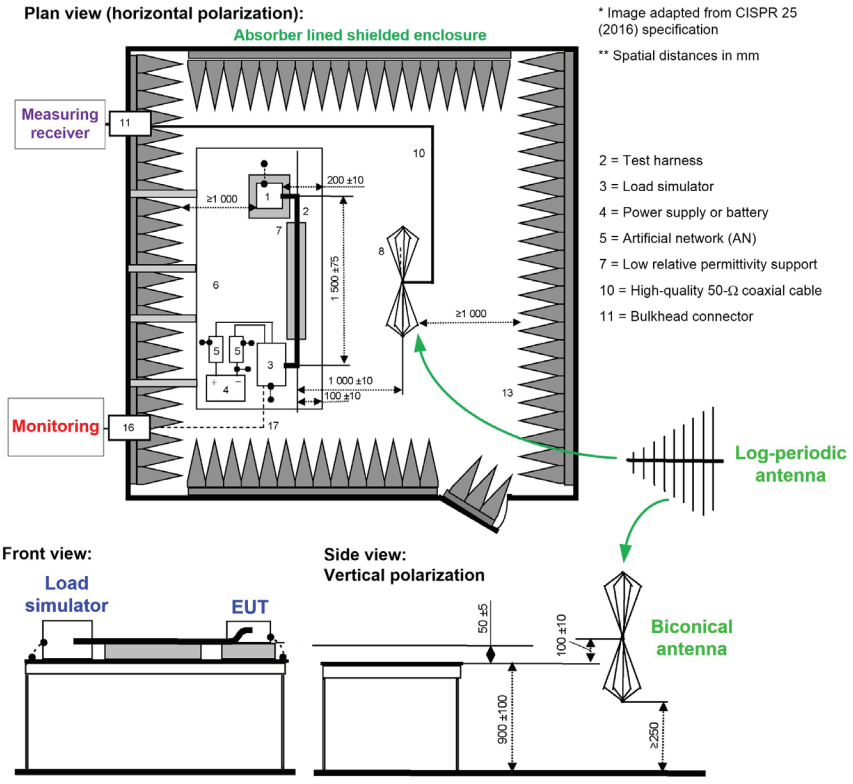


Figure 10. *CISPR 25 radiated emissions measurement setup with biconical antenna (30 MHz to 300 MHz) or log-periodic antenna (200 MHz to 1 GHz).*

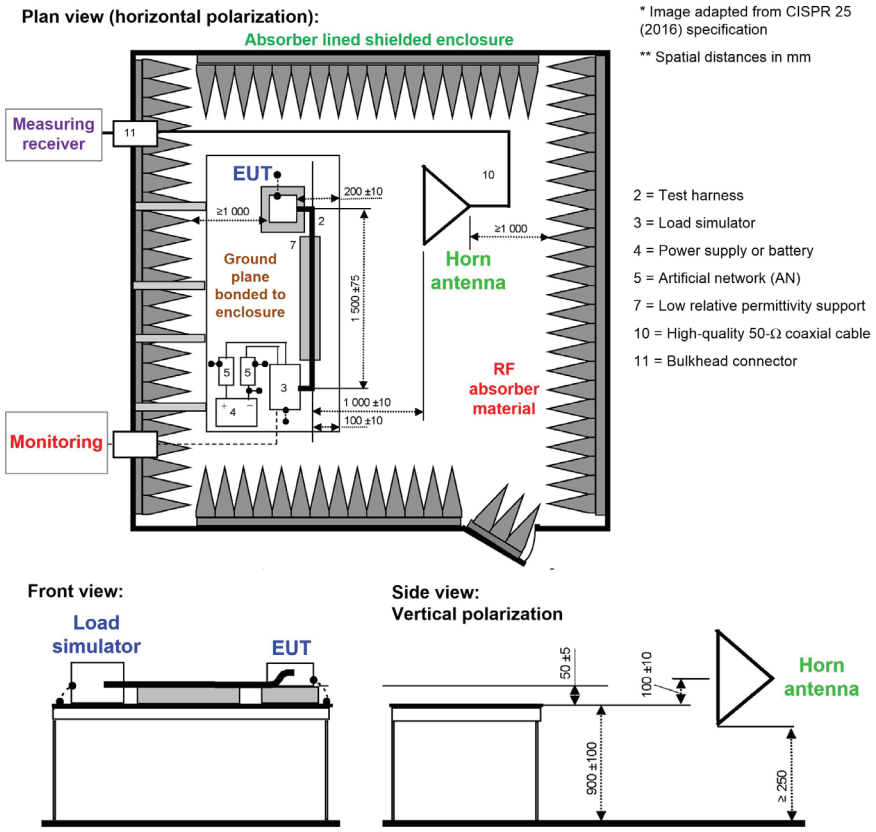


Figure 11. *CISPR 25 radiated emissions measurement setup, horn antenna (above 1 GHz).*

The horn antenna is aligned with the EUT, whereas the other antennas are placed in the midpoint of the wiring harness. All measurements are performed with a 1-m antenna distance. Measurements in the frequency range from 150 kHz to 30 MHz are performed with vertical antenna polarization only. Scans from 30 MHz to 2.5 GHz are performed in both the horizontal and vertical polarizations.

As described earlier, the detected antenna voltage by the EMI receiver combined with the AF provides the electric field strength at the antenna location. Note that independent AFs may apply for horizontal and vertical polarizations, so appropriate AF values are used for measurement in each polarization.

Radiated EMI pre-compliance testing and results

Figure 12 is a photo of the radiated emissions test setup for the Texas Instruments LM53635-Q1 automotive-grade synchronous buck converter [40]. The EUT is powered by a car battery with a line-impedance stabilization network connected on both the positive and negative supply lines.

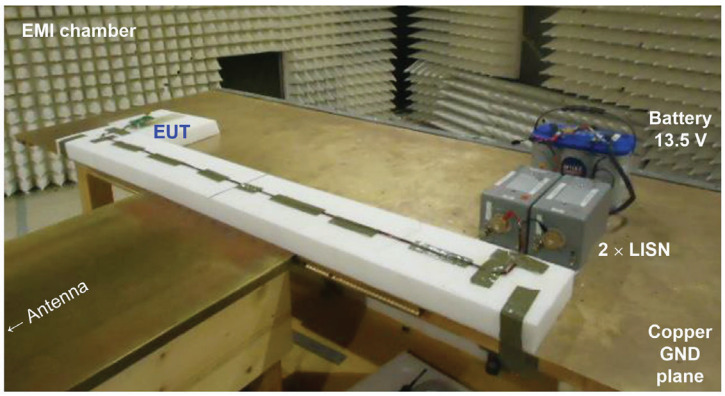


Figure 12. *Photo of CISPR 25 pre-compliance measurement setup.*

The output is 3.3 V at a 3.5-A resistive load. The switching frequency is 2.1 MHz, above the AM band as required in many automotive systems, with spread-spectrum frequency modulation (see Chapter 9) enabled. **Figures 13 through 16** show the measurement results using the various test antennas to pass CISPR 25 Class 5 limits.

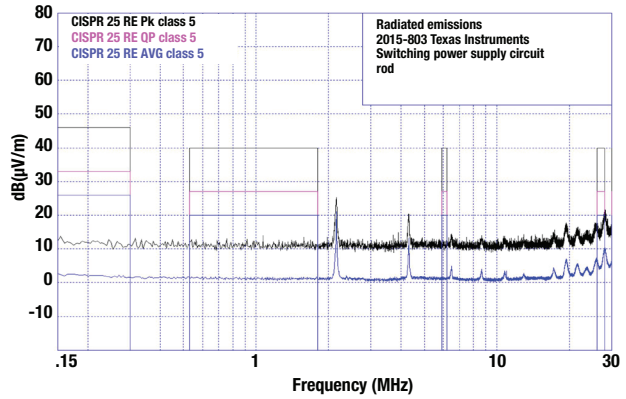


Figure 13. *Radiated emissions results: 150 kHz to 30 MHz, rod antenna, vertical polarization.*

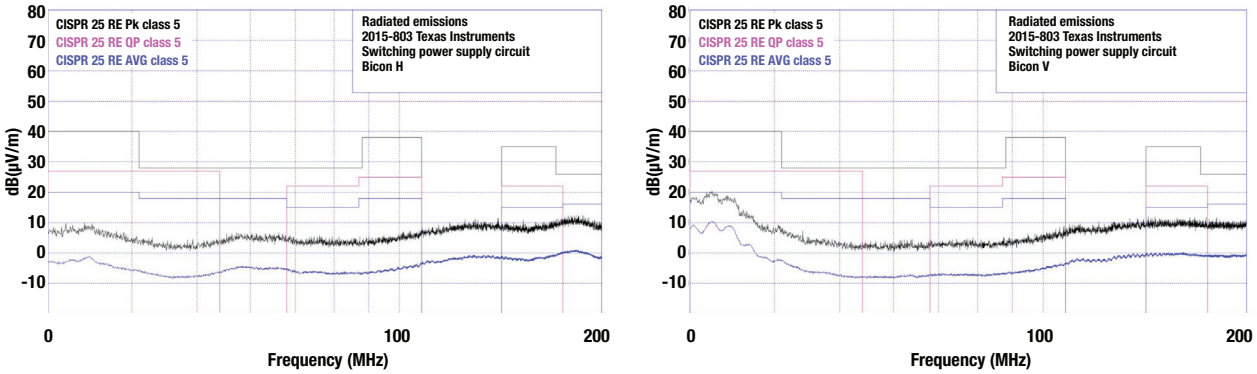


Figure 14. *Radiated emissions results: 30 MHz to 300 MHz, biconical antenna, horizontal and vertical polarizations.*

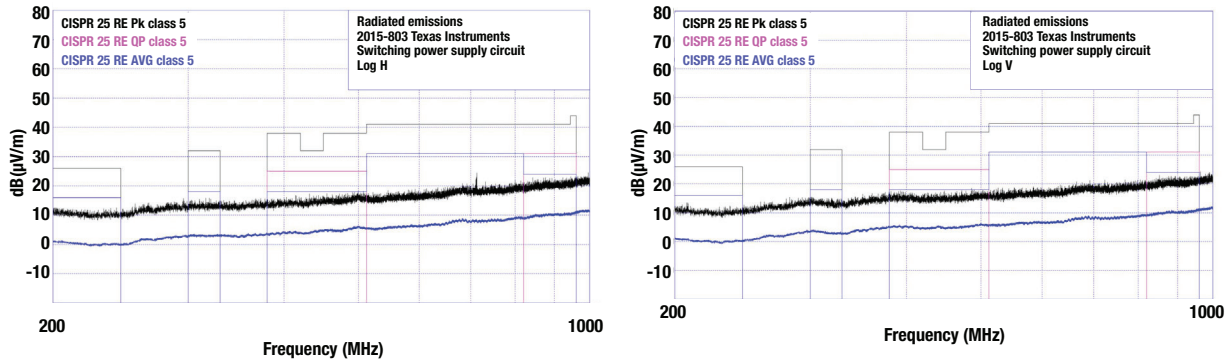


Figure 15. *Radiated emissions results: 200 MHz to 1 GHz, log-periodic antenna, horizontal and vertical polarizations.*

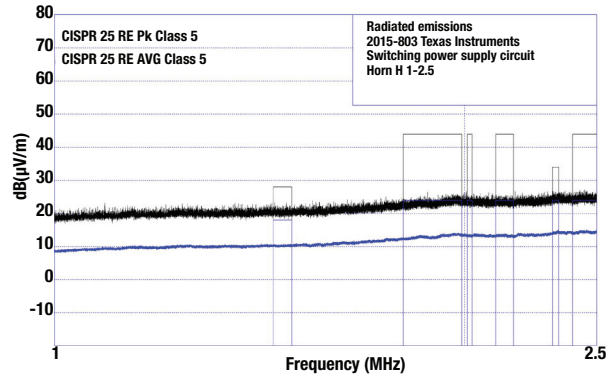


Figure 16. *Radiated emissions results: 1 GHz to 2.5 GHz, horn antenna, horizontal polarization.*

5. Mitigation techniques using integrated FET designs

In general, a converter should pass conducted electromagnetic interference (EMI) by a reasonable margin to have any chance of meeting radiated limits. Fortunately, most steps taken to abate conducted emissions are correspondingly effective in mitigating radiated EMI [42].

Printed circuit board (PCB) layout steps to reduce EMI include minimizing the current "hot loop" area in the layout, avoiding disruption of the current path, using a four-layer PCB with inner ground planes for shielding (yielding much better performance than a two-layer PCB), and routing minimal switch-node copper area to reduce electric field (e-field) radiated coupling.

Converter package type is an important criterion, as new device generations show significantly improved performance in terms of switch-node ringing and pinout design for optimal capacitor placement. From an input filtering standpoint, low-frequency noise (generally less than 10 MHz) is relatively straightforward to suppress with a conventional inductor-capacitor (LC) filter stage, whereas high-frequency noise (above 10 MHz) typically needs an additional common-mode (CM) choke, a ferrite bead filter stage, or both. A metal case shield soldered to the PCB ground plane also effectively mitigates high-frequency emissions.

This chapter:

- Offers practical examples and guidelines to mitigate EMI, specifically for converter solutions with integrated power metal-oxide semiconductor field-effect transistors (MOSFETs) and a controller.

Understanding the EMI challenge

The major source of EMI in DC/DC converters is attributable to the nature of their fast-switching voltages and currents. The EMI related to a converter's discontinuous input or output current is relatively easy to deal with, but a greater concern relates to the harmonic content of the switching transient voltage (dv/dt) and transient current (di/dt), plus the ringing associated with the switching waveforms.

Figure 1 shows the switch voltage waveform of a noisy synchronous buck converter. The ringing frequency ranges from 50 MHz to 200 MHz depending on parasitics. Such high-frequency content can propagate by near-field coupling either to the input supply lines, nearby components or the output bus (for example, a USB cable). Body diode reverse recovery presents a similar issue, exacerbating the ringing voltage as the recovery current flows in the parasitic loop inductance.

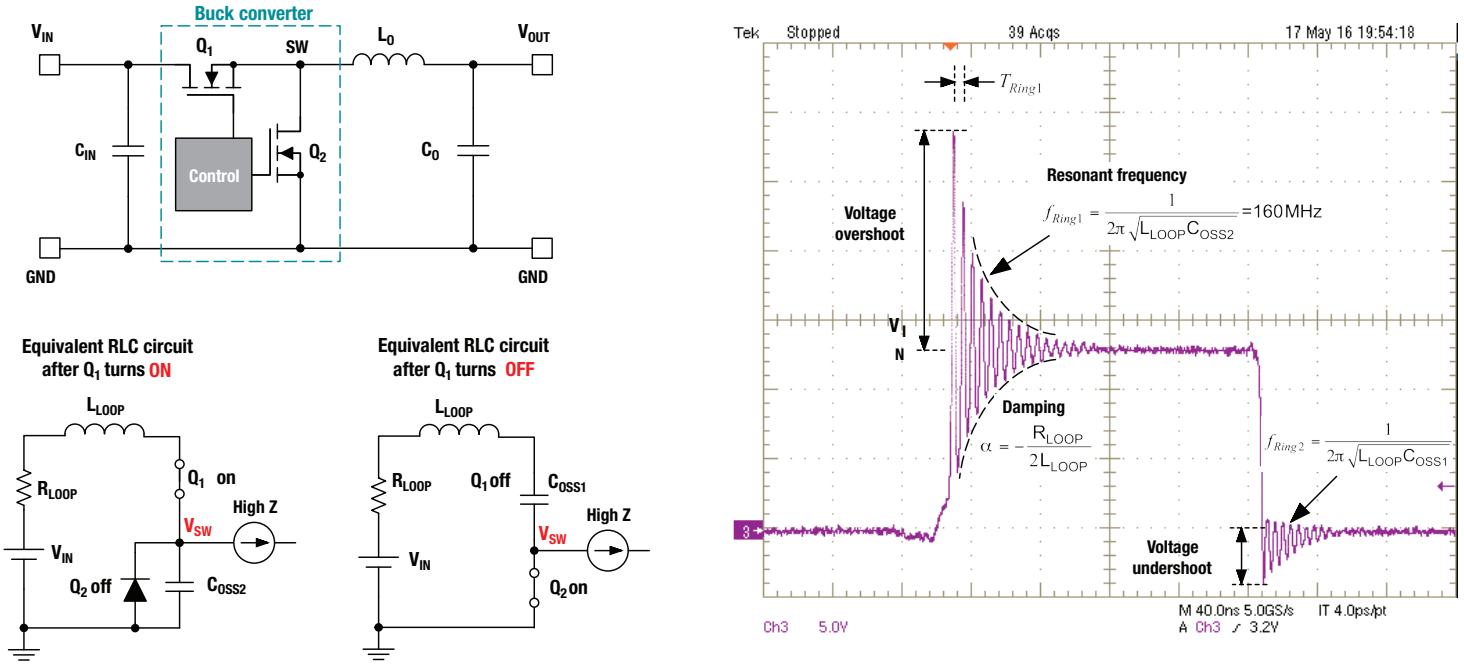


Figure 1. *Switch-node voltage waveform and equivalent circuits during MOSFET turn-on and turn-off switching transitions for a synchronous buck converter.*

The schematic in **Figure 2** identifies the two critical loops for a buck converter circuit. Minimizing the power-loop area is essential because of its proportionality to parasitic inductance and related magnetic field (H-field) propagation. The main design goal is to push the resonant frequency of the parasitic LC tank as high as possible by curtailing the parasitic inductance. This decreases the total stored reactive energy and lowers the switch-voltage peak overshoot.

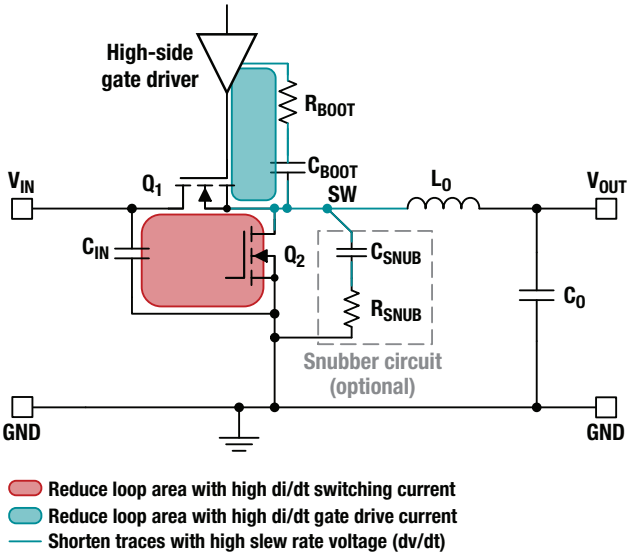


Figure 2. *Simplified synchronous buck converter schematic with critical loops and traces identified for EMI.*

In the boot capacitor loop shown in Figure 2, an optional series boot resistor, designated R_{BOOT}, controls the turn-on speed of the high-side MOSFET. The boot resistor changes the drive-current transient rate and thus reduces the switch voltage and current slew rates during MOSFET turn-on. Another option is to use a snubber circuit from SW to GND. Similarly, this snubber should also occupy a minimal loop area based on its di/dt spike at each switching transition. Of course, snubbers and gate resistors increase switching power loss, leading to a trade-off between efficiency and EMI. Other techniques are required to solve the EMI challenge if efficiency and thermal performance are also important.

Converter PCB layout

Here are the essential guidelines for PCB layout and component placement for a reduced DC/DC converter EMI signature:

- Routing and component placement:
  - Route all power-stage components on the top side of the PCB. Avoid locating the inductor on the bottom side, where it can radiate to the reference plane of the EMI test setup.
  - Place VCC, VDD and/or BIAS bypass capacitors close to their respective pins. Ensure that the AGND pin "sees" the C_{VCC} and C_{BIAS} capacitors first before connecting it to GND.
  - Connect the bootstrap capacitor close to the BOOT and SW pins. Shield the C_{BOOT} capacitor and switch node with adjacent ground copper to reduce CM noise.
- Ground plane design:
  - Position a layer 2 ground plane in the PCB layer stackup as close as possible to the top layer. This provides H-field cancellation, parasitic inductance reduction and noise shielding.
  - Use low z-axis spacing between the top layer and second layer for optimal image plane effectiveness. Define a 6-mil intralayer spacing in the PCB stackup specification.
- Input and output capacitors:
  - Place C_{IN} to minimize the loop area formed by C_{IN} connections to the VIN and PGND pins.
  - Ground return paths for both C_{IN} and C_{OUT} should consist of localized top-side planes. Connect DC current routes using multiple external or internal ground planes.
  - Use 0402 or 0603 case size ceramic input capacitors near the VIN and PGND pins to minimize parasitic loop inductance.
- Inductor and switch-node layout:
  - Locate the inductor close to the SW pin of the integrated circuit (IC). Minimize the switch-node copper surface area to prevent excessive capacitive coupling.
  - Confine switch-node noise using adjacent ground guarding and via shielding.

- Check the inductor dot position to ensure that the end of the inductor winding tied to SW is on the bottom and inside of the winding geometry and shielded by the outer turns of the winding connected to VOUT.
- Use an e-field-shielded inductor if possible. Connect the shield terminals to the PCB ground plane.
- Select an inductor with terminations underneath the package. Avoid large sidewall terminations that can act as radiating antenna.

- EMI management:
  - Route the EMI filter components away from the switch node. Place the EMI filter on the opposite side of the board from the converter if it is not possible to separate it sufficiently from the power stage.
  - Place cutouts on all layers below the EMI filter to prevent parasitic capacitive paths from affecting the filter attenuation characteristic.
  - Place a resistor (preferably less than 10 Ω) in series with C_{BOOT}, if needed, to slow down a buck converter's high-side MOSFET turn-on, reducing the switch-node voltage slew rate, overshoot and ringing.
  - If a switch-node RC snubber is required, connect the smallest footprint component to SW (usually the capacitor).
  - Use a four-layer PCB with inner ground planes to achieve much improved performance relative to a two-layer design. Avoid disruption of the high-frequency current paths near the IC.

EMI input filter

Figure 3 shows a typical multistage EMI input filter. Low- and high-frequency sections provide differential-mode (DM) noise attenuation, and an optional π-stage with a CM choke delivers CM attenuation. An electrolytic capacitor, designated C_{BULK}, has an inherent equivalent series resistance that sets the required damping to reduce the effective Q-factor at the converter input and maintain input filter stability [43].

The self-resonant frequency (SRF) of the DM inductor limits the achievable high-frequency DM attenuation of the first filter stage. A second filter stage is often essential to provide supplemental DM attenuation at a high frequency using a ferrite bead, with impedance typically rated at 100 MHz. Ceramic capacitors, designated C_{F1} and C_{F2}, shunt noise to GND.

In general, the DM filter inductance is sized to attenuate the fundamental and low-frequency harmonics. Use the minimum inductance possible to meet the low-frequency filtering demands, as a higher inductance with more turns increases the inductor's equivalent parallel capacitance and thus the SRF, compromising its performance at high frequencies.

The CM choke, designated L_{CM}, offers a high impedance to CM currents, and its leakage inductance also provides DM attenuation. Nevertheless, this component is undesirable in certain applications where the ground connection must remain intact, making quieter converter designs that obviate the need for a CM choke more favorable.

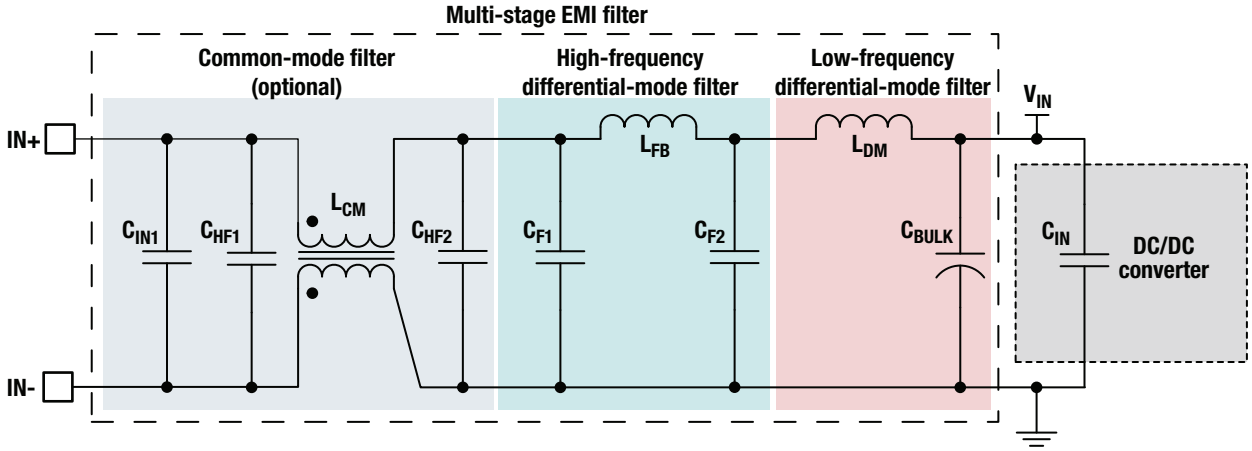
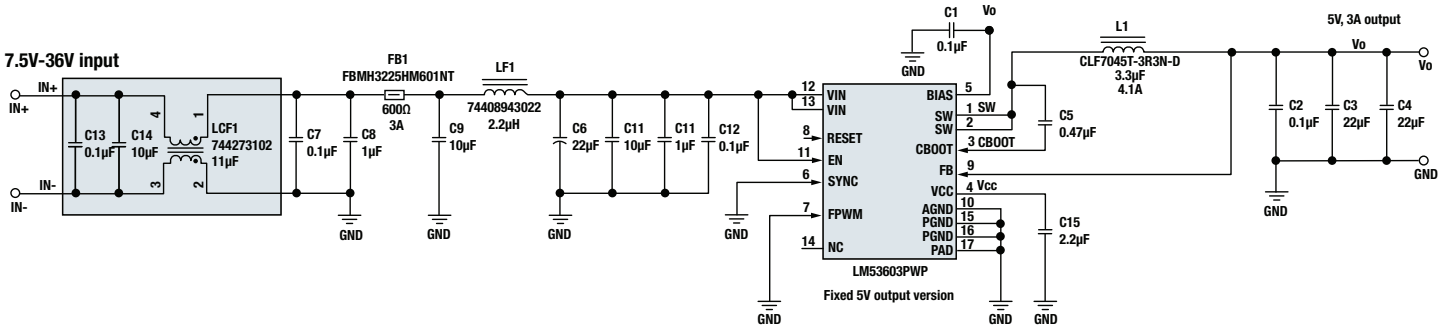


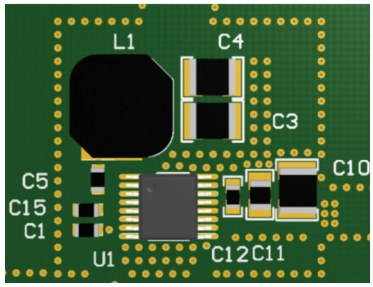
Figure 3. *Three-stage EMI input filter with DM and CM stages.*

To demonstrate the effectiveness of a CM choke, **Figure 4** illustrates the Texas Instruments LM53603, a 36-V, 3-A DC/DC converter solution using a two-layer PCB [44]. The power stage is located on the top layer and the EMI input filter is on the bottom. As the layouts in Figure 4 show, via stitching the ground plane copper around the filter provides a shielding effect. Also, inserting copper plane cutouts on all layers underneath the filter stage avoids any parasitic capacitance that may form between VIN and GND traces, providing a path for noise currents to bypass the CM choke and compromising the filter's impedance characteristic.

Power stage and EMI input filter



PCB layout implementation



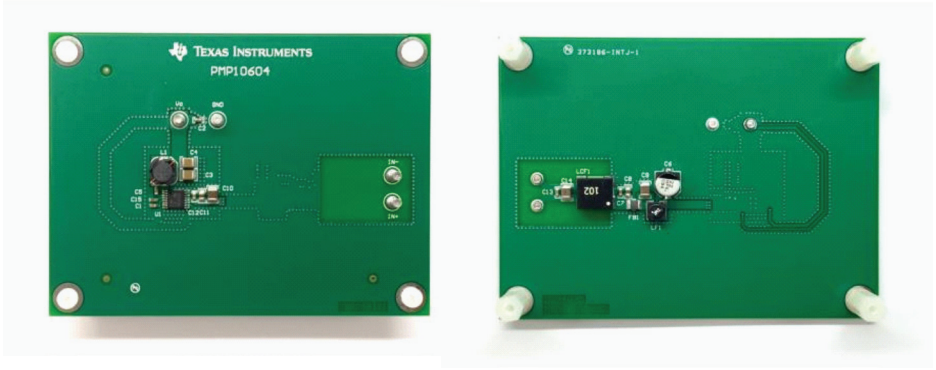


Figure 4. *DC/DC converter schematic and PCB layout implementation.*

Figure 5 presents CISPR 25 conducted emissions measurements from 150 kHz to 108 MHz for the converter design in Figure 4. The results are provided with and without the CM choke. Using a Rohde & Schwarz spectrum analyzer, peak and average detector scans are denoted in yellow and blue, respectively. The limit lines in red are the Class 5 peak and average limits (peak limits are generally 20 dB higher than the average limits).

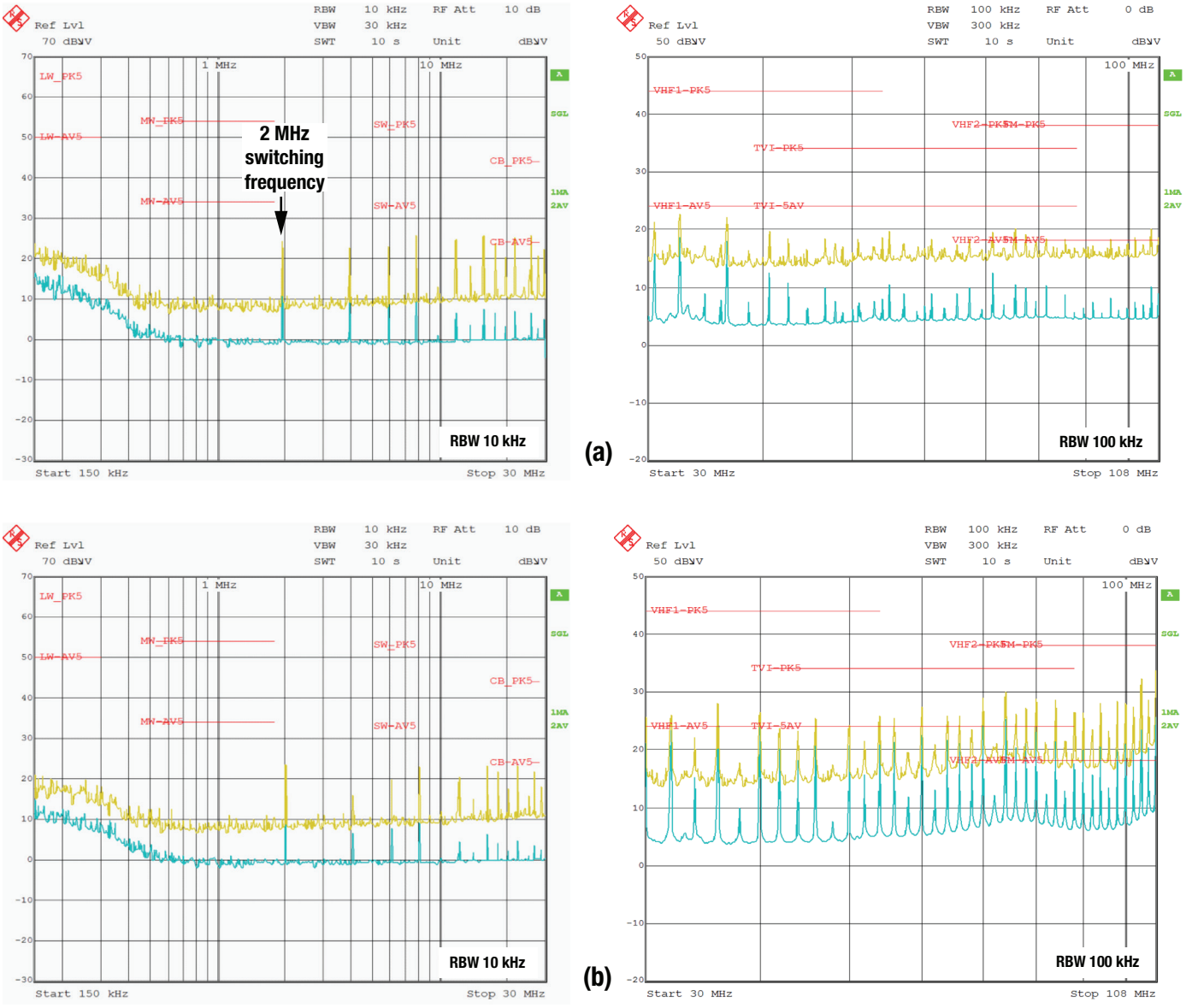


Figure 5. CISPR 25 conducted EMI measurements with CM choke (a); and without CM choke (b).

Metal case shielding

Another very effective way to optimize high-frequency EMI performance is to add a metal case shield [42] to block the radiated electric field. The case is typically made of aluminum and implemented as a frame (open-top) or closed-top design. The shield covers all power-stage components except the EMI filter and is connected to GND on the PCB, essentially forming a Faraday cage with the PCB ground plane.

The result is a dramatic reduction in radiated noise coupling from the switching cell to the EMI filter or onto long input wire connections (which also act as an antenna). Of course, the shield incurs additional component and assembly costs, and thermal management and testing become more difficult. The case of an aluminum can electrolytic capacitor may also provide e-field shielding and can be tactically positioned on the board for this purpose.

DC/DC converter case study

Figure 6 is a schematic of a 60-V, 1.5-A monolithically integrated synchronous buck converter circuit [45] with several features in place for optimal EMI performance. The schematic also shows a two-stage EMI input filter stage designed to meet EMI specifications for automotive or noise-sensitive industrial applications.

To help translate to an optimized PCB layout, the schematic highlights the high-current traces (VIN, PGND, SW connections), noise-sensitive nets (FB) and high dv/dt circuit nodes (SW, BOOT).

Pinout design

The converter IC in Figure 6 has the benefit of a symmetrical and balanced pin arrangement for VIN and PGND. It uses two input loops in parallel that result in effectively half the parasitic loop inductance. These loops are labeled IN1 and IN2 in the PCB layout shown in **Figure 7**. Two capacitors with a small 0402 or 0603 case size, designated C_{IN1} and C_{IN3} in Figure 6, are placed as close as possible to the IC to configure the minimum input loop area. The circulating currents create opposing magnetic moments that result in H-field cancellation and thus lower the effective inductance. To further reduce parasitic inductance, a continuous ground plane for return current underneath the IN1 and IN2 loops on layer 2 of the PCB (immediately below the top layer power circuit) supports a field self-cancellation effect.

Using two ceramic output capacitors, C_{O1} and C_{O2} (one on each side of the inductor) similarly optimizes the output current loops. Having two parallel ground return paths from the output splits the return current in two, helping mitigate the “ground bounce” effect.

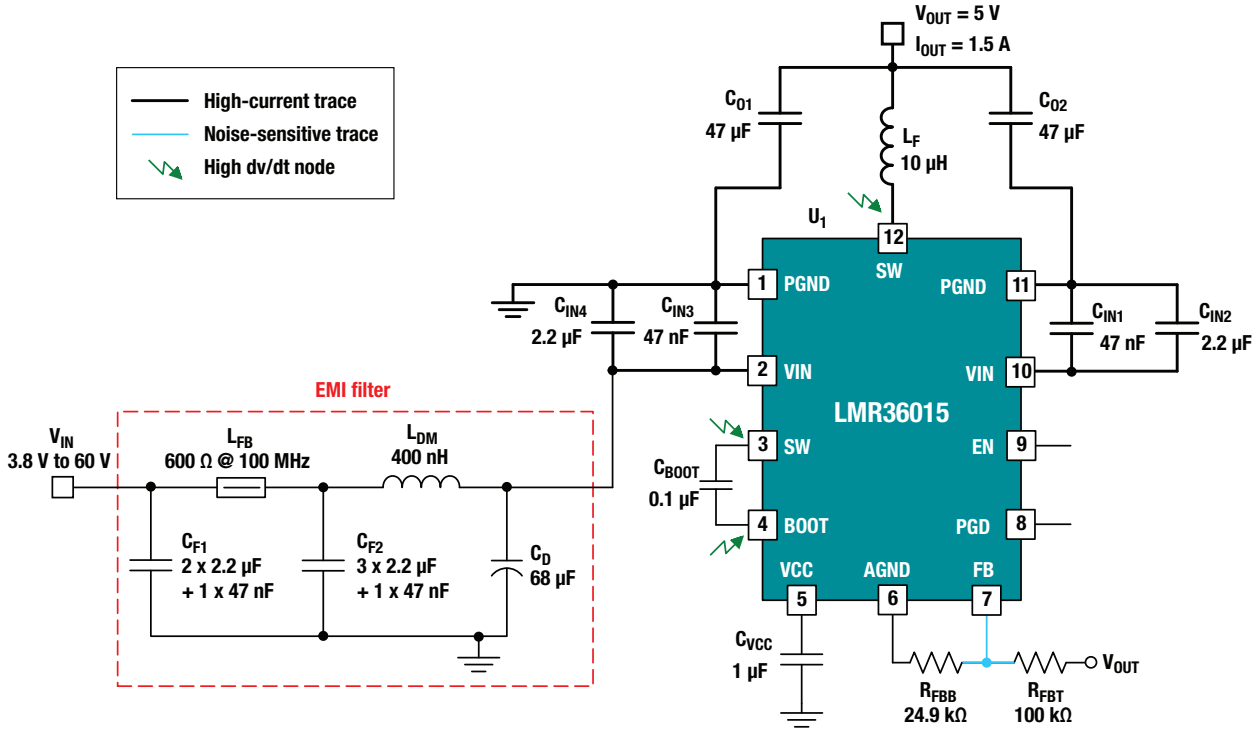


Figure 6. *DC/DC converter with EMI-optimized package and pinout. Included is a two-stage EMI input filter.*

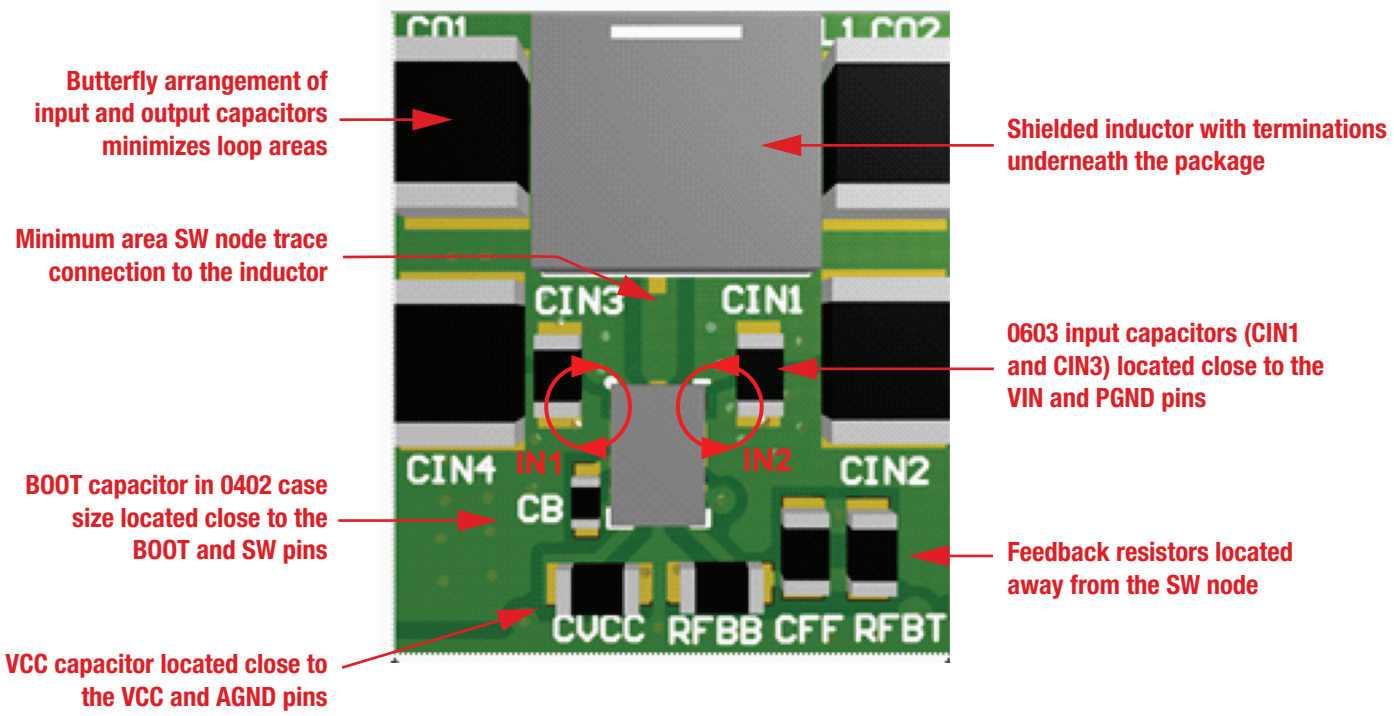


Figure 7. Power-stage layout routed only on the top layer of the PCB.

The SW pin is located at the center of the IC such that the radiated e-field is shielded by adjacent VIN and PGND pins on both sides of the IC. GND plane copper shields the polygon pour connecting the IC's SW pin to the inductor terminal. The single-layer SW and BOOT layout implies that vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during EMI testing.

Package design

In tandem with optimized pinout, power converter IC package design is a key attribute in the quest to improve EMI signatures. For example, HotRod™ package technology from TI uses a flipped-chip-on-leadframe (FCOL) technique that eliminates power device wire-bonds that typically cause high package parasitic inductance.

Figure 8 shows that the IC is flipped upside down and copper posts (otherwise known as bumps or pillars) on the IC are soldered directly to the leadframe. This construction method enables high density and a low profile, as each pin is attached directly to the leadframe. Most important from an EMI standpoint, the HotRod package lowers package parasitic inductance versus traditional wire-bond packages [46].

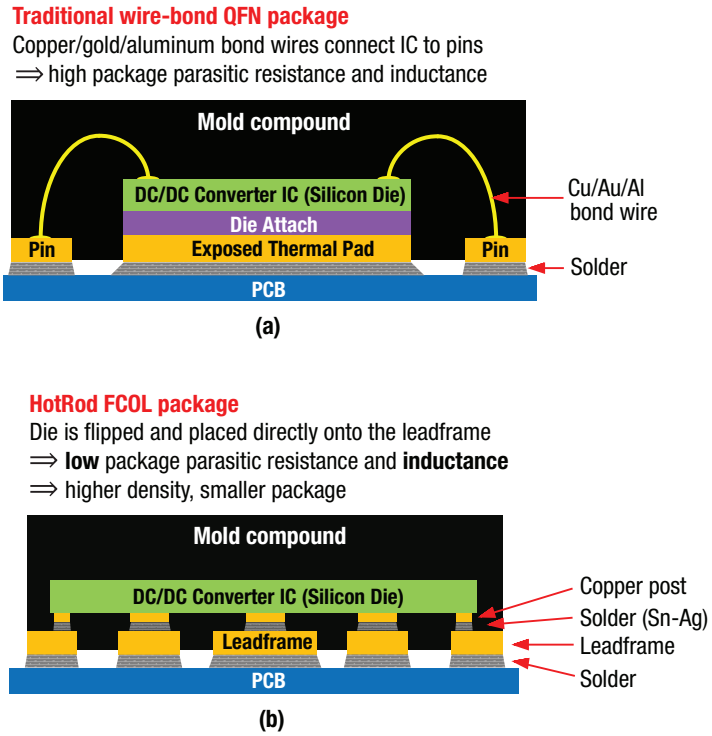


Figure 8. Wire-bond QFN (a) and HotRod FCOL (b) package construction comparison.

Not only does the HotRod package result in much lower ringing at the switching commutations (a 50 MHz to 200 MHz frequency range), it also reduces both conduction and switching losses. **Figure 9** shows the concomitant improvement in switch-node voltage ringing. **Figure 10** shows the conducted emissions measured from 150 kHz to 108 MHz for the converter in Figure 6. The results are in compliance with CISPR 25 Class 5 requirements [47].

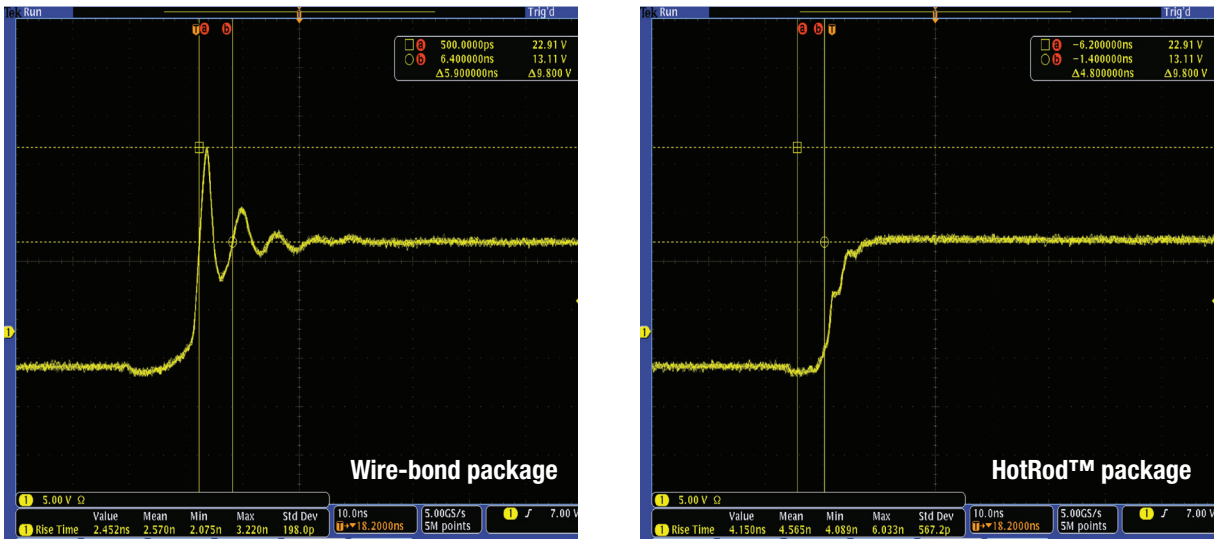


Figure 9. *Switch-node voltage waveform with a traditional wire-bond converter (a); and a HotRod FCOL converter (b).*

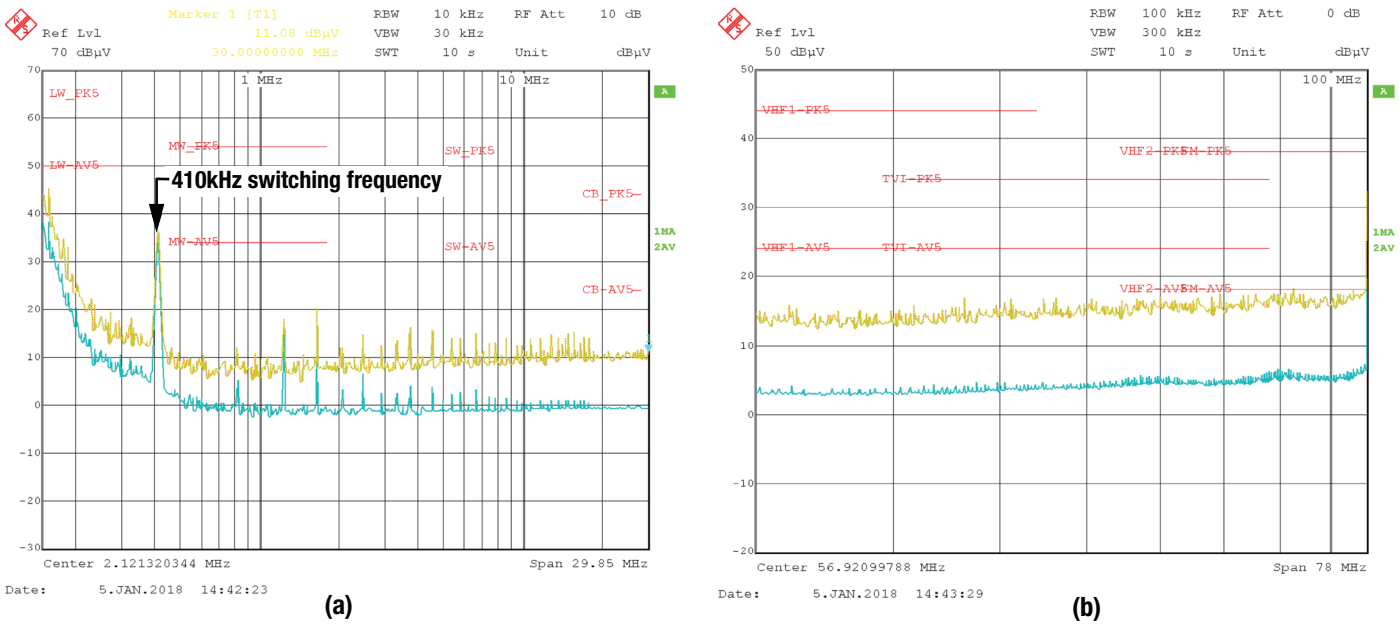


Figure 10. *CISPR 25 conducted emission results, 150 kHz to 30 MHz (a); 30 MHz to 108 MHz (b).*

6. Mitigation techniques using discrete FET designs

The switching transients of power semiconductor devices are the chief sources of both conducted and radiated electromagnetic interference (EMI). This chapter highlights printed circuit board (PCB) layouts to lower EMI in DC/DC regulator circuits that use a controller with external metal-oxide semiconductor field-effect transistors (MOSFETs). The essential layout recommendations are to minimize the current "hot loop" area in the layout; avoid disruption of the current path; use a multilayer PCB with inner ground planes for shielding (yielding much better performance than a two-layer PCB); route short, direct gate-drive traces as differential pairs; and use a minimal switch-node copper area to reduce electric field (e-field) radiated coupling.

An optimized PCB layout can help improve a regulator's EMI signature (without the sacrifice of efficiency or thermal performance associated with other "fixes" commonly used to reduce EMI). Beyond an EMI-aware synchronous buck power stage, you can generally extend these concepts to any DC/DC regulator as long you identify the critical loops and implement the recommended layout techniques.

This chapter:

- Explores EMI abatement in DC/DC regulator circuits that employ a controller driving a discrete pair of high- and low-side power MOSFETs.
- Covers guidelines for laying out a multilayer PCB of a half-bridge design with MOSFETs and a controller to achieve excellent EMI performance. The imperative is to minimize critical loop parasitic inductances through careful power-stage component selection and PCB layout.
- Demonstrates that it's possible to reduce the generation of conducted electromagnetic emissions without sacrificing efficiency or thermal performance metrics.

EMI and controllers

An implementation using a controller and external MOSFETs – such as that shown in the synchronous buck regulator circuit shown in **Figure 1** – offers numerous advantages. These include increased current capability; better thermal performance; and a higher level of flexibility in terms of design choices, component selection and available features.

From an EMI perspective, however, a controller solution with discrete FETs is considerably more challenging to design and implement vis-à-vis a converter with integrated FETs. Two primary considerations apply here. First, the PCB layout of a power stage with MOSFETs and a controller cannot be as compact as a power converter integrated circuit (IC) with optimized pinout and internal gate drivers. Second, dead-time management is typically more precise in a converter IC where the MOSFET switching times are fully characterized. As a result, body diode conduction times are shorter, leading to improved switching performance and lower noise related to reverse recovery.

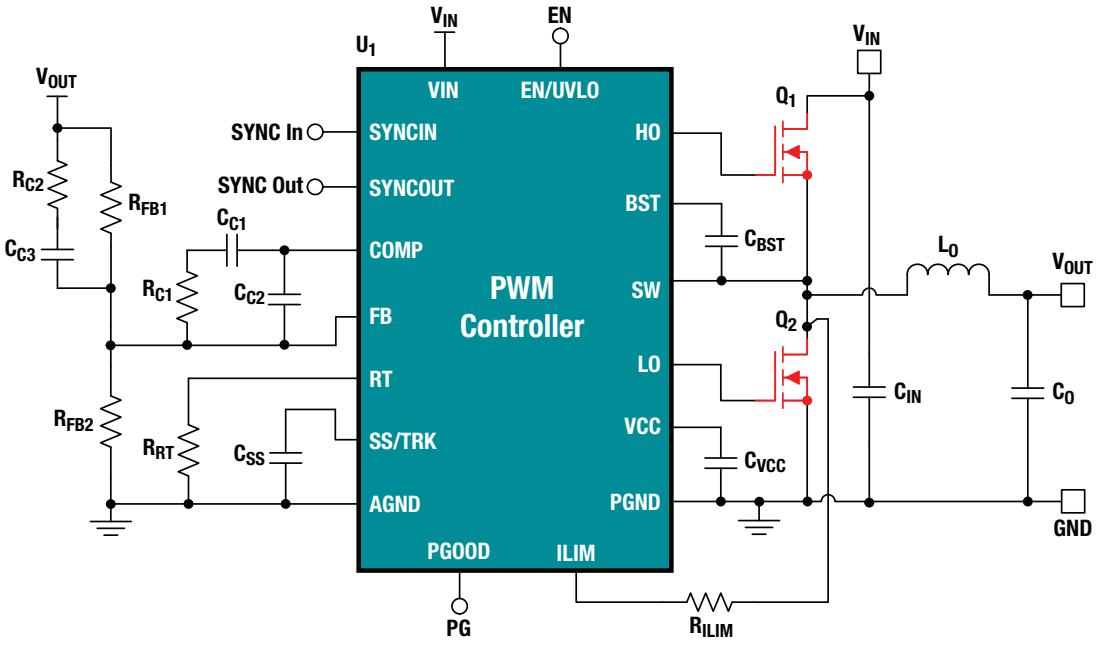


Figure 1. Schematic of a synchronous buck controller driving power MOSFETs Q_1 and Q_2.

Appreciating the EMI challenge

Three essential elements must exist for EMI to occur: an electrical noise source, a coupling path and a victim receptor. It's possible to achieve interference suppression and hence electromagnetic compatibility by addressing any or all of these aspects. In practice, you can employ several techniques to disrupt coupling paths and/or harden potential victims, such as inserting an EMI filter to suppress conducted interference and using shielding to mitigate radiated interference.

The low-frequency EMI spectral amplitude related to a buck regulator's discontinuous input current (or a boost's discontinuous output current) is relatively easy to deal with using a conventional filter stage. However, a greater concern relates to the harmonic content from the high transient voltages (dv/dt) and transient currents (di/dt) associated with the sharp edges of voltage and current during switching commutation. High-current gate drivers (typically integrated in the controller for voltages less than 100 V) can switch power MOSFETs at extremely high speeds. Slew rates greater than 10 V/ns and 1 A/ns are common with conventional silicon FETs, while gallium nitride-based devices make much higher slew rates possible. Chapter 2 investigated relationships between the time-domain characteristics of trapezoidal switching waveforms and their spectral content, explaining that the steepest slope of the waveform determines the high-frequency spectrum asymptotical envelope, and methods to reduce dv/dt and di/dt are thus useful to diminish the EMI generation potential.

In addition to the sharp voltage and current edges, also troublesome is the overshoot/undershoot and subsequent ringing associated with switching waveforms. **Figure 2** shows the switch-node voltage waveform of a hard-switched synchronous buck regulator. The switch-node voltage ringing frequency ranges from 50 MHz to 250 MHz depending on the resonance of the parasitic power-loop inductance (L_{LOOP}) with the MOSFET output capacitance (C_{OSS}). Such high-frequency content can propagate by near-field coupling (see Chapter 4) either to the output bus, nearby components or the input supply lines, and is difficult to attenuate with conventional filtering. Synchronous MOSFET body diode reverse recovery presents similar negative effects, exacerbating the ringing voltage as the diode recovery current flows in the parasitic loop inductance.

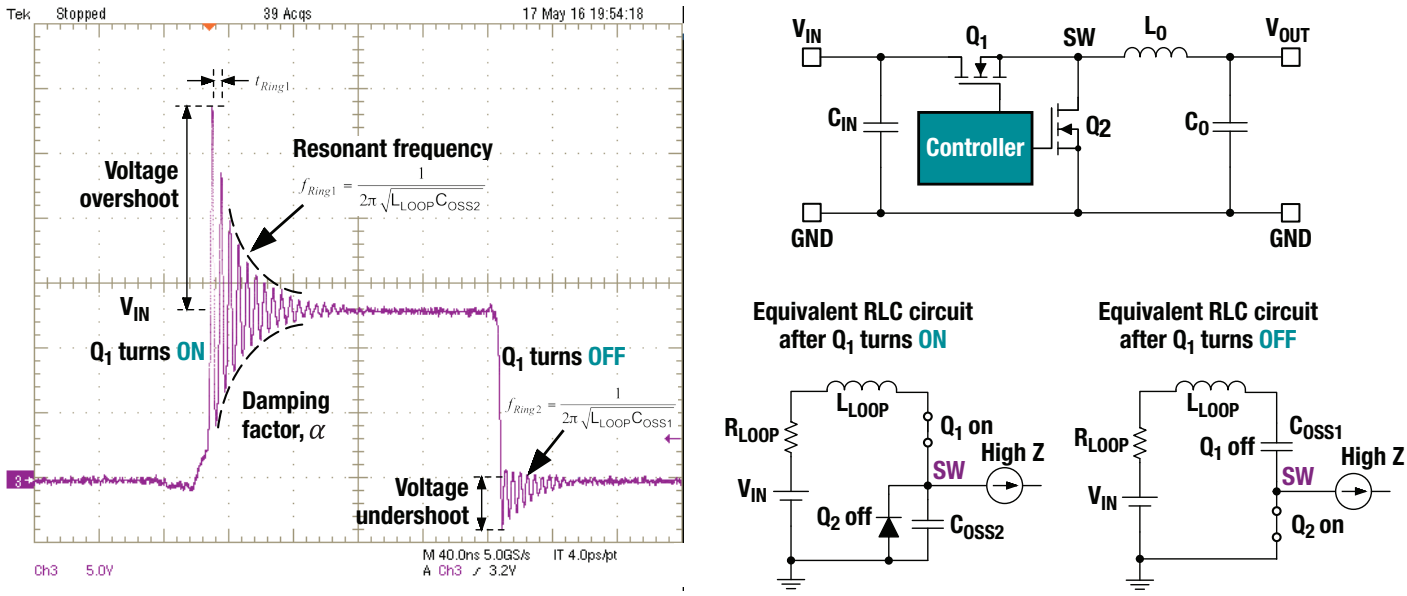


Figure 2. *Switch-node voltage waveform and equivalent circuits during MOSFET turn-on and turn-off transitions for a synchronous buck regulator.*

Figure 3 identifies the critical high-frequency power loop of a buck regulator circuit [48] representing circuit elements with a high slew-rate current. You can apply a similar examination to boost, inverting buck-boost, single-ended primary-inductor converter (SEPIC) and other topologies. Minimizing the area of the power loop is essential because of its proportionality to parasitic inductance and related magnetic field (H-field) propagation (see Chapter 3). The main design goal is to push the resonant frequency of the parasitic LC tank as high as possible by curtailing the parasitic inductance. This decreases the total stored reactive energy and lowers the switch-node voltage peak overshoot and ringing. Also, the equivalent resistance to achieve a critical damping factor is effectively lower, so any ringing decays earlier – especially as the skin effect at high frequencies increases the parasitic resistance of the loop.

Figure 3 also shows the gate driver loops of the high- and low-side MOSFETs during turn-on and turn-off. Special considerations during layout of the power stage (discussed next) ensure that the power-loop, gate-loop and common-source parasitic inductances are as low as possible.

PCB layout design for low EMI

The following items summarize the essential guidelines for component placement and PCB layout for the lowest noise and EMI signature in a DC/DC regulator. Some of these steps are similar to those provided in Chapter 5 for a converter-based design with integrated MOSFETs. Later, I'll provide a PCB layout case study for an EMI-optimized buck regulator.

- Routing and component placement:
  - Route all power-stage components on the top side of the PCB.
    - Avoid locating the switch-node copper and inductor on the bottom side, where it can radiate to the reference plane of the EMI test setup.
  - Place bypass capacitors for VCC or BIAS close to their respective pins.
    - Ensure that the AGND pin "sees" the C_{VCC} and C_{BIAS} capacitors first before connecting it to GND.
  - Connect the bootstrap capacitor adjacent to the controller's BST and SW pins.
    - Shield the C_{BST} capacitor and switch node with adjacent ground copper to reduce common-mode noise.
- GND plane design:
  - Position a layer-2 ground plane in the PCB layer stackup as close as possible to the power-stage components located on the top layer to provide H-field cancellation, parasitic inductance reduction and noise shielding.
  - Use low z-axis spacing between the top layer and second-layer ground plane for optimal image plane effectiveness.
    - Specify 6-mil intralayer spacing in the PCB stackup specification.

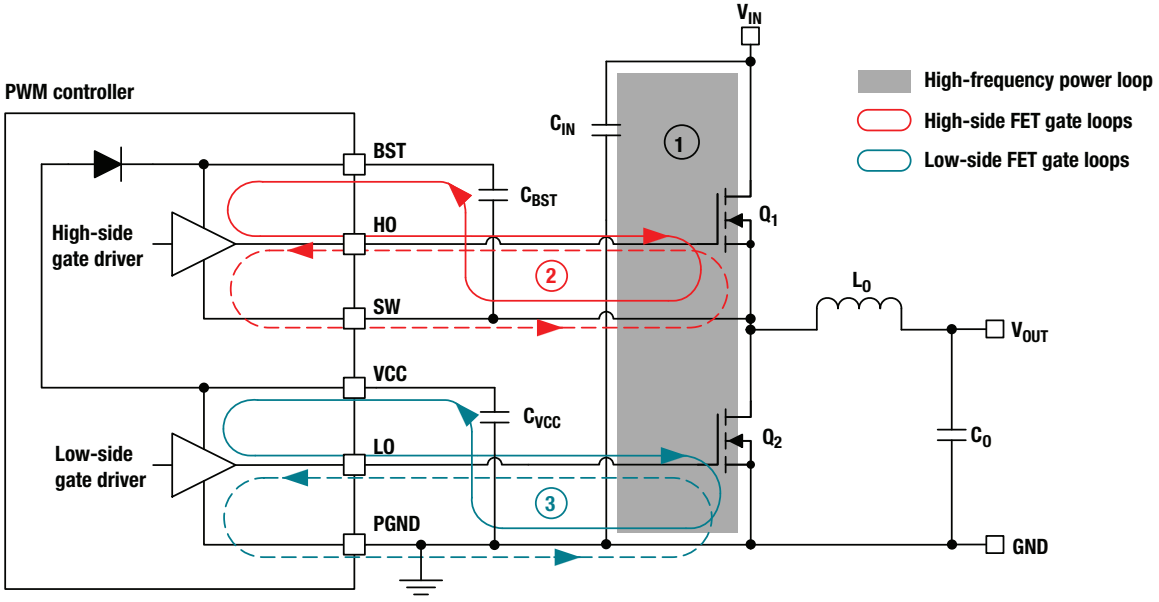


Figure 3. *Identifying the high-frequency current loops critical to EMI for a synchronous buck regulator.*

- Input and output capacitors:
  - Place C_{IN} for a buck regulator to minimize the loop area formed by C_{IN} connections to the power MOSFETs. A similar recommendation applies to C_{OUT} for boost and SEPIC regulators.
  - The power loop classification is lateral or vertical depending on the capacitor placement with respect to the MOSFETs [49].
  - Ground return paths for both C_{IN} and C_{OUT} should consist of localized top-side planes.
    - Connect DC current routes using multiple external or internal GND planes.
  - Use 0402 or 0603 case size ceramic capacitors with low equivalent series inductance (ESL) located close to the MOSFETs to minimize power-loop parasitic inductance.

- Inductor and switch-node layout:
  - Place the inductor close to the MOSFETs.
    - Minimize the switch-node copper polygon area to reduce capacitive coupling and common-mode current. The copper should occupy just the inductor pad and the minimum area required to connect to the MOSFETs' terminals.
  - Confine switch-node noise using adjacent ground guarding and via shielding.
  - Check the inductor's dot position to ensure that the end of the winding tied to the switch node is on the bottom and inside of the winding geometry and shielded by the outer turns of the winding connected to V_{OUT} (for a buck) or V_{IN} (for a boost).
  - Select an inductor with terminations underneath the package.
    - Avoid large vertical sidewall terminations that can act as radiating antenna.
  - Use an e-field-shielded inductor if possible. Connect the shield terminals to the PCB ground plane.
- Gate drive trace layout:
  - Locate the controller as close as possible to the power MOSFETs.
    - Route gate-drive traces for HO and SW differentially with minimal length and loop area directly to the high-side MOSFET's gate and source terminals.
    - Route the gate-drive trace for LO directly to the low-side MOSFET gate above a ground plane with minimal dielectric spacing.
    - Minimize coupling from the power loop to the gate loops by orthogonal routing of the gate-drive traces [49].
- EMI management:
  - Route the EMI filter components to avoid coupling from the electric field radiated by the inductor and switch node.
    - Place the EMI filter on the opposite side of the board from the converter if it is not possible to sufficiently separate it from the power stage.
  - Place cutouts on all layers below the EMI filter to prevent parasitic coupling paths from impacting the filter's attenuation characteristic.
  - Place a boot resistor (preferably less than 10 Ω) in series with C_{BOOT}, if needed, to limit the MOSFET turn-on speed, reducing the switch-node voltage slew rate, overshoot and ringing.
    - The boot resistor changes the drive-current transient rate and thus reduces the switch-node voltage and current slew rates during MOSFET turn-on.
    - For added flexibility, consider using a controller with dedicated source and sink pins for the gate driver(s).
  - Any required switch-node snubber circuit should occupy a minimum loop area based on its transient current spike at each switching transition.
    - Connect the smallest footprint component to SW (usually the capacitor) to minimize its antenna effect.
  - Use a multilayer PCB with inner ground planes to achieve much improved performance relative to a two-layer design.
    - Avoid disruption of the high-frequency current paths near the MOSFETs.
  - Consider using metal case shielding to optimize radiated EMI performance.
    - The shield covers all power-stage components except the EMI filter and is connected to GND on the PCB, essentially forming a Faraday cage with the PCB ground plane.

DC/DC synchronous buck controller case study

Figure 4 shows the schematic of a synchronous buck converter circuit [48] intended for automotive or noise-sensitive industrial applications. It incorporates several included features for improved EMI performance, including constant switching frequency operation, external clock synchronization and switch-node shaping (slew-rate control) by controlled high-side MOSFET turn-on. To help translate to an optimized PCB layout, the schematic highlights the high-current traces (VIN, PGND, SW connections), noise-sensitive nets (FB, COMP, ILIM) and high dv/dt circuit nodes (SW, BST, HO, LO, SYNC). The high di/dt loops are similar to those identified in Figure 3.

Figure 5 shows two lateral loop arrangements of power MOSFETs and input capacitors. The power stage is on the top layer of the PCB with the controller placed on the bottom. The lateral loop design has a circulating current on the top layer (denoted by the white border in Figure 5) that induces an image current on the layer-2 ground plane to achieve flux cancellation and thus lower the parasitic loop inductance.

More specifically, the layout in Figure 5b is modified so that the high-side FET (Q_1) is rotated 90 degrees. This improves heat sinking of Q_1 for better thermal management and allows convenient placement of a low-ESL capacitor (C_{IN1}) in an 0603 case size near the MOSFETs for high-frequency decoupling. The U-shaped layout orientation of the power-stage components positions the output capacitors for a shorter return connection to the low-side MOSFET.

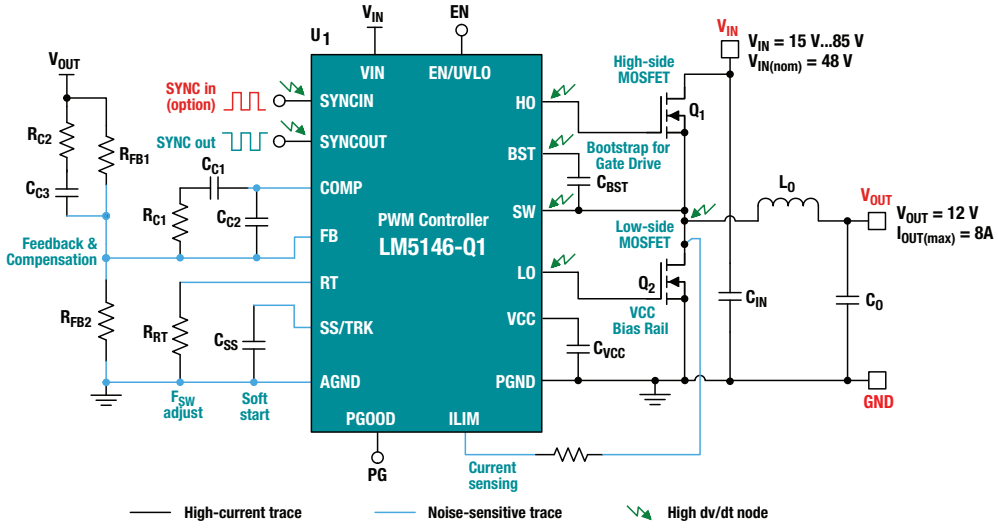


Figure 4. Schematic of a DC/DC buck regulator with important nodes and traces identified for PCB layout.

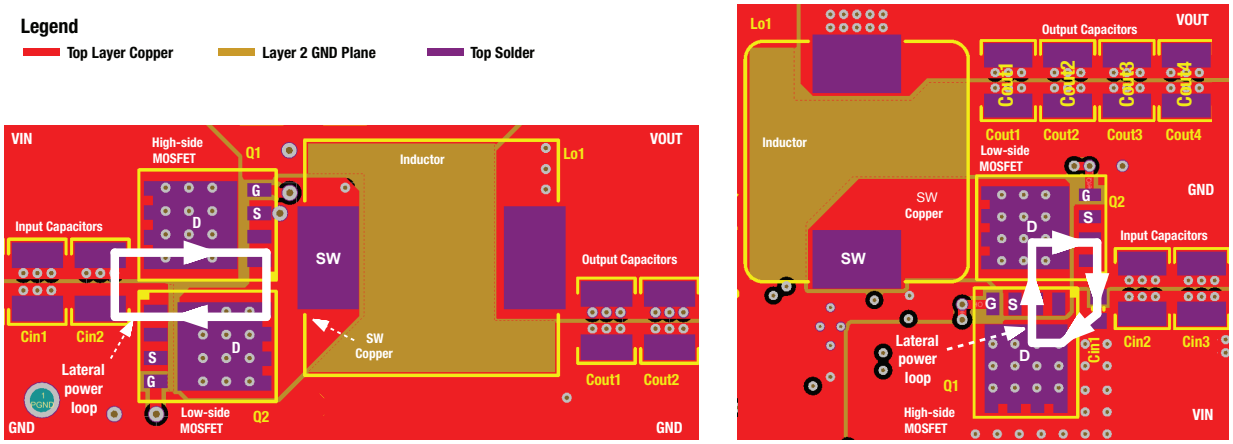


Figure 5. Two conventional lateral-loop layout designs.

Improved PCB layout design

Figure 6 shows an improved layout with the benefit of a reduced power-loop area and high efficiency for a multilayer structure. The design uses layer 2 of the PCB as a power-loop return path [49], [50], [51]. This return path is located directly underneath the top layer, creating a small physical loop size. The currents flowing in opposing directions in the vertical loop provide field self-cancellation, further reducing parasitic inductance. The side view depicted in Figure 6 illustrates the concept of creating a low-profile self-canceling loop in a multilayer PCB structure.

Four 0603 input capacitors with small 0402 or 0603 case sizes and low ESL (located between bulk input decoupling capacitors C_{IN5} and CI_{N6} in Figure 6) are placed as close as possible to the high-side MOSFET. The return connections of these capacitors connect to the layer-2 ground plane with multiple 12-mil vias.

The layer-2 ground plane provides a current return path directly underneath the MOSFETs to the source terminal of the low-side MOSFET.

In addition, the switch-node copper polygon includes just the pad of the inductor and the minimum area required to connect to the MOSFETs. Ground plane copper shields the polygon pour connecting the MOSFETs to the inductor terminal. The single-layer layout for SW and BST implies that vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test. Finally, using two ceramic output caps, C_{OUT1} and C_{OUT2}, on each side of the inductor optimizes the output current loops. Having two parallel return paths from the output splits the return current in two, helping mitigate the “ground bounce” effect.

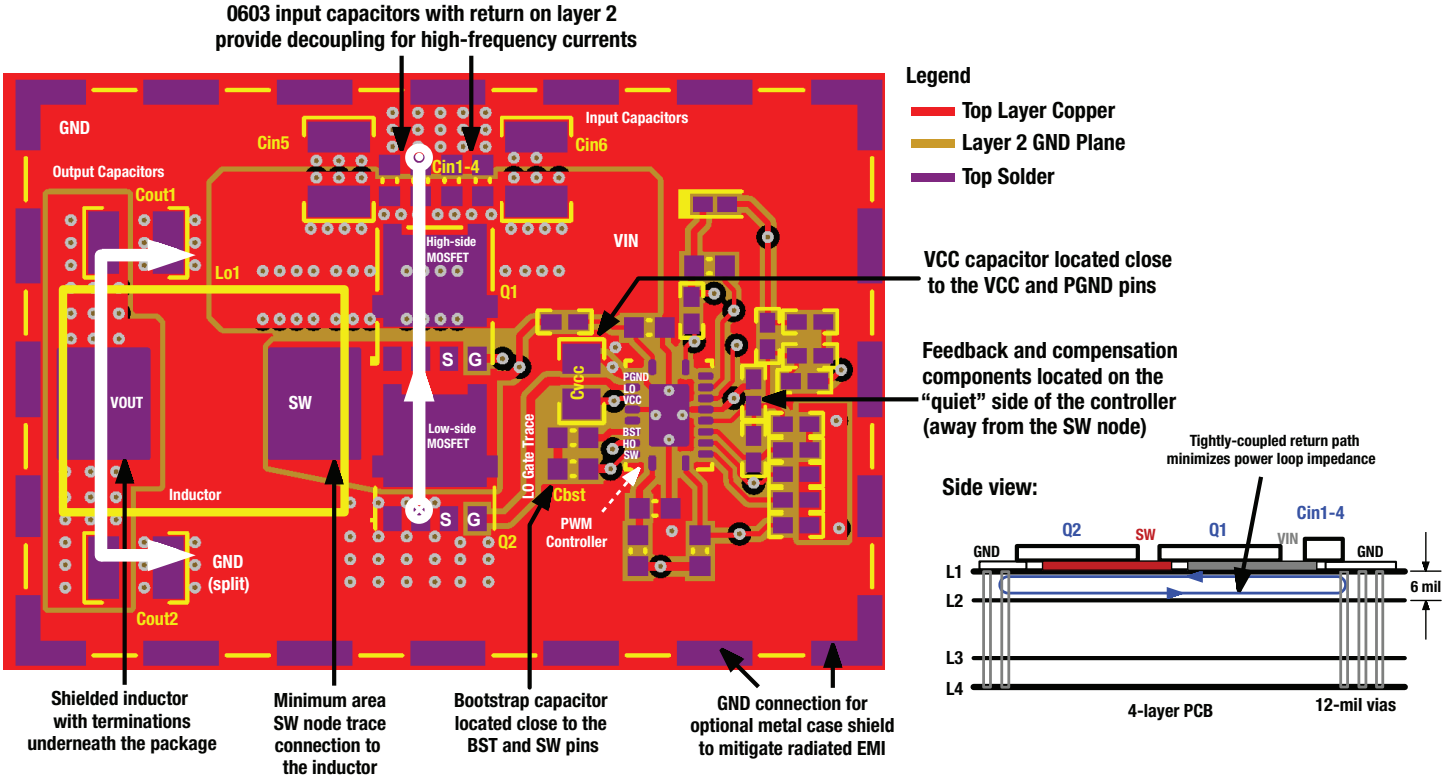


Figure 6. *Layout of power stage and controller with a vertical power-loop design.*

Figure 7a shows the switch-node voltage waveform measured with a wide-bandwidth probe for the regulator in Figure 4 using the optimized layout of Figure 6. Ringing is not evident; just a low-amplitude overshoot and negligible undershoot, which bodes well for EMI performance above 50 MHz. For comparison, **Figure 7b** shows a similar measurement using the lateral loop layout of Figure 5b. The peak overshoot of the optimized layout is lower by approximately 4 V.

Figure 8 shows the conducted emissions measured from 150 kHz to 108 MHz for the converter in Figure 6. Using a Rohde & Schwarz spectrum analyzer, peak and average detector scans are denoted in yellow and blue, respectively. The results are in compliance with Comité International Spécial des Perturbations Radioélectriques (CISPR) 25 Class 5 requirements. The limit lines in red are the Class 5 peak and average limits (peak limits are generally 20 dB higher than the average limits).

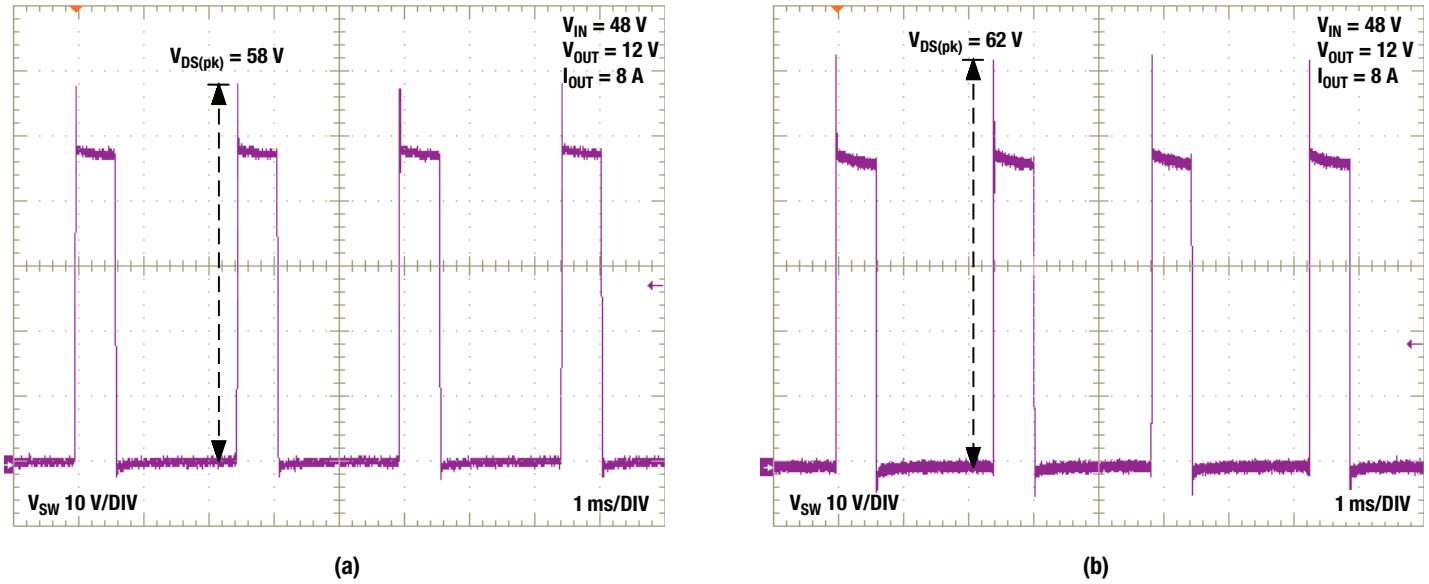


Figure 7. *Switch-node voltage waveforms at V_{IN} = 48 V and I_{OUT} = 8 A: optimized layout (a); lateral loop layout (b).*

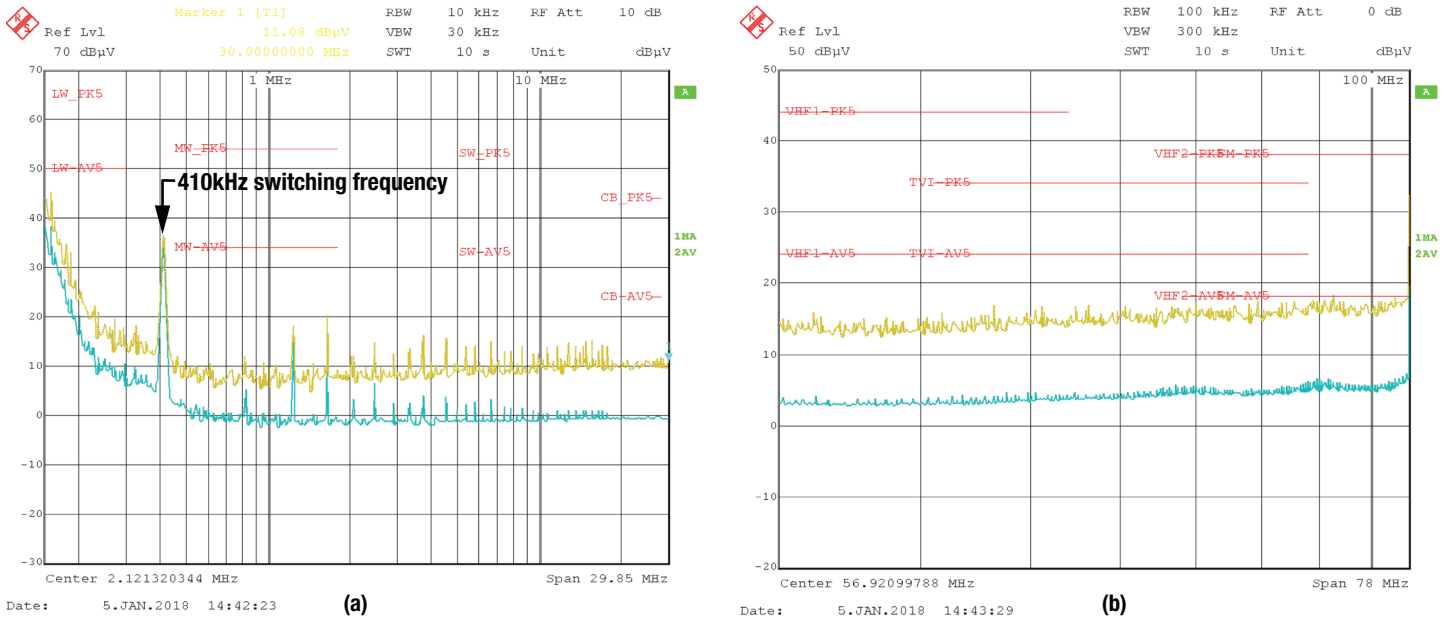


Figure 8. *CISPR 25 conducted emission results: 150 kHz to 30 MHz (a); 30 MHz to 108 MHz (b).*

7. Common-mode noise of a flyback

It's important to understand the impact of transformer interwinding capacitance on common-mode (CM) emissions. CM noise is mainly caused by displacement currents within the transformer interwinding parasitic capacitance and the parasitic capacitance between the power switch and the chassis/earth GND.

From an electromagnetic interference (EMI) perspective, a conventional hard-switched isolated converter is considerably more challenging than its nonisolated counterpart. The performance requirements of high-frequency transformers for isolated DC/DC regulators have recently become more stringent, particularly in terms of EMI. The dynamic interwinding capacitance of the transformer represents a critical coupling path for CM noise.

This chapter:

- Specifically analyzes CM noise for a DC/DC flyback converter, since it is so widely used as an isolated power supply.
- Illustrates a simple, two-capacitor CM noise model of a flyback transformer to model and characterize CM EMI performance.

Flyback topology

Spanning industrial and automotive market segments, DC/DC flyback circuits [52], [53] are a good fit for low-cost isolated bias rails, especially given their easy configuration for single or multiple outputs. Applications requiring isolation include high-voltage metal-oxide semiconductor field-effect transistor (MOSFET) gate drivers for single- and three-phase motor drives, as well as loop-powered sensors and programmable logic controllers used in factory automation and process control.

A flyback implementation, as shown in the schematic of **Figure 1**, offers a robust solution with a simple structure and low component count. If a primary-side regulation technique is available, an optocoupler and its associated circuits are not required for feedback regulation [52], further reducing component count and simplifying transformer design. A transformer with functional-grade isolation provides a straightforward circuit ground separation, while reinforced isolation is useful for high-voltage safety-critical applications.

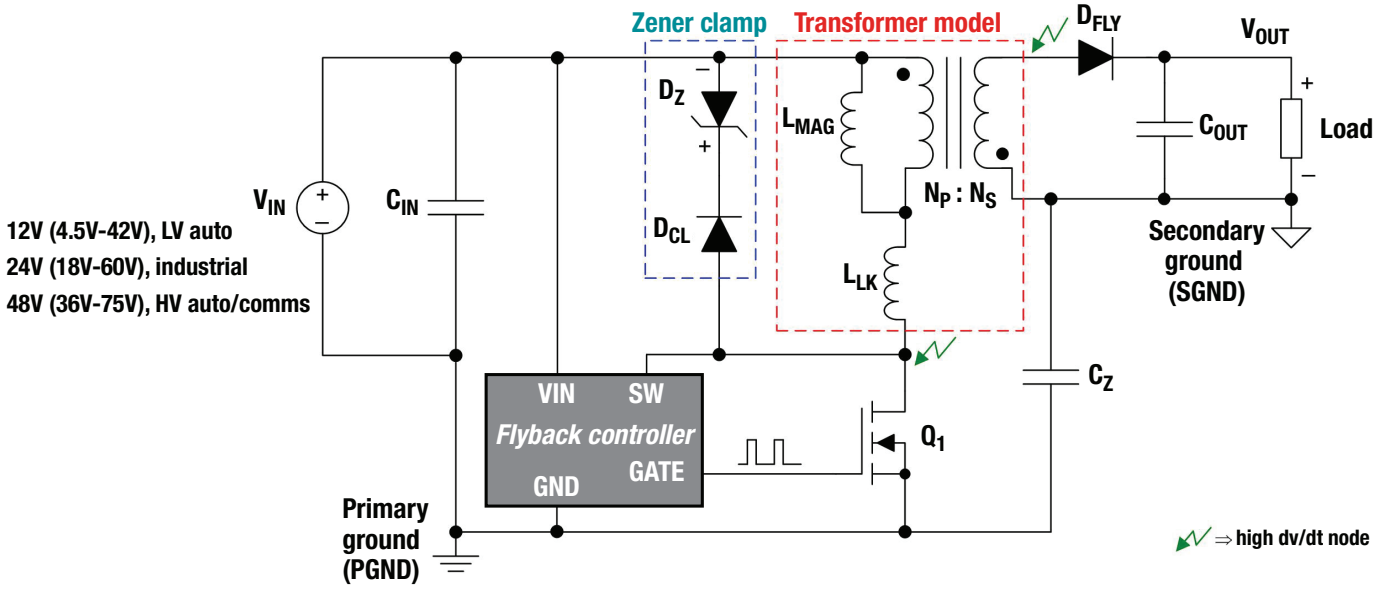


Figure 1. *A DC/DC flyback regulator with a classic 24-V supply or 12-V/48-V input for industrial or automotive battery applications, respectively. The flyback transformer magnetizing and leakage inductances and the circuit parasitic capacitances are denoted explicitly.*

Flyback switching waveform behavior

Figure 2 shows the primary MOSFET and secondary rectifying diode voltage waveforms for a flyback power stage (such as the power stage shown in Figure 1) operating in discontinuous (DCM) and boundary (BCM) conduction modes [52]. Figure 2a highlights the switching waveforms in DCM where the primary MOSFET turns on near the valley of the switch-node resonant voltage swing. Figure 2b shows the waveforms for BCM switching, with quasi-resonant MOSFET turn-on after an approximate one-quarter resonant period delay from when the secondary winding current decays to zero. The primary MOSFET turns on at zero current in both DCM and BCM.

Along with the sharp voltage and current edges during switching, the voltage spike overshoot and subsequent ringing behavior are particularly troublesome as a source of EMI. Each commutation excites damped voltage and current oscillations between switch and diode parasitic capacitances and transformer leakage inductance.

Figure 2 shows the switch-node voltage leading-edge spike and high-frequency ringing at MOSFET turn-off. The ringing behavior depends on the primary-side leakage inductance (L_{LK-P}) resonating with the MOSFET output capacitance (C_{OSS}) plus the transformer's primary intrawinding capacitance (C_P). Similarly, the diode voltage ringing relates to the secondary-side leakage inductance (L_{LK-SEC}) resonating with the diode junction capacitance (C_D) and secondary intrawinding capacitance (C_S). The overshoot and ringing have high transient voltages (dv/dt), so any capacitive couplings to earth GND lead to induced displacement currents and CM noise.

When operating in continuous conduction mode, reverse recovery of the flyback diode when the primary switch turns on presents additional negative effects. Reverse recovery of DFLY exacerbates the ringing voltage and creates a leading-edge current spike that flows in the primary MOSFET as the recovery current gets reflected to the primary side.

Note that the flyback magnetic component behaves mostly as a coupled inductor, as currents typically do not flow in primary and secondary windings at the same time. The switching transitions are the only intervals where true transformer action exists [54], with currents flowing simultaneously in the primary and secondary windings (currents ramping in the leakage inductances).

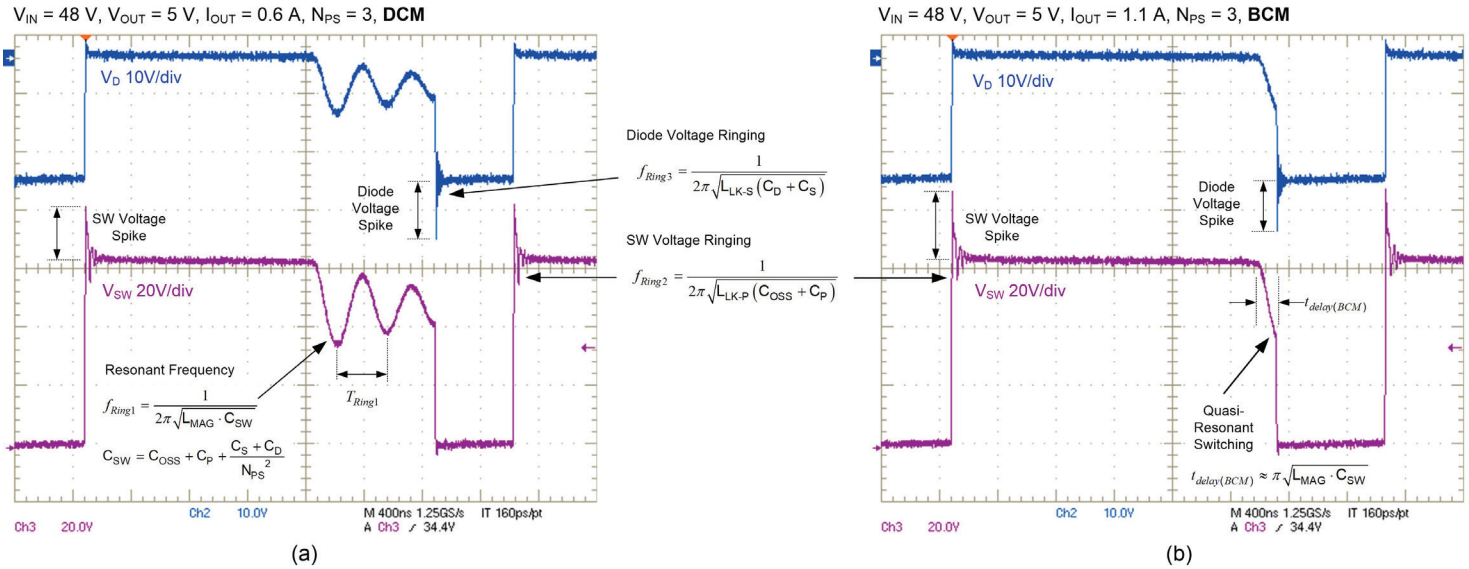


Figure 2. *Primary MOSFET and secondary diode voltage waveforms of a flyback converter: operating in DCM (a); and BCM (b). A Zener diode circuit across the primary winding clamps the voltage spike caused by the leakage inductance resonating with MOSFET and transformer parasitic capacitances.*

CM EMI in an isolated DC/DC flyback regulator

Figure 3 shows a flyback schematic with a line impedance stabilization network (LISN) connected for EMI measurement. Red dashed lines indicate the dominant CM noise current-propagation paths through the parasitic capacitances to earth GND and back to the LISN. A capacitor designated C_Z connected from primary ground (PGND) to secondary ground shunts CM currents on the secondary side back to the primary, advantageously diverting CM current away from C_{SE} that returns via the LISN.

While the high slew-rate voltage of the primary MOSFET drain terminal is the main source of CM noise, the transformer and its parasitic capacitances are the coupling channels through which conducted EMI can propagate from primary to secondary and through the impedance from output circuit to earth GND. The dominant CM current path (denoted by I_{CM-SEC} in Figure 3) is from primary to secondary across the transformer and through the impedance from the output circuit to earth GND. Similar to the techniques for a nonisolated converter, using a small switch-node copper area, connecting the MOSFET heat sink (if needed) to PGND and avoiding switch-node full vias to the bottom side of the board can diminish the coupling from the MOSFET drain to earth GND (denoted by I_{CM-PRI} in Figure 3).

Three main considerations related to the transformer apply here. First, tightly coupling the transformer windings minimizes the leakage inductance in order to achieve high efficiency, reduced switch voltage stress and high reliability. Interleaving is a common technique to reduce the leakage inductance and winding AC resistance; consequently, the interwinding capacitance becomes relatively large.

Furthermore, planar transformers with printed circuit board embedded windings have even higher interwinding capacitance than conventional wire-wound designs given their closely stacked layers and intrinsically large layer surface areas. In any case, applying a pulsating noise voltage source to such distributed parasitic capacitances generates a relatively high displacement current. It flows from primary to secondary windings and returns to earth GND, resulting in large CM noise [55].

Secondly, leakage inductance resonating with parasitic interwinding capacitance may result in severe high-frequency CM noise peaks in the measured EMI spectrum.

Thirdly, the stray near-electric field generated by the high dv/dt nodes may easily couple through the transformer magnetic core, as the core material has a high electric permittivity and presents low impedance to electric fields. However, parasitic capacitance (C_{ME}) from magnetic core to earth is small if the core is wrapped in a copper foil connected to PGND.

In general, optimizing flyback transformer design is not only critical in terms of solution size, profile, efficiency and thermal performance, but also has an outsized impact on CM noise performance.

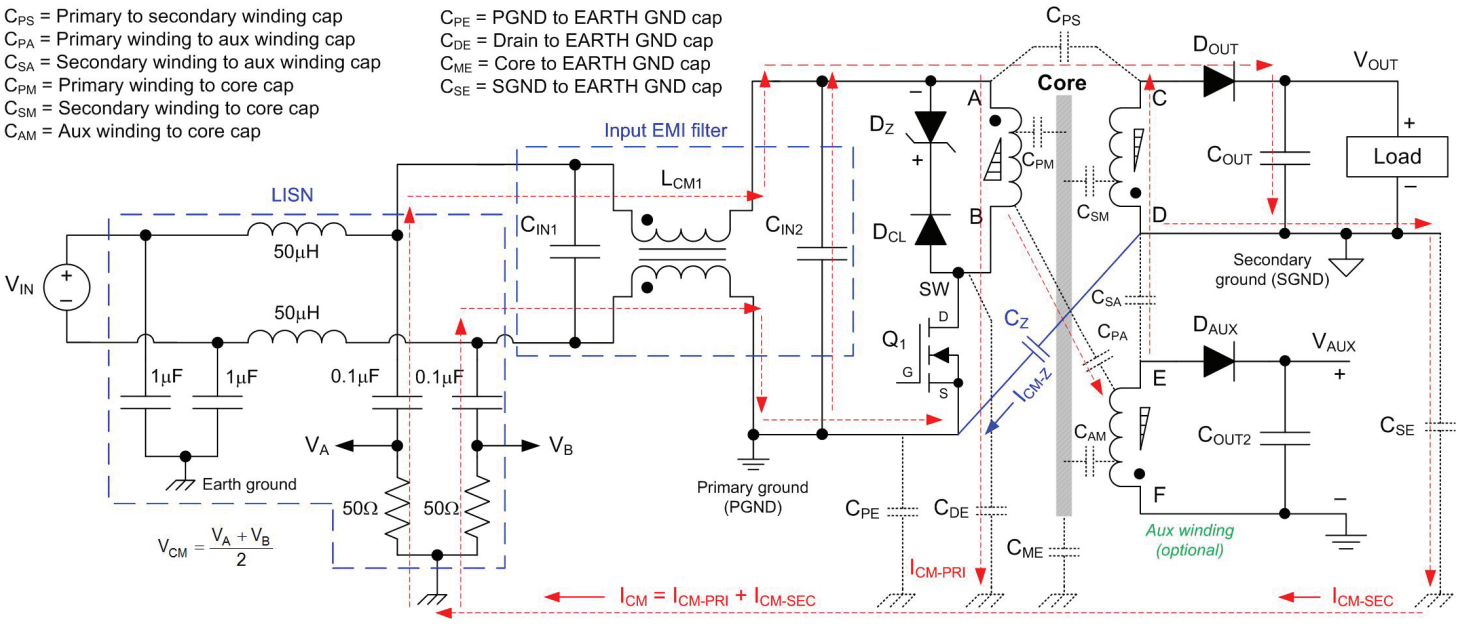


Figure 3. *CM noise current-propagation paths of a two-wire DC/DC flyback regulator with a LISN connected at the input. Also shown is a primary-referenced auxiliary output.*

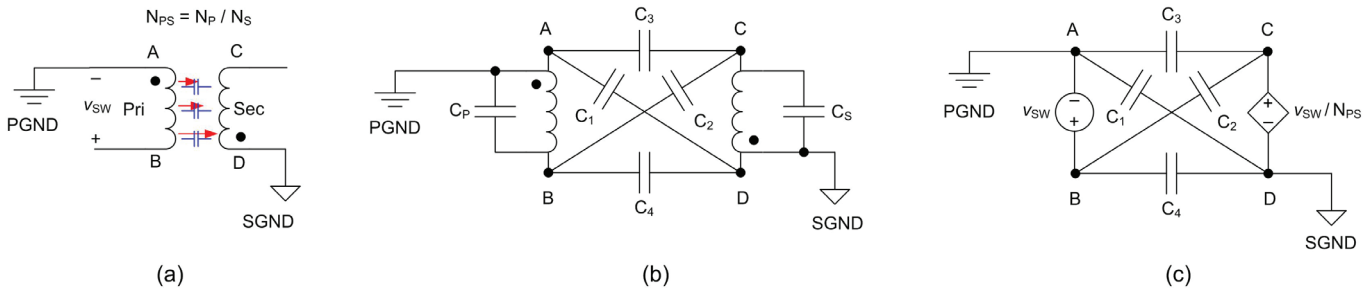


Figure 4. *Two-winding transformer for CM noise analysis (a); six-capacitor CM model (b); four-capacitor CM model (c).*

CM noise analytical model

Figure 4a shows a two-winding transformer with primary and secondary terminals designated (A, B) and (C, D), respectively. Terminal A equivalently connects to PGND based on the input bus capacitor appearing as an effective short at the applicable frequencies for CM noise analysis. **Figure 4b** illustrates the conventional electrostatic model of the transformer. From an energy conservation standpoint, it is possible to model the parasitic capacitance of a two-winding transformer with six capacitances, including four interwinding capacitances (C_1, C_2, C_3, C_4) and two intrawinding capacitances (C_P, C_S).

Other than affecting the dv/dt of the pulsating switch-voltage waveform, the intrawinding capacitances do not impact the displacement currents from the primary to secondary. The six-capacitor model unnecessarily increases the complexity and makes it difficult to calculate the transformer equivalent capacitances.

When substituting nonlinear switching devices with equivalent noise voltage sources (based on the substitution theory for CM noise analysis [56]), however, an independent or dependent noise voltage source in parallel with the transformer windings makes it possible to remove the two intrawinding capacitors. The winding capacitance model reduces to four lumped capacitors as shown in **Figure 4c**, where v_{SW} and v_{SW}/N_{PS} are the switching voltage sources on the primary and secondary windings, respectively. Assuming a low leakage inductance, the winding voltages scale by the transformer turns ratio, N_{PS}, as expected.

Finally, when one of the transformer windings equivalently connects to an independent voltage source (to substitute for a nonlinear switch), two lumped capacitors are then sufficient to characterize the interwinding parasitic capacitances of a two-winding transformer. The derivation of the two-capacitor model is consistent with displacement current conservation [56], [57]. As shown in **Figure 5a**, there are a total of six possible two-capacitor winding capacitance models. **Figure 5b** shows one possible implementation of a two-capacitor CM model (using capacitors C_{AD} and C_{BD}) and its corresponding Thevenin-equivalent circuit.

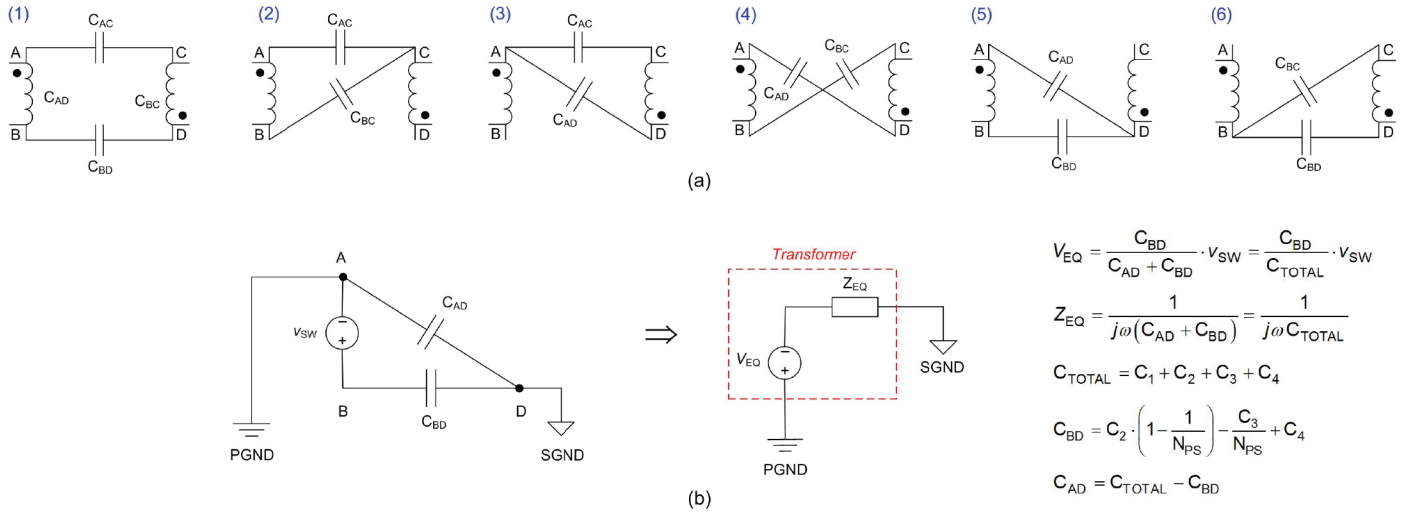


Figure 5. *Six possible two-capacitor CM models (a); two-capacitor CM model with its Thevenin-equivalent circuit (b).*

The two-capacitor CM noise model is flexible to different isolated regulator topologies and facilitates extraction of the transformer lumped capacitance model with experimental measurements [57]. C_{TOTAL} is the structural interwinding capacitance of the transformer measured with an impedance analyzer by shorting the primary and secondary terminals and then treating the transformer as a one-port network. **Equation 1** derives C_{BD} by applying a switching frequency sinusoidal excitation signal with 50-Ω source impedance to primary winding terminals (A, B) and measuring the ratio of voltages V_{AD} and V_{AB}:

$$C_{BD} = (V_{AD}/V_{AB}) \cdot C_{TOTAL} \quad (1)$$

Clearly, the advantage of the model is that simple experimental measurement – without knowledge of the transformer structure or the electric potential distributions along the windings – easily extracts the parasitic capacitances [57].

Flyback regulator CM noise model

Figure 6 shows the CM model for a flyback transformer with primary, secondary, auxiliary and shield windings (similar to Figure 3 but with an included primary-grounded shield winding). N_A and N_{SH} are the primary-to-auxiliary winding and primary-to-shield winding turns ratios, respectively. Figure 6 does not include the couplings from primary to auxiliary and primary to shield windings because the currents flow solely on the primary side and not back to the LISN, and thus do not contribute to measured CM noise. As a result, three 4-capacitor circuits are sufficient to model the primary-to-secondary, auxiliary-to-secondary and shield-to-secondary couplings. Based on the input capacitor acting as low impedance for CM noise, terminal A of the primary winding shorts to PGND.

From the previous discussion, only two independent capacitances and a voltage source are required to describe the CM behavior, the expressions for which are included in Figure 6.

As before, C_{TOTAL} is the measured capacitance between the shorted primary-referenced windings and shorted secondary winding.

To develop a CM noise model for the flyback regulator in Figure 3, the block in **Figure 7** represents the transformer (including primary, secondary, and auxiliary and shield windings) that can be subsequently exchanged for the appropriate two-capacitor CM transformer model. Based on the substitution theorem, all voltages and currents in a circuit will not change when replacing the nonlinear switching devices in the circuit with voltage or current sources that have the exact same time-domain voltage or current waveforms as the original components. Thus, a voltage source (V_{SW}), which has

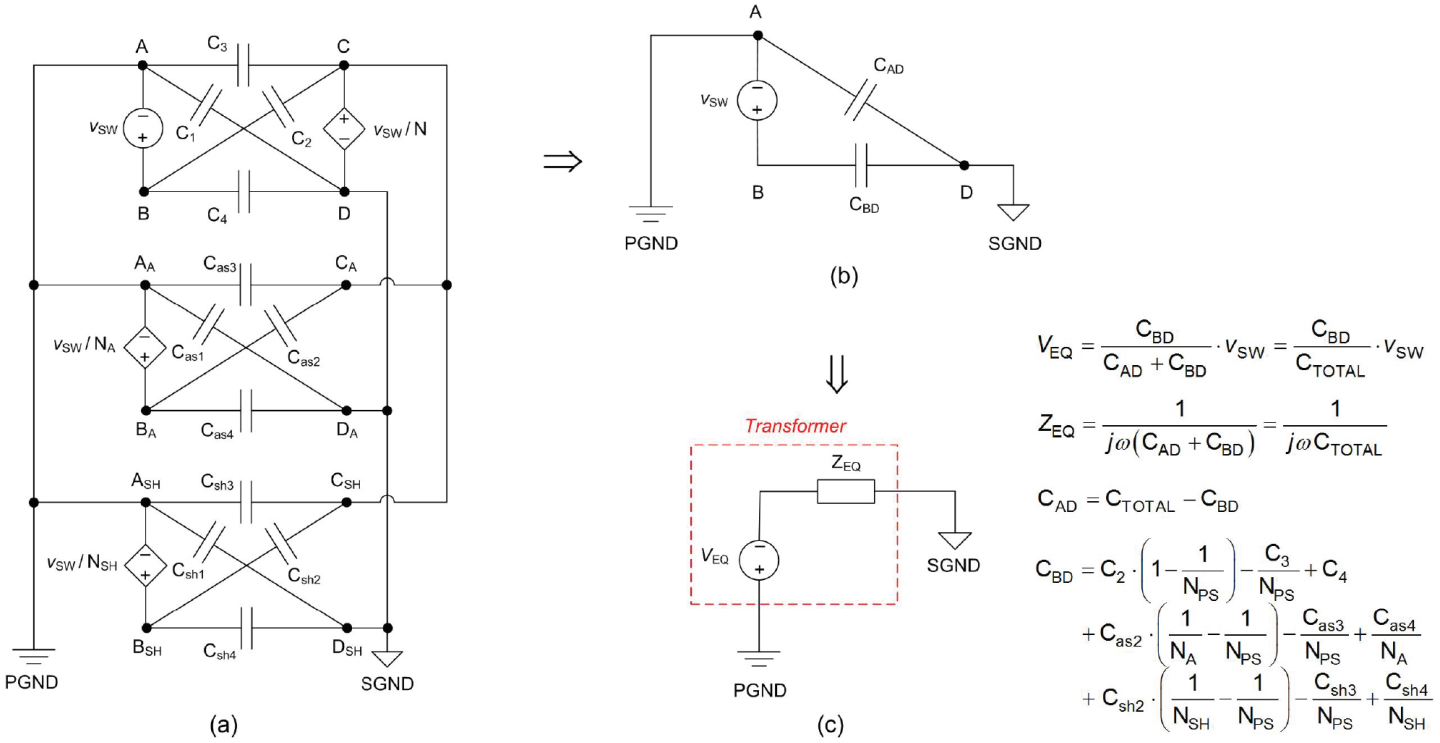


Figure 6. *Lumped CM parasitic capacitance model for a multiwinding flyback transformer (a); two-capacitor CM model (b); Thevenin-equivalent circuit (c).*

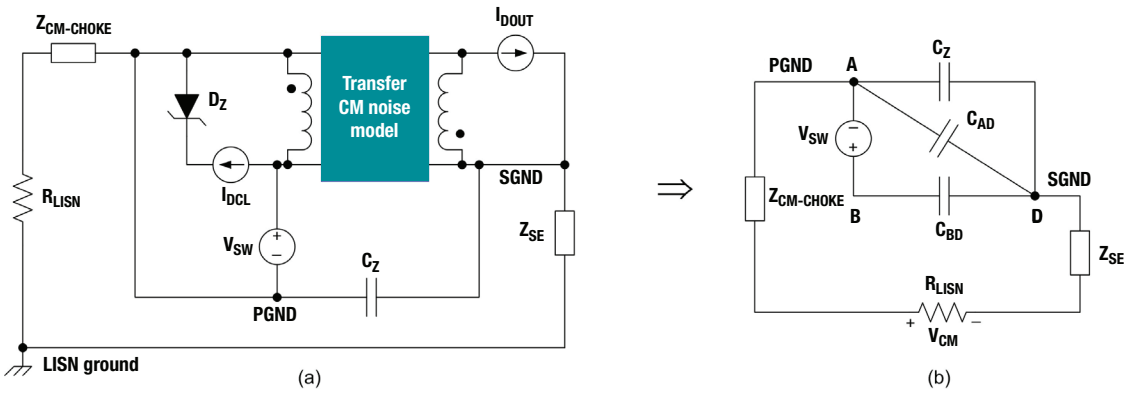


Figure 7. *Flyback circuit model based on the substitution theorem (a); final CM model of the flyback regulator after applying the superposition theorem (b).*

the same voltage waveform as the drain-to-source voltage of the MOSFET, replaces the MOSFET. Similarly, current sources (I_{DOUT} and I_{DCL}), which have the same current waveforms as the diode currents, replace the two diodes. The voltages and currents in the circuit after substitution remain unchanged.

Meanwhile, the input and output capacitors have very small impedances to CM noise, so their impedances are neglected. The CM choke series impedance is designated $Z_{CM-CHOKE}$, and a 25-Ω measuring resistor characterizes the LISN. Finally, the parasitic capacitances that do not significantly contribute to CM noise flowing through the LISN are removed. Figure 7a represents the CM noise model of the flyback regulator after applying the substitution theorem [58].

Components in parallel with voltage sources or in series with current sources are removable, since they do not contribute to the voltages or currents of the network. Superposition theory facilitates analysis of the effects of I_{DCL}, I_{DOUT} and V_{SW} separately. Clearly, I_{DCL} and I_{DOUT} do not generate CM noise, as they are shorted. Figure 7b shows the final CM model, and **Equation 2** provides the CM noise voltage measured at the LISN:

$$V_{LISN} = \frac{R_{LISN}}{j\omega\left(C_{TOTAL}+C_Z\right)+R_{LISN}+Z_{CM-CHOKE}+Z_{SE}} \cdot \frac{C_{BD}}{C_{TOTAL}+C_Z} \cdot V_{SW} \quad (2)$$

Applying circuit simulation that incorporates the measured V_{SW} waveform enables the analysis of CM noise and the impact of various components. The model is accurate, assuming that the impedance of the leakage inductance is much lower than that of the total parasitic winding capacitance, C_{TOTAL}. Clearly, decreasing C_{BD} as well as increasing $Z_{CM-CHOKE}$ or C_Z results in lower noise voltage. Note that if the measured V_{AD} based on Equation 1 is zero, C_{BD} is effectively zero, essentially eliminating the CM noise through the transformer. This is a convenient test to check if a transformer is well-balanced.

The general derivation of the CM noise model based on the two-capacitor transformer model follows six steps:

1. Substitute nonlinear semiconductor devices with either equivalent voltage sources or current sources using the substitution theorem. The rule of substitution is to acquire a CM noise circuit that is easy to analyze, while avoiding voltage loops and current nodes. The voltage and current sources shall have equivalent time-domain waveforms as the originals. Treat the input and output capacitors as short circuits because they have very small impedance to CM noise.
2. If paralleling one transformer winding with a voltage source, replace all other windings with controlled voltage sources because the winding voltages depend on the transformer turn ratios.
3. Simplify the model by removing all components in parallel with voltage sources or in series with current sources.
4. Use one of the two-capacitor models in Figure 5a that most simplifies the CM noise analysis to replace the original transformer.
5. Analyze the CM noise generated by all voltage sources and current sources based on the superposition theorem.
6. Remove the parasitic capacitances that do not contribute to CM noise flowing through the LISN by analyzing the circuit developed using steps 1 through 5. Inspect the CM noise currents based on the resultant CM noise model.

8. Common-mode noise mitigation in isolated designs

Common-mode (CM) noise is one of the major concerns in the design of high-frequency isolated DC/DC converters. Converters operating at a high input voltage – such as the phase-shifted full bridge [59] and the inductor-inductor-capacitor (LLC) series resonant converter [60] – can generate large CM currents in applications such as electric vehicle onboard charging, data-center power systems and radio-frequency power amplifier supplies. The effect is more pronounced when applying gallium-nitride switching devices, as they switch at higher transient voltages (dv/dt) than their silicon counterparts.

As the switching frequency increases to improve power density, a high dv/dt at the primary switching node and associated CM interference through the transformer interwinding capacitance become detrimental to the system. Techniques for mitigating CM noise in isolated designs include using symmetrical topology designs, shielding and balance capacitors.

The winding design method reduces noise by properly arranging the transformer layers and choosing optimal connections between the winding layer terminals and the circuit nodes, while an auxiliary cancellation winding wound on the outside of the transformer achieves CM noise balance. Used individually for some topologies or in combination, these methods achieve better noise reduction for meeting specification requirements and solving complex CM noise issues.

This chapter:

- Reviews a wide variety of techniques, focusing mostly on flyback circuits, that help mitigate CM noise for isolated DC/DC regulator circuits, including:
  - Symmetrical circuit arrangements.
  - Connecting a capacitor between primary and secondary GND.
  - Shielding.
  - Adding balance capacitors.
  - Optimizing transformer winding design.
  - Using an adjustable CM cancellation auxiliary winding.

Symmetrical circuit designs

In a symmetrical topology, switching nodes that have complementary electric potentials with respect to ground are presented in pairs. If the associated parasitic capacitances are the same, the generated CM displacement currents will approximately cancel each other out.

Figure 1a shows the schematic of a two-switch forward converter such as the LM5015, a monolithic two-switch forward DC/DC converter from Texas Instruments [61], [62]. **Figure 1b** presents a flyback converter configured with split primary and secondary windings. Both converters have symmetrical primary-side circuits with out-of-phase voltage switching waveforms, designated SW1 and SW2, that create opposite polarity CM currents and thus lower total CM noise.

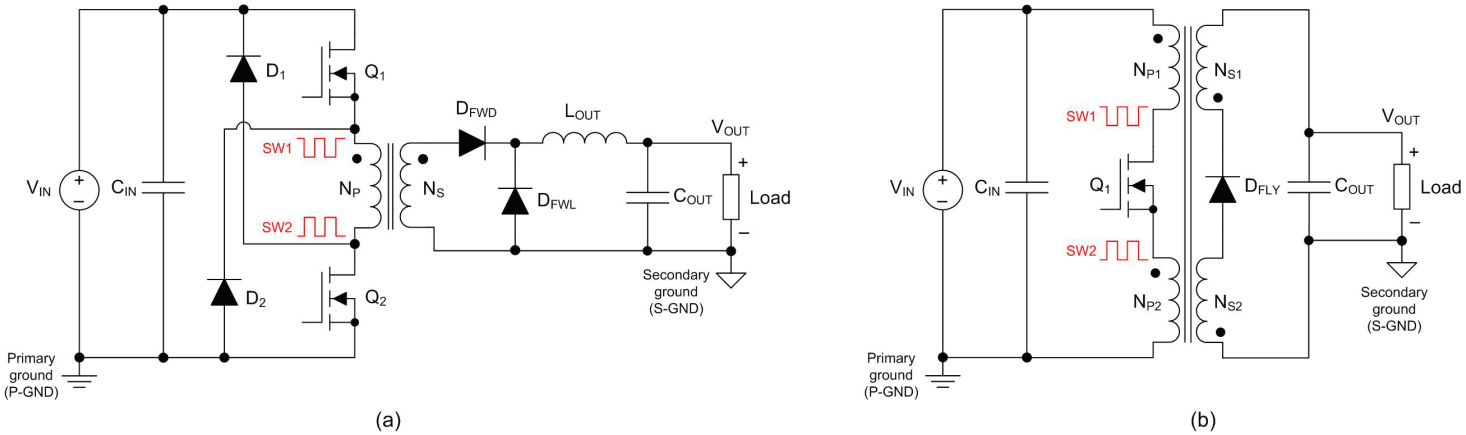


Figure 1. *Balanced-winding topologies with symmetrical primary-side circuits and equal-magnitude, out-of-phase dv/dt switching waveforms for a lower CM noise signature: two-switch forward converter (a); flyback converter with split primary and secondary windings (b).*

The two-switch forward converter in Figure 1a is a well-known topology, but perhaps its favorable CM noise signature is under-appreciated. The balanced-winding flyback converter in Figure 1b also has symmetrical secondary windings. A split winding is usually available if the windings are wound interleaved (to achieve lower leakage inductance). The main drawback of this circuit is that it requires a floating gate driver referenced to SW2.

Similar balanced-winding symmetrical implementations are possible for single-switch forward and LLC resonant converter topologies, as depicted in **Figure 2**. The modified symmetrical circuits require additional components, such as a floating gate driver in the forward converter and an additional switch in the LLC resonant circuit [63], and are only effective for CM attenuation if the transformer physical winding structure yields symmetrical parasitic capacitances. As a result, other techniques are generally necessary to mitigate CM noise and use conventional isolated topology circuits.

Connecting a capacitor between primary and secondary GND

Y-capacitors connected from both line and neutral to chassis GND are commonly used in electromagnetic interference (EMI) input filters to attenuate CM noise in three-wire AC/DC applications. In a two-wire DC/DC system, however, there is no chassis ground connection point; therefore, Y-capacitors cannot connect this way. In such systems, connecting a substitute capacitor between primary GND (PGND) and secondary GND (SGND) can shunt the CM currents that propagate to the secondary back to their primary-side source.

See the capacitor designated C_Z in Figure 1 of Chapter 7. This component is a safety-rated capacitor selected with a voltage rating of 1 kV or higher, well above the required isolation voltage specification. However, galvanic isolation becomes compromised if this capacitor shorts during a fault condition.

Also, the capacitor can conduct excessive current if the SGND connection has a high CM voltage swing relative to the primary, such as in high-side gate driver bias-supply applications. And if the DC/DC stage follows an AC/DC front-end rectifier, the capacitor can conduct line-frequency leakage currents that may be unacceptable in the application or limited by regulation [64-67].

CM balance and cancellation techniques

Balance techniques can reduce CM noise related to transformer winding capacitances based on internal and external transformer balancing. Internal balancing techniques include applying shielding layers [67-69], optimizing the winding design or using cancellation windings. The most common external balance technique is to add a balance capacitor between selected primary and secondary winding terminals [63].

Shielding

Shielding techniques aim to block the near-field electric coupling between a transformer's primary and secondary windings by inserting wire or foil shielding layers, thus reducing the displacement current flowing through the interwinding capacitances.

As an example, **Figure 3a** shows a flyback converter with a traditional one-turn foil shield winding placed between the primary and secondary layers. **Figure 3b** depicts an

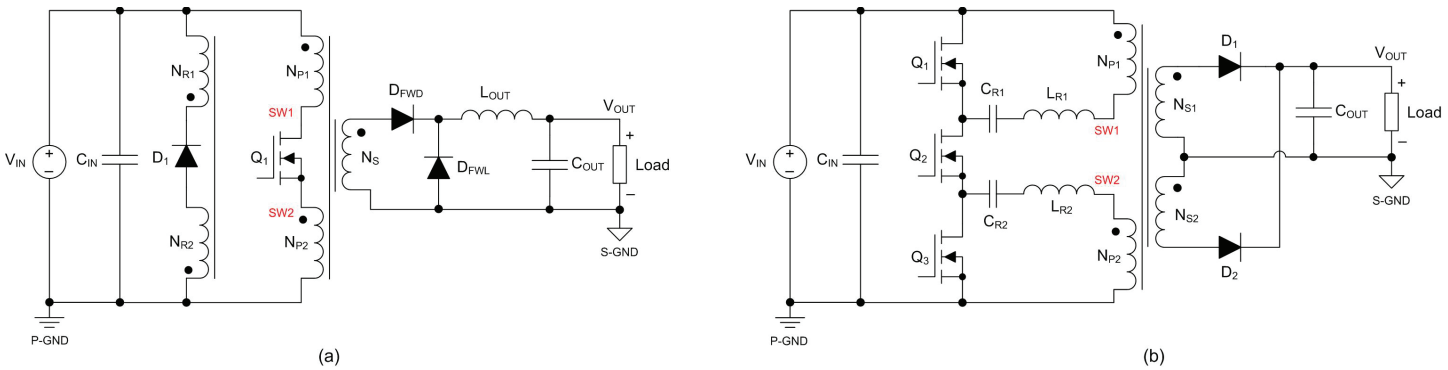


Figure 2. *Symmetrical primary winding design applied to a single-switch forward converter (a); and LLC resonant converter (b).*

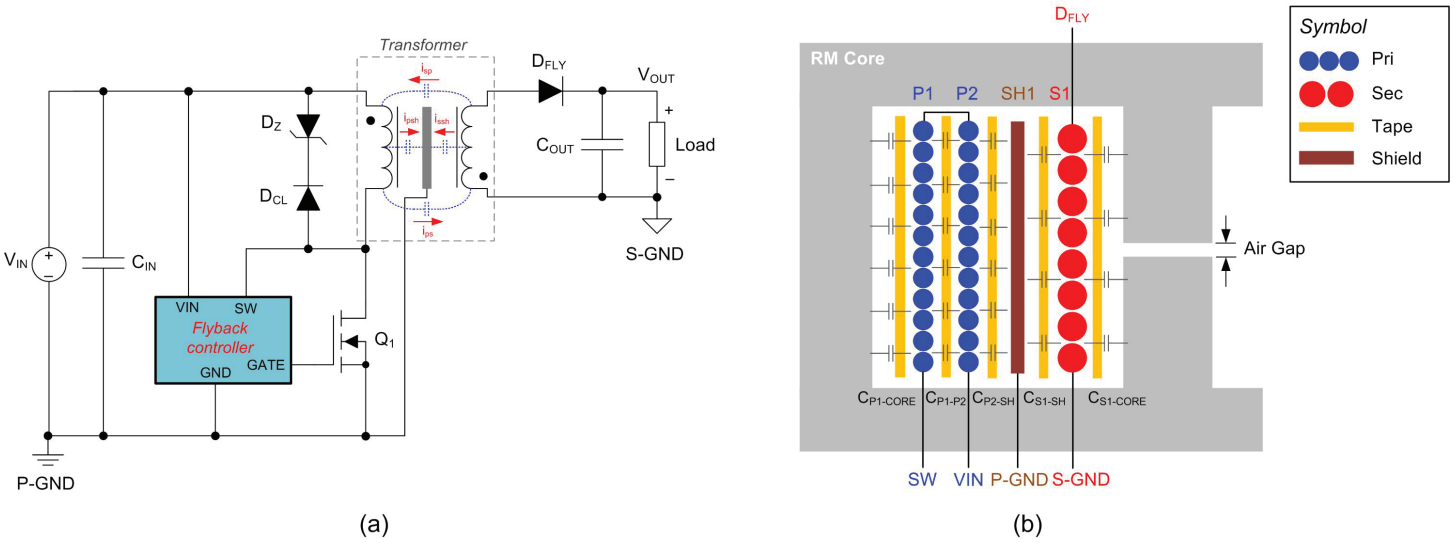


Figure 3. *Flyback converter with conventional electrostatic-foil shield winding placed between the primary and secondary layers and connected to PGND (a); a winding layer structure of one transformer winding window (b).*

rectangular modulus-style core shape with gapped center leg and vertically oriented windings. The winding half window illustrates two series-connected primary layers (2 x 12T), one secondary layer (1 x 8T) and a single shield layer. The noninterleaved winding arrangement is configured as layers designated P1, P2, SH1 and S1. Figure 3 also depicts the intralayer parasitic winding capacitances.

A single shielding layer, SH1, is inserted between primary layer P2 and secondary layer S1. The shield normally connects back to a static electric potential in the primary circuit – the local PGND as shown in Figure 3, for example, or to the input capacitor's positive terminal, also a quiet AC node. The insertion of this shielding layer blocks the electric coupling between P2 and S1 and eliminates the displacement current between P2 and S1.

With the shield in place, i_{psh} will flow into the shield and back to PGND instead of flowing to the output and from there back to chassis GND. However, capacitance still exists between the shield and the adjacent secondary winding. Since the voltage induced in the one-turn shield is not the same as in the secondary winding (the exception being a one-turn secondary), some CM current inevitably flows between the shield and the secondary winding. Driving the shield instead by a tap on an auxiliary winding, such that the average voltage on the shield matches the average voltage on the secondary, can achieve CM balance [69].

There is coupling between the P1 and S1 layers in Figure 3 through the high-permittivity core material. Therefore, while a single shield layer helps attenuate CM noise, it may not eliminate the noise entirely. Another disadvantage is that more shield layers are required as the number of primary-secondary boundaries increases. Importantly, a shield layer increases the space between windings and therefore leads to increased leakage inductance.

In general, a copper foil shield should be as thin as possible in order to reduce eddy current loss caused by the proximity effect. The losses in the shield can become excessive at high switching frequencies, and the shield also increases the total parasitic capacitance reflected to the switch node.

Balancing capacitor value and position

Figure 4a is a schematic of a flyback converter with primary, secondary and auxiliary transformer windings. N_{PS} and N_{AUX} are the primary-to-secondary and the primary-to-auxiliary winding turns ratios, respectively. Again, there is no need to consider the couplings from primary to auxiliary because the currents flow solely on the primary side and thus do not contribute to measured CM noise. Based on the discussion in Chapter 7, two four-capacitor circuits are sufficient to model the primary-to-secondary and auxiliary-to-secondary couplings, as shown in **Figure 4b**.

If the input capacitor acts as low impedance for CM noise, terminal A of the primary winding shorts to PGND. Then, using the simplified two-capacitor model of the transformer, with Z_{SE} modeling the capacitive coupling from SGND to earth, **Figure 4c** gives the final equivalent circuit model for CM noise (see Chapter 7 for additional context and descriptions).

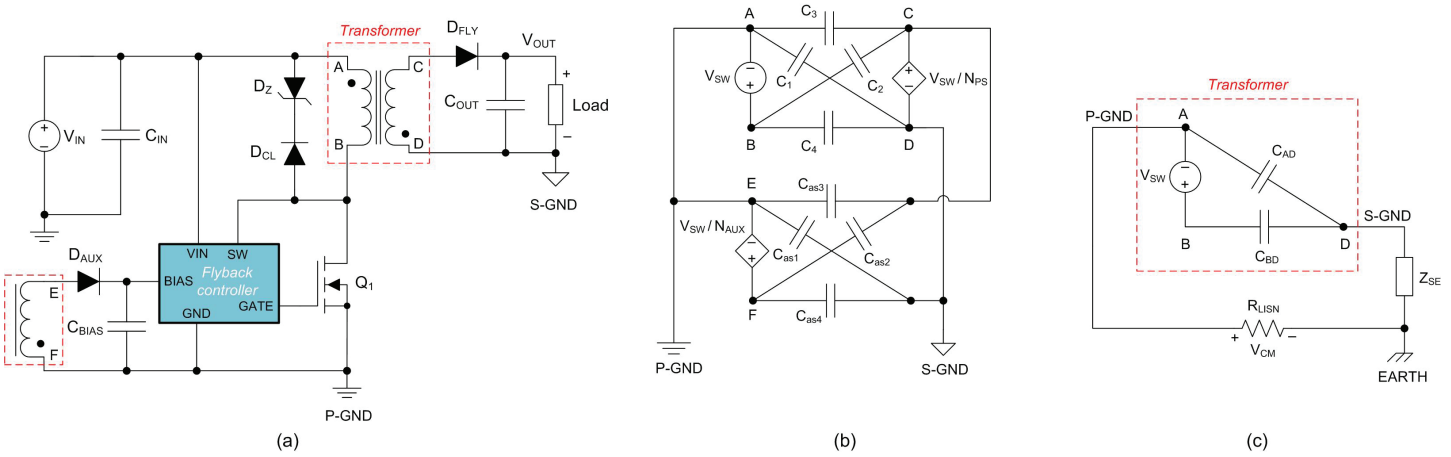


Figure 4. *Flyback converter with auxiliary winding (a); lumped CM parasitic capacitance model for a three-winding flyback transformer (b); CM noise equivalent circuit using a two-capacitor transformer model (c).*

If the input capacitor acts as low impedance for CM noise, terminal A of the primary winding shorts to PGND. Then, using the simplified two-capacitor model of the transformer, with Z_{SE} modeling the capacitive coupling from SGND to earth, Figure 4c gives the final equivalent circuit model for CM noise (see **Chapter 7** for additional context and descriptions).

Equation 1 provides the CM noise voltage measured at the line impedance stabilization network (LISN). Clearly, a decrease of C_{BD} results in lower noise voltage.

$$V_{LISN} = \frac{R_{LISN}}{j\omega C_{TOTAL} + R_{LISN} + Z_{SE}} \cdot \frac{C_{BD}}{C_{TOTAL}} \cdot V_{SW} \qquad (1)$$

Equation 2 gives the theoretical expression for capacitance C_{BD}, and is measured using the technique described in Chapter 7 based on **Equation 3**:

$$C_{BD} = C_2 \cdot \left(1 - \frac{1}{N_{PS}}\right) - \frac{C_3}{N_{PS}} + C_4 + C_{as2} \cdot \left(\frac{1}{N_{AUX}} - \frac{1}{N_{PS}}\right) - \frac{C_{as3}}{N_{PS}} + \frac{C_{as4}}{N_{AUX}} \qquad (2)$$

$$C_{BD} = \left(V_{AD} / V_{AB}\right) \cdot C_{TOTAL} \qquad (3)$$

It is possible to balance C_{BD} to zero [66] by increasing the negative terms in Equation 2. The easiest way is to parallel a capacitor with C_3 across transformer terminals A and C between the primary and secondary sides. The value of this external balance capacitor is $C_{EXT} = N_{PS}C_{BD}$.

Similarly, if C_{BD} is negative (when V_{AD} and V_{AB} measured voltages are out of phase), connecting a balance capacitor equal to the absolute value of C_{BD} in parallel with C_4 across terminals B and D can achieve balance. Note that if the measured V_{AD} from Equation 3 is zero, C_{BD} is effectively zero, essentially eliminating the CM noise through the transformer. This is a very convenient test to determine whether a transformer is well-balanced.

Winding design

As an alternative to balancing capacitors, it is possible to arrange the transformer winding layer positions to improve CM balance. According to the concept of paired layers [63-66], there are layers on the primary and secondary sides that have similar dv/dt; therefore, their overlapping does not generate CM noise. Arranging the average voltages at both ends of the interwinding capacitances to have the similar amplitude and polarity minimizes or nulls the CM current through the capacitances.

The basic principle is to ensure that the adjacent primary and secondary winding layers have similar voltage distributions. Assuming an even distribution of the interwinding parasitic capacitances between the two paired winding layers, it is possible to maintain zero dv/dt over these capacitances such that no CM current is generated.

As an example, consider the flyback converter in Figure 4a and an interleaved three-winding (primary, secondary, auxiliary) transformer. Even though interleaving increases interwinding capacitance, it is often necessary to reduce leakage inductance and proximity effect losses. **Figure 5a** illustrates the winding half-window of a flyback transformer with three series-connected primary layers (3 x 12T), two paralleled secondary layers (2 x 9T) and one auxiliary/bias winding layer (1 x 15T).

Figure 5b illustrates the voltage distribution along the windings. To achieve the lowest CM noise, the adjacent layers between the primary and secondary winding layers should have the lowest average voltage difference. As a result, the interleaved layers of Figure 5a are purposely arranged as S1-P1-S2-AUX-P2-P3.

The average voltage difference between P1 and S1 or S2 is lowest with the terminal connections shown in Figure 5a. P1 starts at VIN (a quiet node) and is positioned adjacent to paralleled secondary layers S1 and S2, as depicted in Figure 5a. Similarly, the AUX winding is adjacent to layer S2, because the voltage difference between AUX and S2 is less than that between S2 and P2 or P3.

The voltage difference between AUX and P2 does not generate CM noise, as both windings reside on the primary side. The displacement currents between them are thus confined to the primary side of the converter and not measured as EMI by the LISN. Conversely, if using a full interleaving winding structure of P1-S1-P2-S2-AUX-P3, the CM noise will significantly increase because of the larger average voltage differences between layer pairs S1 and P2 and P2 and S2.

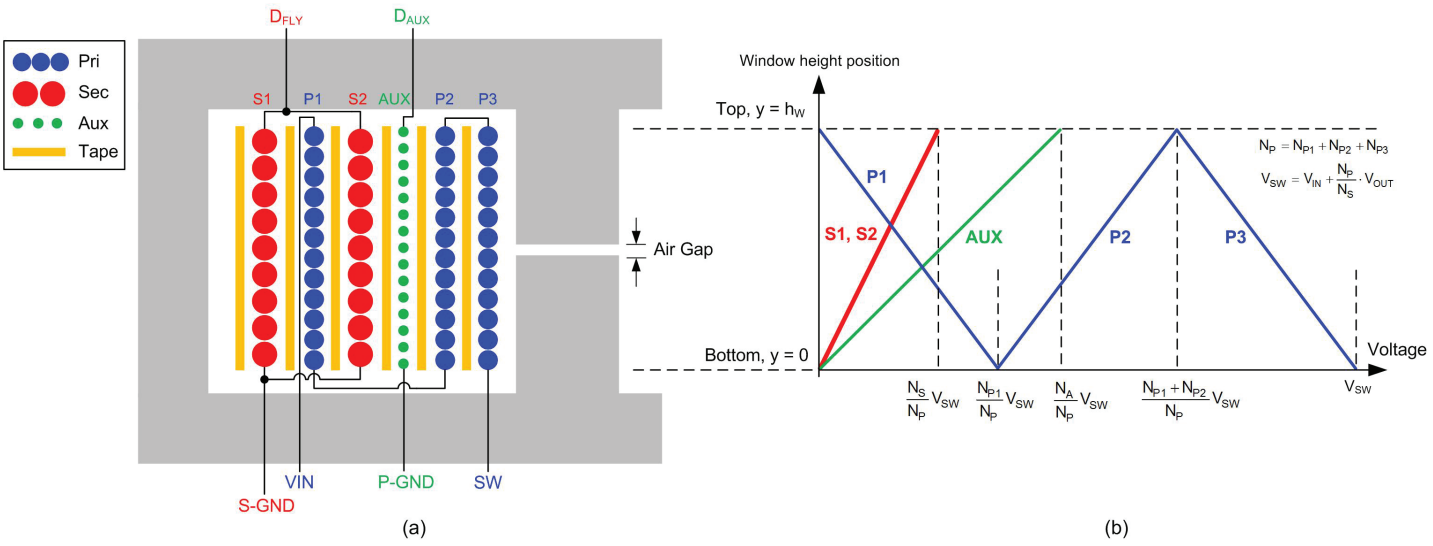


Figure 5. *Flyback transformer with sandwiched winding layer structure (a); voltage distributions of layers across the winding window (b).*

Adjustable auxiliary cancellation winding

An adjustable winding layer enables adjustable cancellation of CM noise. This type of winding, labeled AdjAUX in **Figure 6**, is wound outside of secondary layer S1 to balance the CM noise that is not fully canceled within the winding layers [64], [65]. One terminal of AdjAUX connects to PGND and the other terminal is floating.

Because the voltage difference between AdjAUX and S1 is negative, displacement CM current is flowing from S1 to the AdjAUX winding and then back to the primary side. This helps cancel the displacement CM current flowing from P1 to S1 and S2, as well as from AUX to S2, given the positive voltage difference between P1 and S1, between P1 and S2, and between AUX and S2 layers (P1 and AUX have a higher number of turns on each layer than S1 and S2 in this example). As depicted in **Figure 6b**, the position of the AdjAUX winding is located at the outer layer of the transformer windings, so it is convenient to adjust the number of turns to achieve effective noise cancellation.

As shown in **Figure 6c**, when the AdjAUX winding starts from the top of the winding window, the voltage difference between AdjAUX and S1 layers is largest. Fewer turns achieve the required cancellation effect, whereas more turns will be necessary if the AdjAUX winding is located at the bottom of the window.

There is no eddy current power loss, since the AdjAUX winding is not near the airgap and incurs zero magnetic field (H-field). As a result, the transformer AC winding loss is lower than that with conventional shielding layers. And because there are no shielding layers between winding layers, the mutual coupling between windings is higher, resulting in lower leakage inductance [69]. Finally, when combined with the transformer balance examination technique discussed in Chapter 7, the AdjAUX winding layer offers a convenient design without any in-circuit tests.

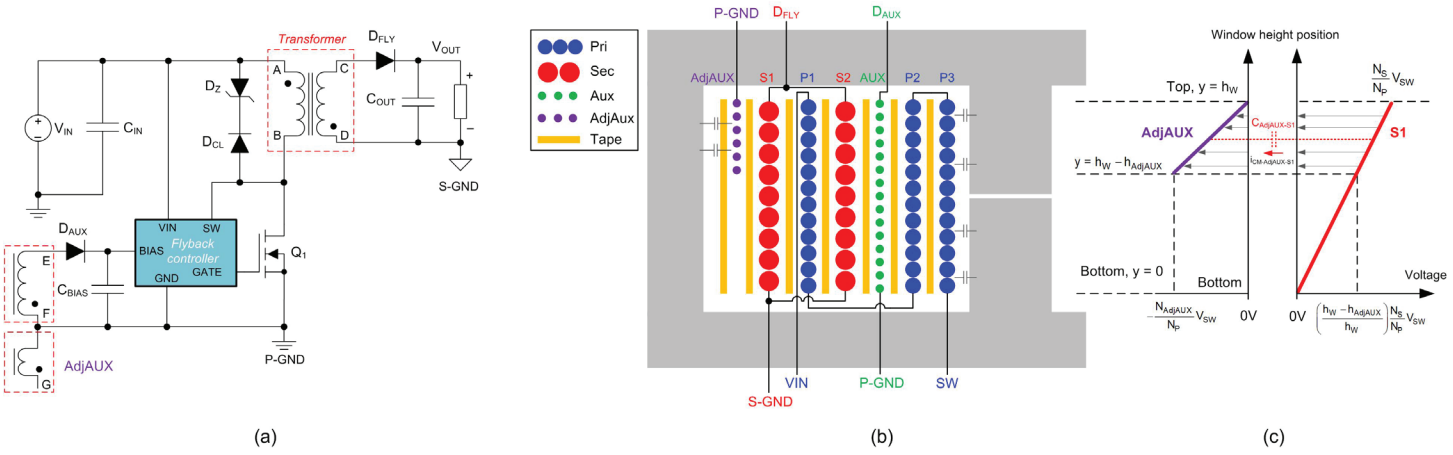


Figure 6. *Adding an adjustable auxiliary winding on the outer layer to cancel CM noise: schematic (a); winding arrangement (b); voltage and current distributions (c).*

9. Spread-spectrum modulation

Complying with electromagnetic standards is an increasingly important task for switching power supplies, not because of excessive total spectral energy, but more so from concentrated energy in specific narrow bands at the fundamental switching frequency and its harmonics.

With a crowded electromagnetic spectrum, switching power supplies are a contributor to the deterioration of the electromagnetic environment. Spread-spectrum techniques seek to alter the shape of the conducted and radiated interfering power spectrum, reducing the level of peak emissions as required by international electromagnetic compatibility (EMC) regulations. The selection of an optimized modulating frequency results in a system-level solution with a smaller footprint and volume, a lower intrinsic cost, and a higher power density.

This chapter:

- Discusses spread-spectrum frequency modulation (SSFM) as a way to distribute spectral energy in the frequency domain and thus flatten the fundamental and harmonic noise peak amplitudes.
- Describes the spread-spectrum effect as an additional and complementary method of noise reduction with respect to the electromagnetic interference (EMI) mitigation techniques described in previous chapters.

Fundamentals of spread-spectrum modulation

The EMI mitigation techniques discussed in Chapters 5 and 6 focused on reducing the antenna factor through careful layout of high slew-rate transient current loops and avoiding sharp transient voltages through suitable snubber and gate-drive circuit design. Effective mostly at high frequencies, these methods seek to adjust the shape of the conducted or radiated noise power spectrum, or both spectrums, by reducing their overall power. The effectiveness at low frequency may be limited, though.

Conversely, spread-spectrum modulation (or dithering), first proposed in 1992 for DC/DC converters [70], aims to reshape the conducted and radiated interfering power spectrum without affecting the total noise power. Through frequency modulation of the reference clock signal in the time domain, the fundamental and harmonic components are swept in the frequency domain according to the modulating signal [70-75]. As depicted in **Figure 1**, each harmonic changes into a number of sideband harmonics with lower amplitudes. The noise spectrum alters from a train of large spectral peaks concentrated at the switching frequency and its harmonics to a smoother, lower and more continuous spectrum.

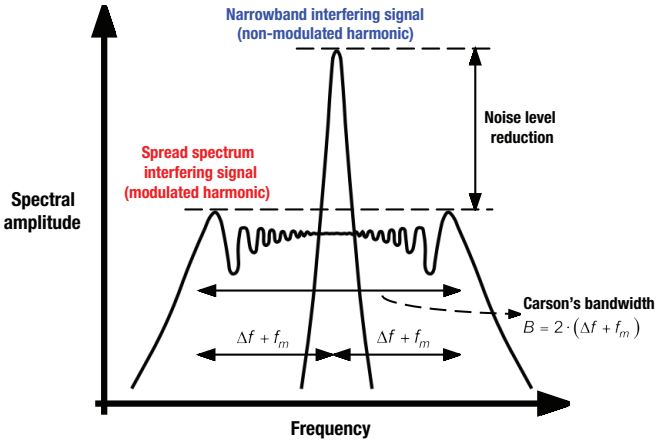


Figure 1. *Spread-spectrum effect.*

From a practical EMC standpoint, when a narrowband EMI source's signal frequency aligns with an EMI victim's sensitive frequency range, a large amount of power can transfer in a given time window, increasing the probability of disturbance or failure of the EMI victim. Spreading the EMI source signal into a bandwidth larger than the EMI victim's sensitivity bandwidth reduces the noise power coupled to the victim, leading to an overall improvement in EMC performance and reliability.

Periodic modulation functions

The main idea behind periodic spread-spectrum modulation techniques is to spread each individual harmonic into a preset frequency band, leading to reduced peak amplitudes and lower EMI levels. Within this context, **Equation 1** provides a generalized analytical expression for frequency modulation of a sinusoidal carrier caused by spread-spectrum modulation:

$$s(t) = A \cdot \cos\left(2\pi f_c t + 2\pi \Delta f \int_{-\infty}^{t} \xi(t)\, d\tau\right) \quad (1)$$

where A is the amplitude of the unmodulated signal, f_c is the carrier frequency and Δf is the frequency deviation.

The normalized periodic modulating function is ξ(t), which expresses the frequency variation of the spread spectrum. **Table 1** gives the mathematical expressions for sinusoidal, triangular and exponential (also known as cubic or "Hershey's kiss") modulation profiles [71]. Here, k_T is a symmetry index of the triangular profile that ranges from 0 to 1, and p designates a concavity coefficient of the exponential profile. The triangular profile has a symmetrical triangular pattern if k_T is 0.5.

Figure 2 shows the sinusoidal, triangular and exponential modulating signals with a 10-kHz modulating frequency. The figure also captures the corresponding spread-spectrum result by modulating a 100-kHz sinusoidal carrier signal consistent with Equation 1. The top of each plot specifies notable instantaneous carrier working frequencies.

Sinusoidal	Triangular (with symmetry index, k_T)	Exponential (with concavity coefficient, p)
$\xi(t) = \sin(2\pi f_m t)$	$\xi(t) = \begin{cases} \frac{2}{k_T} \cdot f_m t, & 0 \le t < \frac{k_T \cdot T_m}{2} \\ \frac{1}{1-k_T} \cdot (1 - 2 f_m t), & \frac{k_T \cdot T_m}{2} \le t < \left(1 - \frac{k_T}{2}\right) \cdot T_m \\ \frac{2}{k_T} \cdot (f_m t - 1), & \left(1 - \frac{k_T}{2}\right) \cdot T_m \le t < T_m \end{cases}$	$\xi(t) = \begin{cases} \frac{1}{e^{p/4 \cdot f_m} - 1} \cdot \left(e^{p \cdot t} - 1\right), & 0 \le t < \frac{T_m}{4} \\ \frac{1}{e^{p/4 \cdot f_m} - 1} \cdot \left(e^{p/2 \cdot f_m} \cdot e^{-p \cdot t} - 1\right), & \frac{T_m}{4} \le t < \frac{T_m}{2} \\ \frac{1}{e^{p/4 \cdot f_m} - 1} \cdot \left(1 - e^{-p/2 \cdot f_m} \cdot e^{p \cdot t}\right), & \frac{T_m}{2} \le t < \frac{3 \cdot T_m}{4} \\ \frac{1}{e^{p/4 \cdot f_m} - 1} \cdot \left(1 - e^{p/f_m} \cdot e^{-p \cdot t}\right), & \frac{3 \cdot T_m}{4} \le t < T_m \end{cases}$

Table 1. *Sinusoidal, triangular and exponential modulation profiles where f_m and T_m are the modulating signal frequency and period, respectively.*

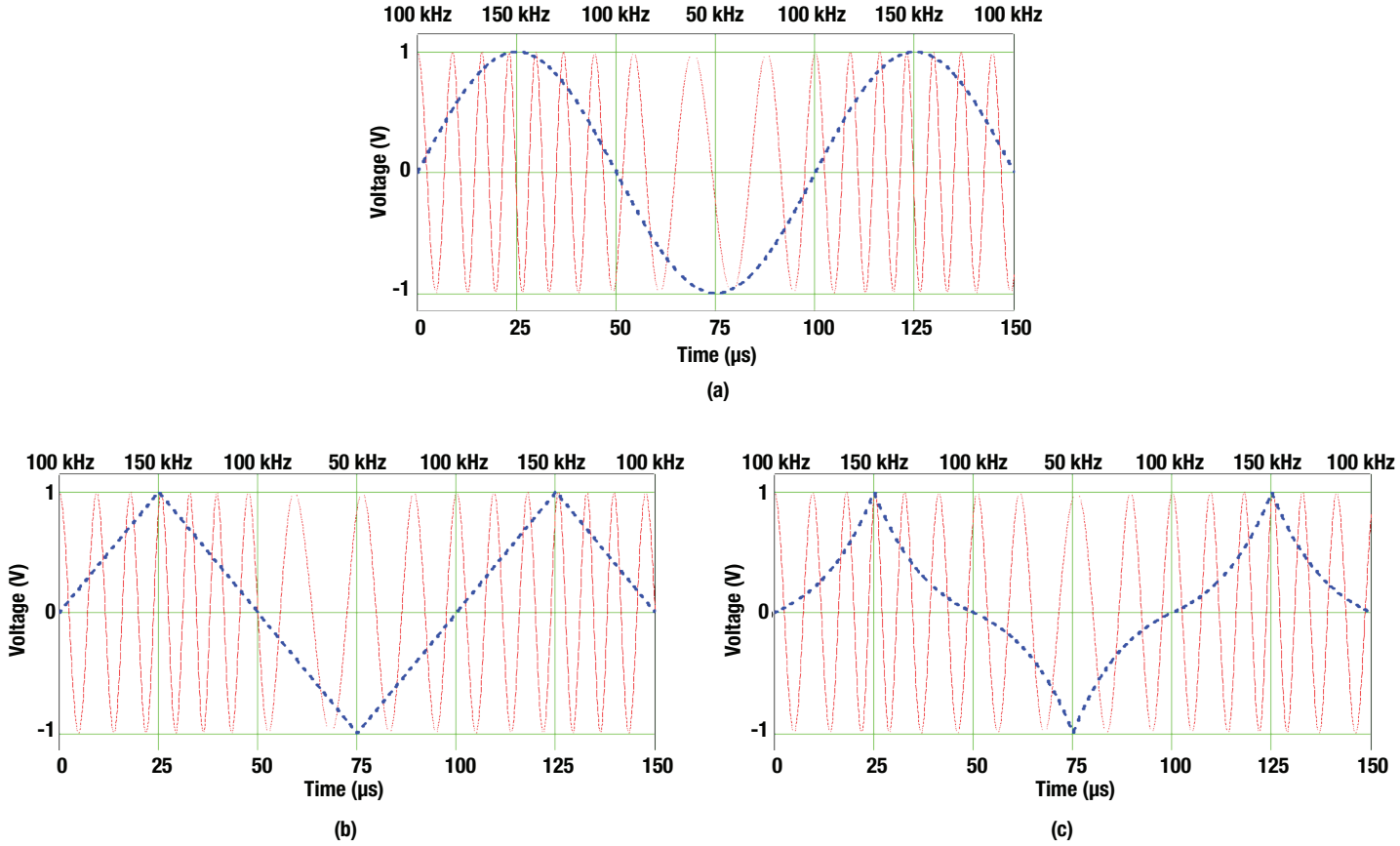


Figure 2. *Sinusoidal (a), triangular (b) and exponential (c) modulation profiles with f_c = 100 kHz, Δf = 50 kHz, f_m = 10 kHz, k_T = 0.5 and p = 70 kHz.*

Equation 2 expresses the modulation index, while **Equation 3** expresses the modulation ratio:

$$m = \frac{\Delta f}{f_m} = \Delta f \cdot T_m \tag{2}$$

$$\delta = \frac{\Delta f}{f_c} \tag{3}$$

The total power of s(t) is equal to $A^2/2$, which is distributed using the spread-spectrum technique according to Carson's bandwidth rule – that is, the energy after spread spectrum is 98% contained in a bandwidth, B (see Figure 1), given by **Equation 4**:

$$B = 2 \cdot (\Delta f + f_m) = 2 \cdot f_m \cdot (1 + m) \tag{4}$$

For a more complicated waveform, such as the switch-node voltage or the input current of a DC/DC regulator, changing the instantaneous frequency is equivalent to applying Equation 1 to each constituent harmonic of the Fourier series expansion, with the only difference being that the nth harmonic is spread within a bandwidth of n times Carson's bandwidth given by Equation 4.

The actual shape of the spectrum of s(t) depends on the modulation parameters Δf and ξ(t). When ξ(t) is a periodic function with period T_m, the spectrum of s(t) is discrete, meaning that it is possible to decompose the signal into a sum of sinusoidal tones at frequency $f_c \pm k/T_m$, each one with amplitude A_k. The computation of A_k for sinusoidal modulation is achieved with Bessel functions [70], [71], while the spectrum shape for triangular modulation has been evaluated using a Matlab simulation [72].

It is only possible to obtain a truly continuous power spectrum in the frequency domain with a nonperiodic modulating function, such as that achieved using a chaotic or random sequence generator and described using the power spectral density. A nonperiodic modulation, in contrast to a periodic spreading technique, enables a measured spectral shape independent of the resolution bandwidth (RBW) setting [76], [77] of the measurement instrument.

Although a sinusoidal spreading technique is easier to analyze and implement, it does not yield the best spectrum shape, and does not maximize the harmonic attenuation. As illustrated in **Figure 3**, the energy in the spectrum of the modulated waveform tends to concentrate at frequencies corresponding to points in the modulation waveform where the time derivative is low, which is near the peaks and valleys of a sinusoidal waveform.

On the other hand, the exponential modulating function has the flattest spectrum and further reduces EMI by compensating for the peaks caused by second-order effects that appear near both ends of Carson's bandwidth. However, the exponential waveform is difficult to implement in practice, typically requiring a complex distortion circuit or a look-up table.

A linear, triangular-shaped modulation represents a good compromise between the modulation profiles illustrated in Figure 3 and is easy to implement in both the analog and digital domains. By selecting an optimized, well-defined frequency of the triangular driving signal to achieve the maximum peak reduction of the measured EMI spectrum, you can realize a robust design for high-volume and cost-optimized applications such as automotive.

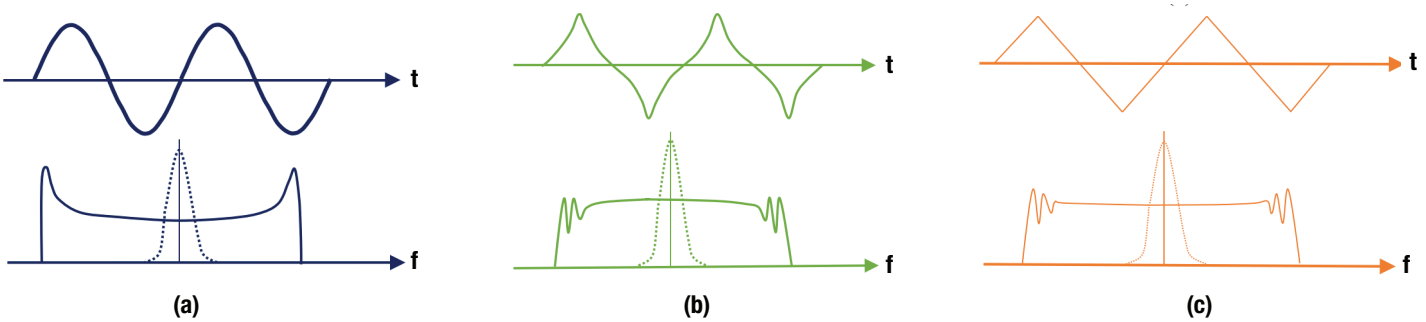


Figure 3. *Sinusoidal (a), triangular (b) and exponential (c) modulation functions and frequency-domain behaviors.*

EMI reduction optimization by spread spectrum

International regulations require that an EMI receiver takes measurements; this receiver is essentially an analog spectrum analyzer with some additional input filters. Given the complexity of the superheterodyne spectrum analyzer [77] (in particular, the nonlinearity of the demodulating envelope detector and the peak/quasi-peak/average detector) for EMI measurements, researchers in [72] used a Matlab model of an EMI receiver to calculate reduced EMI through spreading techniques based on a triangular modulation. This enabled the development of optimization curves for triangular spread spectrum.

As an example, **Figure 4** provides curves for noise-level reduction based on several values of frequency deviation Δf as a multiple of the RBW setting of the EMI receiver. Notice that the EMI reduction performance reduces when m increases above a certain value.

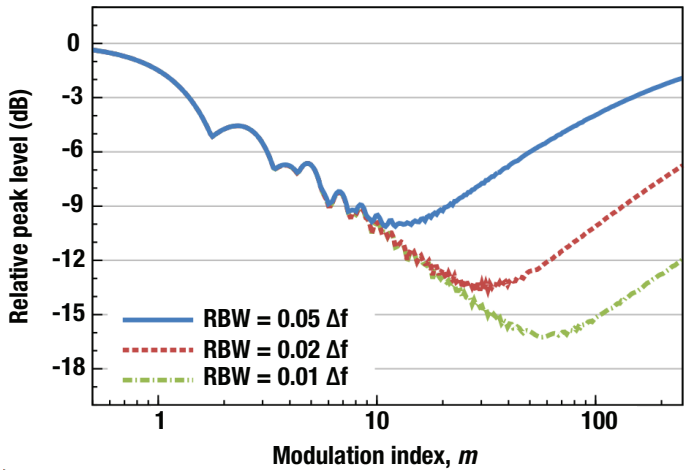


Figure 4. *Noise-level reduction of the triangular modulation power spectrum consistent with the EMI receiver response for different ratios of RBW/Δf, where the modulation index is varied by fixing Δf and changing fm. The 0-dB reference is the unmodulated case.*

Two trade-offs exist when selecting modulation spreading parameters Δf and f_m. First, Δf should be large enough to reduce the measured EMI as well as the interference of the EMI victim. For example, in order to avoid interference within the AM radio band, an automotive DC/DC regulator typically uses an external resistor to set the free-running switching frequency at 2.1 MHz with a 5% to 10% allowable tolerance. To operate above the maximum AM band frequency of 1.6 MHz with adequate margin, a center-spread modulation with Δf in the range of 100 kHz to 150 kHz is appropriate, and avoids large perturbations to the regulator's output voltage ripple amplitude and efficiency performance.

Having established Δf, an additional degree of freedom to optimize EMI performance depends on the choice of modulating frequency. The modulation index m should have an intermediate value according to Figure 4 – high enough to provide EMI attenuation yet low enough that the time-domain effect of the RBW band-pass filter is not applicable. More specifically, if f_m is low, the time interval in which the instantaneous interfering signal frequency is within the RBW filter response time increases. The signal appears unmodulated for a longer time in the measurement window, effectively resulting in a measurement of the unmodulated signal amplitude. This short-term time-domain effect similarly applies to an EMI victim circuit and its sensitivity band.

As a result, a consideration of time-domain behavior is essential for correctly estimating of the impact of spreading techniques when using the appointed EMI measurement setup over the prescribed frequency range. For example, regulations such as Comité International Spécial des Perturbations Radioélectriques (CISPR) 25 for automotive applications impose RBW settings of 9 kHz and 120 kHz for measurements in the frequency bands of 150 kHz to 30 MHz and 30 MHz to 1 GHz, respectively.
As a general rule of thumb, when setting fm close to the mandated RBW, the EMI receiver is able to measure each individual sideband harmonic separately such that the measurement results tally with the expected calculations.

Practical case study

Figure 5 is a schematic of a four-phase synchronous buck regulator circuit [78] using two dual-phase stackable controllers. The controller incorporates several features for EMI reduction, including constant switching-frequency operation, external clock synchronization and switch-node shaping (slew-rate control) with split gate-drive outputs for each power switch.

The controller operates with a resistor-adjustable switching frequency up to 2.2 MHz, with external synchronization possible up to 2.5 MHz. Three options are available to configure the SSFM:

- Apply a carrier frequency signal with the required modulation using the controller's external synchronization (SYNCIN) input.
- Resistively couple a modulation signal to the RT pin.
- Set the modulating frequency with a capacitor at the DITH pin and use the built-in ±5% triangular spread-spectrum (dither) function.

Given a nominal switching frequency of 2.1 MHz, the frequency deviation Δf is 5% or 105 kHz when using the integrated spread-spectrum feature. The EMI receiver uses an RBW filter of 9 kHz for measurements in the range of 150 kHz to 30 MHz. Since EMI filters in spectrum analyzers are usually defined in terms of a -6-dB bandwidth with a four-pole, nearly Gaussian shape [77], applying a correction factor finds the effective -3-dB bandwidth of the 9-kHz RBW filter as approximately 6 kHz. Using **Equation 5** to calculate the normalized resolution finds an optimized modulation index of approximately 10 based on optimization curves similar to Figure 4:

$$\rho = \frac{\text{RBW}(-3dB)}{\Delta f} = \frac{6\text{kHz}}{105\text{kHz}} = 0.057 \quad (5)$$

Equation 6 then derives the required modulating frequency:

$$f_m = \frac{\Delta f}{m} = \frac{105\text{kHz}}{10} = 10.5\text{kHz} \quad (6)$$

Figure 6 shows the switch-node voltage waveform (measured using the regulator in Figure 5) with spread spectrum both enabled and disabled. The waveform of Figure 6b has scope persistence activated to illustrate the switching frequency variation.

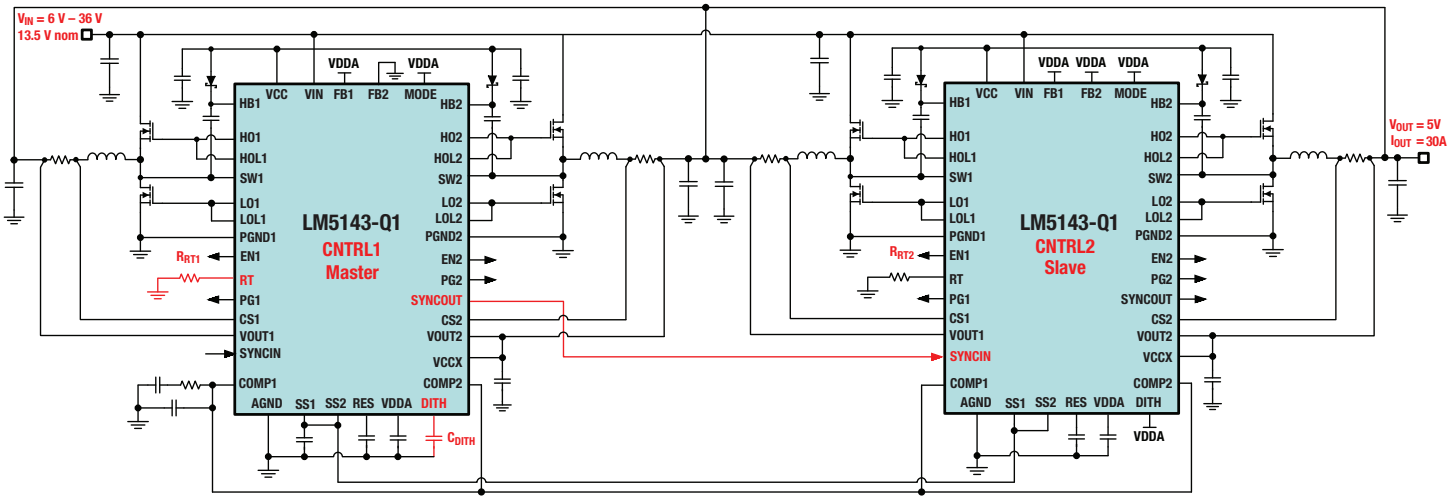


Figure 5. Schematic of a four-phase synchronous buck regulator with triangular spread-spectrum modulation.

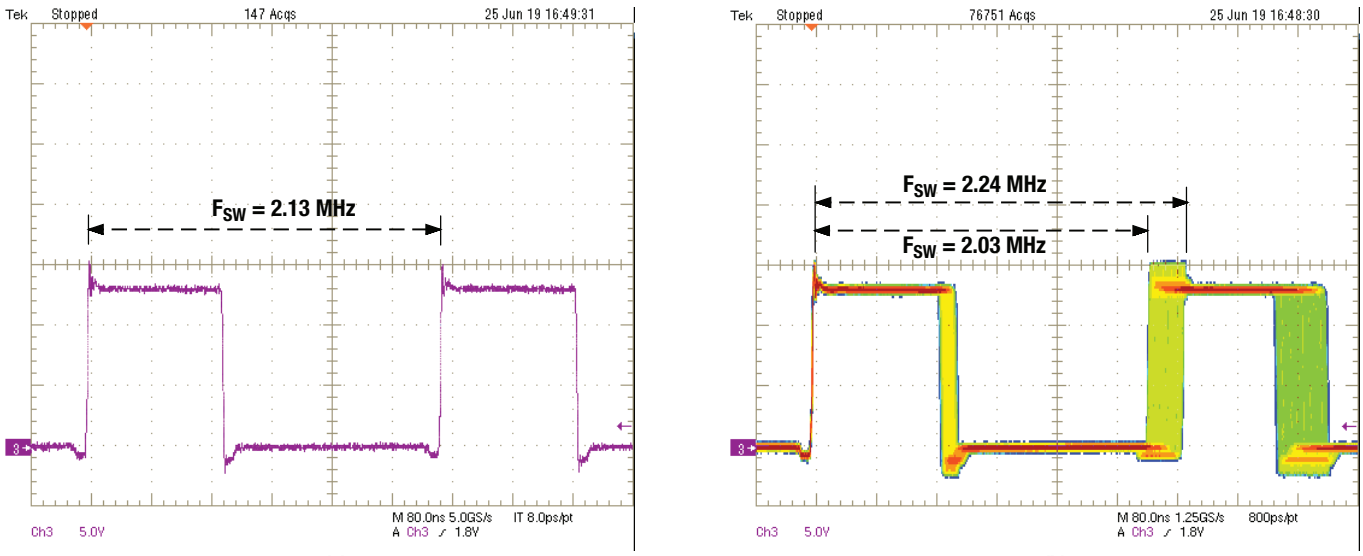


Figure 6. Switch-node voltage waveform (V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 20 A) with spread spectrum disabled (a); and enabled (b).

Figure 7 shows the conducted emissions measured from 150 kHz to 30 MHz for the regulator in Figure 5 with a triangular modulating function set at 10 kHz. Using a Rohde & Schwarz spectrum analyzer, peak and average detector scans are denoted in yellow and blue, respectively. The results are in compliance with CISPR 25 Class 5 requirements. The limit lines in red are the Class 5 peak and average limits (peak limits are generally 20 dB higher than the average limits).

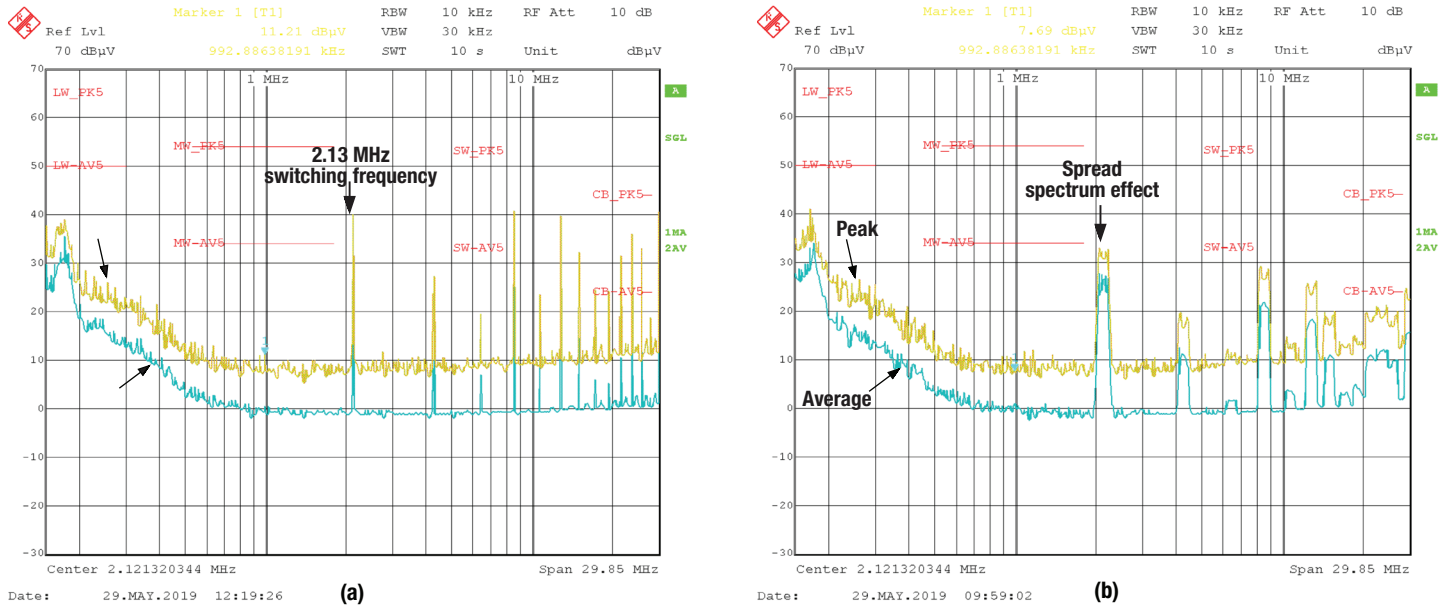


Figure 7. *CISPR 25 Class 5 conducted emission results (150 kHz to 30 MHz) with spread spectrum disabled (a); and enabled (b).*

Additional resources

For more information on EMI go to: TI.com/lowemi

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References

1. "Electromagnetic compatibility of multimedia equipment – Emission requirements." CISPR 32:2015, second edition (or European Norm [EN] 55032:2015). Comité International Spécial des Perturbations Radioélectriques (CISPR): Geneva, Switzerland, October 2019.
2. "Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers." CISPR 25:2016, fourth edition (or EN 55025:2017). CISPR: Geneva, Switzerland, October 2017.
3. Han, Di, Silong Li, Woongkul Lee, Wooyoung Choi, and Bulent Sarlioglu. "Trade-Off Between Switching Loss and Common Mode EMI Generation of GaN Devices – Analysis and Solution." Published in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March 26-30, 2017, pp. 843-847.
4. Wikipedia. "List of common EMC test standards." Last modified Aug. 16, 2020.
5. "Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement." CISPR 22:2008 RLV, sixth edition (or EN 55022:2011). CISPR: Geneva, Switzerland, April 2012.
6. "Directive 2014/30/EU of the European Parliament and of the Council." European Commission: Brussels, Belgium, February 2014.
7. Williams, Tim. 2016. "EMC for Product Designers, Fifth Edition." Boston, Massachusetts: Newnes.
8. "Electromagnetic compatibility (EMC) – Part 6-3: Generic standards – Emission standard for residential, commercial and light-industrial environments. " IEC 61000-6-3:2006+AMD1:2010. International Electrotechnical Commission (IEC): Geneva, Switzerland, February 2011.
9. "Electromagnetic compatibility (EMC) – Part 6-4: Generic standards – Emission standard for industrial environments." IEC 61000-6-4:2006+AMD1:2010. IEC: Geneva, Switzerland, February 2011.
10. "Uniform provisions concerning the approval of vehicles with regard to electromagnetic compatibility." UN ECE Regulation No. 10. United Nations (UN) Economic Commission for Europe (ECE): New York, October 2014.
11. Ford Motor Co. "Welcome to the resource for information regarding Electromagnetic Compatibility Requirements for Ford Motor Company." Accessed Aug. 24, 2020.
12. Parmenter, Kevin, and James Spangler. 2017. "Understanding LISNs is Essential to EMI Pre-Compliance Testing." How2Power Today, October 2017.
13. Hegarty, Timothy, Robert Loke, and David Pace, Texas Instruments. "Understanding EMI and Mitigating Noise in DC/DC Converters." (May 11, 2017). Accessed Oct. 8, 2020. [Online Video].
14. "Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-2: Radio disturbance and immunity measuring apparatus – Coupling devices for conducted disturbance measurements." CISPR 16-1-2:2014. CISPR: Geneva, Switzerland, March 2014.
15. "American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." C63.4-2014, revision of American National Standards Institute (ANSI) C63.4-2009. Institute of Electrical and Electronics Engineers (IEEE): Piscataway, New Jersey, June 2014.
16. Hegarty, Timothy, Robert Loke, and David Pace, Dallas, Texas. "Understanding EMI and Mitigating Noise in DC/DC Converters." (May 11, 2017). Accessed Oct. 8, 2020. [Online Video].
17. Kovačević, I., Florian Krismer, Sebastian Schroth, and Johann Walter Kolar. "Practical characterization of EMI filters replacing CISPR 17 approximate worst case measurements." Published in 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), June 23-26, 2013, pp. 1-10.

18. "IEEE Standard for Methods of Measurement of Radio Frequency Power Line Interference Filter in the Range of 100 Hz to 10 GHz." 1560-2005. IEEE: Piscataway, New Jersey, February 2006.
19. Wang, Shuo. 2005. "Characterization and Cancellation of High-Frequency Parasitics for EMI Filters and Noise Separators in Power Electronics Applications." Ph.D. dissertation, Virginia Polytechnic Institute and State University.
20. Wang, Shuo, and Fred C. Lee. "Investigation of the Transformation Between Differential-Mode and Common-Mode Noises in an EMI Filter Due to Unbalance." Published in IEEE Transactions on Electromagnetic Compatibility 52, no. 3 (August 2010): pp. 578-587.
21. Krismer, Florian, Sebastian Schroth, Hans Ertl, Konstantin Stoychev Kostov, Hans-Peter Nee, and Johann Walter Kolar. "Analysis and Practical Relevance of CM/DM EMI Noise Separator Characteristics." Published in IEEE Transactions on Power Electronics 32, no. 4 (April 2017): pp. 3112-3127.
22. Texas Instruments. n.d. LM5150-Q1 wide V_{IN} automotive low IQ boost controller. Accessed Oct. 8, 2020.
23. Han, Di, Casey T. Morris, Woongkul Lee, and Bulent Sarlioglu. "A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs." Published in IEEE Transactions on Transportation Electrification 3, no. 1 (October 2016): pp. 168-179.
24. Texas Instruments. n.d. Achieving low noise and low EMI performance with DC/DC switching regulators. Accessed Oct. 8, 2020.
25. "LM5145 6-V to 75-V Synchronous Buck DC/DC Controller with Wide Duty Cycle Range."

    Texas Instruments data sheet, literature No. SNVSA14, November 2017, revised May 2020.
26. Paul, Clayton R. 2009. "Inductance: Loop and Partial." Hoboken, New Jersey: Wiley-IEEE Press.
27. Bhargava, Ankit, David Pommerenke, Keong W. Kam, Federico Centola, and Cheung-Wei Lam. "DC/DC Buck Converter EMI Reduction Using PCB Layout Modification." Published in IEEE Transactions on Electromagnetic Compatibility 53, no. 3 (July 2011): pp. 806-813.
28. Mehta, Narendra. "Layout Considerations for LMG5200 GaN Power Stage." Texas Instruments application note, literature No. SNVA729, March 2015, revised September 2015.
29. Kam, Keong, David Pommerenke, Federico Centola, Cheung-Wei Lam, and Robert Steinfeld. "EMC guideline for synchronous buck converter design." Published in IEEE International Symposium on Electromagnetic Compatibility, Aug. 17-21, 2009, pp. 47-52.
30. Taylor, Robert, and Ryan Manack. "Controlling switch-node ringing in synchronous buck converters." Texas Instruments Analog Applications Journal article, literature No. SLYT465, 2Q 2012.
31. Wang, Kangping, Laili Wang, Xu Yang, Xiangjun Zeng, Wenjie Chen, and Hongchang Li. "A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC–DC Converter." Published in IEEE Transactions on Power Electronics 32, no. 6 (August 2016): pp. 4728-4740.
32. Glaser, John S., and David Reusch. "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs." Published in 2016 IEEE Energy Conversion Congress and Exposition, Sept. 18-22, 2016, pp. 1-8.
33. Oswald, Niall, Bernard Stark, Derrick Holliday, Collin Hargis, and Bill Drury. "Analysis of Shaped Pulse Transitions in Power Electronic Switching Waveforms for Reduced EMI Generation." Published in IEEE Transactions on Industry Applications 47, no. 5 (September/October 2011): pp. 2154-2165.
34. Mardiguian, Michel. 2014. "Controlling Radiated Emissions by Design, Third Edition." New York: Springer.
35. "Title 47, Subchapter A, Part 15, Subpart B – Unintentional Radiators, Section 15.109, Radiated emissions limits." Federal Communications Commission Code of Federal Regulations: Washington, D.C., October 2020.
36. "Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement." CISPR 22:2008 RLV (or EN 55022:2011). CISPR: Geneva, Switzerland, April 2012.

37. Singh, Ajinder. "Gas Sensor Platform Reference Design." Texas Instruments reference design guide, literature No. SNOA922, August 2013.
38. Texas Instruments. n.d. "CISPR-22 EMI-Optimized Reference Design Featuring the LMR16030 DC/DC Buck Converter." TI reference design No. PMP15013. Accessed Oct. 9, 2020.
39. "Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers." CISPR 25:2016, fourth edition (or EN 55025:2017). CISPR: Geneva, Switzerland, October 2017.
40. Texas Instruments. n.d. LM53635-Q1 2.5-A/3.5-A, 36-V, synchronous, 2.1-MHz automotive step-down DC/DC converter automotive reference designs. Accessed Oct. 9, 2020.
41. Petkov, Denislav, Dallas, Texas. "Layout Tips for Radiated EMI Reduction in Your Designs." (July 1, 2015). Accessed: Oct. 9, 2020. [Online Video].
42. Mao, Vental. 2018. "There are more ways than you think to reduce conducted EMI." TI E2E™ support forums technical article, April 17, 2018.
43. Sclocchi, Michele. 2010. "Input Filter Design for Switching Power Supplies," Texas Instruments application report, literature No. SNVA538, 2010.
44. Texas Instruments. n.d. "EMI Optimized 2-Layer 15W Power Supply for Automotive with CISPR 25 Class 5 Compliance." TI reference design No. PMP10604. Accessed Oct. 9, 2020.
45. Texas Instruments. n.d. LMR36015 4.2-V to 60-V, 1.5-A ultra-small synchronous step-down converter. Accessed Oct. 9, 2020.
46. De Stasi, Frank, Dallas, Texas. "Reduce EMI and shrink solution size with HotRod packaging." (March 7, 2018). Accessed Oct. 9, 2020. [Online Video].
47. Wiggenhorn, Katelyn, Dallas, Texas. "Eliminate High-Frequency Switch-Node Ringing and Pass CISPR 25 Class 5 without Metallic Shielding or a Common-Mode Choke." (Sept. 11, 2017). Accessed Oct. 9, 2020. [Online Video].
48. Texas Instruments. n.d. LM5146-Q1-EVM12V synchronous buck controller evaluation module. Accessed Oct. 9, 2020.
49. Lidow, Alex, Johan Strydom, Michael de Rooij, and David Reusch. 2014. "GaN Transistors for Efficient Power Conversion, Second Edition." Hoboken, New Jersey: Wiley.
50. Reusch, David, and Johan Strydom. "Understanding the effect of PCB layout on circuit performance in a high frequency gallium nitride based point of load converter." Published in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exhibition, March 17-21, 2013, pp. 649-655.
51. Mehta, Narendra. "Layout considerations for LMG5200 GaN Power Stage." Texas Instruments application note, literature No. SNVA729, March 2015, revised September 2015.
52. Texas Instruments. n.d. LM5180EVM-S05 wide VIN PSR flyback converter single-output evaluation module. Accessed Oct. 9, 2020.
53. Texas Instruments. n.d. LM5180EVM-DUAL wide VIN PSR flyback converter dual-output evaluation module. Accessed Oct. 9, 2020.
54. Texas Instruments. n.d. LM5155-Q1 2.2MHz wide VIN non-synchronous boost/SEPIC/flyback controller. Accessed Oct. 9, 2020.
55. Picard, Jean. "Under the Hood of Flyback SMPS Designs." Texas Instruments Power Supply Design Seminar SEM1900, literature No. SLUP261, 2010-2011.
56. Keough, Bernard, and Isaac Cohen. "Flyback transformer design considerations for efficiency and EMI." Texas Instruments Power Supply Design Seminar SEM2200, literature No. SLUP338, 2016-2017.
57. Xie, Lihong, Xinbo Ruan, and Zhihong Ye. "Equivalent Noise Source: An Effective Method for Analyzing Common-Mode Noise in Isolated Power Converters." Published in IEEE Transactions on Industrial Electronics 63, no. 5 (January 2016): pp. 2913-2924.
58. Zhang, Huan, Shuo Wang, Yiming Li, Qinghai Wang, and Dianbo Fu. "Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Analysis in Isolated DC–DC Converters." Published in IEEE Transactions on Power Electronics 32, no. 11 (January 2017): pp. 8458-8469.

59. Li, Yiming, Huan Zhang, Shuo Wang, Honggang Sheng, Choon Ping Chng, and Srikanth Lakshmikanthan. "Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y-Capacitors in Flyback Converters." Published in IEEE Journal of Emerging and Selected Topics in Power Electronics 6, no. 4 (April 2018): pp. 2287-2301.

60. Scibilia, Robert. "Design Review of a 2-kW Parallelable Power-Supply Module." Texas Instruments Power Supply Design Seminar SEM2200, literature No. SLUP348, 2016-2017.

61. Scibilia, Robert. "Design review of a 2-kW parallelable power supply module." Texas Instruments Power Supply Design Seminar SEM2200, literature No. SLUP349, 2016-2017.

62. Scibilia, Robert, Dallas, Texas. "Design Review of a 2-kW Parallelable Power-Supply Module." (Aug. 25, 2016). Accessed Oct. 9, 2020. [Online Video].

63. Huang, Hong. "Designing an LLC Resonant Half-Bridge Power Converter." Texas Instruments Power Supply Design Seminar SEM1900, literature No. SLUP263, 2010-2011.

64. Huang, Hong. "Designing an LLC Resonant Half-Bridge Power Converter." Texas Instruments Power Supply Design Seminar SEM1900, literature No. SLUP256, 2010-2011.

65. Chu, Yongbin, and Shuo Wang, "A Generalized Common-Mode Current Cancellation Approach for Power Converters." Published in IEEE Transactions on Industrial Electronics 62, no. 7 (January 2015): pp. 4130-4140.

66. Texas Instruments. n.d. High Voltage Monolithic Two-Switch Forward Isolated DC-DC Converter Evaluation Board. Accessed Oct. 9, 2020.

67. Bai, Yongjiang, Xu Yang, Dan Zhang, Xinlei Li, Wenjie Chen, and Weihao Hu. "Conducted EMI Mitigation Schemes in Isolated Switching-Mode Power Supply Without the Need of a Y-Capacitor." Published in IEEE Transactions on Power Electronics 32, no. 4 (June 2016): pp. 2687-2703.

68. Li, Yiming, Huan Zhang, Shuo Wang, Honggang Sheng, Choon Ping Chng, and Srikanth Lakshmikanthan. "Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y-Capacitors in Flyback Converters." Published in IEEE Journal of Emerging and Selected Topics in Power Electronics 6, no. 4 (April 2018): pp. 2287-2301.

69. Li, Yiming, Huan Zhang, Shuo Wang, Honggang Sheng, Srikanth Lakshmikanthan, and Choon Ping Chng. "Techniques of the modeling, measurement and reduction of common mode noise for a multi-winding switching transformer." Published in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March 26-30, 2017, pp. 2511-2518.

70. Kong, Pengju, and Fred C. Lee. "Transformer structure and its effects on common mode EMI noise in isolated power converters." Published in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Feb. 21-25, 2010, pp. 1424-1429.

71. Yang, Yuchen. 2018. "EMI Noise Reduction Techniques for High Frequency Power Converters." Ph.D. dissertation, Virginia Polytechnic Institute and State University.

72. Chen, Henglin, and Ji Xiao. "Determination of Transformer Shielding Foil Structure for Suppressing Common-Mode Noise in Flyback Converters." Published in IEEE Transactions on Magnetics, 52, no. 12 (July 2016): article sequence No. 8401809.

73. Keough, Bernard, and Isaac Cohen, "Flyback transformer design considerations for efficiency and EMI." Texas Instruments Power Supply Design Seminar SEM2200, literature No. SLUP338, 2016-2017.

74. Keough, Bernard, and Isaac Cohen, "Flyback transformer design considerations for efficiency and EMI." Texas Instruments Power Supply Design Seminar SEM2200, literature No. SLUP339., 2016-2017.

75. Keough, Bernard, and Isaac Cohen, Dallas, Texas, " Flyback Transformer Design Considerations for Efficiency and EMI." (Aug. 25, 2016). Accessed Oct. 9, 2020. [Online Video].

76. Lin, Feng. 1992. "Reduction of power supply EMI emission by switching frequency modulation." Master's thesis, Virginia Polytechnic Institute and State University.

77. Balcells, Josep, Alfonso Santolaria, Antonio Orlandi, David Gonzalez, and Javier Gago. "EMI reduction in switched power converters using frequency modulation techniques." Published in IEEE Transactions on Electromagnetic Compatibility 47, no. 3 (October 2005): pp. 569-576.

78. Pareschi, Fabio, Riccardo Rovatti, and Gianluca Setti. "EMI Reduction via Spread Spectrum in DC/DC Converters: State of the Art, Optimization and Tradeoffs." Published in IEEE Access 3 (December 2015): pp. 2857-2874.

79. Pareschi, Fabio, Gianluca Setti, Riccardo Rovatti, and Giovanni Frattini. "Practical Optimization of EMI Reduction in Spread Spectrum Clock Generators with Application to Switching DC/DC Converters." Published in IEEE Transactions on Power Electronics 29, no. 9 (September 2014): pp. 4646-4657.

80. Rice, John. "Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications." Texas Instruments Power Supply Design Seminar SEM1800, literature No. SLUP269, 2008-2009.

81. Rice, John. "Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications." Texas Instruments Power Supply Design Seminar SEM1800, literature No. SLUP283, 2008-2009.

82. Gamoudi, Rabiaa, Dhia Elhak Chariag, and Lassaad Sbita. "A Review of Spread-Spectrum-Based PWM Techniques – A Novel Fast Digital Implementation." Published in IEEE Transactions on Power Electronics 33, no. 12 (February 2018): pp. 10292-10307.

83. "Making EMI Compliance Measurements." Keysight Technologies application note, 2015.

84. "Spectrum Analysis Basics." Keysight Technologies application note AN150, 2016.

85. Hegarty, Timothy. "LM5143-Q1 4-phase buck regulator design for automotive ADAS applications." Texas Instruments application report, literature No. SNVA870, March 2019.

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