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Product-level Reliability of GaN Devices

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***Abstract*—To enable the widespread adoption of GaN products, the industry needs to be convinced of product-level reliability. The difficulty with product-level reliability lies with the diverse range of products and use conditions, a limited ability for system-level acceleration, and the complication from non-GaN system failures. For power management applications, however, it is possible to identify fundamental switching transitions. This allows the device to be qualified in an application-relevant manner. In this paper, we explain how hard-switching can form a fundamental switching transition for power management products. We further show that the familiar double-pulse tester is a good hard-switching qualification test vehicle. The methodology is explained in the context of the existing qualification framework for silicon transistors.**

***Index Terms*—Gallium nitride, life testing, power conversion, power transistors, semiconductor device reliability**

I. Introduction

The industry now takes the reliability of silicon transistors for granted, as evidenced by their widespread use in products. This is a result, not only of longstanding experience, but also of the development of credible reliability and qualification methodology. Technology is qualified by running standardized stress tests [1]-[3], and by validating lifetime requirements [4]. This methodology originated from detailed work on the understanding of failure modes, their acceleration and modeling, and a statistical framework to assure a minimum level of quality.

The stress tests, however, were developed more than twenty years ago, with the Joint Electron Device Engineering Council (JEDEC) JESD47 document released in 1995 and the Automotive Electronics Council (AEC) founded in 1994. The qualification procedure has remained essentially unchanged over the years, whereas technology and its uses have changed. For example, power conversion circuitry using hard-switched transistors is now much more widespread. There is also tremendous interest in emerging materials like GaN and SiC for power management applications.

Transistors from emerging materials are being judged as "passing qual" when run through the standardized stress tests described in [1]-[3]. While the standard silicon-based qualification recipe is a worthy manufacturing, quality and reliability milestone, it is not clear what it means for emerging transistors in terms of device lifetime, failure rates and application-relevance. This is because the failure modes, activation energies, and acceleration factors are likely to be different than those used for Si. In addition, the reliability test conditions may not be representative of the product use-case so may not accelerate valid failure mechanisms.

For successful technology adoption, it is important to develop credible reliability and qualification methodology. A successful methodology allows the industry to gain confidence that parts will last for the desired lifetime in the end-use application without many customer returns. It also allows users to easily benchmark components and suppliers.

II. What does qualification mean?

Traditional qualification testing [1]-[3] or "qual" involves many tests, which may be classified into three categories: device, package, and electrostatic discharge (ESD). In this paper, we focus on device-relevant testing. In order for the industry to develop GaN-specific methodology, it is important to understand the fundamentals and assumptions behind traditional qualification. It is also important to know what "passing qual" means. The knowledge may be summarized in the form of the three questions below:

A. *How long is the device qualified for?*

This is typically perceived to be 10 years[*]. The calculation arises by running a 1000h test at a junction temperature of 125°C and extrapolating to a use-temperature of 55°C with an activation energy of 0.7 eV. Additionally, discrete FETs are commonly qualified at 80% of the minimum breakdown voltage, e.g. a 600V FET is qualified at 480V. The 80% value is common practice and not specified by present standards[†].

The ten-year assumption falls apart for power FETs, even those made from Si. Several scenarios are calculated in [6]. The typical use-temperature of power FETs is about 100-110°C. If qualification is run at 150°C, then the non-accelerated time for use at 105°C is only 1.1 yrs, far short of a ten year lifetime. Further, thermal acceleration for silicon assumes an activation energy of 0.7 eV, whereas activation energies for GaN are likely to be different. Recent power GaN literature shows a wide range [7]-[13], from 0.1 eV to 1.84 eV. Voltage acceleration is also used [11],[14]. The variation is expected, due to different failure modes and architectures. Indeed, power GaN transistors comprise both depletion and enhancement mode (d- and e-mode) FETs. Further, d-mode FETs are Schottky [9] or Insulated-gate [12] and are either cascoded with a low-voltage Si FET [12] or an IC [15] for

[*] The traditional calculation results in nine years [1].
[†] The current documentation [3] specifies qualification at the maximum rated DC reverse voltage. An 80% criteria exists in historical documentation [5]

failsafe reasons. E-mode architectures are either junction-gate [11],[16],[17] or recessed insulated-gate [18].

B. *Is the stress-testing representative of actual usage*?

Traditional qualification testing does not consider the switching conditions of power management. High-Temperature Reverse Bias (HTRB) and High Temperature Gate Bias (HTGB) are static tests. High Temperature Operating Life (HTOL) is configured to bias operating nodes and is typically applied on logic and memory devices [19]. Confidence has been built in the qualification methodology for Si devices over the years. This is because the long-standing experience has resulted in a detailed understanding of failure modes, the device design knowledge to avoid them, and the development of proxy tests e.g. substrate current monitoring for Hot-Carrier Injection (HCI) robustness [20]. For emerging technologies, however, switching robustness needs to be proven by running the device under actual-use conditions.

C. *Will there be many field-failures?*

Passing qualification with silicon assumptions means that the lot-tolerant percent defective (LTPD) value is one [1] and failure in time (FIT) rate is established to be less than about 50 (60% confidence level) [21]. The LTPD calculation arises from the statistics of zero fails out of 231 (3 lots x 77) parts. LTPD=1 means that one can state with 90 percent confidence that less than one percent of the parts in a lot will fail when run for the non-accelerated time. The FIT rate calculation arises from the total number of non-accelerated device hours. In practice, for mature processes, the pooling of multiple qualification runs increases the total number of parts and device hours, allowing lower FIT rate and LTPD projections.

In order to get accurate statistics, the acceleration factor needs to be determined for GaN, and the testing needs to be predictive of actual-use conditions. The acceleration factor is also used in early failure testing (ELFR) [1],[22], which is used to assess the infant mortality rate.

III. Application-Relevant Qualification

Both JEDEC and AEC standards are based on sound fundamentals, but lag technology introduction. For example, the discrete power metal-oxide semiconductor field-effect transistor (MOSFET) was developed in the late 1970s [23], but it was not until the early 1990s that JEDEC developed a qualification standard. A standard is not needed to make technology reliable. It is a deep understanding of the technology; its failure modes; and knowledge of testing, qualification and product operation.

The qualification standards [1]-[3] are stress-based, consisting of documented, standardized procedures that prescribe accelerated test conditions. New technology qualification adds a knowledge-based approach, summarized in Fig. 1. This builds upon the existing framework by adding testing and lifetime modeling for GaN specific failure modes, e.g. dynamic on-resistance (dRon) degradation. It also adds new stress tests, to represent application-use.

GaN has shown great promise in many power conversion topologies, e.g. buck and boost converters, bridgeless PFC

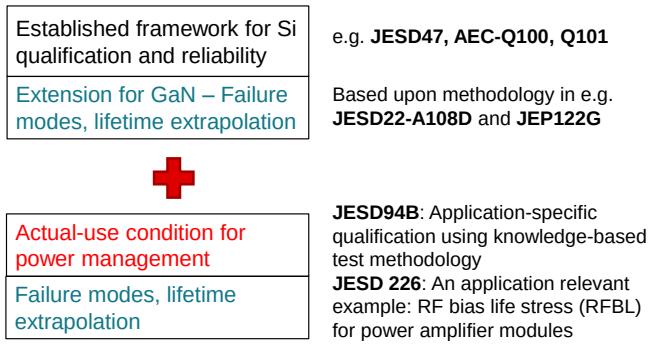

Figure 1: Qualification framework for GaN, built upon JEDEC documentation. The silicon framework is extended for GaN-specific failure modes and application-relevant testing is added.

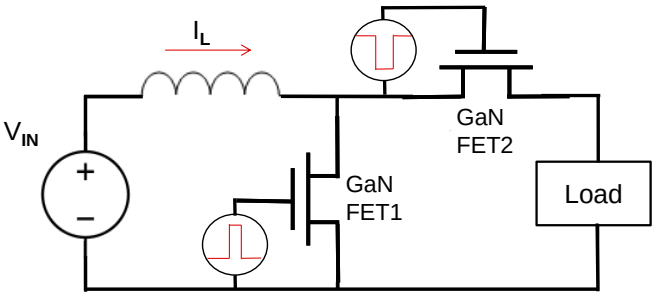

Figure 2: Boost-converter schematic

circuits, inverters, LLC converters etc. The question arises as to how GaN would be qualified for all these end applications. Although JEDEC specifies the need for dynamic testing, it does not prescribe conditions, citing the ever-evolving applications and material sets in our industry [24]. It is not straightforward to assure product-level reliability in a broad sense. In addition to application diversity, products contain many non-GaN parts and the system is not typically designed for accelerated testing, or for running in an oven at 150°C. Running product reliability under accelerated conditions would cause many non-GaN failures, making it difficult to extract useful information. Another difficulty is the energy requirement. In order to run many power converters, one would need to dissipate tens of thousands of watts.

One approach to this problem is to identify an application stress condition common to a class of devices. For example, JESD226 [25] takes such an approach for power amplifier modules (PAMs). The documentation states "*This method is intended to refine and focus the myriad of biasing options down to a standard that can be applied industry-wide so that users of PAMs can gain confidence that devices successfully completing this test method will exhibit adequate reliability for the anticipated use conditions*".

There is a large class of power management products that place similar stresses on the power transistor. To illustrate, consider the hard-switched boost converter schematic in Fig. 2. Teaching waveforms for both the high and low side FETs are shown in Fig. 3, and the different operating regions are described in Table 1. Table 1 also lists the bias stress on each FET. As can be seen, the devices need to withstand the following five types of stresses:

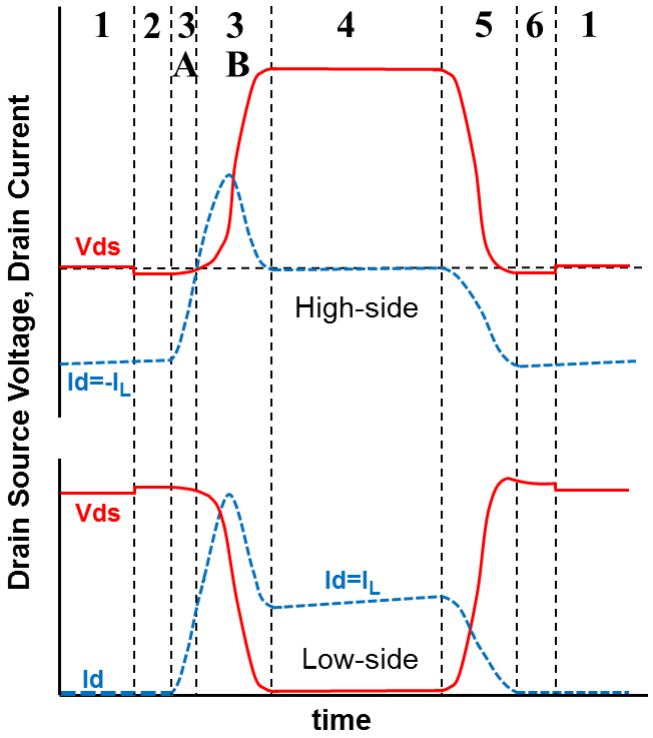

Figure 3: Teaching waveforms for the drain voltage and current for high and low-side FETs of a boost converter. The third quadrant drop is exaggerated.

Table 1: A summary of the waveform regions in Fig. 3, showing the device state and type of stress

		Low-side FET		High-side FET	
	mode	state	stress	state	stress
1	boost	off	drain bias	on	gate bias
2	dead time	off	drain bias	off	third quadrant
3	switching	on	hard switching	off	soft switching
4	charge inductor	on	gate bias	off	drain bias
5	switching	off	soft switching	off	soft switching
6	dead time	off	drain bias	off	third quadrant

- Device off with high drain bias
- Device on with high gate bias
- Third quadrant operation
- Hard-switching turn-on
- Soft-switching turn-off

Breaking down the switching waveform into individual device stresses allows the task of application-relevant device reliability to be simplified. A good qualification regimen will provide all the needed tests without adding unnecessary testing for conditions that are already covered. Of these five stresses, the first two are covered by standard qualification testing (HTRB and HTGB). Third-quadrant operation is likely to be low risk, due to the low voltages involved.

This leaves the switching transitions. Although hard-switching waveforms are well known [26], it may not be clear why the turn-off transistion has been classified as "soft-switched" for the FET. This is because the FET channel is

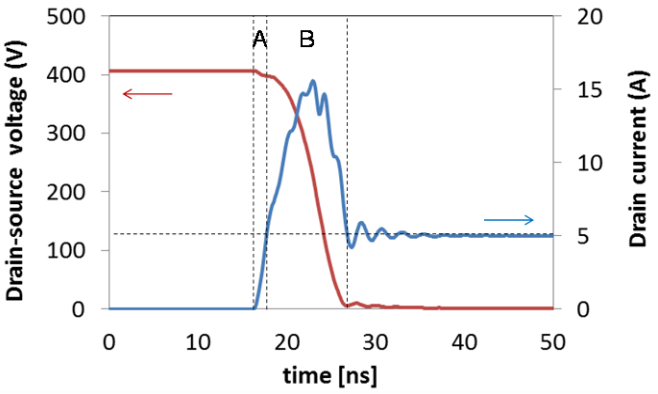

Figure 4: Turn-on hard-switched waveform for the low-side FET in a boost converter. The switching current significantly exceeds the inductor current. Regions "A" and "B" correspond to the hard-switching regions in Fig. 3.

switched off when the drain voltage is low (end of region 4 in Fig. 3). As the transition progresses, the flow of drain current serves to raise the drain voltage by charging the FET output capacitance rather than flowing through the channel.

The turn-on of the low-side FET, however, is hard-switched. In fact, during turn-on, the drain current can significantly exceed the inductor current (region 3B in Fig. 3). This is due to the discharge of the capacitance at the switching node and is exacerbated by the high slew rates offered by GaN. Simulated waveforms of the low-side FET turn-on transition in a 200V:400V boost converter with an inductor current of 5A are shown in Fig. 4. In this case, the peak switching drain current is 15A, about three times the inductor current. The actual FET channel current will be a few amperes higher. This is because during turn-on, the drain capacitance discharges through the channel. During hard-switching, the FET is simultaneously subjected to high currents and voltages, resulting in significant hot carrier generation, for which the device needs to be robust. Even though the transition is short, a few nanoseconds of severe hot-carrier stress per cycle at hundreds of kHz amounts to milliseconds every second.

Further still, large device arrays can experience non-uniform switching. This can crowd the current into the portion of the array that turns on first, and exceed the local rating. High dv/dt switching also can introduce capacitive current into unwanted regions of the device, such as terminations. Stress testing needs to be done, especially to ensure that devices are robust both to the hard-switching hot-carrier stress and to the high slew rates.

IV. HARD-SWITCHING STRESS

It is not difficult to see that hard-switching will result in different stress than off-state operation. Consider Fig. 5, which contrasts high-voltage (480V) off and on (Id=5A) static conditions. A generic GaN FET structure with one gate field-plate and two source field plates [27], was simulated using the Sentaurus Device TCAD package. GaN parameters are from [28]. The simulation shows the electric-field profile to be similar because the space charge due to the current flow is much less than the polarization-induced charge. The main differences are due to hot-carriers.

Hot-carrier effects are illustrated in Fig. 5, showing that at Id=5A, hot electrons are scattered deeper into the buffer layer and that hot-carriers are generated at the ends of the field plates. Deeper scattering of hot electrons into both the buffer layer and dielectrics results in more trapping in these layers and at interfaces. These trapped charges can increase dynamic on-resistance [13]. Holes generated by impact-ionization can enter dielectrics and cause TDDB damage [29]. Many dielectrics have a low valence-band offset to AlGaN, which makes it easier for holes to enter. Hard-switching also causes large instantaneous thermal power dissipation.

Hard-switching testing does not presently form part of the traditional Si-based qualification procedure. If hard-switching testing is not done, it will not be known whether the device is robust to the above effects. It will also not be known whether the device is robust to high dv/dt effects mentioned earlier. The magnitude of the hard-switching stress is considerable, as seen from an I-V locus plot of the turn on switching waveform of Fig. 4, shown later in Fig. 7.

For broad power management use, GaN must also be robust in soft-switching applications. Hard-switching is more stressful than soft-switching, making it likely that a device robust for hard-switching at the desired slew-rates will also be robust for soft switching. There is not much in the literature, regarding electrical overstress seen during soft-switching [30]. It will take time for industry to build up failure knowledge and develop predictive reliability methodology. However, a device passing "qual" *and* hard-switching provides greater assurance of product-level reliability than one passing "qual" alone.

V. HARD-SWITCHING TEST VEHICLE

Breaking down the application-switching profile into its constituent stresses, as shown in table 1, makes it straightforward to use a test vehicle. It removes the complexity of application diversity by qualifying the *intrinsic device* for hard-switching. The use of a test vehicle is in accordance with JESD94B [24], which states "*A test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms*". An ideal test vehicle should be simple, well-known and non-proprietary. In addition, it needs to be energy efficient, since running statistically-relevant sample sizes can easily waste tens of thousands of watts.

A good test vehicle is the well-known "double-pulse" tester, widely used for the characterization of semiconductor switching dynamics. A search revealed its use by 42 different industrial and university groups. It is also the subject of several application notes. In addition, it is also being used for the hard-switching robustness testing of GaN [16]. The latter means that two major companies not only independently realized the need for hard-switching stress-testing for GaN, but also chose the same test vehicle.

The double pulse tester, while used in double-pulse mode for switching dynamics [31], is used in continuous-pulse mode for reliability testing. It's simplicity minimizes system related failures from other components. A high-reliability SiC Schottky diode is used for the high-side device, eliminating high-side drive issues like Common Mode Transient Immunity (CMTI) or unintended shoot-through. The familiar

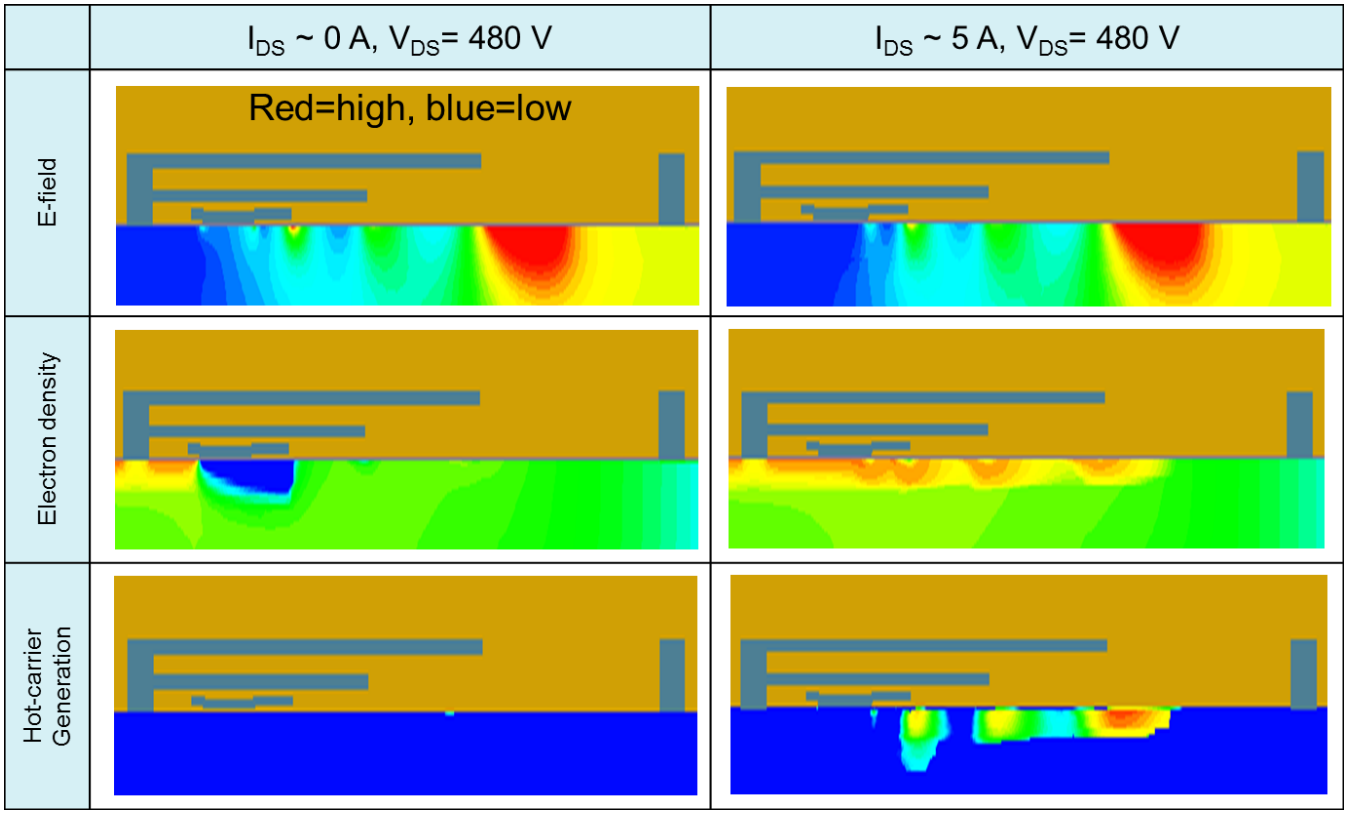

Figure 5: TCAD simulations of a typical GaN FET, showing the effects of current flow at high voltage

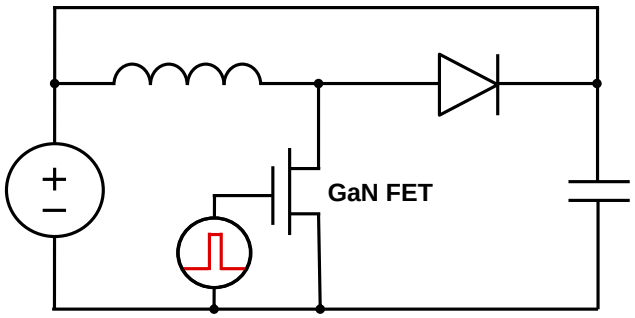

Figure 6: Schematic of the inductive hard-switching test vehicle

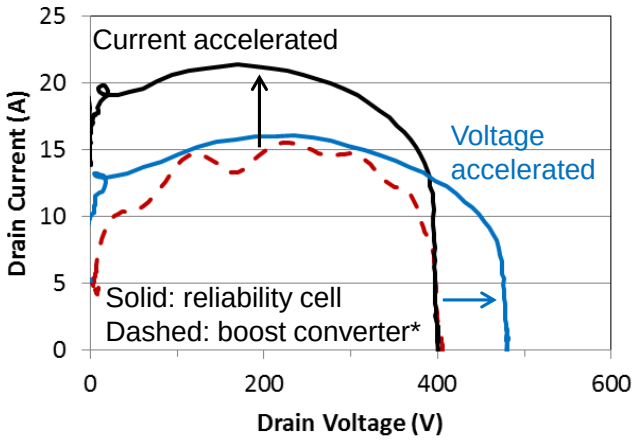

Figure 7: I-V locus showing voltage and current acceleration capability. The boost converter is simulated and the reliability cell data is measured.

schematic shown in [16] is re-drawn in Fig. 6 as a boost-converter with input tied to output. Energy-efficient operation is achieved by using short turn-on pulses. It can stress devices individually at different currents, voltages, temperatures, slew rates and switching frequencies, allowing lifetime prediction studies. It provides application-relevant hard-switching stress as shown in Fig. 7. The figure shows the turn-on I-V loci of the boost-converter of Fig. 4 and the hard-switching test vehicle, showing not only the relevance of the switching-stress profile, but also the ability to provide both voltage and current acceleration. The hard-switching vehicle also subjects the device to the turn-off transition (not shown).

The test vehicle can readily provide information on the two main GaN failure modes: hard-switching robustness and dynamic Rds-on degradation. Poor robustness is easy to detect – the device simply fails catastrophically. Dynamic Rds-on, however, needs to be measured at the timescales of application switching, since the degradation can recover quickly, in microseconds [32]. This means that it needs to be measured in-situ, since stopping the stress will cause significant recovery. The measurement also needs to be high-resolution to resolve milliohm changes. This is done by means of a clamp circuit [33],[34], which allows the use of lower (higher-resolution) voltage ranges on the oscilloscope.

The stress conditions need to be chosen appropriately to ensure acceleration. Dynamic Rds-on has been seen to worsen with hot electrons [17], [35] and temperature [36]. An increase in dRon can reduce efficiency and cause thermal runaway, as seen in [36]. Although many authors report dRon degradation

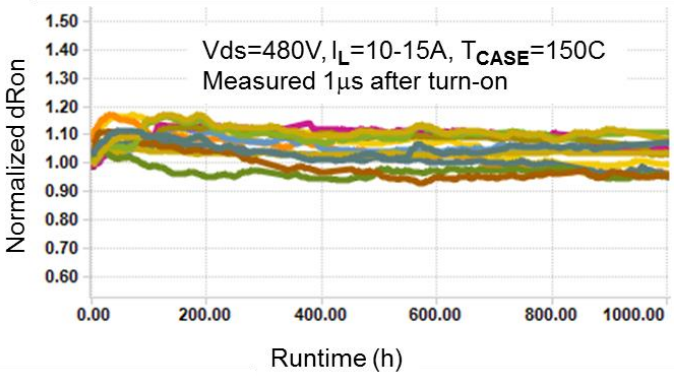

Figure 8: Dynamic Rds-on measured *in-situ* at 150°C in the hard-switching test vehicle under accelerated stress, showing that devices are stable.

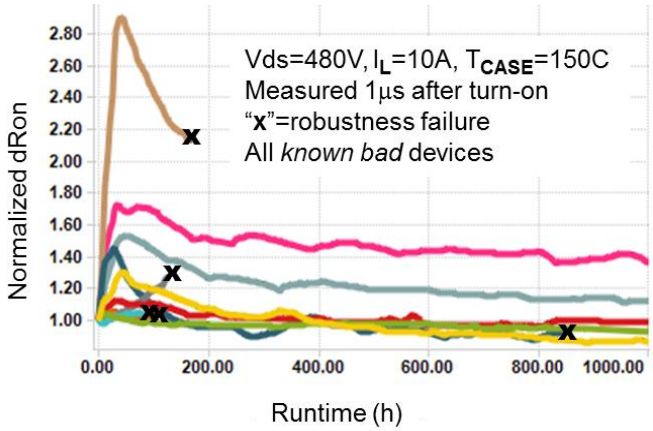

Figure 9: Dynamic Rds-on for *known bad* devices showing that the hard-switching vehicle can discriminate between good (see Fig. 8) and bad devices for both dRon and device robustness.

[12],[13],[16],[17], [32], [36],[37] there is no report of its time evolution under typical qualification stress conditions, e.g. 1000h at 150°C. The time evolution is important to monitor, since device stress can cause an increase in the trap density [38],[39] and a corresponding increase in dRon.

We have run accelerated tests on multiple GaN devices. Tests were run at Vds=480V, 10-15A inductor current, and a case temperature of 150°C in the hard-switching test vehicle. These are stringent test conditions. Devices are robust and show good dRon stability, as shown in Fig. 8. The measurement was done *in-situ* at 150°C. The test vehicle can indeed discriminate between good and bad devices, and to validate this, we have also run *known bad* parts. As shown in Fig. 9, the hard-switching stress is able to detect parts that have poor dRon. The testing also shows that some known bad parts have an increase in dRon followed by a recovery. This phenomena may not be detected by conventional methods. The hard-switching test vehicle is also able to detect parts with poor robustness, as also shown in Fig. 9.

VI. Conclusions

The assurance of product-level reliability is a complex undertaking. The task can be simplified by focusing the biasing conditions of a class of products to a standard. This allows application-relevant stress of the device in a test vehicle. Hard-switching is a fundamental transition for a large

class of power management applications. It is stressful on the device due to hot-carrier, high dv/dt and thermal effects. Devices are not stress-tested for hard-switching during traditional qualification, making it unclear what the outcome means in terms of application-relevance.

A hard-switching reliability test-vehicle based on the familiar double-pulse tester is shown to successfully stress-test GaN devices to ensure both robustness and stable dynamic Rds-on under accelerated conditions. This hard-switching cell can also differentiate between good and bad devices. This testing plays an important role to assure confidence in the product-level reliability of GaN devices.

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REFERENCES

[1] JEDEC Standard JESD47I, "Stress-Test-Driven Qualification of Integrated Circuits," July 2012.
[2] AEC-Q100, Rev. H, "Failure Mechanism based Stress Test Qualification for Integrated Circuits," Sept. 2014.
[3] AEC-Q101, Rev. D1, "Failure Mechanism based Stress Test Qualification for Discrete Semiconductors in Automotive Applications," Sept. 2013.
[4] JEDEC publication JEP122G, "Failure Mechanisms and Models for Semiconductor Devices," Oct 2011.
[5] AEC-Q101 Rev C, "Stress Test Qualification for Automotive Grade Discrete Semiconductors," June 2005.
[6] S. R. Bahl, "A comprehensive methodology to qualify the reliability of GaN products," *Texas Instruments whitepaper*, available at www.ti.com/lit/slyy070 or at www.ti.com/GaN
[7] E. Zanoni *et. al*, "Reliability and failure physics of GaN HEMT, MISHEMT and p-gate HEMTs for power switching applications: Parasitic effects and degradation due to deep level effects and time-dependent breakdown phenomena," *Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, p. 75, 2015.
[8] M. Meneghini *et. al*, "Extensive Investigation of Time-Dependent Breakdown of GaN-HEMTs submitted to OFF-State Stress," *IEEE Transactions on Electron Devices*, v. 62, n.. 8, p. 2549, 2015.
[9] M. Meneghini *et. al*, "Evidence for Temperature-Dependent Buffer-Induced Trapping in GaN-on-Silicon Power Transistors," *International Reliability Physics Symposium (IRPS)*, p. 2E.2.1, 2015.
[10] P. Moens *et. al*, "On the Impact of Carbon-Doping on the Dynamic Ron and Off-state Leakage Current of 650V GaN Power Devices," Proceedings of the *27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, p. 37, 2015.
[11] M. Tapajna, O. Hilt, E. Bahat-Treidel, J. Wurfl, and J. Kuzmik, "Gate Reliability Investigation in Normally-off p-type-GaN cap/AlGaN/GaN HEMTs under Forward Bias Stress," *IEEE Electron Device Letters*, In press, 2016
[12] T. Kikkawa *et. al*, "Commercialization and Reliability of 600 V GaN Power Switches," *International Reliability Physics Symposium (IRPS)*, p. 6C.1.1, 2015.
[13] M. Wespel *et. al*, "High-Voltage Stress Time-Dependent Dispersion Effects in AlGaN/GaN HEMTs," *International Reliability Physics Symposium (IRPS)*, p. CD.2.1, 2015.
[14] A. Lidow, R. Strittmatter, C. Zhou, Y. Ma, "Enhancement Mode Gallium Nitride Transistor Reliability," *International Reliability Physics Symposium (IRPS)*, p. 2E.1.1, 2015.
[15] M. D. Seeman, S. R. Bahl, D. I. Anderson and G. A. Shah, "Advantages of GaN in a High-Voltage Resonant LLC Converter," *Applied Power Electronics Conference (APEC)*, p476, 2014.
[16] S. Kaneko *et. al*., "Current-collapse-free Operations up to 850 V by GaN-GIT utilizing Hole Injection from Drain", Proceedings of *the 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, p. 41, 2015.
[17] I. Hwang *et. al*., "Impact of Channel Hot Electrons on Current Collapse in AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, v. 34, n. 12, p. 1494, 2013.
[18] D. Marcon, Y. Saripalli, and S. Decoutere, "200mm GaN-on-Si epitaxy and e-mode device technology," *International Electron Devices Meeting (IEDM)*, p. 414, 2015.
[19] JEDEC Standard JESD22-A108D, "Temperature, Bias, and Operating Life," June 2005.
[20] C. Hu *et. al*., "Hot-Electron-Induced MOSFET Degradation – Model, Monitor, and Improvement," *IEEE Transactions on Electron Devices*, v. 32, n. 2, p. 375, 1985.
[21] JEDEC Standard JESD85, "Methods for Calculating Failure Rates in Units of FITs," July 2001
[22] JEDEC Standard JESD74A, "Early Life Failure Rate Calculation Procedure for Semiconductor Components," Feb 2007
[23] A. Lidow, T. Herman, H. W. Collins, "Power MOSFET Technology," *International Electron Devices Meeting (IEDM)*, p. 79, 1979.
[24] JEDEC Standard JESD94B, "Application Specific Qualification Using Knowledge Based Test Methodology," Oct. 2015.
[25] JEDEC Standard JESD226, "RF Biased Life (RFBL) Test Method," Jan. 2013.
[26] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics (Second Edition), Springer, 2001.
[27] R. Chu *et. al*,, "1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic ON-Resistance." *IEEE Electron Device Letters*, v. 32, n. 5, p. 632, 2011.
[28] V. Bougrov, M. E. Levinshtein, S. L. Rumyantsev, A. Zubrilov, "Properties of Advanced Semiconductor Materials GaN, AlN, InN, BN, SiC, SiGe," John Wiley & Sons, New York, 2001
[29] S. R. Bahl *et. al*, "New Source-side Breakdown Mechanism in AlGaN/GaN Insulated-Gate HEMTs," Proceedings of the *25th International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, p. 420, 2013
[30] S. R. Bahl and M. D. Seeman, "New Electrical Overstress and Energy Loss Mechanisms in GaN Cascodes," *Applied Power Electronics Conference (APEC)*, p1262, 2015
[31] Cree Application note CPWR-AN09
[32] J. Bocker *et. al*., "Experimental Analysis and Modeling of GaN Normally-off HFETs with Trapping Effects," *17th European Conference on Power Electronics and Applications*, 2015
[33] B. Lu *et. al*., "Extraction of Dynamic On-resistance in GaN Transistors under Soft- and Hard-switching Conditions", *IEEE Compound Semiconductor IC Symposium (CSICS)*, 2011.
[34] N. Badawi and S. Dieckerhoff, "A new method for dynamic Ron extraction of GaN power HEMTs,", *PCIM Europe*, p1010, 2015
[35] M. Meneghini *et. al*., "Impact of Hot Electrons on the Reliability of AlGaN/GaN High Electron Mobility Transistors," *International Reliability Physics Symposium (IRPS)*, p. 2C.2.1, 2012.
[36] C. Liu *et. al*., "Breakthroughs for 650V GaN Power Devices," *IEEE Power Electronics Magazine*, p. 44, Sept. 2015.
[37] K.-Y. Roy *et al*.," A Next Generation CMOS-Compatible GaN-on-Si Transistors for High Efficiency Energy Systems," *International Electron Devices Meeting (IEDM)*, p. 229, 2015.
[38] A. Sozza, *et al*., "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," *International Electron Devices Meeting (IEDM)*, p. 590, 2005.
[39] J. Joh and J. A. del Alamo, "Time Evolution of Electrical Degradation under High-Voltage Stress in GaN High Electron Mobility Transistors," *International Reliability Physics Symposium (IRPS)*, p. 422, 2011.

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