Transformer structures that achieve low EMI with low- and high-side rectifiers

By Bernard Keogh, *System Engineer, High Voltage Controllers, Cork, Ireland*
Max (Jun) Wang, *Application Engineer, Power Delivery, Shanghai, China*

Introduction

Many adapter and charger designs limit the value of the Y-capacitor in the electromagnetic-interference (EMI) filter to limit the leakage current, which in turn improves the sensitivity and performance of touchscreens. Using a smaller Y-capacitor value typically forces the use of larger and higher-loss common-mode (CM) filter chokes in the EMI filter, which adds cost, size and weight to the adapter and reduces its efficiency.

A high-frequency gallium-nitride (GaN) based active-clamp flyback adapter design using TI's UCC28782 controller achieves low CM EMI and complies with EMI standards even when using a small-value Y-capacitor. This article reviews this design's internal transformer structure and its contribution to CM EMI. Analysis also covers how the design should be changed for a low-side rectifier versus a high-side rectifier. Finally, EMI test results are shown for a low-side rectifier design with an appropriate transformer structure.

Sources and causes of CM EMI

CM EMI takes the form of high-frequency current flowing between the AC line (L and N) terminals and earth. A combination of the AC line feed cables and power-supply output cables transmit CM EMI signals generated by a power supply. To avoid interference with nearby radio communications, the CM noise amplitude must be attenuated to meet the required EMI standard limits.

As illustrated in Figure 1, CM currents can flow directly from the power-supply circuit to earth through the parasitic capacitance associated with each switched node. CM currents also flow from primary to secondary via parasitic capacitance between transformer windings. CM performance is very dependent on printed circuit board layout and mechanical construction, as well as the internal construction of the transformer.

Mitigating CM EMI

There are three main ways to suppress CM noise:
- Shield the CM noise generators.
- Arrange the power circuit so that it is balanced for low CM noise, particularly the transformer.
- Add enough filtering to limit the CM noise.

There are two possible arrangements of the transformer's internal winding layers that are balanced for low CM noise. One arrangement uses a high-side synchronous rectifier (SR) and the other method uses a low-side SR.

Figure 1. CM noise current paths
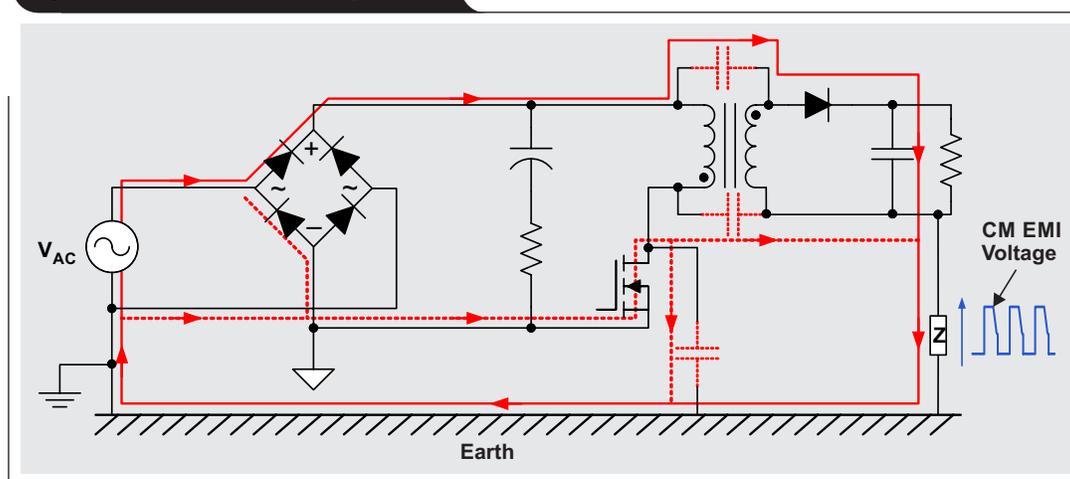
Transformer structure and its impact on CM EMI

Figure 2 is a cross-section of a typical interleaved flyback transformer. Figure 3 shows how this transformer would be connected in-circuit to an active-clamp flyback power stage for both a low- and high-side SR. Figure 3 also shows the induced voltage at both ends of each winding layer. The only significant difference is the polarity of the voltage across the secondary winding—for the high-side SR, it's in phase with the primary voltage, and for the low-side SR, it's out of phase.

Designers often use SR field-effect transistors (FETs) instead of diodes to achieve better efficiency for the rectifier. Placing the SR FET on the low side offers ease of use with simplified driving and sensing, but does come with the trade-off of higher CM noise caused by the polarity inversion of the secondary winding voltage.

Figure 2. Typical interleaved flyback transformer with no shielding or CM noise mitigation
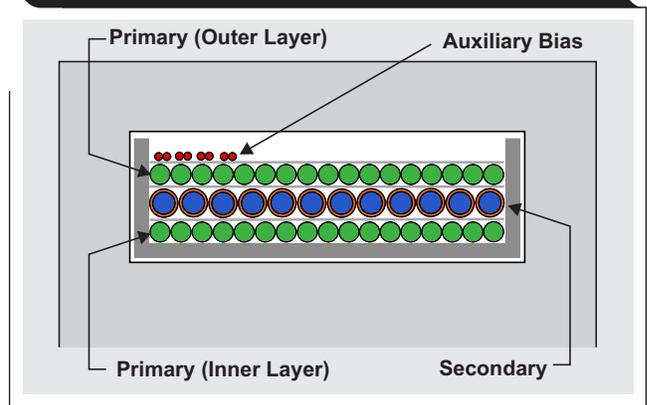
Figure 3. Connection of active-clamp-flyback circuit to the transformer and winding voltages

(a) When using low-side SR
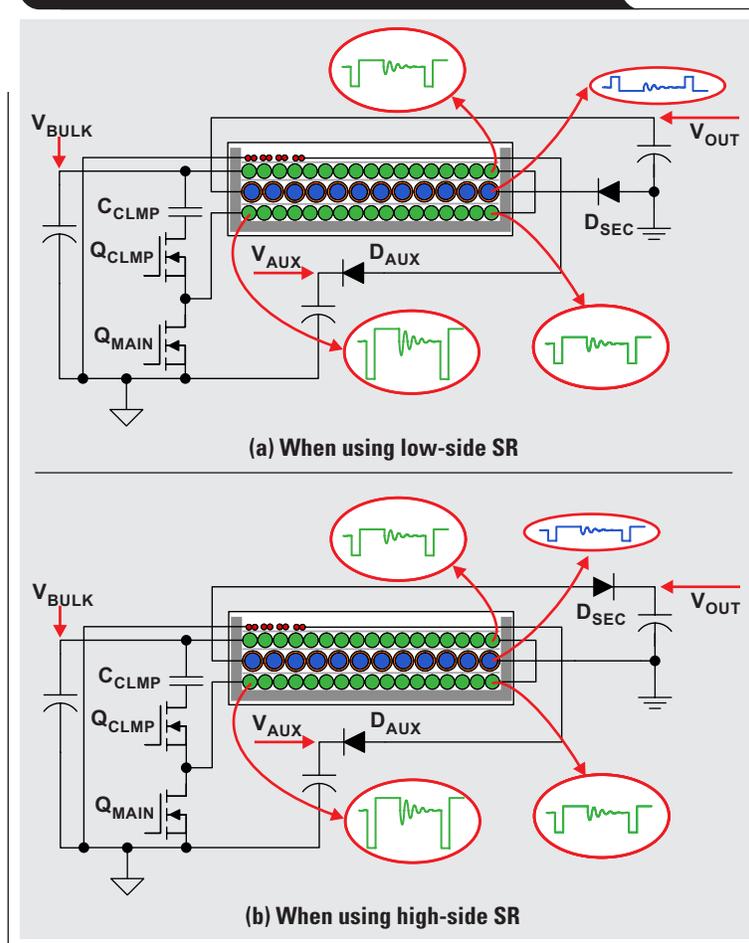
(b) When using high-side SR

Figure 4 shows simplified transformer structures by replacing each winding layer with a rectangular block that has voltage equal to the average of the voltage across the layer's width. Also shown is the parasitic capacitance between each layer and the voltages across each capacitor. In the case of the low-side SR, the secondary voltage swings in the opposite direction versus the primary layers, having a net additive effect on the CM voltage between the primary and secondary layers.

The high-side SR has an advantage because all voltages have the same polarities, which provides some degree of net cancellation by reducing the net primary-to-secondary CM voltage. The degree of natural CM cancellation with the high-side SR depends on the relative voltage on the primary and secondary layers, the number of winding layers, and the arrangement of those layers.

Transformer CM EMI mitigation for low- versus high-side SRs

Reducing the net CM voltage as close as possible to zero requires a slight modification of the transformer structures, as shown in Figure 5a. The secondary winding is sandwiched between two auxiliary layers for shielding and CM balance. The outer primary-referenced auxiliary bias

winding (shown in red) is moved inside, in between one of the primary-to-secondary interfaces. The auxiliary bias layer has the same number of turns as the secondary layer, but is typically wound with thinner wire because its required current rating is much lower. Winding the auxiliary layer with several parallel strands of thinner wire completely fills the layer, enabling the auxiliary layer to act as a shield and preventing any CM noise from coupling from the outer primary layer to the secondary layer.

For the high-side SR, positioning an identical auxiliary layer in between the other primary-to-secondary layer interface—this is a dummy CM balance winding—is again meant to shield CM noise from the main primary winding. But since the CM balance winding has the same number of turns as the secondary layer and the auxiliary bias layers, CM balance is achieved for the secondary layer. The secondary layer is effectively shielded by two auxiliary layers, one on either side, and with exactly the same voltage induced on all three layers. Since all three layers have the same induced voltage, there is close to zero CM current flowing into the secondary layer. This structure should deliver very low CM EMI and require a smaller external CM filter size.

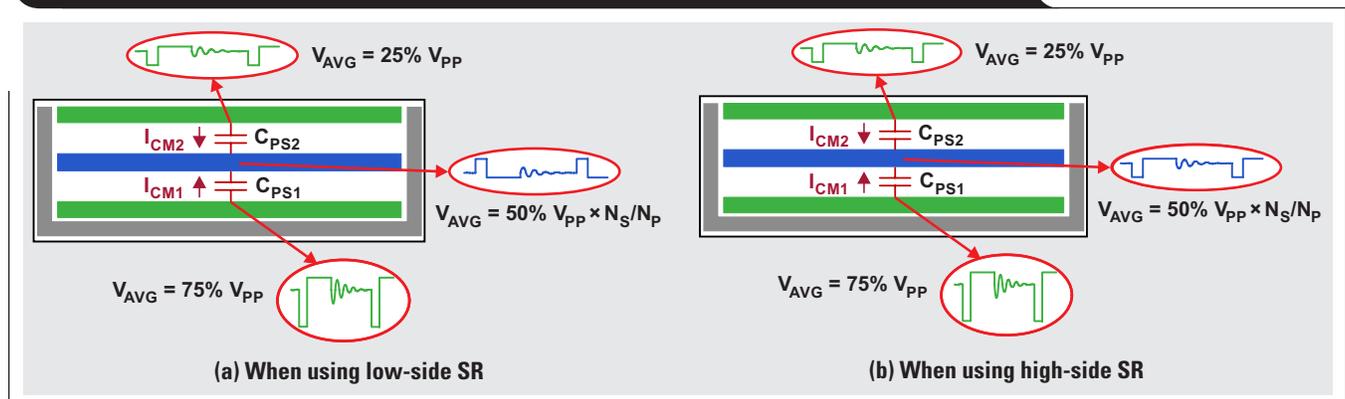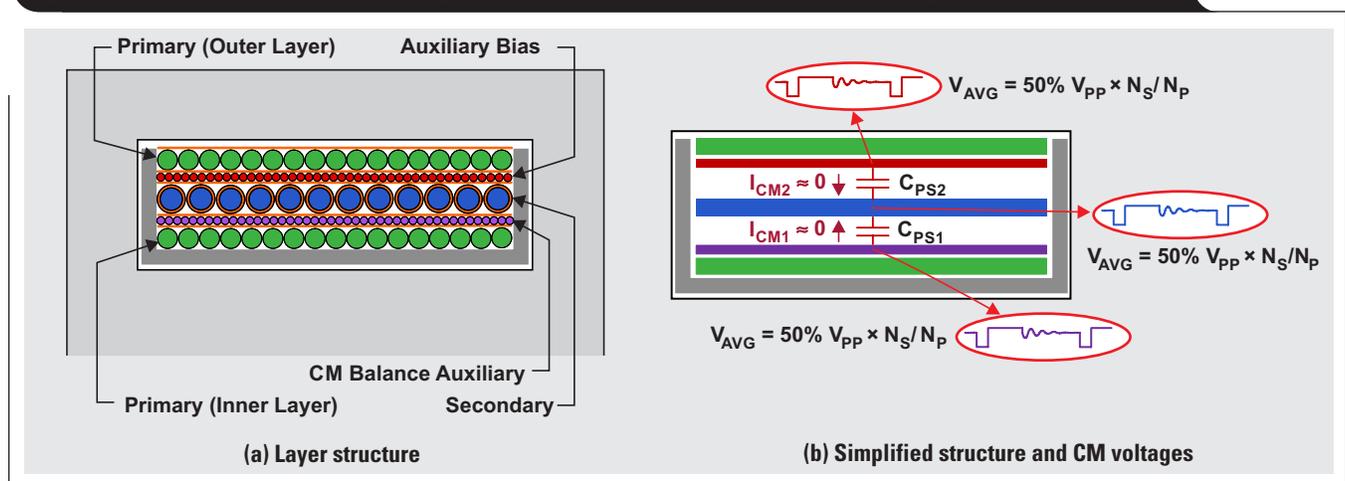**Figure 4. Simplified active-clamp flyback transformer structure and CM voltages**

(a) When using low-side SR   (b) When using high-side SR

Figure 5. Improved active-clamp flyback transformer with internal shielding and CM balance

(a) Layer structure   (b) Simplified structure and CM voltages

The simplified cross-section in Figure 5b shows the equivalent layers as capacitor plates, with the average voltage on each plate. Also shown is how CM current flowing from each auxiliary layer to the secondary layer is approximately zero, since both sides of each parasitic capacitance have the same voltage.

The low-side SR uses the same structure. In this case, however, since the auxiliary and secondary layers have opposite polarities, the net CM signal is additive. The auxiliary CM balance layer that is positioned in between the other primary-to-secondary interface is again wound with multiple parallel strands to fill the layer for shielding. But the auxiliary CM balance layer requires more turns in order to cancel the effect of CM current flow between the auxiliary bias layer and the secondary layer.

Equation 1 demonstrates how to calculate the nominal ideal number of turns in the cancellation layer. The secondary-layer polarity inversion is included in the equation, and the final result clearly shows the additive effect. In this case, with a 5T secondary layer and a 5T auxiliary bias layer, the cancellation layer requires 15T. This is considerably higher than the 5T cancellation layer required for the high-side SR case. In practice, the auxiliary cancellation layer usually requires more turns than

the ideal value predicted by Equation 1, and some iteration is often required find the optimum value.

$$
\begin{aligned}
N_{cancel} &= N_{aux\_bias} - \left(-N_{sec}\right) - \left(-N_{sec}\right) \\
&= N_{aux\_bias} + 2N_{sec}
\end{aligned}
\tag{1}
$$

Designers can adopt many other structures, beyond what is shared in Figure 5, to achieve a similar CM balance for other applications. The final structure will depend on constraints like cost (since the cancellation layers add to the transformer's manufacturing cost), leakage inductance (extra layers in between the primary-to-secondary layers increase leakage inductance), the transformer's parasitic capacitance and the repeatability of the solution in high-volume manufacturing.

EMI test results

Figures 6 and 7 show conducted EMI results taken on the final design for the low-side SR. Note that the result remains under European Norm (EN) 55032 Class B limits with good margin. The inherently low CM EMI from the balanced transformer structure enables the use of a small value Y-capacitor for the CM EMI filter—only 330 pF—yet still meets EN 55032 Class B EMI limits with margin. The high-side SR can achieve a similar result, again due to the CM-balanced transformer structure.

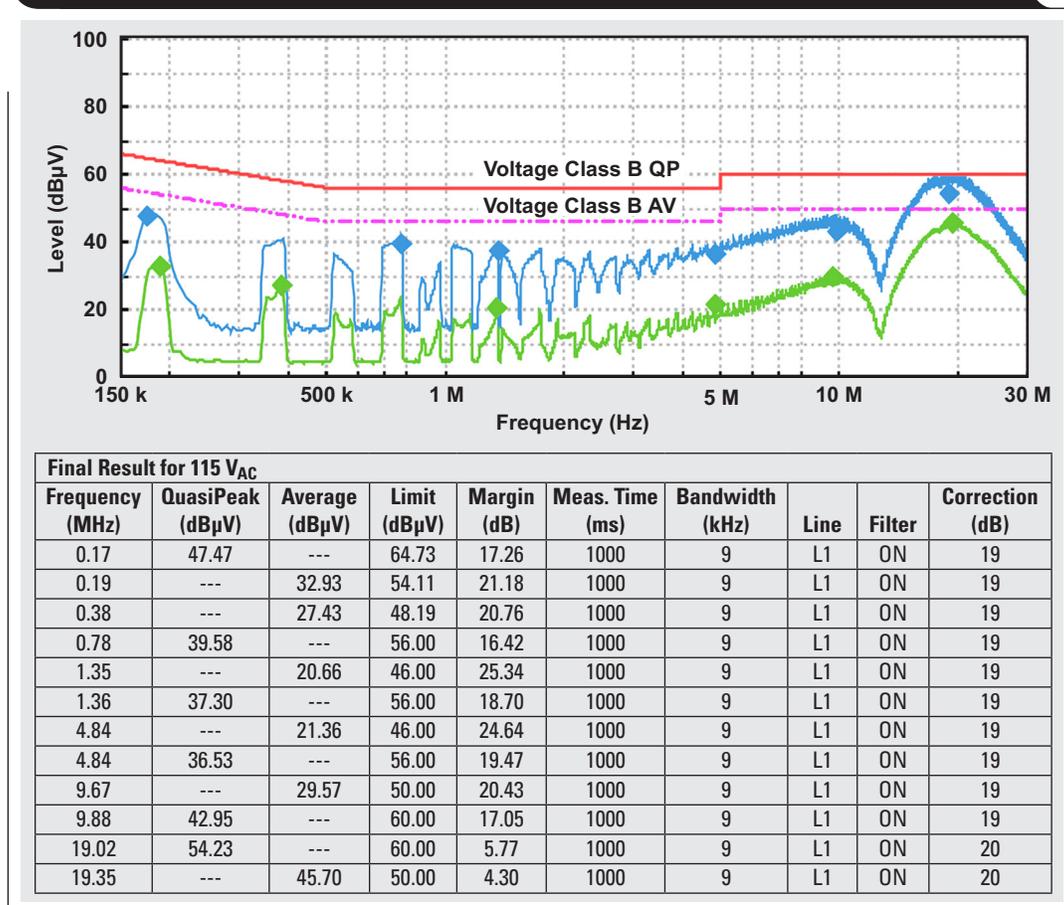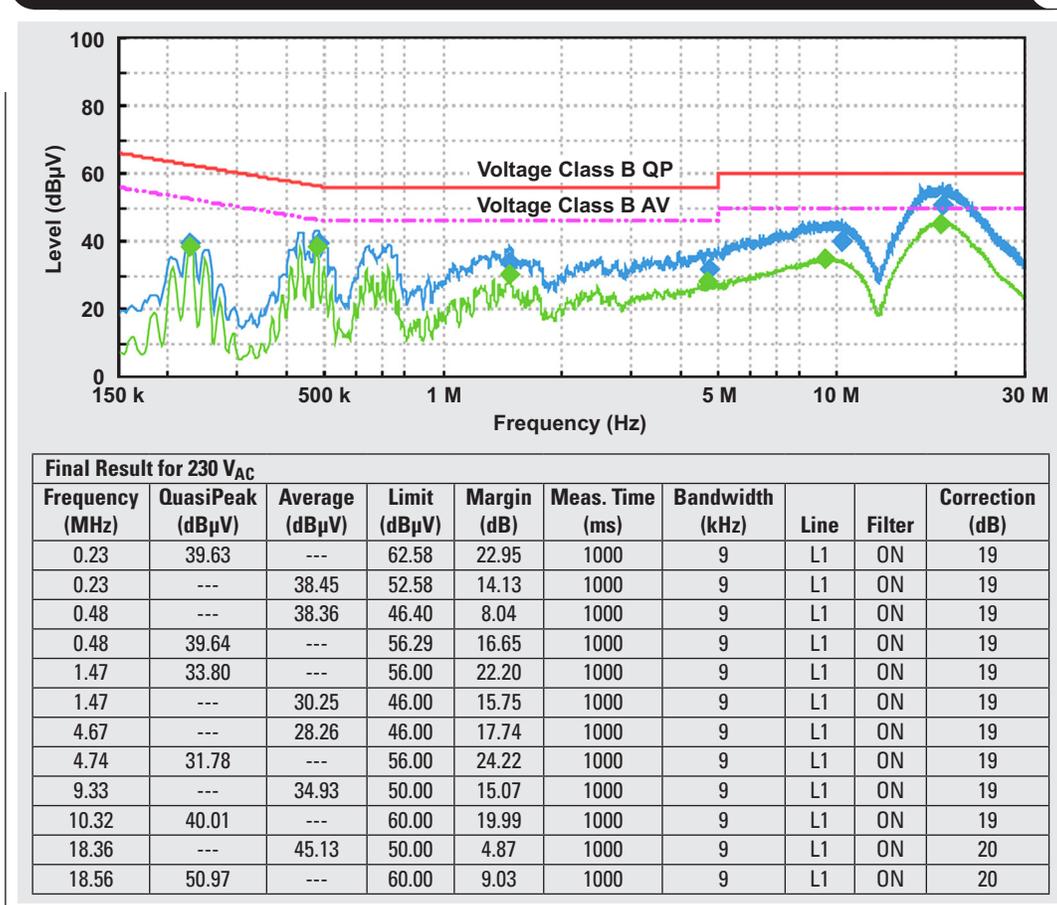**Figure 6. Final conducted EMI result for a low-side SR at a 65-W load for 115 V$_{AC}$**

Final Result for 115 V$_{AC}$									
Frequency (MHz)	QuasiPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Meas. Time (ms)	Bandwidth (kHz)	Line	Filter	Correction (dB)
0.17	47.47	---	64.73	17.26	1000	9	L1	ON	19
0.19	---	32.93	54.11	21.18	1000	9	L1	ON	19
0.38	---	27.43	48.19	20.76	1000	9	L1	ON	19
0.78	39.58	---	56.00	16.42	1000	9	L1	ON	19
1.35	---	20.66	46.00	25.34	1000	9	L1	ON	19
1.36	37.30	---	56.00	18.70	1000	9	L1	ON	19
4.84	---	21.36	46.00	24.64	1000	9	L1	ON	19
4.84	36.53	---	56.00	19.47	1000	9	L1	ON	19
9.67	---	29.57	50.00	20.43	1000	9	L1	ON	19
9.88	42.95	---	60.00	17.05	1000	9	L1	ON	19
19.02	54.23	---	60.00	5.77	1000	9	L1	ON	20
19.35	---	45.70	50.00	4.30	1000	9	L1	ON	20

Figure 7. Final conducted EMI result for a low-side SR at a 65-W load for 230 V$_{AC}$

Final Result for 230 V$_{AC}$									
Frequency (MHz)	QuasiPeak (dBμV)	Average (dBμV)	Limit (dBμV)	Margin (dB)	Meas. Time (ms)	Bandwidth (kHz)	Line	Filter	Correction (dB)
0.23	39.63	---	62.58	22.95	1000	9	L1	ON	19
0.23	---	38.45	52.58	14.13	1000	9	L1	ON	19
0.48	---	38.36	46.40	8.04	1000	9	L1	ON	19
0.48	39.64	---	56.29	16.65	1000	9	L1	ON	19
1.47	33.80	---	56.00	22.20	1000	9	L1	ON	19
1.47	---	30.25	46.00	15.75	1000	9	L1	ON	19
4.67	---	28.26	46.00	17.74	1000	9	L1	ON	19
4.74	31.78	---	56.00	24.22	1000	9	L1	ON	19
9.33	---	34.93	50.00	15.07	1000	9	L1	ON	19
10.32	40.01	---	60.00	19.99	1000	9	L1	ON	19
18.36	---	45.13	50.00	4.87	1000	9	L1	ON	20
18.56	50.97	---	60.00	9.03	1000	9	L1	ON	20

A high-line input voltage (230 V$_{AC}$) is typically the EMI bottleneck, given the lack of "free" frequency dithering as a result of a reduced bulk capacitor voltage ripple and the consequent reduction in switching frequency variation over the AC half cycle. The UCC28782's built-in frequency dithering at high line helps reduce EMI and increase the margin of passing, further supporting the flexibility to use a low-value Y-capacitor. As Figures 6 and 7 indicate, both the high and low lines achieve similar pass margins.

Conclusion

A flyback transformer's structure does affect CM EMI. For the best CM EMI cancellation, the transformer's structure must be adjusted according to the location of the rectifier. Studying how the rectifier location impacts CM EMI generation reveals how the transformer structure must change to reduce CM EMI for both cases. The fundamentally lower CM noise signal for a high-side SR enables the use of a simpler structure inside the transformer compared to a design using a low-side SR.

The inherently low CM EMI performance of this flyback transformer structure enables designers to use a small-value Y-capacitor in the EMI filter. This is a big benefit for touchscreen applications, which require low leakage current in order to improve their resolution and sensitivity.

References

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3. Bob Mammano and Bruce Carsten, "Understanding and Optimizing Electromagnetic Compatibility in Switchmode Power Supplies," TI Power Supply Design Seminar SEM1500 (SLUP202), November 2002.

Related Web sites

Product information:
UCC28782
UCC28782 active-clamp-flyback evaluation module
UCC28780
UCC28780 ZVS flyback reference design

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