Using a high-frequency switching regulator without a linear regulator to power a data-converter system

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Introduction

Test and measurement applications need faster sampling and data-conversion rates. Since supply-voltage noise affects clock-jitter performance, the need for a quiet rail is more important than ever. Linear regulators or low-dropout regulators (LDOs) can remove ripple noise, but at the expense of efficiency, board space, cost and other penalties.

This article shows how a high-frequency DC/DC converter offers low ripple noise and good power-supply ripple rejection compared to a 400-kHz DC/DC converter followed by an LDO. Also Included is a comparison of each solution's efficiency, board space, transient response and cost.

Selecting the application

Two different power supplies were designed and built to show the trade-offs of a high switching-frequency DC/DC converter and a traditional DC/DC converter post-regulated with an LDO. For both designs, the input voltage is 12 V, the output voltage is 1.8 V, and the output current is 4 A. The goal was to demonstrate whether a low-noise DC/DC converter switching at a high frequency will eliminate the need for an LDO by blocking the noise to the data-converter system. No other noise-reducing techniques (such as additional bypass capacitors or power-supply filters) were implemented to further reduce the noise.

The comparison features two DC/DC converters from Texas Instruments: A two-phase TPSM84A22 power module, switching at 4-MHz and set to a 1.8 V output; and a LMZ31506 synchronous-buck power module, switching at 400-kHz and set to 2.0 V along with the 4-A TPS7A85 LDO post-regulating from 2.0 V to 1.8 V. For discrete DC/DC converter designs without an integrated inductor, see the 10-A TPS54A20 and 6-A TPS54622, which are integrated inside the TPSM84A22 and LMZ31506 modules, respectively.

Solution size comparison

When comparing the board designs side by side, the 4-MHz design shown in Figure 1 has a clear size advantage over the traditional 400-kHz with the LDO design shown in Figure 2. Even though both power modules are the same size, the 400-kHz solution is 3.3-times larger. Because the 4-MHz design switches at a faster frequency, the size of the inductors and capacitors are small enough to integrate completely within the module's package.

Obviously, switching at a higher frequency reduces the total component area. When designers working with data-converter systems face height or area constraints, the higher switching-frequency capability of the 4-MHz design is advantageous. Table 1 shows the area and height results.

Table 1. Solution area and height comparison

Design	Total Area (mm^2)	Maximum Height (mm)	Module Size (mm)	LDO Size (mm)
400 kHz + LDO	640	2.8	9 × 15 × 2.8	3.5 × 3.5
4 MHz	195	2.3	9 × 15 × 2.3	N/A

Figure 1. 4-MHz design

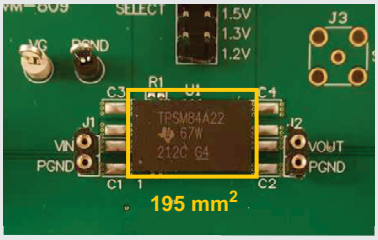
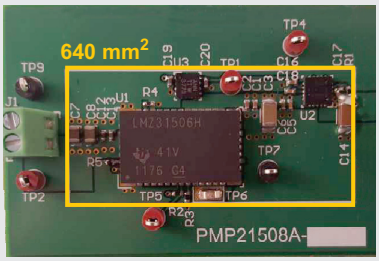


Figure 2. 400-kHz design with an LDO



Power-supply noise affecting data-converter systems

For data-converter systems, the signal-to-noise ratio (SNR) shown in Equation 1 relates to the sampling frequency (f_{MAX}) and the jitter on the sampling clock (t_{JITTER}). Random fluctuations in the sampling clock will cause time-sampling errors that corrupt the conversion signal. Another factor affecting data-converter system performance is the power-supply rejection of the data converter itself. Most analog-to-digital converters (ADCs) have a power-supply rejection of about 40 dB to 60 dB in the 100-kHz to 1-MHz range. Therefore, a 14-bit ADC powered by a switching regulator that has an output voltage ripple of 40 mV would degrade the ADC's performance to 12 bits. With improvements in technology that allow faster switching frequencies, the additional LDO may not be necessary.

$$SNR = 20 \log (1/2\pi \times f_{MAX} \times t_{JITTER}) \quad (1)$$

Efficiency comparison

The efficiency of a DC/DC converter is one of the more important attributes to consider when designing a power supply. Excessive heat can affect the measurement accuracy of data-converter systems; some applications such as semiconductor test equipment must rely on unique cooling schemes, like top-side and liquid-cooled heat sinks. Table 2 shows the typical power-loss attributes for a buck converter.

Table 2. Buck converter efficiency components and factors

Loss Attributes	Factors
MOSFET driving loss	Function of gate charge, drive voltage, switching frequency
MOSFET switching loss	Function of V_{IN}, I_{OUT}, MOSFET rise/fall time, switching frequency
MOSFET resistance	$I^2 \times R_{DS(on)}$
Inductor losses	$I^2 \times$ DC resistance + AC core loss
Capacitor losses	$I^2_{RMS} \times$ equivalent series resistance (ESR)
IC loss (Iq)	Check data sheet for Iq when the IC is operating

In addition to higher inductor losses, fast-switching DC/DC converters also have higher MOSFET driving and switching losses. The additional LDO with the 400-kHz design dissipates a significant amount of power, making the 4-MHz design much more attractive at higher currents. According to Table 3, the 4-MHz design saves about 1 W of power compared to the 400-kHz design with the LDO, while delivering 7.2 W. At lighter loads, the traditional 400-kHz design has better performance. The break-even point is about 1.5 A, which depends on the specific modules and linear regulator chosen. Both power supplies operate in continuous conduction mode (CCM), which is best when powering data converter systems.

Table 3. Efficiency comparison

400-kHz Design with LDO			4-MHz Design			Difference	
I_{OUT} (A)	Efficiency	P_{Loss} (W)	I_{OUT} (A)	Efficiency	P_{Loss} (W)	Difference (%)	Difference (W)
0	0.0%	0.27	0	0.0%	0.61	0.0%	0.34
0.4	67.6%	0.35	0.4	54.2%	0.61	–13.4%	0.27
1	76.6%	0.55	1	73.9%	0.64	–2.7%	0.09
2	79.7%	0.91	2	83.3%	0.73	3.5%	–0.19
3	79.7%	1.37	3	85.9%	0.89	6.2%	–0.47
4	77.2%	2.06	4	86.8%	1.10	9.6%	–0.96

Thermal comparison

Power losses are converted into heat and are derived mainly from the integrated circuit (IC) and inductor within the module. Table 4 shows the temperature rise for each inductor and IC. Higher temperatures increase the MOSFET on-resistance and inductor direct-current resistance (DCR), compounding a decrease in efficiency. When comparing the thermal images for each design in Figures 3 and 4, operating at a full 4-A load, it is easy to discern the advantage of the 4-MHz design. Although the size of each power module is identical, the output current ratings for the 4-MHz and 400-kHz modules are 10 A and 6 A, respectively.

Table 4. Thermal comparison at full load

Design	Peak Module Temperature	Peak LDO Temperature
400 kHz + LDO	57.8°C	51.6°C
4 MHz	37.1°C	N/A

Figure 3. Thermal image of 4-MHz design

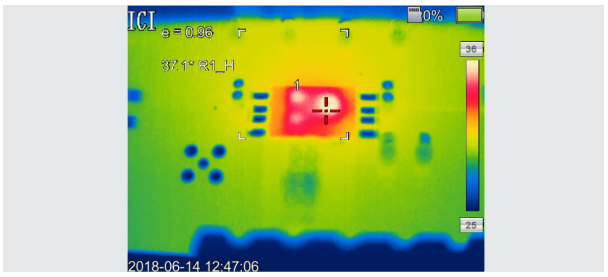
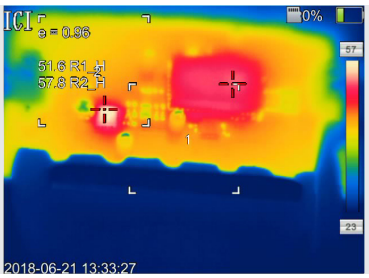


Figure 4. Thermal image of 400-kHz design with LDO



Transient-response performance

Figures 5 and 6 show the load-transient waveform for each design. Each design was subjected to a 3-A load step with a 1-A/µs slew rate. The 4-MHz design clearly has an advantage with a high 400-kHz loop bandwidth, as compared to the 400-kHz design with a 40-kHz loop bandwidth.

Figure 5. Transient response of the 4-MHz design

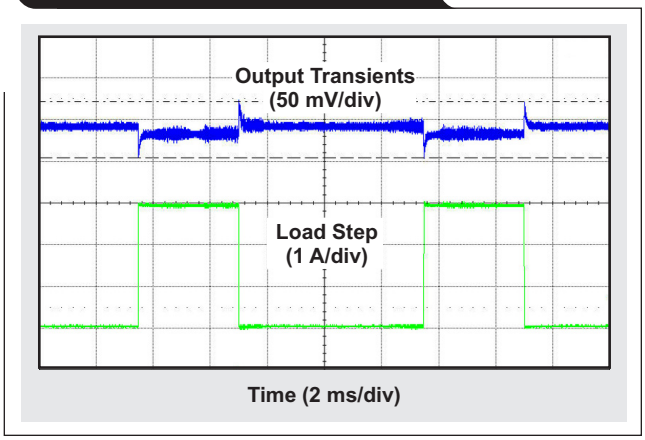
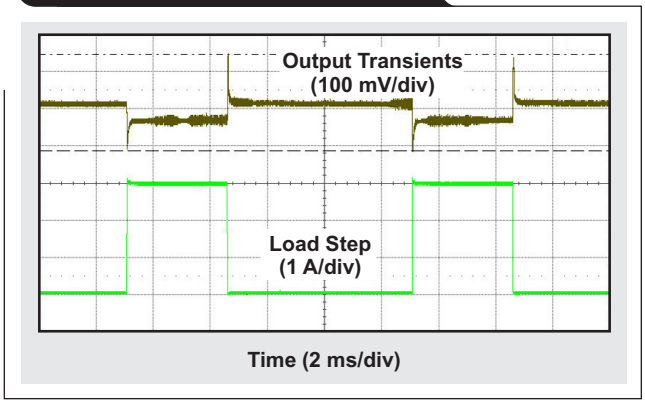


Figure 6. Transient response of the 400-kHz design with LDO



A faster switching frequency and faster loop bandwidth enabled a much faster transient-response time and reduced voltage undershoots and overshoots. Table 5 shows the results.

Table 5. Transient-response summary at 1 A/µs with a 1-A to 4-A transition

Design	Undershoot	Undershoot Response	Overshoot	Overshoot Response
400 kHz + LDO	113 mV	15 µs	146 mV	20 µs
4 MHz	31.5 mV	20 µs	35.5 mV	25 µs

Output ripple comparison

The output-ripple waveforms in Figures 7 and 8 show that the 4-MHz design has an advantage of 4.8 mV in peak-to-peak output voltage ripple compared to the 400-kHz design with the LDO, based on the amount of capacitance used for each design. A 5-mV ripple improvement is significant in data converter systems, especially without the LDO.

The varying ripple on the 400-kHz waveform is common at the output of LDOs operating at a full load due to the DC bias effect on the ceramic capacitor at its output. Adding additional or higher-value capacitors will mitigate the DC bias effect.

Figure 7. Voltage ripple of the 4-MHz design

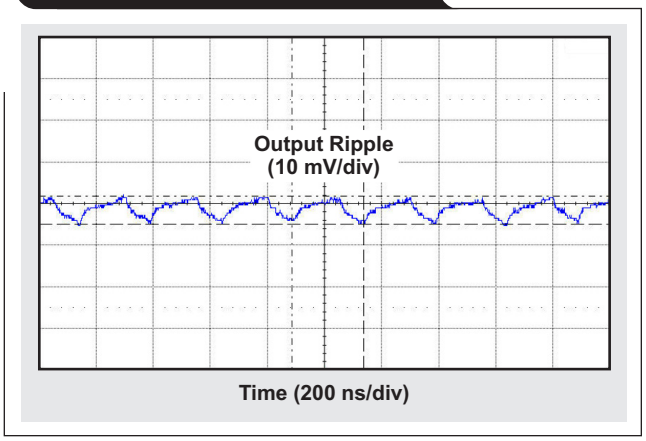
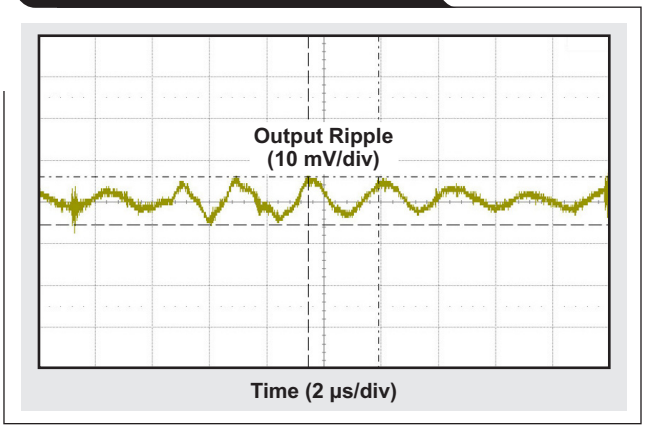


Figure 8. Voltage ripple of the 400-kHz design with LDO



Power-supply ripple rejection and output-voltage noise

Power-supply rejection ratio or power-supply ripple rejection is a measure of a circuit's power-supply rejection expressed as a log ratio of output noise to input noise. For LDOs, power-supply ripple rejection measures the regulated output-voltage ripple compared to the input-voltage ripple over a wide frequency range (10 Hz to 1 MHz is common), expressed in decibels (dB) with the output voltage noise expressed in microvolts (µV). Output-voltage noise is a very critical parameter in test and measurement, communication system, and radio-frequency (RF) applications.

Each design was measured with a spectrum analyzer to compare the output-voltage noise. In Figure 9, the 400-kHz design shows spikes at the harmonics of the 400-kHz switching pulse, and the spurs have a peak noise of only 14.9 µV. The 4-MHz design in Figure 10 shows voltage spikes at 2 MHz, 4 MHz and 8 MHz; however, the peak noise is 135 µV, which is quite low for a switching regulator. When considering the 12-bit ADC12DJ3200 RF-sampling ADC, the output-voltage noise of the 4-MHz design is low enough to negate the need for an LDO.

Cost comparison

Table 6 shows that the cost of the 400-kHz module and LDO are higher at the suggested resale price on the TI Web site. The 400-kHz design will also require additional components to support the module and LDO, such as input and output capacitors, as well as their associated surface-mount manufacturing costs.

Table 6. Cost comparison

Design	Module Cost	LDO Cost	Additional Components	Solution Cost
400 kHz + LDO	$5.45 at 1 Ku	$3.50 at 1 Ku	$0.60 at 1 Ku	$9.55 at 1 Ku
4 MHz	$7.50 at 1 Ku	N/A	N/A	$7.50 at 1 Ku

Figure 9. Noise plot for the 400-kHz design with LDO

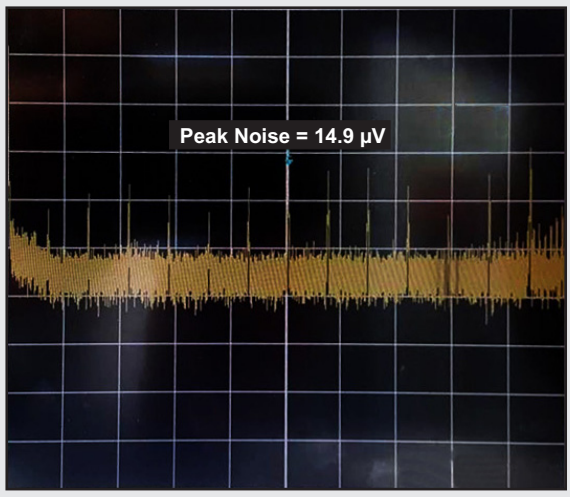
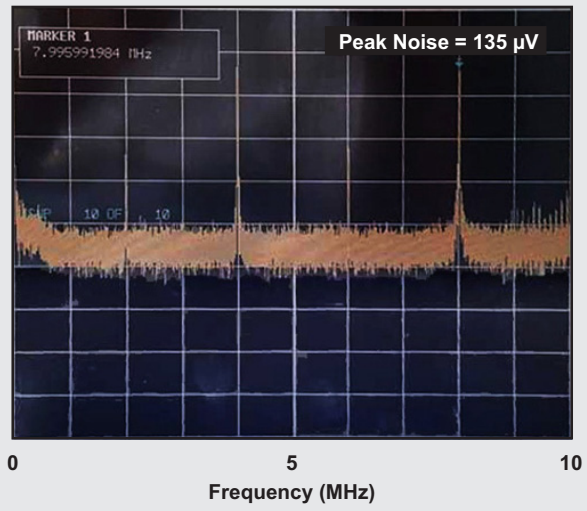


Figure 10. Noise plot for the 4-MHz design



Conclusion

There are trade-offs to designing with high-frequency switching converters and modules. But when an LDO is added, many of those advantages disappear. Table 7 summarizes the comparisons between each design. The 4-MHz design is the clear winner, which shows that high-switching-frequency converters can actually block noise from the critical frequency range of data-converter systems.

Table 7. Comparison summary

Attribute	400-kHz Design with LDO	4-MHz Design	Advantage
Size	640 mm^2	195 mm^2	4-MHz design
Full-load efficiency	77.2%	86.8%	4-MHz design
Power loss	2.06 W	1.1 W	4-MHz design
IC temperature	57.8°C + 51.6°C	37.1°C	4-MHz design
Transient over-shoot	146 mV	35.5 mV	4-MHz design
Ripple voltage	11.5 mV	6.7 mV	4-MHz design
Output voltage noise	14.9 µV	135 µV	400-kHz design
Solution cost	$9.55 at 1 Ku	$7.50 at 1 Ku	4-MHz design

By using a higher-frequency power module or DC/DC converter, the LDO can be left off the board and the efficiency, thermal, ripple, and cost benefits can be realized while maintaining the data-converter resolution on the circuit board. To further reduce noise, bypass capacitors or power-supply filters can be added.

References

1. Thomas Neu, “Designing a modern power supply for RF sampling converters,” Texas Instruments Analog Applications Journal (SLYT720), 2Q 2017.

Related websites

Product information:
TPSM84A22
TPS54A20
LMZ31506
TPS54622

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