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Contents

Introduction 3

Automotive

Two-step calibration of sensor signal conditioners 4
 Mixed-signal integrated circuits (ICs) for sensor signal conditioning are widely used today in sensor applications. This article examines the calibration of sensor signal-conditioning algorithms implemented in signal conditioners that transmit data in analog form. The calibration scheme described addresses the analog signal-chain errors introduced by the analog circuits in front and back of the digital circuits.

Industrial

Designing an anti-aliasing filter for ADCs in the frequency domain 7
 When developing a data acquisition (DAQ) system, it is usually necessary to place an anti-aliasing filter before the ADC to rid the analog system of higher-frequency noise and signals. Typically, evaluations of this type of circuit consist of the offset, gain, linearity, and noise. This article evaluates the system's signal path from a frequency perspective and describes the relationship of six frequencies that impact the design of a DAQ system.

Tips and tricks for high-speed, high-voltage measurement 10
 High-speed, high-voltage circuits that use gallium nitride (GaN) and silicon carbide (SiC) power FETs are posing measurement challenges to power-conversion designers. This article describes a few probe circuits and methods to measure probe performance. Included is an embedded-probe circuit that minimizes loading and can safely measure voltages up to 600 V with rise times as short as 3.5 ns.

Communications

JESD204B multi-device synchronization: Breaking down the requirements 15
 There are numerous applications like phased-array radars, distributed antenna arrays, and medical imaging machines that make use of synchronized signal chains. Most systems that require multiple synchronized signal chains also require synchronization of ADCs and DACs. This article describes the four basic requirements for synchronization of JESD204B ADCs and DACs. Included are two examples of clocking implementations that show how to achieve conditions for overall system synchronization.

Advanced linear equalization in multi-gigabit systems 20
 The use of linear equalization in the analog domain still plays an important support role in the realm of high-speed signal conditioning. This article evaluates the equalization techniques used to restore balance between the various frequency components to ensure robust error-free operation across a broad spectrum of serial protocols, including 10GbE Ethernet, PCIe and SAS. Also described is the concept of link training and adaptive signal conditioning.

Personal Electronics

Stabilizing difference amplifiers for headphone applications 24
 Stabilizing headphone amplifiers is a unique challenge because of the difference-amplifier topology and the requirements for low output impedance, low distortion, low noise, and high CMRR. This article presents an enhanced amplifier solution that provides stable operation into capacitive loads without increasing the output impedance at low frequencies or degrading the common-mode rejection.

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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these “how-to” articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

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Two-step calibration of sensor signal conditioners

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Introduction

Mixed-signal integrated circuits (ICs) for sensor signal conditioning are widely used today in sensor applications such as pressure, temperature and position monitoring. In these signal conditioners, the conditioning of the output signal from the sense element is performed with mixed-signal circuits, which are a combination of analog and digital circuits. Moreover, the actual conditioning of the sense-element signals is implemented in the digital domain. The conditioned signal is the output of the sensor signal conditioner. The sensor output is transmitted to a control or monitoring system either in analog or digital form. If an analog form of transmission is used, the processed digital signal must be converted back to analog form.

This article examines the calibration of sensor signal-conditioning algorithms implemented in signal conditioners that transmit data in analog form. Note that sensor calibration includes the sense-element non-idealities as well as signal-conditioner non-idealities, such as offset and gain errors. The calibration scheme will take care of analog signal-chain errors of the analog circuit that are in front and back of the digital circuits.

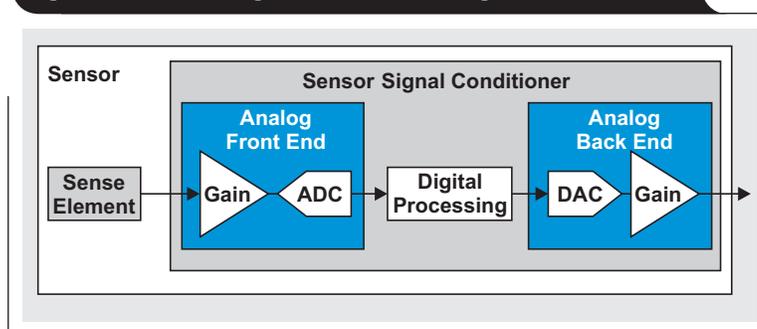
Sensor signal conditioners

The electrical output of a sense element is usually small in value and has non-idealities, such as offset, sensitivity errors, and nonlinearities. These non-idealities cause errors in measurements. Sensor signal conditioners are used to minimize these non-idealities. An example of these types of conditioners is the PGA400-Q1 from Texas Instruments.

Mixed-signal conditioners

Figure 1 shows a block diagram of a mixed-signal conditioner with analog output. Mixed-signal conditioners implement front-end analog circuitry to connect with a sense element. Because the output of a sense element is usually very small, the front end consists of a gain stage followed by an analog-to-digital converter (ADC). The ADC is used to digitize the output of the sense element, which means that flexible techniques of digital signal processing can be used to condition the sense element signal. The gain stage may consist of single-ended differential amplifiers or instrumentation amplifiers, which depends on the sense-element pinout.

Figure 1. Block diagram of a mixed-signal conditioner



After the data from the front end is conditioned by the digital circuitry, it is sent to the back end for transmission to a control or monitoring system. The transmission of the conditioned signal can occur in either analog or digital form. In order to transmit the conditioned digital signal in analog form, a digital-to-analog converter (DAC) with a buffer or gain stage converts the digital value into analog form. Again, the PGA400-Q1 is an example of this type of signal conditioner.

Errors in analog signal chain

The sense-element output is usually a signal with a very low span; in other words, the range of its output signal is small. Because of this, the conditioning of the sense-element output starts with a gain stage. As a result, the sense-element output is subject to different sources of amplifier errors such as input offset, gain and nonlinearity errors. These errors are in addition to the offset and nonlinearity errors inherent to the sense element itself.

The signal conditioners discussed in this article also have analog outputs that are typically generated with a DAC followed by a gain stage. This means that the conditioned signal is also subject to amplifier errors such as input offset, gain and nonlinearity errors in the analog output stages. These errors in the sensor conditioner occur as a result of mismatches between devices and components inside the IC. The errors can become exacerbated by how large a gain is applied to the sense element output signal, or to the conditioned output signal prior to being transmitted to the control or monitoring system.

Note that signals from sense elements have non-idealities. Therefore, the sense-element output is corrected for these non-idealities during sensor manufacturing, often with the help of a signal conditioner. It is during this calibration process that the errors in the analog signal chain are taken into consideration.

Figure 2 illustrates an example of an uncalibrated sensor signal conditioner and the desired output of a calibrated sensor conditioner with respect to the sense-element input signal. Note that the uncalibrated output includes non-idealities of both the sense element and analog circuits in the signal conditioners signal flow.

Two-step calibration process

The two-step calibration process consists of:

1. *Calibration of the back-end analog circuit errors*
This calibration accounts for errors introduced to the signal after being conditioned by the digital circuits and converted back to analog form.
2. *Calibration of the front-end analog circuit errors*
This calibration accounts for input offset, gain and non-linearity errors introduced in the signal from the sense element prior to being digitized.

Figure 3 shows the sections within the sensor conditioner that are related to the two-step calibration process.

The order of the calibration process matters because the calibration of the back-end analog circuits provides the “desired” output values needed for the calibration of the sense element and the front-end analog circuits.

Back-end circuit calibration

The calibration goals for the back-end and front-end analog circuits are nearly the same—to reduce errors introduced by the analog signal chain non-idealities and thereby improve accuracy of the sensor output. However, the data points used to calibrate the back-end circuits come from within the sensor conditioner, not the sense element.

To truly calibrate the back-end circuits, the DAC and the rest of the output analog circuitry has to be isolated from the digital signal-conditioning circuits. The external calibration system then writes to the DAC directly and measures the output of the back-end analog circuits (output pin of the signal conditioner). Standard curve-fitting algorithms are used to curve-fit the data. This curve is used to determine the DAC value required in the calibration of the sense-element output. Note that the number of data points needed for this calibration depends on the non-idealities present in the back-end analog circuits. Since the data points are controlled by the user and not the sense element, the calibration is usually done with only a few data points. Additionally, if the back-end analog circuit behavior changes with temperature, this process must be repeated at different temperatures.

Once the transfer function of the back-end analog circuit and the desired DAC codes are determined, these DAC codes are then incorporated in the calculations for the calibration of the front end.

Figure 2. Ideal output of a calibrated sensor versus the signal from the sense element

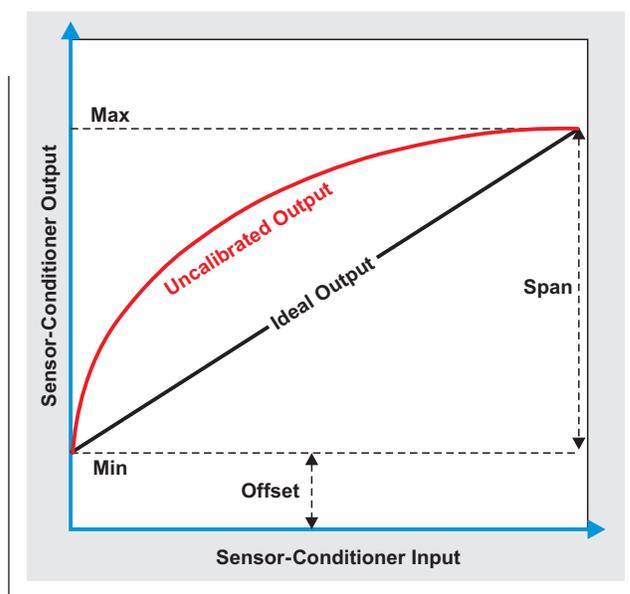
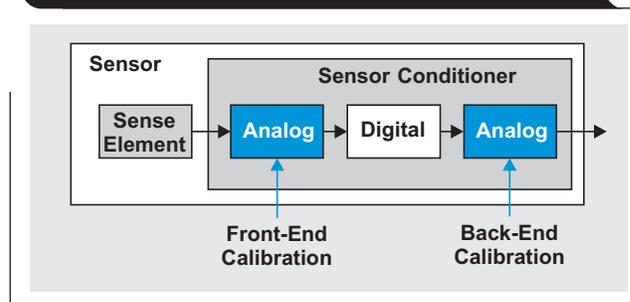


Figure 3: Sensor calibration requires both front-end and back-end curve fitting



Front-end calibration

Front-end calibration depends largely on the output signal linearity of the sense element. Moreover, since the calibration of the sensor is performed by the manufacturer, time and cost are also driving factors. As mentioned earlier, different methods, depending on the desired accuracy of the sensor, can be implemented.

In general, the sensor conditioner uses mathematical algorithms to calibrate the sensor output when the sense element is excited by the specific stimulus related to the application (pressure and temperature, for example). The number of measurements depends on the capability of the sensor conditioner to process the data, as well as the time required to calibrate the sensor. For example, the front-end of a pressure sensor could be calibrated by measuring the output of the ADC at three input signal points. Standard curve-fitting techniques can be used to determine the desired transfer function from ADC output to DAC input. This is accomplished using the ADC data and

DAC code calculated during calibration of the back-end circuits. However, the same three pressure points could be taken at three different temperatures. This would turn into nine total measurements—three pressure values at three temperatures. The resulting mathematical expression for the output of the sensor conditioner is then a second order equation:

$$\text{Output} = \left(h_0 + h_1T + h_2T^2 \right) + \left(g_0 + g_1T + g_2T^2 \right)P + \left(n_0 + n_1T + n_2T^2 \right)P^2 \quad (1)$$

where $h_0, h_1, h_2, g_0, g_1, g_2, n_0, n_1$ and n_2 are the coefficients used to match the output of the sense element to the desired output of the sensor conditioner. Because the back-end circuit results are used to calculate these coefficients, back-end calibration must be preformed first.

As can be inferred, three different pressure measurements across three different temperatures (3P:3T) would be more time-consuming and complex than just three pressure measurements all at one temperature (3P:1T). However, the sensor's output could be more accurate for

the former compared to that of the latter. Depending on the application and capabilities of the sensor conditioner, a combination of these could be used, such as two pressure measurements at two temperatures (2P:2T) or four pressure measurements at four temperatures (4P:4T).

Conclusion

A two-step calibration process can be used in mixed-signal sensor conditioners with analog outputs. The process improves the accuracy of the sensor in general by mitigating errors in the analog signal chain.

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Designing an anti-aliasing filter for ADCs in the frequency domain

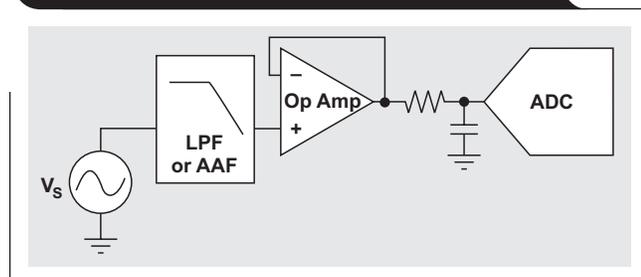
By Bonnie C. Baker

Senior Applications Engineer

Introduction

Data acquisition (DAQ) systems are found across numerous applications where there is an interest to digitize a real-world signal. These applications can range from measuring temperatures to sensing light. When developing a DAQ system, it is usually necessary to place an anti-aliasing filter before the analog-to-digital converter (ADC) to rid the analog system of higher-frequency noise and signals. Figure 1 shows the general circuit diagram for this type of application.

Figure 1. Basic topology of a DAQ circuit



The DAQ system starts with a signal, such as a waveform from a sensor, V_s . Next is the low-pass filter (LPF) or anti-aliasing filter (AAF) and the operational amplifier (op amp) configured as a buffer. At the output of the buffer amplifier is a resistor/capacitor pair that drives the ADC's input. The ADC is a successive-approximation-converter ADC (SAR ADC).

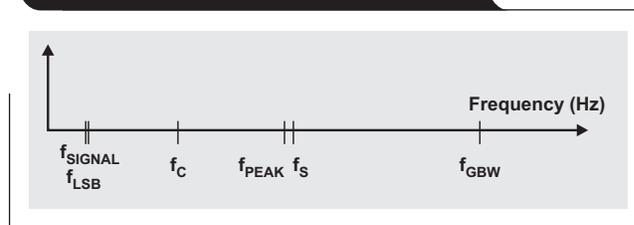
Typically, evaluations of this type of circuit consist of the offset, gain, linearity, and noise. Another perspective in evaluation involves the placement of events in the frequency domain.

There are six frequencies that impact the design of this system:

1. f_{SIGNAL} – Input signal bandwidth
2. f_{LSB} – Filter frequency with a tolerated gain error that has a desired number of least significant bits (LSBs). It is preferable that f_{LSB} is equal to f_{SIGNAL}
3. f_c – LPF corner frequency
4. f_{PEAK} – Amplifier maximum full-scale output versus frequency
5. f_s – ADC sampling frequency
6. f_{GBW} – Amplifier gain bandwidth frequency

Figure 2 shows the general relationship between these frequencies.

Figure 2. Basic relationship of f_s , f_{GBW} , f_{PEAK} , and f_c



For the following evaluation, the example system uses the following throughout:

- Input signal bandwidth of 1 kHz (f_{SIGNAL})
- Low-pass filter corner frequency of 10 kHz (f_c)
- SAR-ADC sampling frequency of 100 kHz (f_s)
- Dual operational amplifier, single-supply OPA2314

Determine maximum signal frequency (f_{SIGNAL} , f_{LSB}) and acceptable gain error

The first action is to determine the bandwidth of the input signal (f_{SIGNAL}). Next, determine the magnitude of the acceptable gain error from the LPF or AAF^[1]. This gain error does not occur instantaneously at the frequency that is chosen to be measured. Actually, at DC, this gain error is zero. The LPF gain error progressively gets larger with frequency. An LSB error in dB equals

$$20 \times \log [(2^N - \text{err})/2^N],$$

where N is the number of converter bits and the whole number, err , is the allowable bit error. This error is found by examining the SPICE closed-loop gain curve.

In this example, the signal bandwidth is 1 kHz and acceptable gain error is equal to one code, which is equivalent to 1 LSB. For a 12-bit ADC where err equals 1 and N equals 12, the gain error equals -2.12 mdB.

Using a TINA-TI™ SPICE model to analyze a fourth-order, 10-kHz low-pass Butterworth filter, the closed-loop gain response is shown in Figures 3 and 4. In both figures, the location of the “b” cursor identifies the point where gain error is -2 dB ($f_{1-LSB} = 1.04$ kHz).

In Figure 3, the measurement window shows that the marker at “b” is at 1.04 kHz. The window also shows the -2 dB^[2] difference between frequency markers “a” and “b” on the y-axis.

Figure 4 zooms in on the y-axis of the Butterworth filter’s action before the filter passes through its corner frequency (f_C). The first observation of this response is that the gain curve has a slight up-shoot before it begins to slope downwards. This upward peak reaches a magnitude of approximately $+38$ dB. This is a fundamental characteristic of a fourth-order, Butterworth low-pass filter.

If a higher gain error is acceptable, Table 1 shows the change in f_{1-LSB} , versus the LSB value.

Table 1. LSB error versus f_{1-LSB}

| LSB error (LSB) | LSB error (dB) | f_{1-LSB} |
|-----------------|----------------|-------------|
| 1 | -0.002 | 1.04 kHz |
| 2 | -0.004 | 1.47 kHz |
| 3 | -0.006 | 1.82 kHz |
| 4 | -0.008 | 2.11 kHz |

Filter corner frequency (f_C)

Note that the corner frequency (f_C) of the low-pass filter at the frequency where the attenuation of closed-loop frequency response is -3 dB. If a fourth-order LPF is chosen, f_C is approximately ten times higher than f_{1-LSB} . SPICE simulations with the WEBENCH® Filter Designer allows this value to be determined quickly. When designing a single-supply filter in the filter designer, select the multiple-feedback (MFB) topology, which exercises the amplifiers with a static DC common-mode voltage that is at mid-supply. Figure 5 shows a circuit diagram of this fourth-order, 10-kHz Butterworth LPF.

Figure 3. Gain error at 1.04 kHz equals -2 dB of a fourth-order, 10-kHz Butterworth LPF

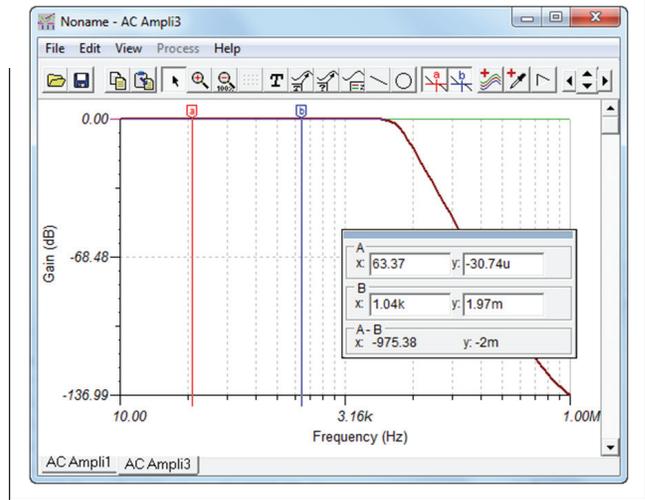


Figure 4. Closed-loop gain response of a fourth-order, 10-kHz Butterworth filter

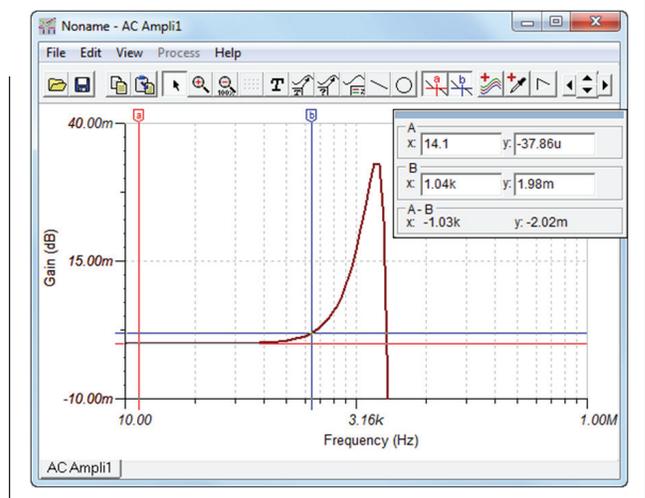
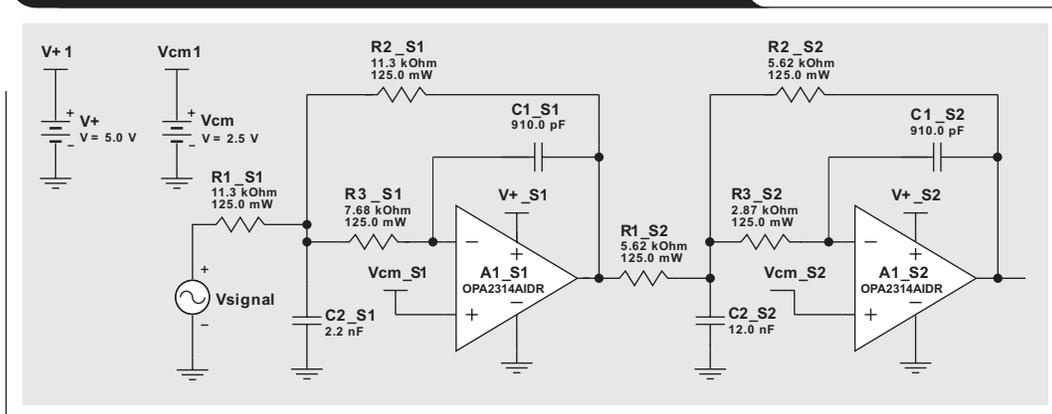


Figure 5. Fourth-order, Butterworth LPF with $f_C = 10$ kHz



Define the amplifier's gain bandwidth frequency (f_{GBW})

The low-pass filter's Q factor, gain (G), and corner frequency (f_C) determine the amplifier's minimum allowable gain bandwidth (f_{GBW}). When finding the Q factor, first identify the type of filter approximation (Butterworth, Bessel, Chebyshev, etc.) and the filter order^[2]. As previously specified, the corner frequency is 10 kHz. In this example, the filter approximation is Butterworth and the gain is 1 V/V. Finally, this is a fourth-order filter. The determination of the gain bandwidth of the amplifier is:

$$f_{GBW} = 100 \times Q \times G \times f_C \quad (1)$$

In this system, f_{GBW} must be equal to or greater than 1.31 MHz (as verified by WEBENCH Filter Designer). The gain bandwidth of the OPA2314 dual amplifier is 2.7 MHz.

Amplifier's maximum full-scale output

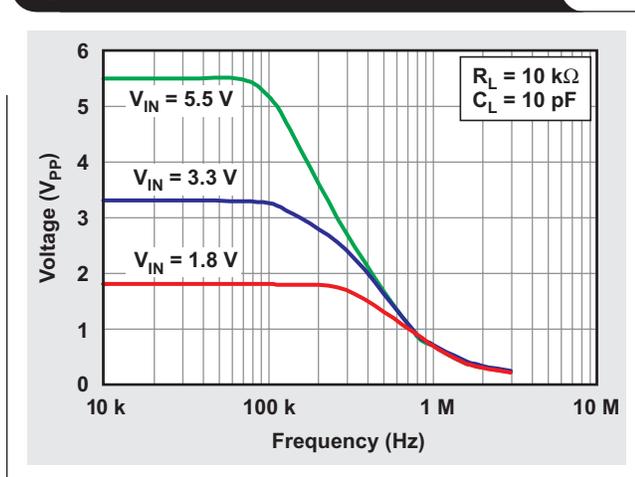
In most applications, it is imperative that the amplifier is capable of delivering its full-scale output. This may or may not be true. One check is to get a rough estimate from the amplifier's slew-rate specification.

A conservative definition of the maximum output voltage per frequency for an amplifier is equal to approximately $f_{PEAK} = SR / (V_{PP} \times \pi)$, where SR is the amplifier's datasheet slew rate and V_{PP} is the peak-to-peak specified output swing. Note that the amplifier's rise and fall times may not be exactly equal. So the slew-rate specification of the datasheet is an estimate.

The datasheet slew rate of the OPA2314 amplifier is 1.5 V/ μ s and in the 5.5-V system, V_{PP} equals 5.46 V. While the amplifier is in the linear region, the rail-to-rail output with a 5.5-V power supply is equal to 5.46 V. Figure 6 shows the tested behavior of the OPA2314 with an output range that goes beyond the linear region of the amplifier.

The calculated maximum output voltage of the OPA2314 occurs at approximately 87.5 kHz. However, in Figure 6, the maximum value with bench data is shown to be approximately 70 kHz. This discrepancy exists because of

Figure 6. OPA2314 maximum output voltage



the mismatches between the amplifier rise and fall times and the responsiveness of the amplifier at the peaks and valleys of the sinusoidal input voltage swing.

SAR-ADC sampling frequency

The challenge now is to identify the sampling frequency of the SAR ADC. Given a 1-kHz maximum input signal, it is imperative that the SAR ADC samples the signal more than one cycle per second. Actually, over ten times is preferable. This implies that a 10-kHz sampling ADC will work.

Additionally, it is important to eliminate signal-path noise when possible. If the SAR ADC is converting at higher frequencies above the corner frequency of the filter, that portion of the noise will not be aliased back into the system. Consequently, a 100-kHz sampling SAR ADC meets the requirements.

If the sampling frequency is 100 kHz, the Nyquist frequency is 50 kHz. At 50 kHz, the frequency response of the low-pass filter is down by approximately 50 dB. This level of attenuation limits the impact on noise going through the system.

Conclusion

The development of a DAQ system in the frequency domain can present interesting challenges. A system consisting of a filter and a SAR ADC is usually evaluated with the performance specifications of the DC- and AC-amplifier and the converter. This article, however, evaluated the system's signal path from a frequency perspective.

The important frequency specifications are the signal bandwidth, filter corner frequency, amplifier bandwidth, and converter sampling speed. Even though the signal bandwidth is small, 1 kHz, the required AAF corner frequency should be 10 times higher than the signal bandwidth in an effort to reduce high-frequency gain errors. Additionally, the converter's sampling frequency is higher than expected in an effort to reduce complications caused by noise aliasing.

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2. Bonnie Baker, "Analog Filters and Specification Swimming: Selecting the right bandwidth for your filter," On Board with Bonnie, TI blog, Nov 8, 2013.

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Tips and tricks for high-speed, high-voltage measurement

By Grant Smith

Business Development Manager

Introduction

High-voltage circuits that also have high-speed devices, such as the recently introduced gallium nitride (GaN) and silicon carbide (SiC) power FETs, are posing measurement challenges to power conversion designers. Lower-voltage GaN FETs (<100 V), when paired properly to low-inductance gate drivers, can be switched in as little as 1 ns. High-voltage 600-V GaN FETs, and even higher-voltage 1200-V SiC FETs with special low-inductance layout and high-current drivers, also can be switched at 1-MHz rates with rise and fall times of under 20 ns. During design validation, it is a challenge to manually probe such high-voltage circuits safely in compliance with standards like the Environmental Safety and Health (ESH) guidelines. Another consideration is the requirement to protect test personnel from accidentally touching energized areas with dielectric safety barriers and the use of personal safety equipment such as rubber gloves and eye protection. These safety concerns make probing even more difficult.

This article describes a few high-speed and high-voltage probe circuits and methods to measure probe performance. The objective is to show how to bring high voltages down to safe levels with good DC accuracy and high AC fidelity, and then be able to route these signals over coax into 50-Ω equipment.

Measurement review

Measuring the voltage of a circuit with a probe loads it both resistively and capacitively, and at high frequencies, even inductively. Loading the circuit also adds distortion and ringing to the original signal. The concept is similar to the Heisenberg uncertainty principle, which is about the quantum nature of an electron's position and momentum and reveals something about the science of electrical

measurement. The basic conclusion is that any attempt to measure voltage or current actually changes it.

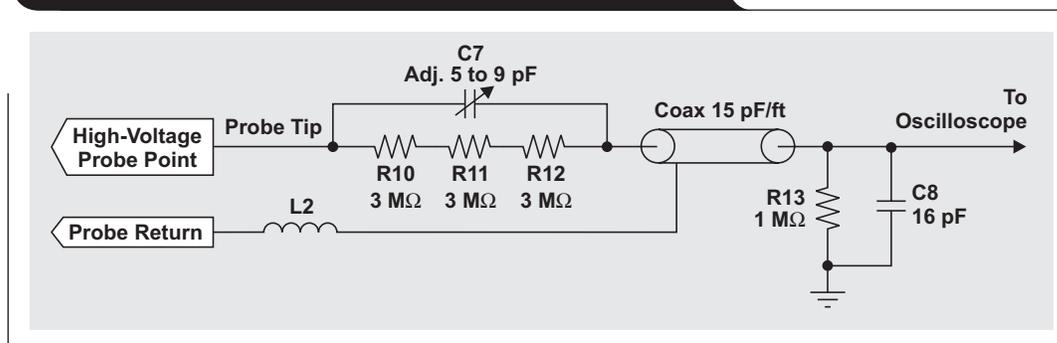
Measuring current with a current probe adds loop area and inductance, as well as distortion and time delays that can complicate estimates for instantaneous power dissipation ($V \times I$). Measuring currents by measuring the voltage across a low-value shunt resistor is also a common approach. However, the inductance of the resistor must be considered when frequencies are above 10 MHz, or rise and fall times below 30 ns are present. At the megahertz switching frequencies possible with wide-bandgap power conversion and with the short rise and fall times present, it is important to revisit probe circuits and some of their limitations.

Figure 1 shows a simplified schematic of a 10:1 10-MΩ, 500-MHz scope probe. Resistors R10, R11 and R12 provide a 9-MΩ resistance in the tip of the probe in parallel with a variable compensation capacitor (C7). At DC, the 10-to-1 divide ratio is obtained by the 1-MΩ DC input resistor of the scope (R13) and the 9-MΩ resistance in the tip. To give 1% or better accuracy in voltage measurement, the circuit to be measured must have a source impedance of 100 kΩ or less. Active probes can have higher input impedances, but typically are limited to tens of volts^[1].

Wide-bandgap power FETs

Recently introduced wide-bandgap power semiconductor devices such as SiC and GaN FETs are helping designers meet next-generation efficiency and power-density requirements. These wide-bandgap devices support higher breakdown voltages across a smaller area than traditional silicon (Si) devices. Designers of these devices are reducing capacitances and geometries to improve speed through the channels. The high mobility of GaN and the lateral structure of GaN power FETs gives rise to

Figure 1. Simplified schematic of an oscilloscope probe



higher capabilities of carrier concentration and lower on-resistance ($R_{DS(on)}$) values when compared to Si devices of the same size. These features allow GaN FETs to be about one-third the size of Si FETs, yet have equivalent voltage and current carrying capability.

Reverse recovery charge (Q_{rr}) is one of the dominant power-loss mechanisms of Si power-FET switching. Both GaN and SiC FETs are majority-only carrier devices. GaN FETs have no body diode, which means they have no reverse recovery charge (Q_{rr}). SiC FETs do have a body diode like Si devices, but with lower stored reverse charge. When validating designs with recently released GaN and SiC power devices, it is important to quantify the losses in the specific application or power-converter architecture. Also, trade-offs should be evaluated for devices that require different approaches for gate-drive circuitry, controller parameters, and system-performance goals.

Measuring the voltage waveforms on the drain, gate and source with sufficient accuracy and bandwidth is critical. It is also important to monitor these waveforms over temperature as wide-bandgap devices perform differently than Si devices. One key parameter of any switching FET is $R_{DS(on)}$. The $R_{DS(on)}$ of Si FETs is known to approximately double from 25°C to 125°C. SiC devices have much less increase in $R_{DS(on)}$ and are specified to operate to 200°C or higher. GaN FETs also have temperature dependence, as well as an OFF-state, voltage-dependent on-resistance mechanism called dynamic $R_{DS(on)}$. Si or SiC FETs have not been shown to have this complex effect. GaN's dynamic $R_{DS(on)}$ has been reported to change as soon as several hundred nanoseconds after turn on to several minutes, depending on the cause of the change^[2].

Figure 2 shows a simple power-factor correction (PFC) boost topology^[3]. For universal 85- to 270-VAC applications, the drain signal on Q1 can be as high as 400 V or higher with line surges. In the case of a GaN FET-based design, the OFF-to-ON waveform can have a dv/dt of >150 V/ns, and a fall time of approximately 3.5 ns. The simple relationship of signal bandwidth (BW) = $0.35/t_{fall}$ gives an estimate of 100 MHz. To achieve less than 2%

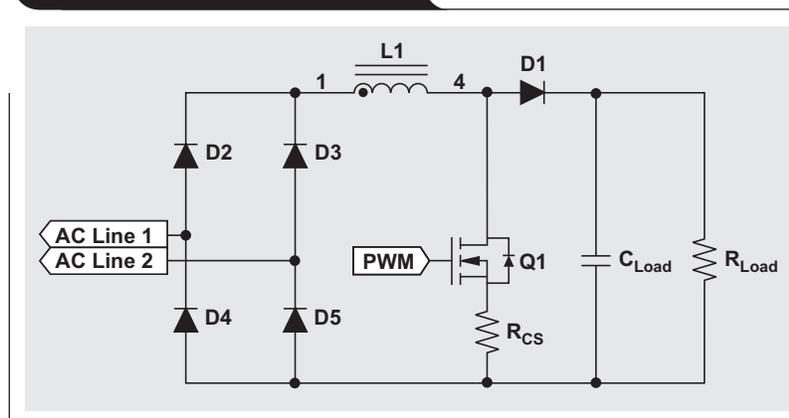
measurement error, the probe network and signal chain should have a bandwidth of 5 times this, or 500 MHz.

Referring back to Figure 1, note that without the compensation capacitor (C7), the 9-M Ω probe-tip resistance in front of the approximately 50 pF of cable capacitance that is in parallel with the 16 pF of scope input capacitance forms a low-pass filter with a bandwidth of only about 250 Hz, which is two million times lower than needed. To compensate, C7 in parallel with the 9-M Ω resistance is tuned to add a zero in the frequency response. This action cancels out the pole and provides a flat frequency response.

Another way to look at this is that C7 maintains the 9-times impedance ratio of the probe tip to the impedance of the cable and scope input across a wide bandwidth, until parasitic inductance and transmission line effects start to dominate. Unfortunately, 9 times the ratio of impedances means that there will never be an impedance match between the probe tip and the scope input. If you try to build this circuit, as I did, using off-the-shelf 50- Ω coax as the cable, it will perform very poorly. What comes into play, at approximately $1/(\text{round-trip travel time})$ along the cable, is a very strong reflection or ringing due to the 9-times impedance mismatch.

A little research on my part, including tearing open an old probe and doing some old school reverse engineering, revealed a secret, which is the basis for my first tip and trick. The center conductor of the scope probe cable is resistive. I measured about 300 Ω between the output of the tip and the input to the Bayonet Neill-Concelman (BNC) adapter box, where the compensation is actually done. Like magic, adding loss to the path between the tip and the scope attenuates reflections and gives a flat response. I later discovered that this was patented by Tektronix in 1956^[4]. Since patent lifetimes are about 20 years, this one has long since expired and is freely open for reuse.

Figure 2. PFC boost converter



Back to circuit loading

At 500 MHz, without the lossy transmission line, the input impedance of the cable at the output of the probe is only about 5 Ω . As described in the patent, adding loss increases the cable input impedance and allows for a smaller value of probe-tip capacitance for compensation. Adjusting the compensation capacitor to be approximately 7 pF gives the probe an impedance of about 45 Ω at the tip that is used to touch the circuit. Such a low probe impedance could degrade a voltage measurement from a signal with greater than a few ohms of series impedance due to loading.

GaN FETs, like Si FETs, exhibit a C_{oss} that is a function of drain voltage, but are typically two-to-four times lower than Si FETs. One commercially available 600-V, 150-m Ω GaN FET reports a C_{oss} of approximately 40 pF at 400 V, and a commercially available 600-V, 190-m Ω Si super-junction FET reports a C_{oss} of 100 pF at 100 V, similar to a 1200-V SiC FET at 100 V.

The 7-pF capacitance of the probe tip, without loss in the line in the simple probe shown Figure 1, should be reduced to 1 pF or less to provide minimal signal loading for GaN and SiC FET testing.

Reduce probe capacitance

Reducing capacitance can be accomplished in multiple ways. One trick is to use twinax cables and actively drive the shield for lower-frequency signals. Another option is to reduce the length of the cable as much as possible and then adding an active low-capacitance, wideband amplifier with high input impedance. In order to use an active amplifier and still maintain the capability for high-voltage measurement, adding a wideband, low-capacitance voltage attenuator is also required. The VCA824 from Texas Instruments is an example of a wideband, fully-differential

amplifier with high input impedance that can drive 50- Ω lines. It has an input common-mode range of ± 1.5 V and a >700-MHz small-signal bandwidth, as well as an input impedance of 1 pF in parallel with 1 M Ω . Using this amplifier for drain voltages as high as 600 V will require a 1000:1 voltage attenuator that is flat from DC to >500 MHz and an input capacitance of less than 2 pF.

The impedance and power dissipation of this attenuator needs to be taken into consideration. Here are the competing requirements. Ideally, the impedance will be high enough to prevent overloading the circuit and reduce power dissipation. Implementing the attenuator with a 1-M Ω resistive impedance keeps the power dissipation to less than 400 mW when probing up to 600 V. Keeping the impedance lower gives a wider bandwidth while driving the parasitic board capacitance and amplifier's input capacitance.

Figure 3 shows an improved probe circuit that provides a 1000:1 divide ratio and only takes about 1 inch of signal-path length. The free on-line trace-impedance calculator tool^[5] provided an estimate of the parasitic capacitance. For example, a 1-oz microstrip line, 6-mils wide and 4 mils above a ground plane with FR-4 (er 4.0), is about 2.7 pF per inch. To further reduce parasitic capacitance from the resistor dividers, an RF engineering trick was used to mount the 2-W-capable, 2512 SMT resistors on their sides. This minimizes the area of the signal-path conduction over ground. Also, the 1000:1 divide ratio was broken into two sections: 2:1 and 500:1. The input capacitance of this embedded probe is approximately 1.5 pF.

The 200 k Ω of DC resistance ($R2 + R3$) results in a fairly high power dissipation, 1.8 W at 600 V, but allowed using approximately 1-pF compensation capacitance and get over 500 MHz of frequency response.

Figure 3. Schematic of improved high-voltage probe

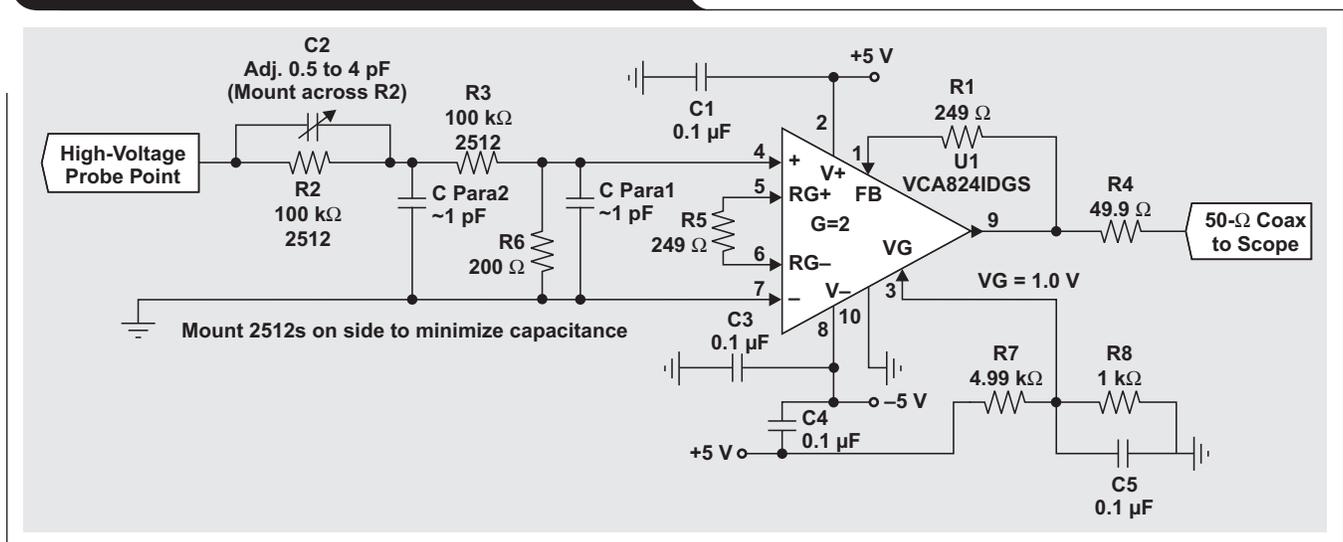


Figure 4 shows the circuit board with the side-mounted 2512's and the tuning cap in parallel.

Performance results are shown by two plots of the drain voltage output to the scope in Figures 5 and 6. The blue plot is from a 10:1 commercial scope probe. The purple plot is from a network that is buffered by the VCA824 and another TI wideband mux, the OPA4872, which is driving 10 feet of 50-Ω coaxial cable. The plot in Figure 5 is before tuning and the plot in Figure 6 is after tuning.

Figure 4. Embedded high-voltage probe implementation

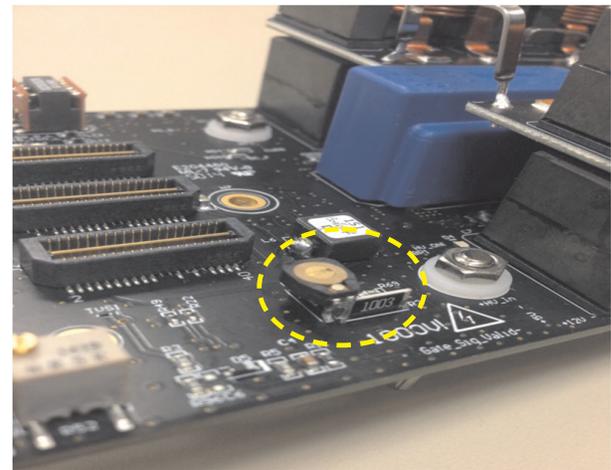


Figure 5. Comparison of probes before compensation/tuning

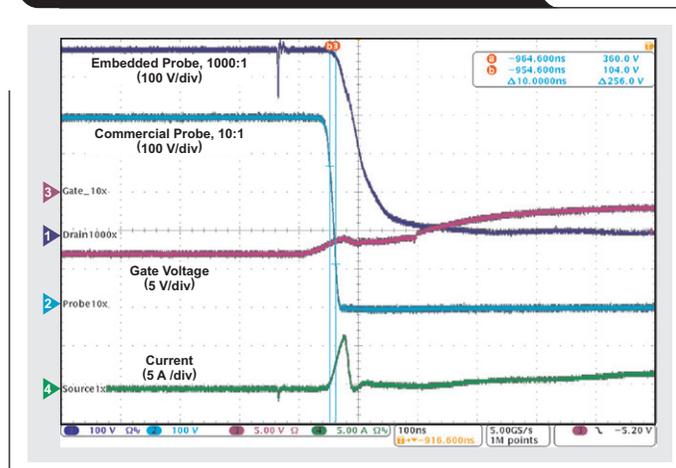
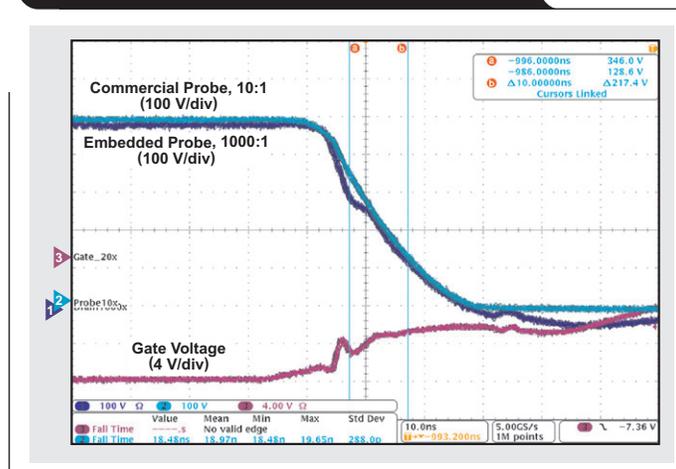


Figure 6. Comparison of probes after tuning compensation cap



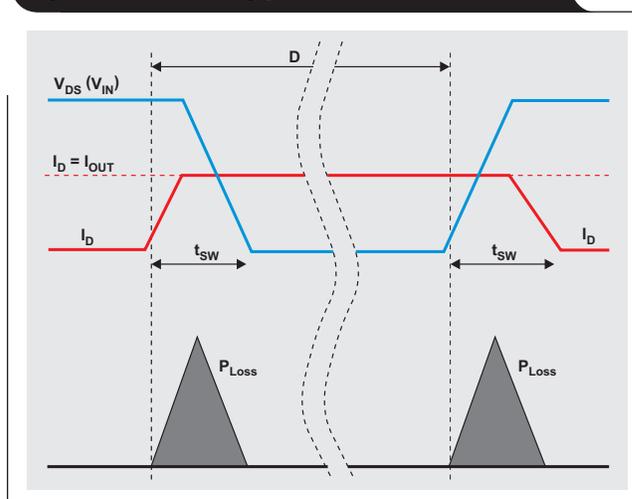
After compensation, the waveform from the embedded probe on the drain was used to estimate switching losses. Figure 7 shows how the turn-on and turn-off losses can be calculated. The total loss per cycle is the area under both triangular VI curves. To reduce measurement error, it is important to have good voltage accuracy as well as good current accuracy and skew matching (<2 ns) between both the voltage and current waveforms.

To accurately measure device current, another VCA824 amplifier was used to differentially measure the (Kelvin-connected) voltage across a current-sense resistor, R_{CS} , between the FET source and ground. Using a wide-body 6432, low-inductance (<200 pH) resistor with a value of $0.100\ \Omega$ provided a current-measurement range of $\pm 15\ \text{A}$. The green trace in Figure 5 shows the source-current waveform derived from the differential voltage measurement multiplied by 10. Note that the triangular 6-A current spike at FET turn on is due to the device's gate and drain charge. Figure 5 also shows the gate-to-ground waveform as the red trace. Skew matching was accomplished by using equal-length routes from the device to the buffer amps and then equal-length runs of $50\text{-}\Omega$ coax to the scope.

Conclusion

In summary, it was shown how an easy-to-implement, embedded-probe circuit can measure voltages up to 600 V, with rise and fall times as short as 3.5 ns. To minimize capacitive loading, a 1-inch $50\text{-}\Omega$ microstrip line, along with two $100\text{-k}\Omega$, 2-W resistors and one $200\text{-}\Omega$ resistor to ground, is used to implement a wideband 1000:1 attenuator. This configuration drives the fully-differential VCA824 amplifier that offers high input impedance, a >700-MHz bandwidth and a $\pm 1.5\text{-V}$ input common-mode range. Also shown was how the device current can be measured with the differential VCA824 using a Kelvin connection across a $0.1\text{-}\Omega$ resistance between the device's source and ground. With skew-matched voltage and current waveforms, a designer can use the oscilloscope's waveform math to multiply and integrate them to provide accurate estimates of device losses.

Figure 7. Switching power-loss estimation



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Related Web sites

Gallium Nitride (GaN) Solutions:

www.ti.com/gan
www.ti.com/lit/slyy070
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JESD204B multi-device synchronization: Breaking down the requirements

By Matt Guibord

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Introduction

A common trend in wireless transceivers, such as cellular communications systems, is to adopt beamforming technology to enable better system sensitivity and selectivity. This trend results in an increased number of antennas per system and requires synchronization between each antenna to achieve precise control of signal phases during transmission and reception. Synchronization, however, is not limited to just communications systems. There are numerous applications that make use of synchronized signal chains, including phased-array radars, distributed antenna arrays, and medical imaging machines.

Most systems that require multiple synchronized signal chains also require synchronization of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The JESD204B serialized interface for high-speed ADCs and high-speed DACs has simplified the process for achieving synchronization while also enabling higher antenna density by reducing layout size and the number of device pins. So it should not be a surprise that another trend is an increased adoption of JESD204B data converters in these systems. System and device requirements for synchronization of JESD204B ADCs and DACs can be a bit confusing for first-time users of the standard. The

objective of this article is to clarify the requirements for achieving synchronization among subclass 1 JESD204B devices and simplify the discussion to just the applicable portions of the standard.

Synchronization requirements

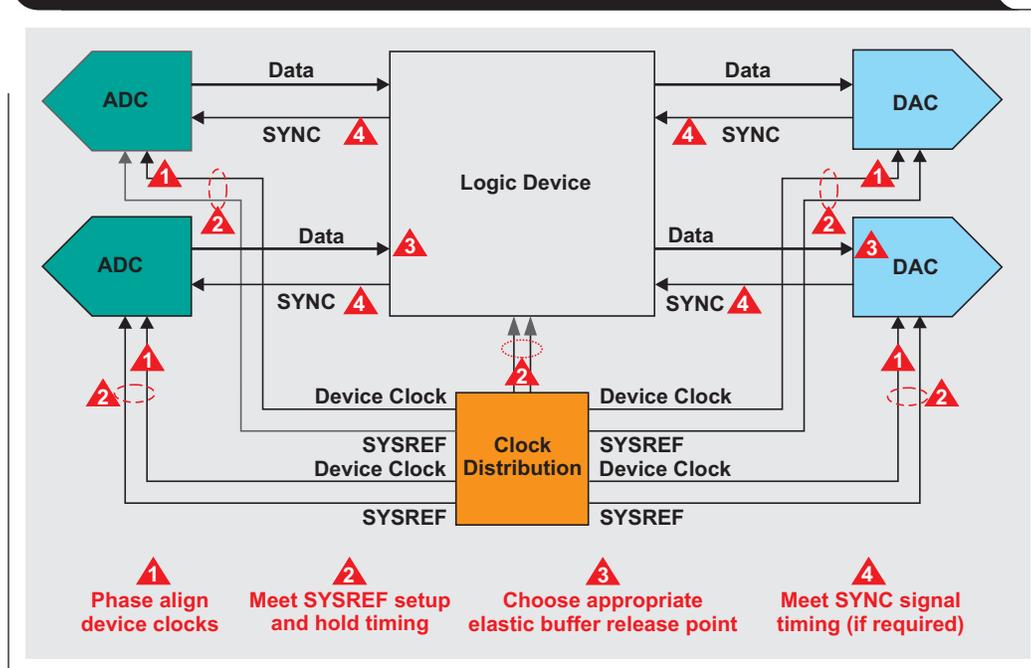
Achieving synchronization of data converters in a JESD204B system can be broken down into the four basic requirements visualized in Figure 1.

1. Phase align the device clocks at each data converter
2. Meet setup-and-hold times for SYSREF relative to the device clock at each data converter and logic element
3. Choose appropriate elastic buffer release points in the JESD204B receivers to guarantee deterministic latency
4. Meet SYNC signal timing requirements (if required)

Phase aligning device clocks

In a JESD204B system, the device clock is used either as the converter's sampling clock (with or without a divider), or as a reference for a phase-locked loop (PLL), which generates the sampling clock. As such, the phase alignment of the device clocks at each converter is critical for maintaining alignment of the sampling instances in each

Figure 1. Requirements for multi-device synchronization in JESD204B systems



converter. The alignment of the device clocks is dependent on how well the propagation delays on the clock distribution paths are controlled, including how well the alignment is maintained over temperature changes.

SYSREF requirements

The SYSREF signal is the most important signal for achieving repeatable system latencies and synchronization. The two requirements for the SYSREF signal are that it meets setup-and-hold times relative to the device clock, and that it runs at an appropriate frequency. Note that SYSREF can be implemented as a single pulse that removes the frequency requirement; however, this also requires DC coupling of the SYSREF signal. In many cases, DC coupling of the SYSREF signal is not possible due to input common-mode voltage requirements.

SYSREF timing requirements

The most challenging requirement for SYSREF is setup-and-hold timing. For lower-speed pipeline ADCs and base-band DACs (<1 GSPS), the setup-and-hold requirement is not as difficult. However, for faster devices such as gigasample ADCs and RF-sampling DACs, the higher device clock rate reduces the setup-and-hold window for SYSREF and may require dynamic delay adjustment to maintain timing over all conditions.

JESD204B allows for flexibility in how data converters are clocked. For instance, some devices contain an integrated PLL that allows a lower-frequency device clock to be used, which is then multiplied up to create the converter's sampling clock. The device clock still captures SYSREF, but the lower frequency greatly eases the setup-and-hold requirements. Additionally, devices may contain features that either aid in meeting timing or relaxing the requirements. If proper timing cannot be met, then an external calibration procedure will likely be needed to achieve synchronization.

Choosing the frequency of SYSREF

There is a limitation on frequencies that can be used for continuous or gapped-periodic SYSREF signals. Note that this does not apply for single-pulse implementations. The main requirement is that the SYSREF signal must run at a frequency equal to or at an integer division of the local multi-frame clock (LMFC) frequency. This requirement is

given in Equation 1, where f_{BITRATE} is the interface bit rate of the serializer/deserializer (SerDes), F is the number of octets per frame, K is the number of frames per multi-frame block, and n is any positive integer.

$$f_{\text{SYSREF}} = \frac{f_{\text{BITRATE}}}{10 \times F \times K \times n} \quad (1)$$

Note that the K parameter can be changed to adjust the SYSREF frequency, but each device may have its own limitations on possible K values in addition to the standard's limitation of $17 \leq F \times K \leq 1024$.

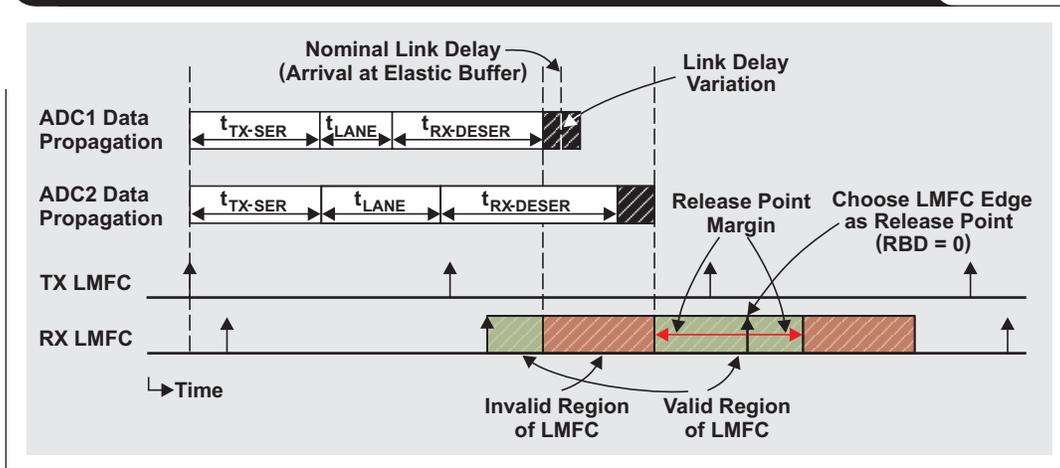
There may be additional requirements on the frequency of SYSREF if the device uses internal clock dividers or SYSREF for synchronization of other digital features. For instance, if a device uses an internal clock divider to generate the sampling clock, then the divider needs to be synchronized to maintain sampling clock phase alignment in all devices. This sets an additional limitation on the SYSREF frequency because it must be an integer division of both the LMFC frequency and the lowest internally-generated frequency. Typically, this is not an issue, but it should be verified that the calculated SYSREF frequency meets this requirement and then adjust it accordingly.

Elastic buffer release point

The third requirement for synchronization is to select a proper elastic buffer release point in the JESD204B receiver to achieve deterministic latency. The elastic buffer is the key block for achieving deterministic latency. It does so by absorbing variations in the propagation delays of the serialized data as it travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against variations in the delays. An incorrect release point will result in a latency variation of one LMFC period.

Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer (referenced to an LMFC edge) and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must guarantee that the data for all lanes arrives at all devices before the release point occurs.

Figure 2. Defining the valid region of LMFC for elastic-buffer release point



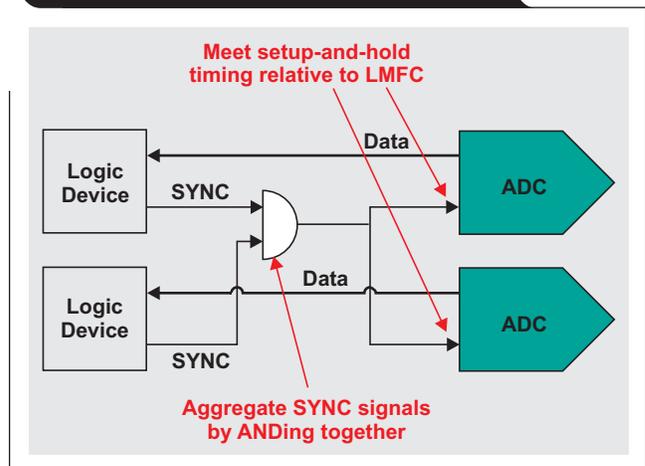
It is easier to demonstrate this requirement by using a timing diagram (Figure 2) that shows the data for two ADCs. The second ADC has a longer routing distance and results in a longer link delay. First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC edge so that it occurs within the valid region of the LMFC cycle. In Figure 2, the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side.

SYNC signal timing

As data converter sampling rates have increased, so has the desire to maintain low interface speeds. This is often accomplished by implementing digital up-converters (DUCs) in DACs or digital down-converters (DDCs) in ADCs. The DUCs and DDCs often implement numerically-controlled oscillators (NCOs) that must be synchronized in all devices to maintain overall system synchronization. The most common approach is to synchronize the NCOs by using the LMFC rising edge and elastic-buffer release point. In ADCs, the NCOs can be synchronized using the first LMFC edge that occurs after the SYNC signal is deasserted, which corresponds to the start of the initial lane alignment sequence (ILAS) transmission. In DACs, the typical approach is to synchronize the NCOs when the elastic buffer is released.

There is a timing requirement on the SYNC signal in order to achieve multi-device synchronization between multiple ADCs or DACs that utilize NCOs. The SYNC signal must be deasserted by all receivers on the same LMFC edge and received at the transmitters in the same LMFC cycle. The simplest approach to meeting the first requirement is to AND the SYNC signals from all receivers together, then distribute this aggregated signal to each transmitter (Figure 3). This also sets a requirement on the

Figure 3. Aggregating SYNC signals to synchronize NCOs in ADCs



SYNC signal in that it must meet the needed setup-and-hold times relative to the LMFC edge in the transmitting device. If DDCs or DUCs are not used in the ADCs or DACs, then there is no requirement for SYNC signal timing and each device can start up at independent times and still achieve synchronization.

Example clocking schemes

The most difficult synchronization requirement is meeting the SYSREF-to-device clock-timing relationship. To address these concerns, two examples of clocking implementations are examined.

Typical JESD204B clocking scheme

The easiest way to maintain proper setup-and-hold times for SYSREF is to use a single clocking device that implements device clock and SYSREF pairs. These pairs maintain good phase alignment over all conditions because of the matched outputs. One example is the LMK04828 from Texas Instruments, which implements seven pairs of

device-clock and SYSREF outputs. Figure 4 shows an example system using the LMK04828 to clock multiple ADS42JB69 ADCs. This scheme can be used for low-sample-rate converters or for gigasample converters with internal PLLs. A JESD204B-compliant clock jitter cleaner, such as the LMK04828, also can be used as a clock distributor and SYSREF generator by bypassing the PLLs in favor of a higher-performance input clock while still maintaining the benefit of the matched output pairs.

Gigasample ADC and DAC clocking schemes

Clocking of JESD204B gigasample converters is more challenging when the device does not have an internal PLL or if the PLL is bypassed to achieve certain performance targets. One example of such a high-speed data converter is the ADC12J4000, which can operate at up to 4 GSPS and requires a 4-GHz device clock. Figure 5 shows an example clocking tree using TRF3765 RF synthesizers to generate the 4-GHz clocks and the LMK04828 to generate the reference clocks and SYSREF signals.

In this case, the system designer can make use of programmable delays in the clock jitter cleaner and data converter to meet setup-and-hold times over all conditions. Furthermore, the ADC12J4000 has a dirty SYSREF capture feature that checks for setup-and-hold time issues. The combination of these features enables proper capture of SYSREF over all temperatures after some minor characterization of the delay variations in the system. First, the dirty SYSREF capture can be used to find the optimal nominal-delay settings. Then, as the system conditions change, the dirty capture bit can be monitored to find setup-and-hold time issues. When a timing issue is found, the clock jitter cleaner or data converter SYSREF delays can be used to shift the SYSREF signal back into the appropriate region. After characterizing the delays, the system can monitor the temperature and adjust the delays as necessary.

Figure 4. Using LMK04828 to synchronize multiple JESD204B data converters

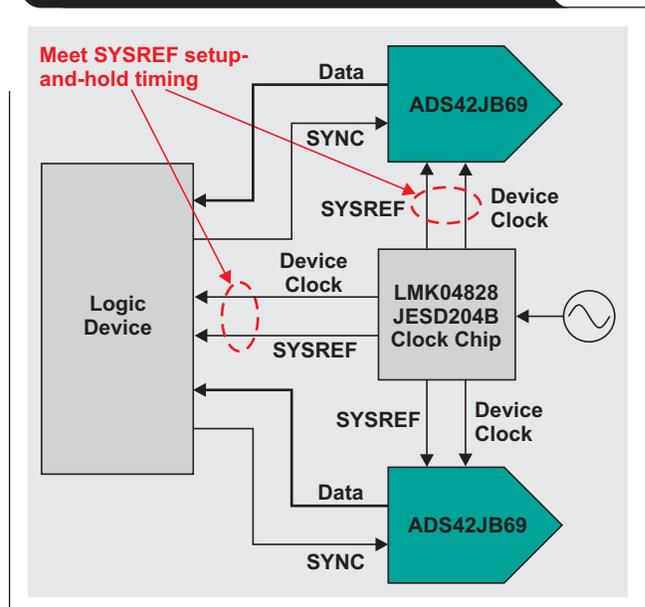
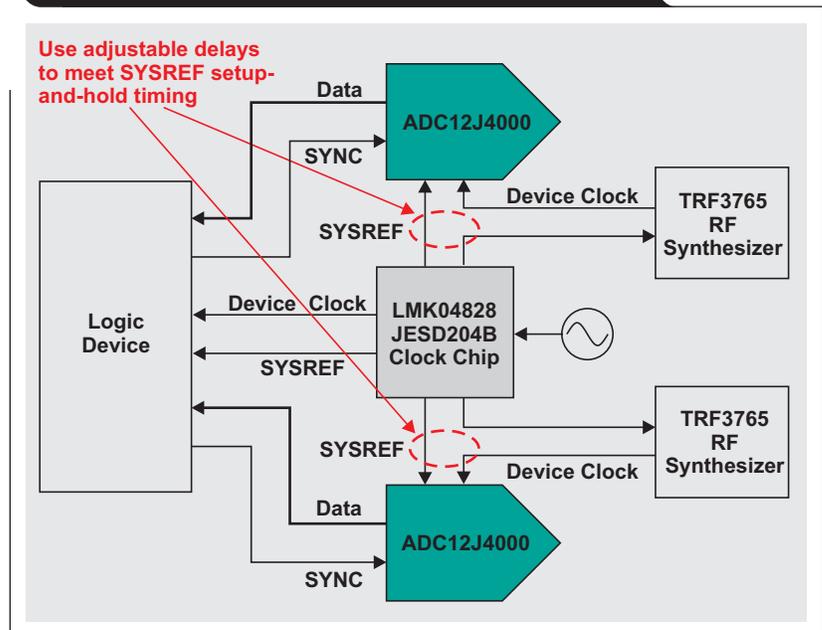


Figure 5. Using LMK04828 and TRF3765 to synchronize multiple gigasample data converters



Conclusion

System designers must have a good understanding of the four main requirements for synchronization of JESD204B ADCs and DACs. Clock-distribution path requirements are important to maintain phase control for both the device clock and SYSREF signals. Also, the SYSREF signal must meet setup-and-hold times relative to the device clock and at an appropriate frequency. Another synchronization requirement is a proper elastic buffer release point in the JESD204B receiver to archive deterministic latency. Additional SYNC timing may be required in systems that use DDCs or DUCs. Two examples of clocking implementations were provided to show how to achieve conditions for overall system synchronization.

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Advanced linear equalization in multi-gigabit systems

By Lee Sledjeski
Applications Engineer

Introduction

While today's widespread need for signal equalization in electronics may seem to be a recent phenomenon, there are examples of linear equalization in telecommunications dating back well over a century. In fact, continuous time linear equalization (CTLE) is just part of a signal conditioning ecosystem designed to aid in the transmission and reception of high-speed digital signals. This compensation or conditioning of the digital signals is usually called emphasis in the transmit domain and equalization in the receive domain.

What is linear equalization and why it is it needed?

Equalization is a process or technique used to restore balance between the various frequency components which together make up an electronic signal. In an simple analogy, audio equalizers are often used to help boost signal components which speakers have difficulty reproducing, or our old ears can no longer hear efficiently. Moving from audio speakers to signals on a PCB or in a cable, a similar issue is encountered. As high-speed signals pass through the transmission media, high-frequency signal components are quickly attenuated due to the physical properties of the conductor and the surrounding dielectric.

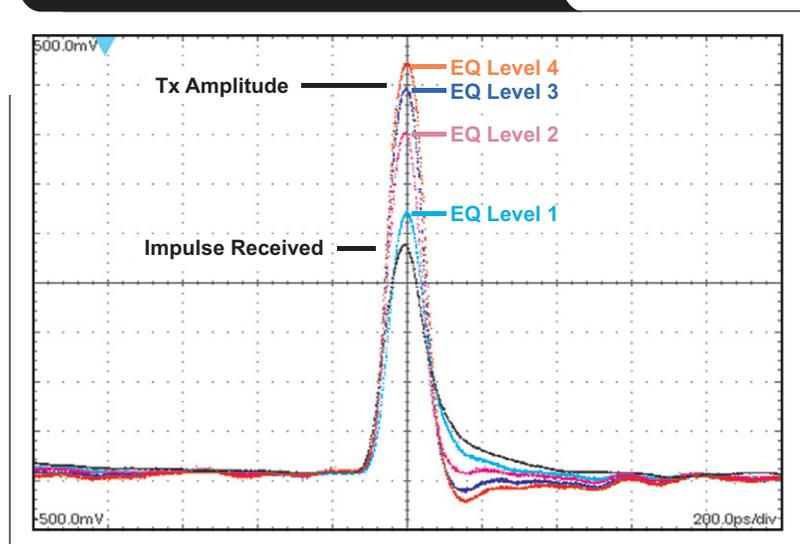
CTLE performance

Modern telecommunication standards must embrace and specify faster data rates to help satisfy the increasing appetite for instantaneous information around the globe. This almost ensures that CTLE will continue to be specified in serial data standards under development now and in the future. At an overview level, the linear gain or high-pass boost by CTLE circuitry helps to expand the incoming signal envelope. CTLE, in combination with digital equalization strategies like decision feedback equalization (DFE), can enable robust signal reception across media with levels of signal attenuation not possible with DFE alone. A more in-dept view is provided by time-domain waveforms and frequency-domain plots to highlight common CTLE characteristics and how they impact an actual eye diagram.

In Figure 1, the received time-domain impulse is initially launched into a 10-inch length of FR4 transmission media with an output differential voltage of 800 mV_{pp}. After traversing the FR4 transmission media, the received impulse amplitude is reduced by half and the trailing-edge energy has spread well past the original bit width or unit interval (UI) boundary. In this example, a DS125BR820 equalizer from Texas Instruments was attached at the far end of the 10-inch trace to demonstrate the CTLE function and its effectiveness for reducing jitter due to channel losses. As the CTLE level is gradually increased to match the channel loss, it is able to restore the impulse amplitude and adjacent bit interference. Looking at the amplitude and timing features on the impulse response provides insight into system response to a pseudo-random binary sequence (PRBS) pattern. This method simply time shifts and sums each of the PRBS transitions as an impulse. In the strict mathematical sense, the impulse in Figure 1 does not have infinite amplitude and zero width, but it is still a good intuitive way to look at CTLE performance.

Without CTLE, even a simple data pattern clearly shows the effect of reduced amplitude and pulse-spreading for the single-bit transitions within the eye diagram. The addition of CTLE reduces these effects by equalizing the amplitude of all transitions in the data pattern and minimizing the pulse spreading across bit boundaries. In

Figure 1. Impulse response after 10-inch FR4, with and without CTLE



eliminating the interaction between bits, inter-symbol interference (ISI) is minimized and the eye opening is improved. This can be seen in Figure 2 by comparing the eye diagrams.

Frequency domain

Another way to examine CTLE is in the frequency domain. The FR4 used in the time domain experiment can be measured to determine its frequency domain characteristics. The same measurement tool is also used to measure the CTLE characteristics. Typically, the optimum eye-diagram results are achieved when the attenuation of the transmission media is matched by the CTLE gains out to a frequency close to the Nyquist frequency across a wide range of frequencies. The example shown in Figure 3 shows the transmission loss and CTLE gain associated with a 12-Gbps serial data rate. For a 12-Gbps signal, a repeating pattern of 101010 binary symbols produces a 6-GHz fundamental frequency. This combination results in a total system response of the media + CTLE that is ideally zero or flat.

Taking this technique to extreme levels of attenuation and high-frequency gain uncovers a CTLE limitation. As the frequency domain plot shows, a CTLE circuit can provide considerable boost to the high-frequency signal components. Internally, the CTLE is designed to minimize any random jitter (RJ) additions to the high-speed signal. Externally, it is impossible for the CTLE gain to discriminate between signal and system noise. Therefore, all aspects of the incoming data receive a boost, and this effect is made more apparent at higher CTLE boost.

Figure 2. Eye diagrams without CTLE (top) and with CTLE (bottom)

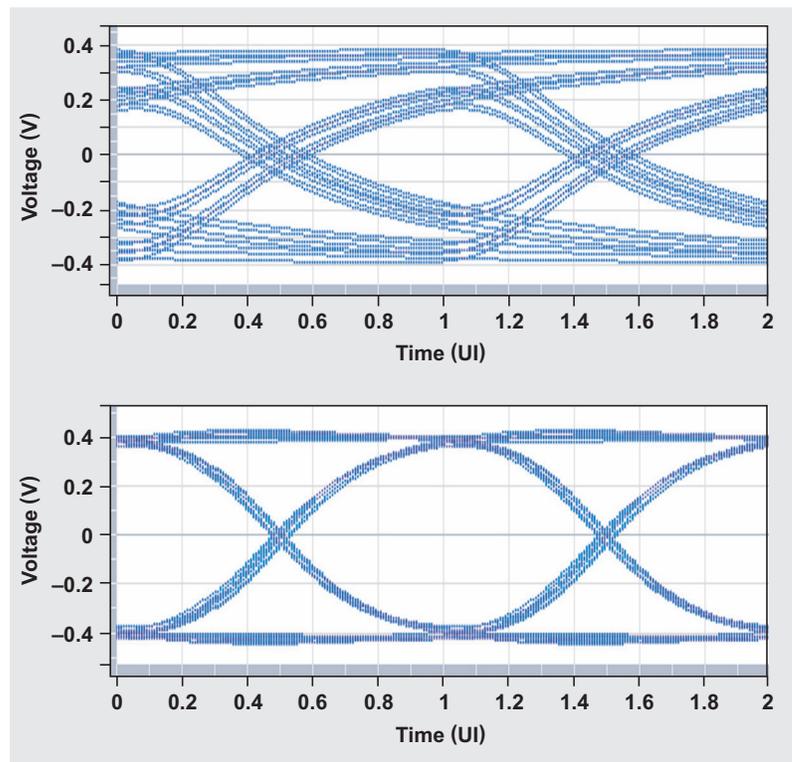


Figure 3. FR4 attenuation and idealized CTLE gain

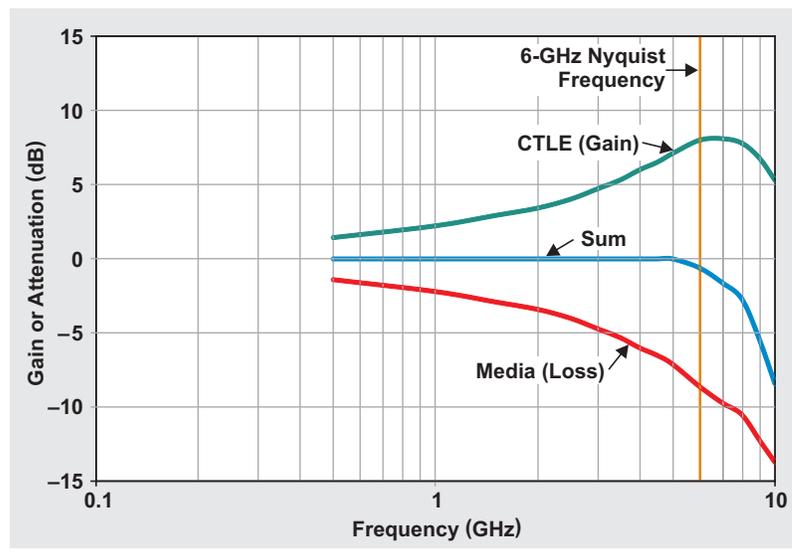
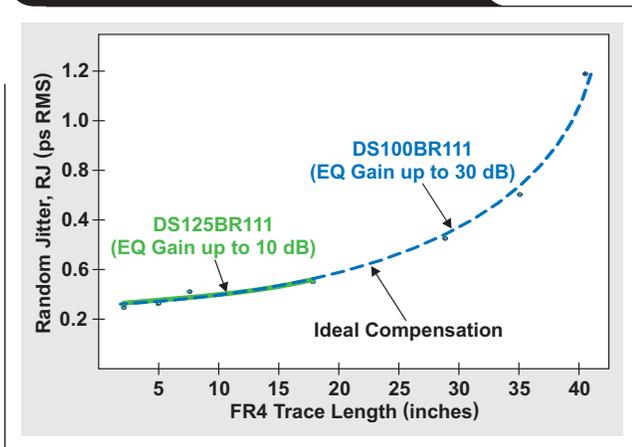


Figure 4. CTLE gain vs. additional RJ



As shown in Figure 4, when higher levels of CTLE gain are required to compensate for transmission losses, jitter-decomposition software recognizes the increased levels of RJ. High levels of RJ can result in bit errors. Fortunately, CTLE in a low-to-medium dose can be applied without significant increases in measured RJ. In fact, CTLE solutions continue to be specified and used for media compensation at data rates above 25 Gbps. Currently, 25-Gbps interfaces are limited to a very small portion of the total interface market. Most designers still have the opportunity to come up to speed in standards like PCI Express® (PCIe), 10-gigabit Ethernet (10GbE), and serial attached SCSI (SAS), which range from 8 to 12 Gbps.

Link training

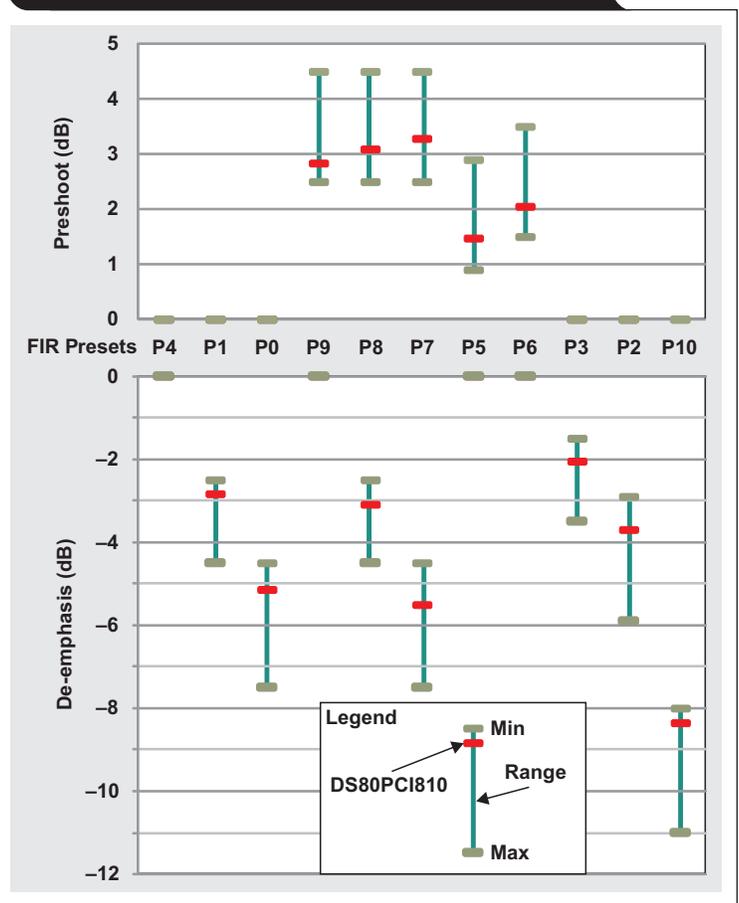
One thing all these standards have in common is the concept of link training and adaptive signal conditioning. Although the specifics and algorithms will vary, all incorporate methods that allow receivers (Rx) to feedback or recommend finite impulse response (FIR) coefficient changes to the transmit (Tx) device. Working through this process enables the Rx/Tx pair to arrive at a total channel solution for signal compensation without external intervention. A linear equalizer inserted into a lossy channel designed to use link training must maintain and preserve the linearity of the channel while providing sufficient gain to effectively turn a long channel into a shorter, less lossy channel. The DS125BR820 exhibits sufficient bandwidth and dynamic range to accommodate maximum-amplitude signals from industry-standard transmitters.

In PCIe applications, a linear equalizer can be placed adjacent to an add-in-card (AIC) connector. Standards-based software testing is used to exercise the host transmitter to sequence through the full range of Tx preset values with varied amounts of FIR energy. A comparison in both Table 1 and Figure 5 shows how an equalizer can

Table 1. Ideal and measured PCIe transmit preset values

| PCIe Tx Preset | Preset Binary Value | Ideal Vb | Measured Vb | Ideal | | Measured | |
|----------------|---------------------|----------|-------------|-------------|------------|-------------|------------|
| | | | | Post Cursor | Pre Cursor | Post Cursor | Pre Cursor |
| P4 | 0100'b | 1000 | 1070 | 0 | 0 | 0 | 0 |
| P1 | 0001'b | 668 | 772 | -3.5 | 0 | -2.8 | 0 |
| P0 | 0000'b | 500 | 592 | -6 | 0 | -5.1 | 0 |
| P9 | 1001'b | 668 | 772 | 0 | 3.5 | 0 | 2.8 |
| P8 | 1000'b | 501 | 592 | -3.5 | 3.5 | -3.1 | 3.1 |
| P7 | 0111'b | 402 | 479 | -6 | 3.5 | -5.5 | 3.3 |
| P5 | 0101'b | 803 | 903 | 0 | 2 | 0 | 1.5 |
| P6 | 0110'b | 750 | 845 | 0 | 2.5 | 0 | 2.1 |
| P3 | 0011'b | 750 | 845 | -2.5 | 0 | -2.1 | 0 |
| P2 | 0010'b | 603 | 699 | -4.5 | 0 | -3.7 | 0 |
| P10 | 1010'b | 335 | 409 | -9.5 | 0 | -8.4 | 0 |

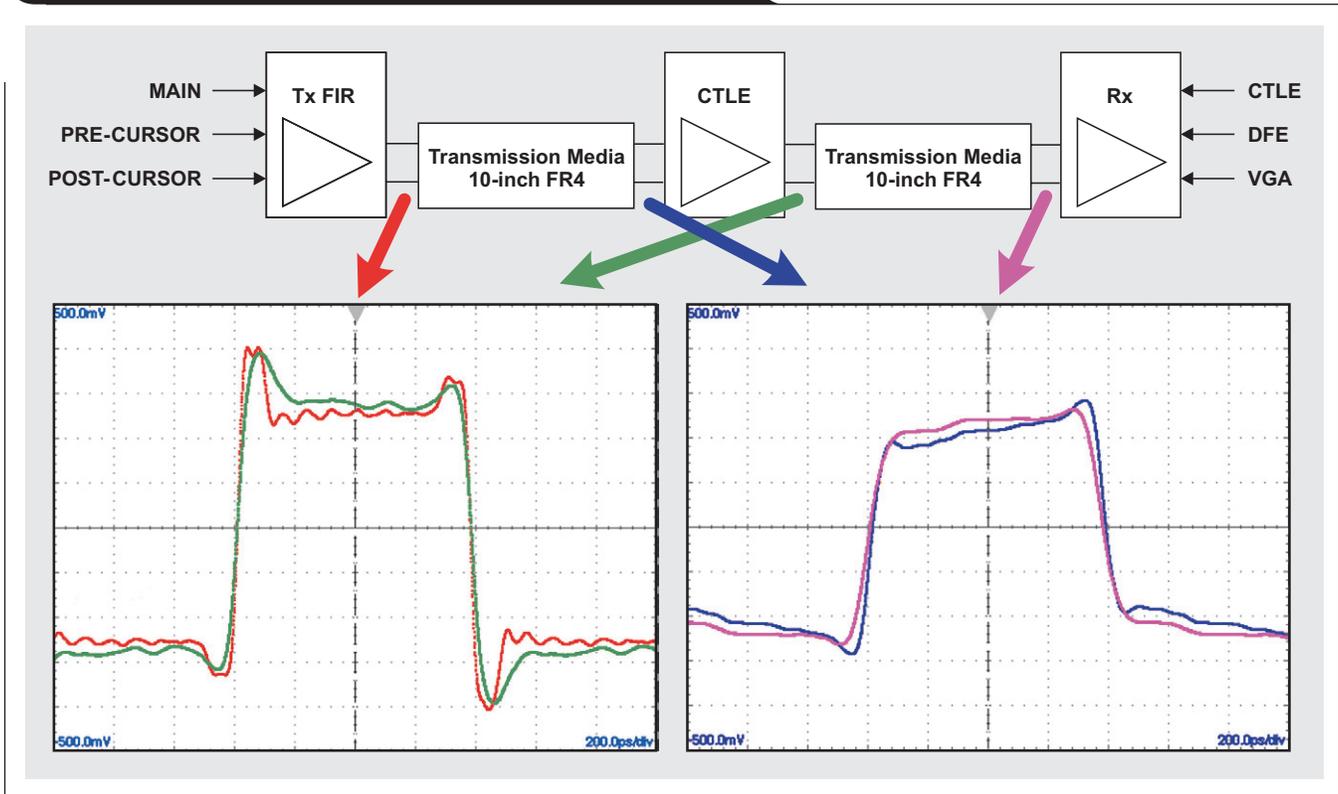
Figure 5. Graphical representation of measured PCIe Tx preset values



preserve the pre-cursor and post-cursor energy within the allowed PCIe standard margins.

The combination of linear equalization and output drive creates a high level of FIR transparency. This enables the equalizer to reproduce and successfully pass on all

Figure 6. Restored TX FIR energy using linear equalization



PCIe 3.0 Tx preset values at the AIC connector. PCIe 3.0 performance of the DS80PCI810 from Texas Instruments has been verified at a recent PCI-SIG Compliance Workshop. As of this article's publication, it is the only linear equalizer currently listed on the PCIe 3.0 Integrator's List. PCIe Tx presets are tested using a specific compliance pattern and oscilloscope software to extract and calculate the measurement values. This testing helps to ensure robust operation in PCIe-compliant channels.

While a system integrator looks at this type of specification and measured data with a very critical eye, a more intuitive feel for the CTLE performance is easier to generate with waveforms captured at the full bit rate or speed. In a modern digital system, it is important to understand the waveform characteristics at several locations within the transmission channel. The waveform sequence in Figure 6 shows a 10GbE waveform at several points (match arrow color to waveform color) along the channel.

Modern methods of adapting Tx and Rx equalization easily allow for 20- to 30-inch links at the 10-Gbps data rate. The additional linear equalizer may not always be a requirement at this distance, but it is a good length to show how a linear equalization scheme can effectively reduce the equalization requirements of other system-level components. As seen in Figure 6, a linear equalizer can restore lost amplitude to the high-frequency components embedded in the waveform transitions while simultaneously preserving the low-frequency amplitude characteristics. By placing the CTLE midway through the

20-inch channel, it allows the waveforms to be paired up to show equivalent waveforms at the CTLE input and Rx input. Inserting the CTLE has reduced the effective channel length by 10 inches or almost 9 dB.

Conclusion

Using linear equalization adds mere picoseconds of latency and minimal additive jitter to the serial link. This increases the effective solution space for transmission and reception of high-speed signals. It is clear that digital-signal processing and communication will continue to dominate the infrastructure of new communication standards. However, the use of linear equalization in the analog domain still plays an important support role in the realm of high-speed signal conditioning, thereby ensuring robust error-free operation across a broad spectrum of serial protocols, including 10GbE Ethernet, PCIe and SAS.

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Stabilizing difference amplifiers for headphone applications

By John Caldwell

Analog Applications Engineer

Introduction

The recent increase in popularity of high-fidelity headphones and lossless audio formats has caused many manufacturers of personal electronics to add high-quality audio outputs to their devices. As a result, 24-bit/192-kHz audio digital-to-analog converters (DACs), once reserved for home high-fidelity systems, are now being incorporated into mobile devices such as cell phones, tablets, and portable music players. These DACs deliver extremely low-distortion signals, but are unable to drive headphones directly. To take full advantage of these high-performance parts, a well-designed headphone amplifier must also be added to the system.

Traditional headphone amplifier circuit

The DAC output is often a differential signal which must be converted to a single-ended signal by the headphone amplifier circuit. In Figure 1, a traditional difference amplifier consists of an operational amplifier (op amp) and four matched resistors that amplifies the difference between the complementary DAC outputs. The amplifier also rejects signals common to both outputs, such as even-order distortion. The amplifier should not add unwanted noise or distortion to the signal, or change the system's overall frequency response. Perhaps, most importantly, the amplifier must be stable when headphones are connected to the output. As fundamental as this last point is, it is often overlooked in headphone amplifier design.

Headphone impedance characteristics

Headphones are not a simple resistive load, although their nominal impedance specifications (typically between 16 and 600 Ω) would seem to imply otherwise. Figure 2 shows the measured impedance of a 64- Ω (nominal) headphone from 10 Hz to 10 MHz (1 channel shown). The red curve gives the impedance magnitude and the blue curve is the phase angle.

Figure 1. A traditional difference amplifier converts differential output to a single-ended signal

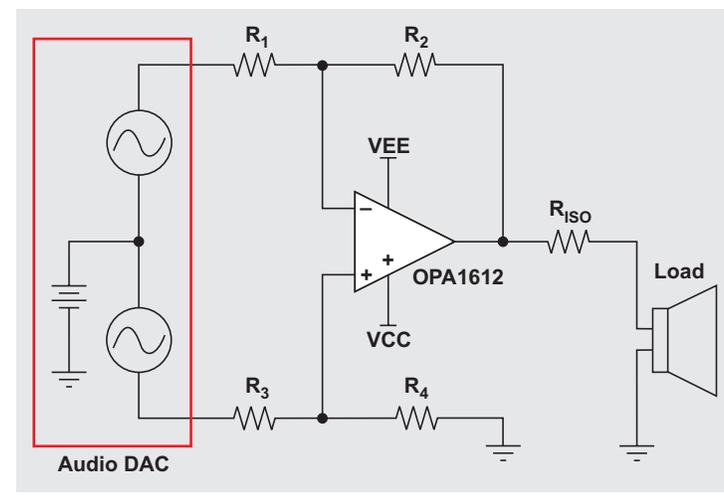
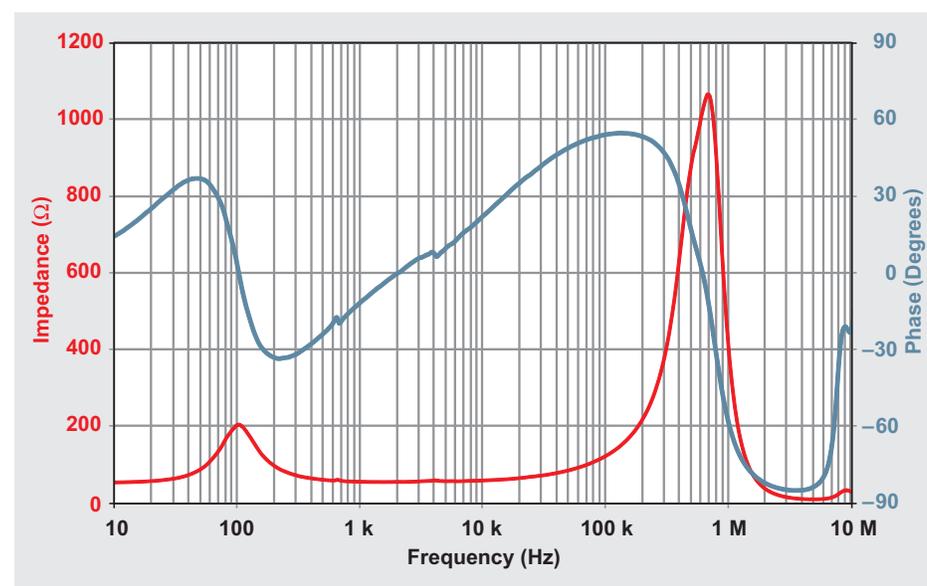


Figure 2. Measured impedance of 64- Ω headphones



Two resonant peaks are clearly evident in the impedance plot. The low-frequency resonance at 100 Hz is produced by the mechanical and electrical properties of the drivers in the headphones. The high-frequency resonance is created from the interaction of the cable

capacitance with the inductance of the cable and driver voice coil. From a stability perspective, the high-frequency resonance has the potential to cause the most problems. Above this resonant point, the headphone is a capacitive load, as is evident from negative phase angle. Capacitive loads introduce a pole into the open-loop gain curve of an amplifier, degrading the phase margin and potentially causing oscillation.

The most common solution to this issue is to add a resistor (R_{ISO} in Figure 1) in series with the amplifier output to isolate the load capacitance from the feedback loop and preserve the phase margin. While this solution is effective at maintaining stability, it also degrades the system's audio performance for several reasons. First, the output voltage of the amplifier circuit is no longer load-independent. Consider that the amplifier's output impedance forms a voltage divider with the load impedance. Because the load is not resistive, as illustrated in Figure 2, the voltage at the headphones varies over frequency.

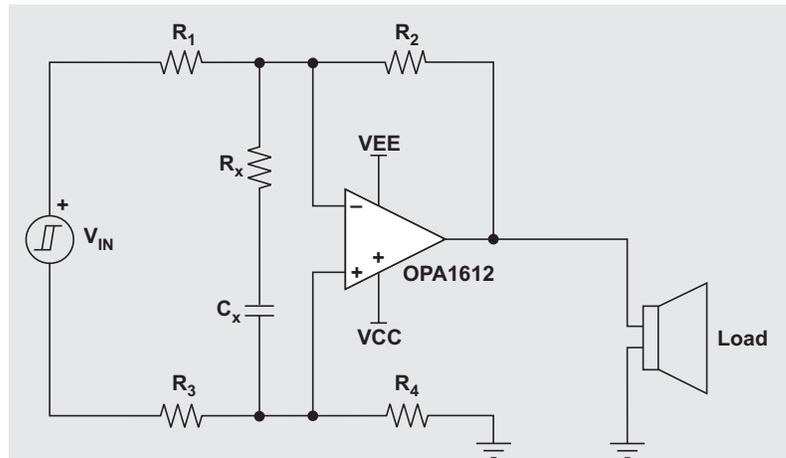
Second, the current drawn by headphone drivers is not perfectly linear. This is partly because the impedance of the driver changes as a function of where the cone and voice coil assembly is in its range of motion. As the cone progresses through its range of motion, the impedance curve may change dramatically, thus distorting the current drawn by the driver. If the amplifier has a non-zero output impedance, this distorted current will also distort the voltage signal at the amplifier output, potentially degrading audio quality^[1]. A low-output impedance is crucial for achieving high performance in headphone amplifier circuits.

Enhanced headphone amplifier circuit

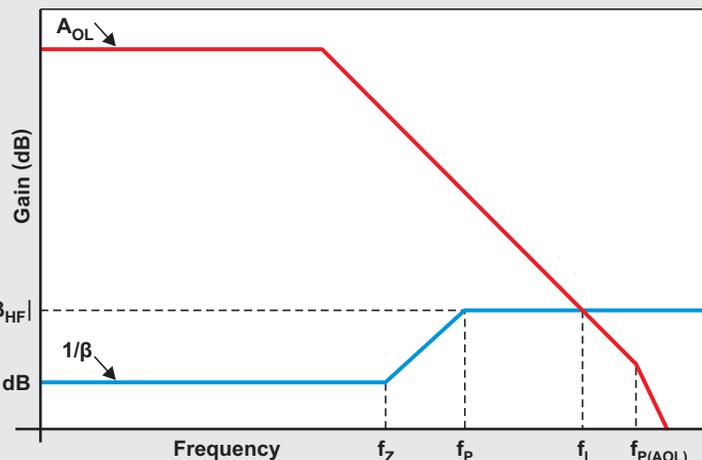
There are some amplifier circuits that solve the problem of driving large capacitive loads while maintaining low output impedance by enclosing the isolation resistor inside the amplifier feedback loop and using a dual feedback topology^[2]. However, in the difference amplifier circuit, enclosing the isolation resistor in the feedback loop degrades the circuit's common-mode rejection ratio (CMRR), which is crucial for eliminating distortion from the DAC output signal.

A solution to this problem is shown in Figure 3a. Figure 3b shows response curves for the open-loop gain (A_{OL}) and the inverse feedback factor ($1/\beta$). In this topology, resistor R_X and capacitor C_X introduce a pole-zero

Figure 3. Amplifier solution for large capacitive loads



(a) Amplifier circuit with R_X/C_X network



(b) Open-loop gain and inverse feedback factor

pair in the $1/\beta$ curve. By increasing the magnitude of $1/\beta$ at the frequency where it intersects the open-loop gain curve (f_i), the system can achieve reasonable phase margin without increasing the output impedance at audio frequencies or degrading the CMRR. Furthermore, adding R_X and C_X to the circuit does not affect the circuit's closed-loop transfer function.

For the circuit in Figure 3a to be stable, the intersection frequency (f_i) must be less than the frequency of the second pole in the A_{OL} curve ($f_{P(AOL)}$), but greater than the pole in the $1/\beta$ curve (f_p):

$$f_{P(AOL)} > f_i > f_p \tag{1}$$

On the other hand, to provide the best audio performance possible, f_z and f_p should be as far above the audio bandwidth as possible. Above the zero-frequency, the noise and distortion of the circuit will be increased by the

reduction in loop gain. As is often the case, the requirements for stability and high performance need to be balanced in the design process.

To illustrate the design of this circuit, an OPA1612 was configured to drive the headphones used for Figure 2. Figure 4 shows the TINA-TI™ simulation schematic for the design process. For simplicity, the four resistors of the difference amplifier are matched (R1, R2, R3, R4 = R).

Inductor LT is used to break the amplifier's feedback loop. The circuit's loop gain is measured by the voltage probe labeled AOLB. The feedback factor, β , is measured directly at the op amp inputs by differential voltage probe B. A differential voltage probe must be used because this technique incorporates both positive and negative feedback. The net feedback factor is the difference of the individual negative and positive feedback factors^[2]. The post-processor in TINA-TI can be used to generate additional curves from these voltage probes. For example, the open-loop gain curve is generated by dividing the loop gain by the feedback factor. The $1/\beta$ curve is produced by taking the inverse of the B probe.

A 400-pF capacitor (CL) connected to the output represents the high-frequency impedance of the headphones. This value is determined by taking the impedance of the headphones (Figure 2) where the phase is most negative, which is a good representation of a worst-case capacitive loading from headphones. In simulation, a second pole in the A_{OL} curve caused by this load capacitance can occur at 5.7 MHz where the A_{OL} magnitude is approximately 25 dB. In order to satisfy the criteria in Equation 1, the magnitude of the inverse feedback factor at high frequencies

$(1/\beta_{HF})$ must be greater than 25 dB. This is calculated using the equation:

$$\left| \frac{1}{\beta_{HF}} \right| = \frac{2R}{R_X} + 2 > 25 \text{ dB} \tag{2}$$

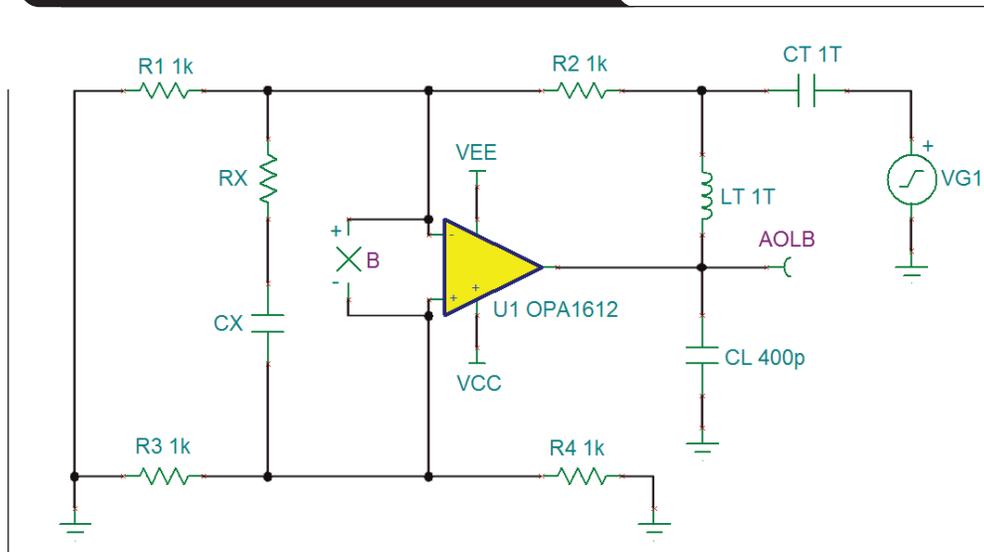
Using 1 k Ω as the value of all difference-amplifier resistors allows the value of R_X to be calculated:

$$\begin{aligned} \left| \frac{1}{\beta_{HF}} \right| &> 10^{\left(\frac{25 \text{ dB}}{20}\right)} = 17.78 \\ &= \frac{2(1 \text{ k}\Omega)}{R_X} + 2 \rightarrow R_X < 126.7 \Omega \end{aligned} \tag{3}$$

A value of 118 Ω for R_X ensures sufficient noise gain for stable operation. Next, C_X was selected so that the pole frequency is well below 5.7 MHz. A conservative design rule is to place the pole frequency at one-tenth the intersection frequency, as long as the resulting zero is not near the audio bandwidth. In this example, placing the pole frequency at 570 kHz would position the zero near 57 kHz, a bit too low for high-performance audio systems. As a compromise, the pole was placed at one-fifth the intersection frequency:

$$\begin{aligned} f_P &= \frac{5.7 \text{ MHz}}{5} = 1.14 \text{ MHz} \\ &= \frac{1}{2\pi C_X R_X} \rightarrow C_X = 1.183 \text{ nF} \end{aligned} \tag{4}$$

Figure 4. TINA-TI™ simulation schematic used to determine loop stability



A value of 1.2 nF is very close to the calculated value for C_X . The resulting zero frequency is:

$$f_z = \frac{1}{2\pi C_X (R_X + R)} = 118.6 \text{ kHz} \quad (5)$$

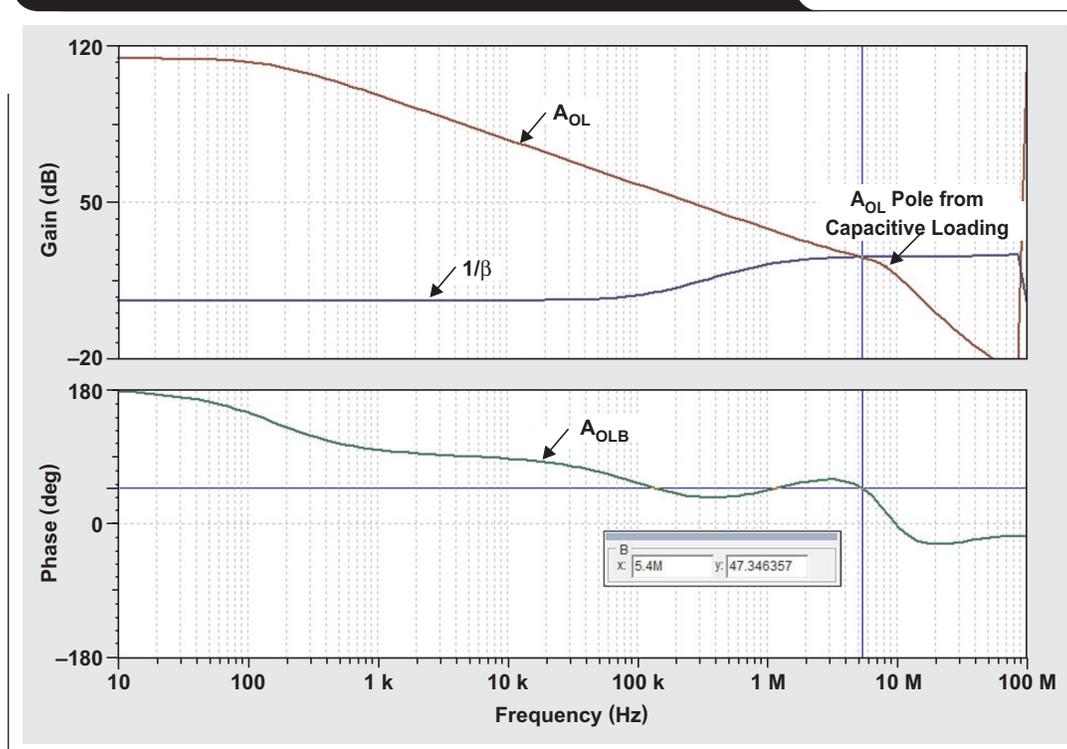
The 118.6-kHz zero frequency is sufficiently above the audio bandwidth to avoid degrading the circuit's performance.

An AC transfer characteristic simulation was performed and the results are shown in Figure 5. The open-loop gain and $1/\beta$ curves are shown in the magnitude plot (top). The $1/\beta$ curve intersects the A_{OL} curve at 5.4 MHz. At this point the phase of the loop gain (A_{OLB} , bottom) shows 47.35° of phase margin. Removing the R_X and C_X network

would cause the $1/\beta$ curve to intersect the A_{OL} curve below the second pole created by the capacitive loading. In this case, the phase at the intersection point becomes -52.37° , which indicates an unstable system.

A difference amplifier circuit employing the previously calculated values of R_X and C_X was built and its measured performance was compared to a traditional difference amplifier using an isolation resistor of 47.5 Ω . The same 64- Ω headphones (Figure 2) were used as the load for these tests. It is extremely important to test headphone amplifier circuits with actual headphones because simply using a resistor will not reveal the detrimental effects of the output impedance.

Figure 5. Loop stability plots generated with TINA-TI™ model



The closed-loop gain of the two circuits is shown in Figure 6. As mentioned previously, the series resistor used for stability forms a voltage divider with the headphone impedance. The result is that the gain of the traditional amplifier circuit varies by 4.13 dB over the measured bandwidth. Conversely, the circuit employing the R_X/C_X network has extremely low output impedance, and its gain is essentially independent of the load impedance. The gain variation of the R_X/C_X circuit is 0.03 dB over the measurement bandwidth.

The effects of the series output resistor are also evident in the measured total harmonic distortion (THD) when driving the 64- Ω headphones. Figure 7 shows plots for the measured THD versus frequency for the two solutions with a 300-mV_{rms} output level. Adding a series resistor drastically reduces the THD performance due to the non-linear current draw of the headphones. At low frequencies, where the cone excursion of the headphone drivers is highest, the THD is over 55 dB worse for the traditional amplifier that employed a series output resistor.

Conclusion

Stabilizing headphone amplifiers is a unique challenge because of the difference amplifier circuit topology and the requirements for low output impedance, low distortion, low noise, and high CMRR. The enhanced amplifier solution presented allows for stable operation into capacitive loads without increasing the output impedance at low frequencies or degrading the common-mode rejection. Using this technique, headphone amplifier circuits can be designed that are stable for typical headphone loads and provide exceptional audio performance.

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2. J. Graeme, "Optimizing Op Amp Performance," New York, McGraw-Hill, 1997. Print

Figure 6. Measured closed-loop gain of the two amplifiers

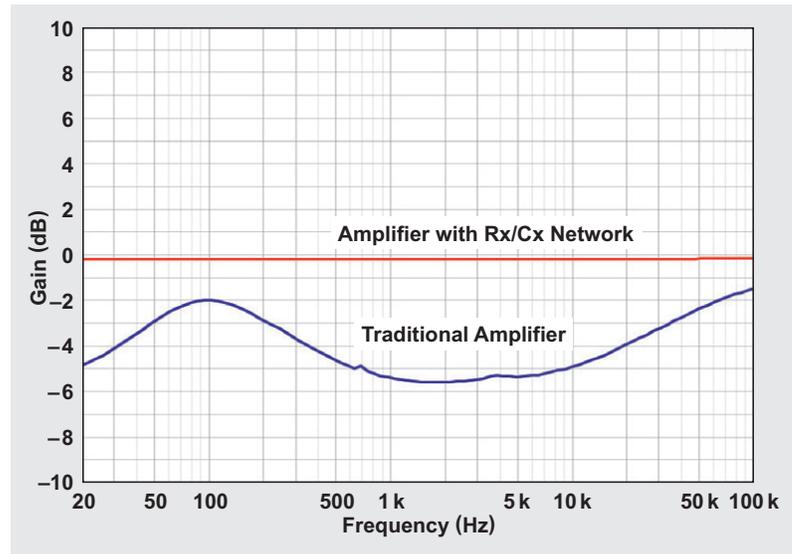
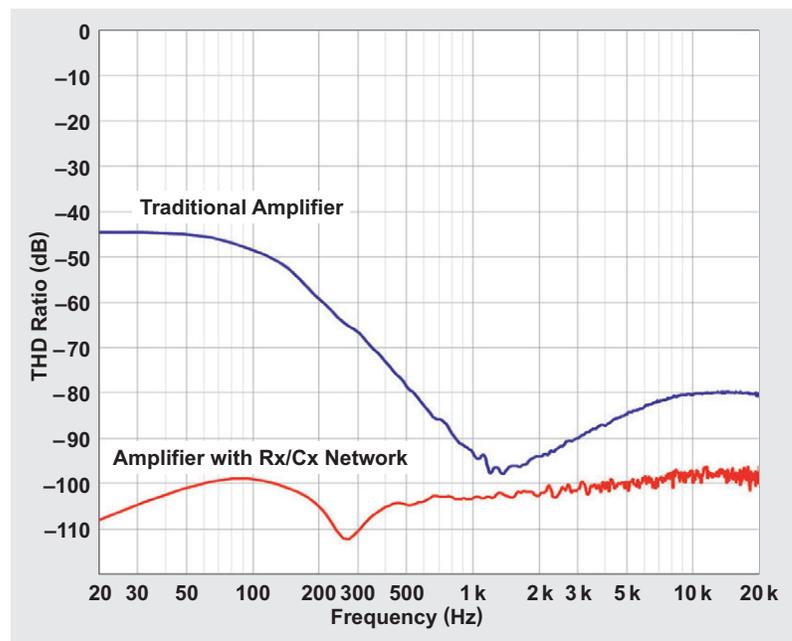


Figure 7. Measured THD of the two solutions



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