High-Performance Analog Products

Analog Applications Journal

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Contents

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Introduction

The *Analog Applications Journal* is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they apply to the following product categories:

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Grounding in mixed-signal systems demystified, Part 1

By Sanjay Pithadia, *Analog Applications Engineer,*
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Introduction

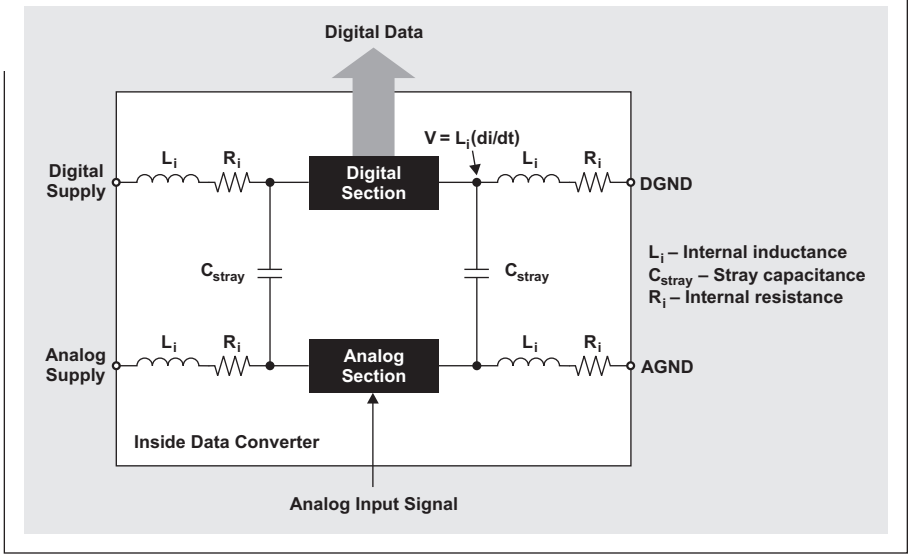
Every signal-processing system requires mixed-signal devices, such as analog-to-digital converters (ADCs) and/or digital-to-analog converters (DACs). The need for processing analog signals with a wide dynamic range imposes the requirement to use high-performance ADCs and DACs. Maintaining performance in a noisy digital environment is dependent upon using good circuit-design techniques like proper signal routing, decoupling, and grounding.

Undoubtedly, grounding is one of the most discussed subjects in system design. Though the basic concepts are relatively simple, the implementation is difficult. For linear systems, the ground is the reference against which the signal is based; and, unfortunately, it also becomes the return path for the power-supply current in unipolar supply systems. An improper application of grounding strategies can degrade the performance in high-accuracy linear systems. There is no "cookbook" that guarantees good results, but there are a few things that, if not done properly, can cause issues.

This article is the first of a two-part series that looks closely at the grounding techniques used in mixed-signal systems. Part 1 explains typical terminologies and ground planes and introduces partitioning methods. Part 2 explores techniques for splitting the ground planes, including pros and cons. It also explains grounding in systems with multiple converters and multiple boards. Part 2 will appear in a future issue of *Analog Applications Journal*.

A term often used in system design is *star ground*. This term builds on the theory that all voltages in a circuit are referred to as a single ground point, or star ground point. The key feature is that all voltages are measured with respect to a particular point in the ground network, not just to an undefined ground wherever one can clip a probe. Practically, it is difficult to implement. For example, in a star ground system, drawing out all signal paths to minimize signal interaction and the effects of high-impedance signal or ground paths causes implementation problems to arise. When power supplies are added to the circuit, either they add unwanted ground paths or their supply currents flowing in the existing ground paths are large enough or noisy enough to corrupt the signal transmission.

Figure 1. AGND and DGND pins in a data converter



Interpretation of AGND and DGND pins in mixed-signal devices

Digital- and analog-design engineers tend to view mixed-signal devices from different perspectives, but every engineer who uses a mixed-signal device is aware of analog ground (AGND) and digital ground (DGND). Many are confused about how to deal with these grounds; and, yes, much of the confusion comes from how the ADC ground pins are labeled. Note that the pin names, AGND and DGND, refer to what's going on inside the component and do not necessarily imply what one should do with the grounds externally. Data-converter datasheets usually suggest tying the analog and digital grounds together at the device. However, the designer may or may not want the data converter to become the system's star ground point. What should be done?

As illustrated in Figure 1, the grounds inside a mixed-signal IC are typically kept separate to avoid coupling digital signals into the analog circuits. An IC designer cannot do anything about the internal inductance and resistance (negligible compared to the inductance) associated with connecting the pads on the chip to the package pins. The rapidly changing digital currents produce a voltage (di/dt) in digital circuits, which inevitably couples into the analog circuits through the stray capacitance.

The IC works well in spite of such coupling. However, in order to prevent further coupling, the AGND and DGND

pins should be joined together externally to the same low-impedance ground plane with minimum lead lengths. Any extra external impedance in the DGND connection can cause more digital noise and, in turn, can couple more digital noise into the analog circuit through the stray capacitance.

Analog or digital ground plane, or both?

Why is a ground plane needed? If a bus wire is used as a ground instead of a plane, calculations must be done to determine the bus wire's voltage drop because of its impedance at the equivalent frequency of most logic transitions. This voltage drop creates an error in the final accuracy of the system. To implement a ground plane, one side of a double-sided PCB is made of continuous copper and is used as a ground. The large amount of metal has the lowest possible resistance and lowest possible inductance because of the large, flattened conductor pattern.

The ground plane acts as a low-impedance return path for decoupling high-frequency currents caused by fast digital logic. It also minimizes emissions from electromagnetic interference/radio-frequency interference (EMI/RFI). Because of the ground plane's shielding action, the circuit's susceptibility to external EMI/RFI is reduced. Ground planes also permit high-speed digital or analog signals to be transmitted via transmission-line (microstrip or stripline) techniques, where controlled impedances are required.

As mentioned earlier, the AGND and DGND pins must be joined together at the device. If the analog and digital grounds have to be separated, should both be tied to the analog ground plane, the digital ground plane, or both?

Remember that a data converter is *analog*! Thus, the AGND and DGND pins should be connected to the analog ground plane. If they are connected to the digital ground plane, the analog input signal is going to have digital noise summed with it, because it is probably single-ended and referenced to the analog ground plane. Connecting the pins to a quiet analog ground plane can inject a small amount of digital noise into it and degrade the noise margin of the output logic. This is because the output logic is now referenced to the analog ground plane and all the other logic is referenced to the digital ground plane. However, these currents should be quite small and can be minimized by ensuring that the converter output does not drive a large fan-out.

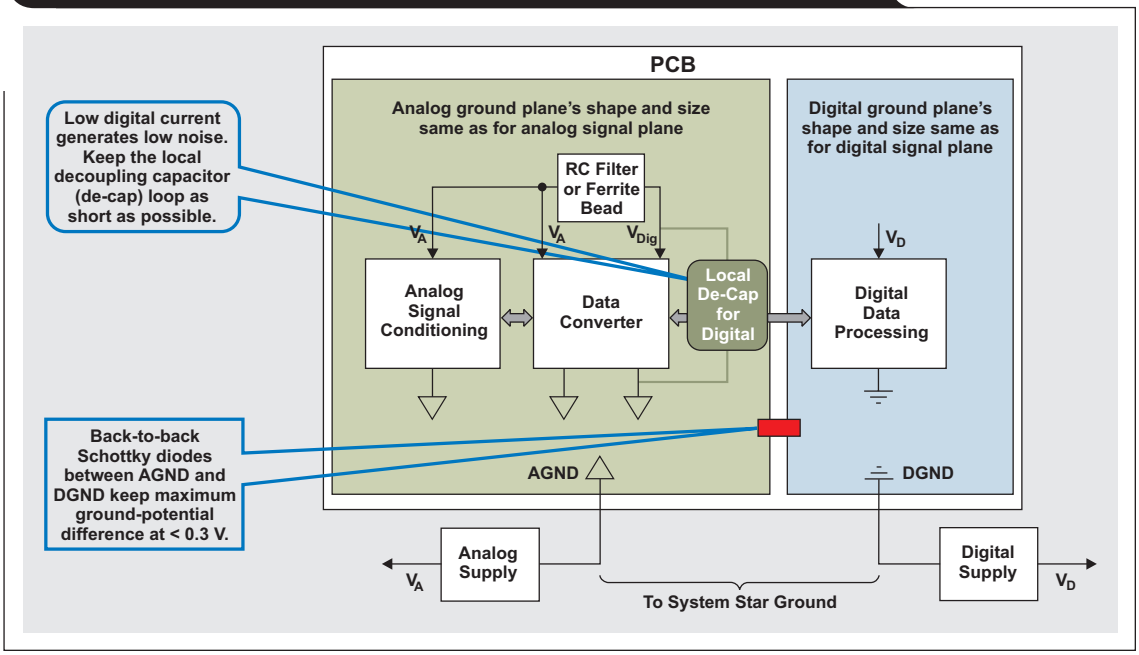
It is possible that the devices used in a design have either low digital currents or high digital currents. The grounding scheme is different for both cases. Traditionally, data converters may be thought of as low-current devices (such as flash ADC). But today's data converters with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC contains a complex digital filter that adds considerably to the digital current in the device.

Grounding data converters with low digital currents

As mentioned, a data converter (or any mixed-signal device) is analog. In any system, the analog signal plane is where all the analog circuitry and mixed-signal devices are placed. Similarly, the digital signal plane has all the digital data-processing circuits. The analog and digital ground planes should have the same size and shape as the respective signal planes.

Figure 2 summarizes the approach for grounding a mixed-signal device with low digital currents. The analog ground plane is not corrupted because the small digital

Figure 2. Grounding data converters with low internal digital currents



transient currents flow in the small loop between V_{Dig}, the local decoupling capacitor, and DGND (the green line). Figure 2 also shows a filter between the analog and digital power supplies. There are two types of ferrite beads: high-Q resonant beads and low-Q nonresonant beads. Low-Q beads are commonly used for power-supply filtering in series with the power connection.

Grounding data converters with high digital currents

The circuit in Figure 2 depends on the decoupling capacitor between V_{Dig} and DGND to keep the digital transient currents isolated in a small loop. However, if the digital currents are significant enough and have components at DC or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current that flows outside the loop between V_{Dig} and DGND must flow through the analog ground plane. This may degrade performance, especially in high-resolution systems. An alternative grounding method for a mixed-signal device with high levels of digital currents is shown in Figure 3. The AGND pin of the data converter is connected to the analog ground plane, and the DGND pin is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the device's AGND and DGND pins. The analog and digital circuits must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

Connecting analog and digital ground planes

Figures 2 and 3 show optional back-to-back Schottky diodes connecting the analog and digital ground planes. The Schottky diodes prevent large DC voltages or low-frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed-signal IC if they exceed 0.3 V, because they appear directly between the AGND and DGND pins.

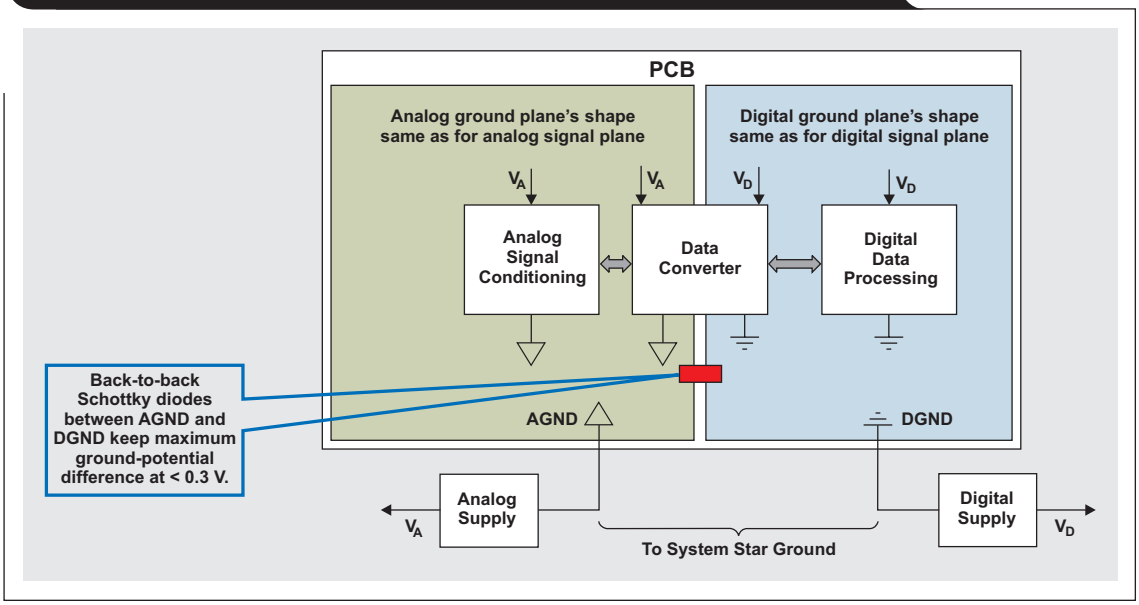
As an alternative to the back-to-back Schottky diodes, a ferrite bead can provide a DC connection between the two planes but isolate them at frequencies above a few megahertz where the ferrite bead becomes resistive. This protects the IC from DC voltages between AGND and DGND, but the DC connection provided by the ferrite bead can introduce unwanted DC ground loops and may not be suitable for high-resolution systems. Whenever AGND and DGND pins are separated in the special case of ICs with high digital currents, provisions should be made to connect them together if necessary.

Jumpers and/or strap options allow both methods to be tried to verify which gives the best overall system performance.

Isolation or partitioning: Which is important for ground planes?

A common concern is how to isolate the grounds so that the analog circuit does not interfere with the digital circuit. It is a well-known fact that digital circuitry is noisy. Saturating logic draws large, fast current spikes from its supply during switching. Conversely, analog circuitry is quite vulnerable to noise. It is not that the analog circuit might interfere with the digital logic. Rather, it is possible that the high-speed digital logic might interfere with the low-level analog circuits. So the concern should be how to prevent digital-logic ground currents from contaminating the low-level analog circuitry on a mixed-signal PCB. The first thought might be to split the ground planes to isolate DGND from AGND. Although the split-plane approach can

Figure 3. Grounding data converters with high internal digital currents



be made to work, it has many problems--especially in large, complex systems.

There are two basic principles of electromagnetic compatibility (EMC):

1. Currents should be returned to their sources locally and as compactly as possible. If not, a loop antenna should be created.
2. A system should have only one reference plane, as two references create a dipole antenna.

During EMC tests, most problems are observed when traces are routed across a slot or a split in a ground or power plane. Since this routing causes both radiation and crosstalk issues, it is not recommended.

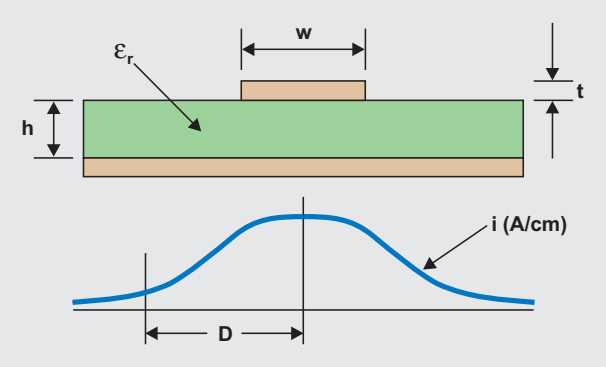
It is important to understand how and where the ground currents in a split plane actually flow. Most designers think only about where the signal current flows and ignore the path taken by the return current. The high-frequency signals have a characteristic of following the path of least impedance (inductance). The path's inductance is determined by the loop area that the path encloses. The larger the area that the current has to travel to return to the source, the larger the inductance will be. The smallest inductance path is directly next to the trace. So, regardless of the plane--power or ground--the return current flows on the plane adjacent to the trace. The current spreads out slightly in the plane but otherwise stays under the trace. The actual distribution is similar to a Gaussian curve in nature. Figure 4 illustrates that the return-current flow is directly below the signal trace. This creates the path of least impedance.

The current-distribution curve for the return path is defined by

$$i\ (A/cm) = \frac{I_O}{\pi h} \times \frac{1}{1+\left(\frac{D}{h}\right)^2},$$

where I_O is the total signal current (A), h is the height of the trace (cm), and D is the distance from the trace (cm). From this equation it can be concluded that digital ground currents resist flowing through the analog portion of the ground plane and so will not corrupt the analog signal.

Figure 4. Distribution of return current



For reference planes, it is important that the clearance sections of vias do not interfere with the return current's path. In the case of an obstacle, the return current finds a way around it, as shown in Figure 5. However, this rerouting will most likely cause the current's electromagnetic fields to interfere with the fields of other signal traces, introducing crosstalk. Moreover, this obstacle adversely affects the impedance of the traces passing over it, leading to discontinuities and increased EMI.

Part 2 of this two-part article series will discuss the pros and cons involved in splitting the ground planes and will also explain grounding in systems with multiple converters and multiple boards.

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2. "Analog-to-digital converter grounding practices affect system performance," Application Report. Available: www.ti.com/sbaa052-aaj

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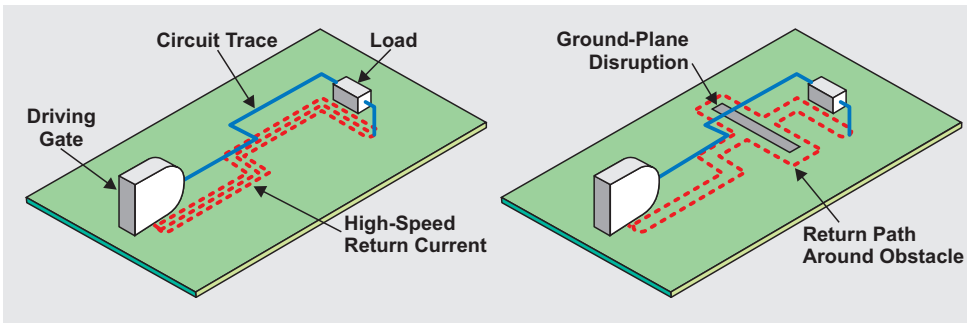
Figure 5. Return current with and without slot



Add a digitally controlled PGA with noise filter to an ADC

By Kai Gossner
Field Application Engineer

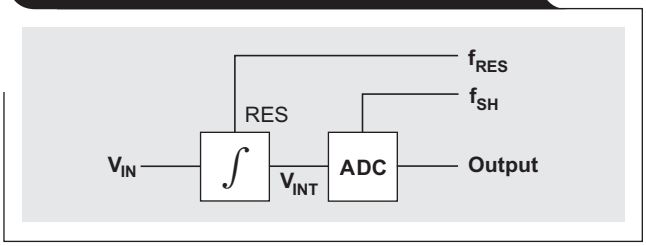
Introduction

In some applications, a signal with high dynamic range needs to be digitized. A common method of digitization is to add an external programmable gain amplifier (PGA) in front of the analog-to-digital converter (ADC). Only a few microcontrollers have internal PGAs. However, nowadays PGAs are available in a single chip with one or multiple input channels. Such PGAs add additional costs to the system and usually consume more power as a fixed-gain solution.

This article describes how to implement a PGA by using just a single resettable integrator, with the following benefits:

- The solution is economical and easy to design.
- Gain can be digitally controlled and calibrated.
- Signal noise is reduced with a low-pass filter, which is especially useful in noisy microcontroller environments and for small analog signals. The cutoff frequency automatically adjusts with the chosen sample rate.
- The zero-level voltage reference can be controlled externally, which makes it handy for single-supply circuits where the zero level usually is set to $V_{REF}/2$.

Figure 1. Basic block diagram of the PGA



The basic circuit

Figure 1 shows the basic circuit, where an integrator is added in front of the ADC. The integrator can be reset with the signal f_{RES} (1 = integrator is reset). The ADC is controlled with the signal f_{SH}, which connects to the ADC's sample-and-hold (SH) unit (1 = sample, 0 = hold). A falling edge starts the analog-to-digital conversion cycle.

Figure 2 shows a single analog-to-digital (A/D) conversion cycle with the circuit from Figure 1. The cycle is split into four periods:

1. *Integrator reset period:* Resets the integrator to "0."
2. *Integration period:* The integrator reset signal is released and the integrator starts to integrate.
3. *Sample period:* The ADC's sample-and-hold unit samples the integrator output, V_{INT}.
4. *A/D conversion period:* The sample-and-hold unit holds the voltage, and the ADC starts to convert.

Figure 2. Single A/D cycle with gain = 1

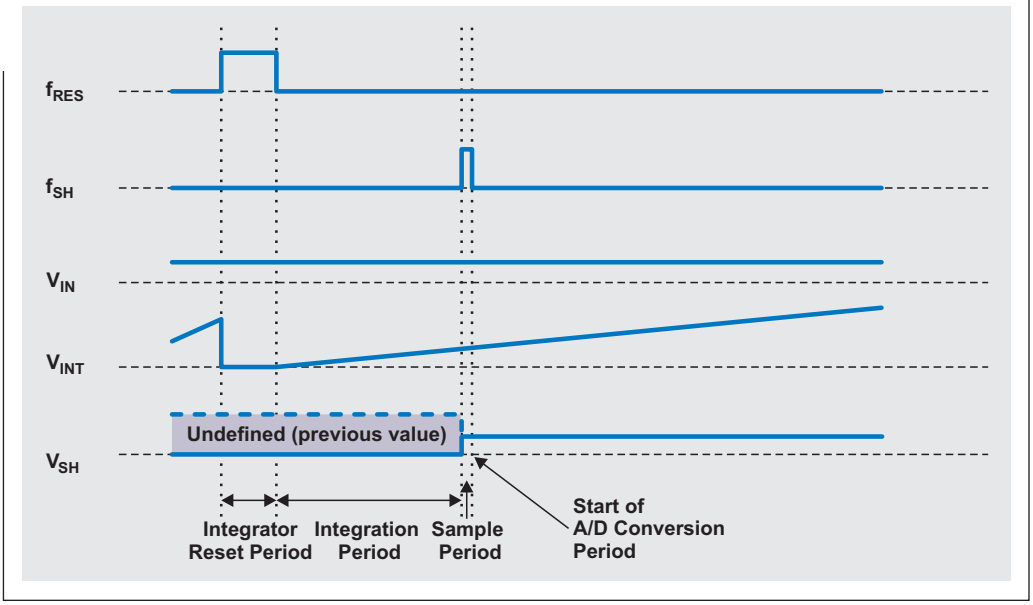
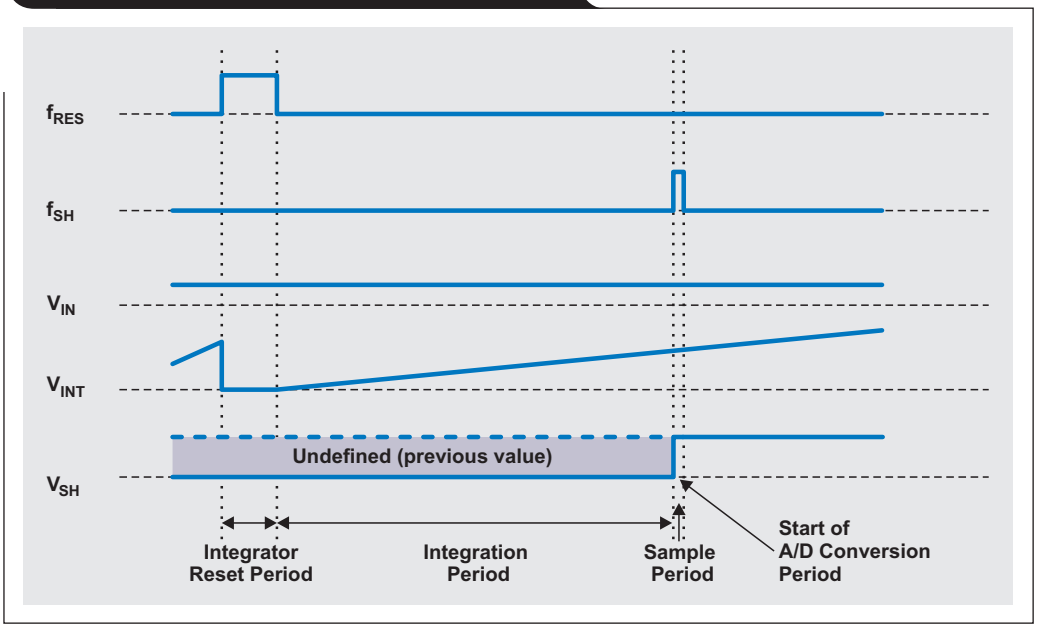


Figure 3. Single A/D cycle with PGA gain = 2



The duration of the integration period defines the PGA's gain, as the voltage on its input influences the slope linearly: A doubling of the integration time doubles the gain. Figure 3 demonstrates this influence. The integration period is doubled and the voltages V_{SH} are increased by a factor of two.

A nice benefit from this integration scheme is that the input signal is averaged during the integration period, which reduces out-of-band noise from the input signal, V_{IN}. The filter's impulse response is of finite duration and is comparable to the behavior of a digital FIR filter rather than to that of a standard low-pass filter.

Practical configuration of a PGA

An inverting amplifier can be built with a single operational amplifier (Figure 4). The integrator can be reset by short-circuiting the capacitor, C, with the switch element, S. The components R and C influence the integrator's gain.

The signal V_{COM} defines the integrator's zero-level voltage and can be set, for example, to $V_{REF}/2$, where V_{REF} is the ADC's reference voltage. The integrator is reset to this voltage when the capacitor is discharged. Usually a V_{COM} signal is present in the system anyway. Often it is used as a virtual ground or bias voltage for single-supply analog signal chains.

Figure 4. Practical configuration of the PGA

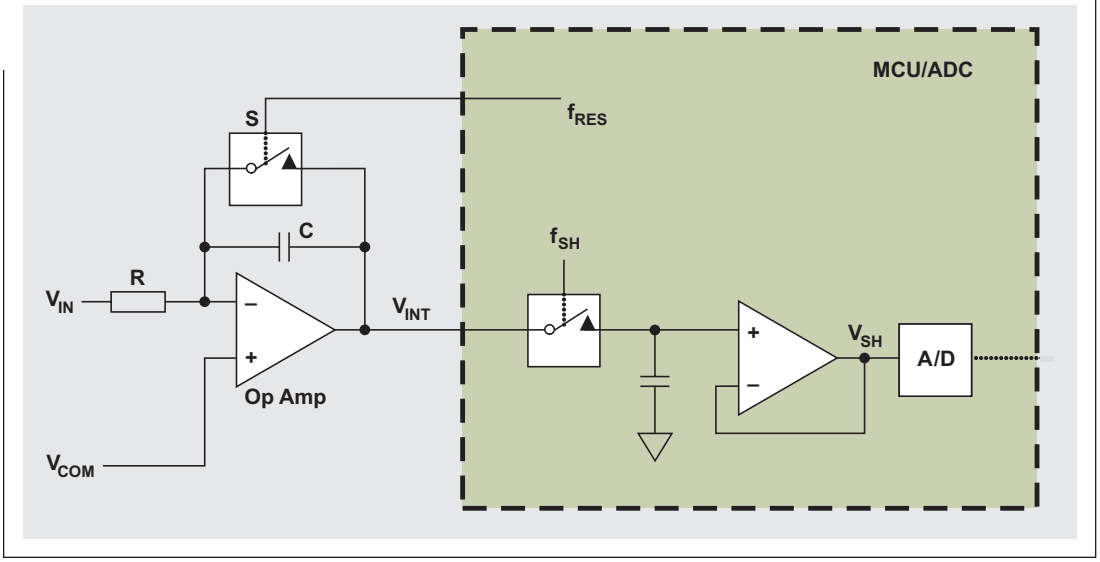


Figure 5. SPICE-simulation results of circuit in Figure 4

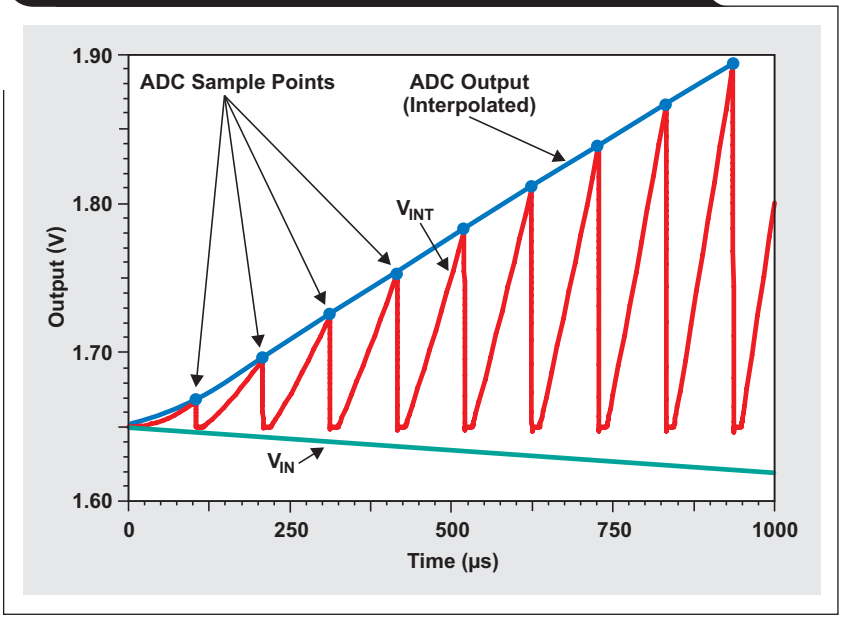


Figure 5 shows SPICE-simulation results of the circuit in Figure 4. The blue dots mark the sample moments of the ADC. As shown, the signal V_{IN} is amplified by a factor of about –8. The red signal is inverted to the green due to the integrator's inverting behavior.

How it works

The sample rate, the maximum desired gain, and the A/D conversion time influence the selection of the integration constant defined by the components R and C. As shown in Figures 2 and 3, the integrator needs enough time to reach the gain, G, within the duration of the integration period, t. The dependency of G and t can be calculated as

$$G = \frac{-t}{R \times C}.$$

The close time (integrator reset period) of the switch (S) depends on the impedance of the switch and the value of the capacitor (C).

Calibration

Tolerances of R and C lead to modification of the gain factor. The capacitor should have a very small piezo effect to get a very linear integration. Capacitors can have an especially large tolerance--for example, 20%. This is just the initial tolerance, which can be calibrated once. Tolerances due to aging effects are very small (less than 1% per year).

The gain and offset can be calibrated in the same way as with a standard ADC by applying known voltages to the input and calculating correction values for offset and gain based on expected and actual values. The calibration can be done for each gain factor used in the application.

Circuit variations

Using the PGA as a low-pass filter only (gain = 1)

In case input-signal amplification is not wanted, it is possible to use the PGA circuit only as a noise filter. The integrator constant can be set to a value that leads to a fixed

gain of 1. In this case the integration phase can start immediately after the sample, and the hold stage can be set to hold mode (Figure 6).

Non-inverting integration

The circuit in Figure 4 uses an inverting integrator. When this inversion is not acceptable, it is possible to use a non-inverting integrator by adding a single-supply inverting buffer in front of the integrator.

Conclusion

This article has presented a cost-effective and simple way to implement PGA functionality in cost- and power-driven applications. Its filtering properties also reduce costs by eliminating the need for an external filter, which is often present in front of ADCs. Nevertheless, this method cannot replace a PGA in all cases; for example, high sample rates or very large gain variations make such a solution difficult to realize.

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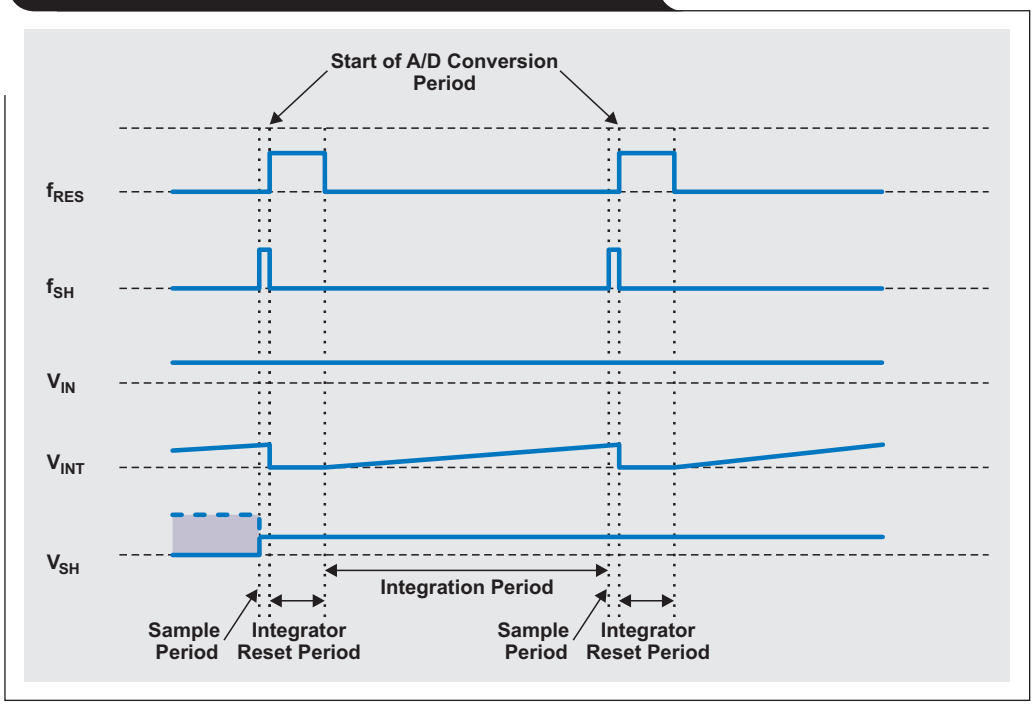
Figure 6. PGA circuit used as a filter only (gain = 1)



Design of a 60-A interleaved active-clamp forward converter

By Brian King
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Introduction

In 48-V-input telecommunications systems, power supplies with a capacity of 100 to 250 W are sufficient to cover many applications. Forward converters are a good choice for these applications. At lower output voltages, synchronous rectification in the secondary circuitry improves efficiency and simplifies system thermal design. Active-clamp forward converters work well in these applications because of the ease of implementing synchronous rectification.

In most cases, the output currents of forward converters are commonly limited to around 30 A. Beyond this current, the inductor design and conduction losses in the secondary circuitry become difficult to manage. From a power standpoint, the primary circuitry (number of parallel FETs) becomes a limiting factor for power ratings above 250 W. In systems with higher power, it is necessary to move to a different topology like the full bridge, or operate two or more forward converters in parallel to increase the output power.

Load-share ICs work great for paralleling supplies that use diodes to rectify their outputs. Diode-rectified supplies allow current to be sourced only from the power supply. Power supplies with synchronous rectifiers, however, can both source and sink power, which can wreak havoc with some load-share controllers. This is particularly true at start-up, where the feedback loop is overridden by the primary controller's slow-start circuit, and the two paralleled supplies could attempt to regulate the output to different voltage levels. These issues can be circumvented by interleaving two separate power stages. This article presents the design of a 5-V, 300-W interleaved isolated supply that is powered from a standard 36- to 72-V telecom input.

Designing the interleaved power stage

In this design example, splitting the power into two interleaved power stages reduces the current in the secondary of each phase to 30 A. This is much more manageable than the 60 A that would be required in a single-phase supply. Both phases actually need to be designed to carry a little more than 30 A to account for phase imbalances. Designing the power stage begins by selecting the turns ratio and inductance for the power transformers. A feature of the active-clamp forward converter is its ability to run at duty cycles of over 50%. It is best to design for a maximum duty cycle of no greater than 75% so that the transformer's reset voltage does not become excessive. In this example, a turns ratio of 4.5:1 results in a duty cycle of around 63% at a 36-V input. Switching each phase at 200 kHz provides a good balance between size and efficiency. Setting the primary inductance at 100 µH ensures that sufficient magnetizing current is flowing to drive the commutation of the power MOSFETs during the switching transitions. The primary inductance and switching frequency determine the value of the resonant capacitor in the clamp. In this case, a 0.1-µF capacitor sets the resonant frequency at 50 kHz.

The output inductors are determined just as in any buck-derived topology. An inductance of 2 µH is used, resulting in 8.5 A of peak-to-peak ripple current in each phase with a worst-case input of 72 V. Accounting for a 20% phase imbalance, the inductor must be able to carry at least 41 A of peak current without saturating.

The output capacitors are selected to meet the requirements for output ripple voltage and for voltage excursions due to load transients. Interleaving the power stages results in some cancellation of the ripple current seen by the output capacitors. The amount of ripple-current cancellation is dependent on the duty cycle and the phase angle between the two phases. Total cancellation occurs with a 50% duty cycle only when the two phases are synchronized 180° out of phase. This reduction in ripple current reduces the number of capacitors required based on the ripple-voltage requirements and the RMS current ratings of the capacitors. For this design, four 180-µF polymer capacitors rated for 4-A RMS each are sufficient to keep the peak-to-peak ripple voltage below 50 mV. More capacitance can be added to support large load transients if necessary.

Selecting the primary MOSFETs is also straightforward. The peak drain voltage is the sum of the input voltage and the resonant transformer's reset voltage. The RMS primary current comprises the reflected load current and the transformer magnetizing current. It is important to select a minimal number of cost-effective transistors and to keep the power loss in each transistor manageable. For this design, each phase uses two 150-V, 50-mΩ MOSFETs in parallel, with a worst-case loss per FET of approximately 700 mW.

Figure 1 shows how self-driven synchronous rectifiers are implemented in each phase of the active-clamp forward converter. One set of synchronous rectifiers (Q4, Q5, and Q6) sees the input voltage reflected through the transformer, while the other set (Q1, Q2, and Q3) sees the transformer's reset voltage reflected to the secondary side. With the selected turns ratio, MOSFETs rated at 30 V are sufficient for this design. Most of the power loss in these components is due to conduction loss. Paralleling multiple 7-mΩ MOSFETs for each phase results in a worst-case loss per FET of around 800 mW. This ensures that the junction temperatures are reasonable, even with a 20% phase imbalance. The gate-drive components Q12, Q13, Q15, and Q16 serve two functions. First, they protect the MOSFET gates from voltage spikes on the switching waveforms. Second, they provide a buffer so that the transformer's secondary windings are not directly connected to a large amount of gate capacitance. This is important to ensure that the power MOSFETs commutate quickly during the switching transitions.

Figure 1. Gate-drive conditioning circuitry for a self-drive synchronous rectifier

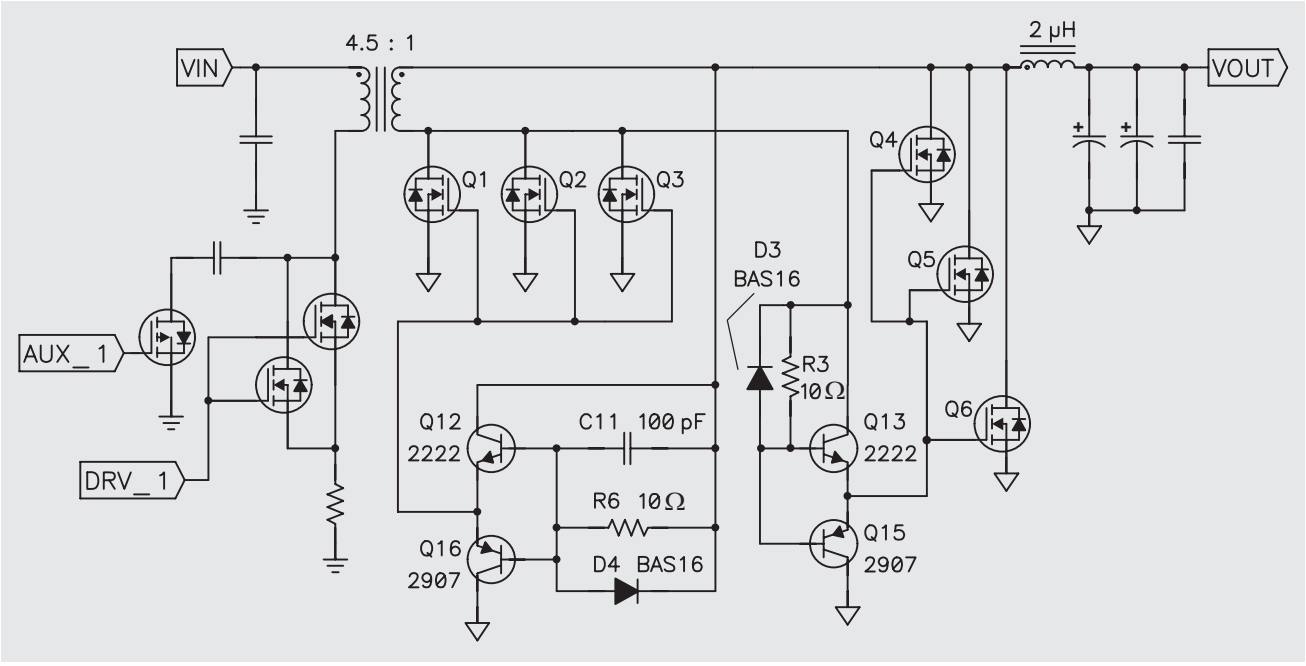


Figure 2. Interleaved controllers sharing feedback network and soft-start circuit

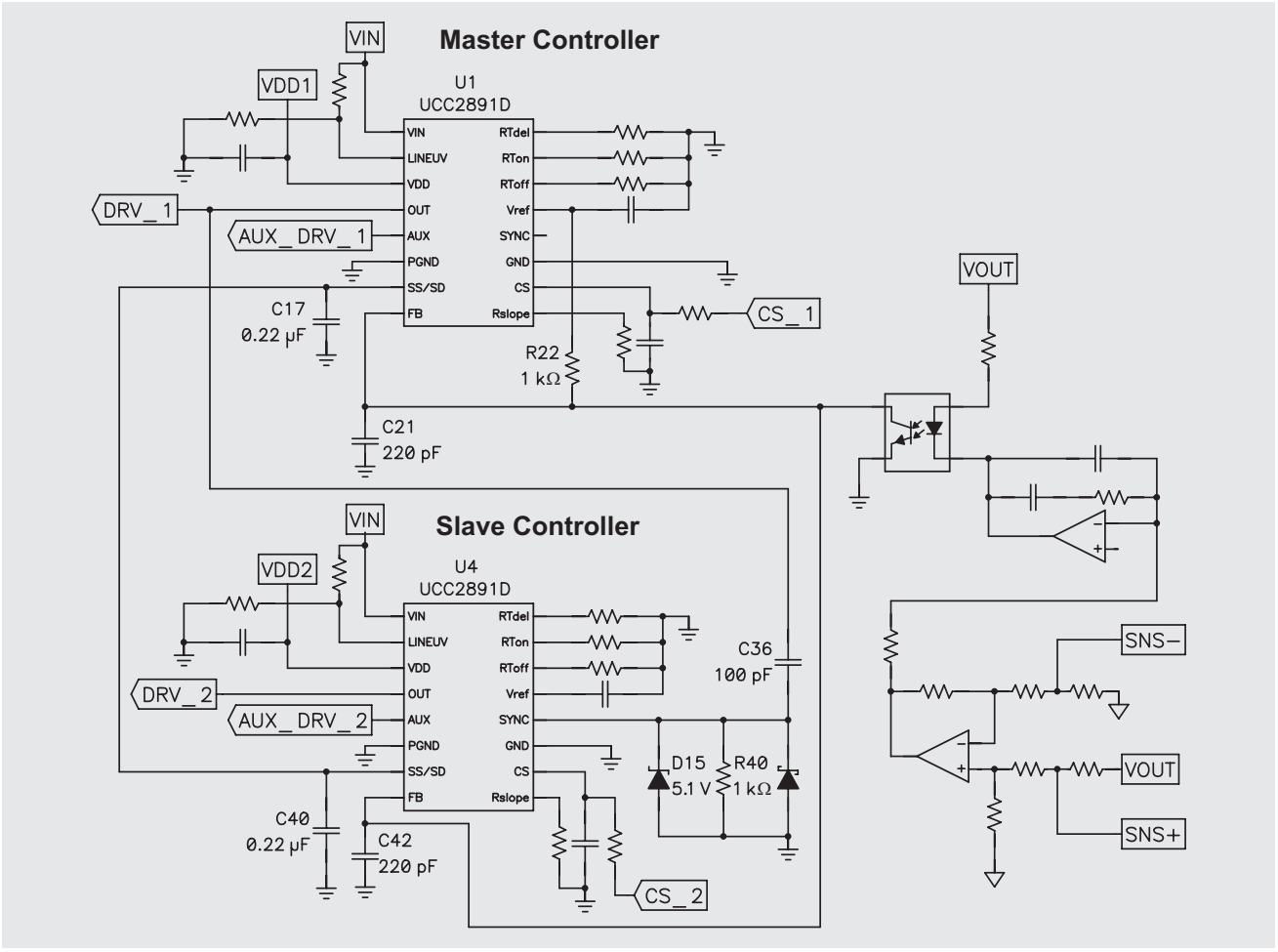
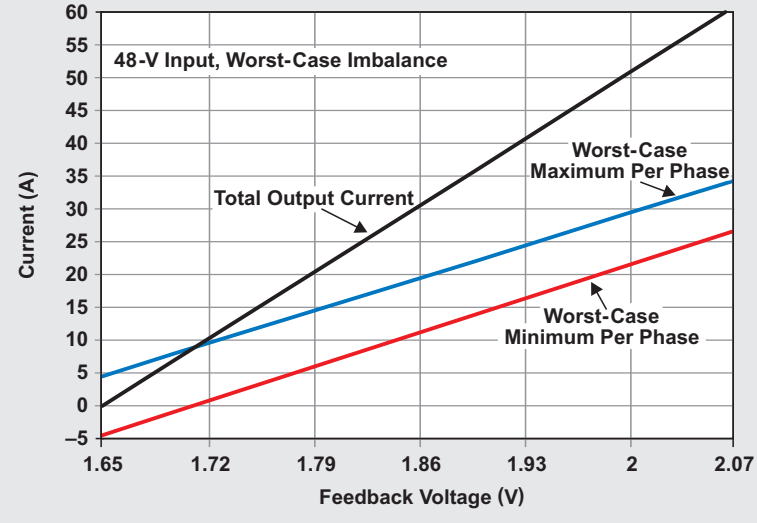


Figure 2 shows how two controllers can be connected in parallel so that they share a common feedback signal and soft-start circuit. With peak-current-mode control, each power stage behaves as a current source that is controlled by the voltage at the feedback pin. A single error amplifier regulates the output voltage by simultaneously controlling the feedback pins of the two controllers. Current imbalance between the two phases is mostly determined by variations of the offsets inside the controllers and by the tolerances of the current sense and slope compensation. Figure 3 plots the current in each phase versus the feedback voltage for a total tolerance resulting in the maximum error between phases. This is not of much concern at high load levels, as one stage will just carry a heavier burden. At light loads, however, the error can allow one phase to sink current, forcing the other phase to source extra current. This leads to increased losses at

Figure 3. Variation in offsets can lead to phase-current imbalance



light loads. The phase imbalance must also be considered when the current limit is programmed.

Synchronization is implemented by designating one controller as the master and the other as the slave. The clock frequency of the slave controller is set 10% slower than that of the master clock to ensure synchronization. The gate-drive signal of the master is used as the clock for the slave. Some conditioning components are needed to shape the magnitude and duration of the synchronization pulse.

For proper start-up, timing is critical. Start-up must be completed before the V_{DD} voltage on either chip falls below the UVLO OFF level, or neither controller will be able to start. Tying the two soft-start pins together ensures that both converters initiate the start-up sequence at the same time. In case of a fault, this also allows both controllers to be disabled by discharging the soft-start capacitance.

The efficiency of this power supply is shown in Figure 4. With a nominal 48-V input and a load current of 60 A, the supply's efficiency is over 92%. The converter's ability to convert to an isolated and regulated 5-V output with no intermediate bus and minimal power loss simplifies the system design and reduces the power demand on the upstream AC/DC rectifier.

Conclusion

In summary, interleaving active-clamp forward power stages can result in a cost-effective and efficient design. The design must account for current imbalances between the phases and ensure proper synchronization and start-up. If properly designed, interleaving extends the practical power range of the active-clamp forward converter to around 500 W and easily supports load currents of up to 60 A.

Please visit www.ti.com/tool/PMP2214 for more information on this design, including the complete schematic, bill of materials, and test results.

Related Web sites

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www.ti.com/power-aaj

www.ti.com/ucc2891-aaj
www.ti.com/pmp2214-aaj

Subscribe to the AAJ:
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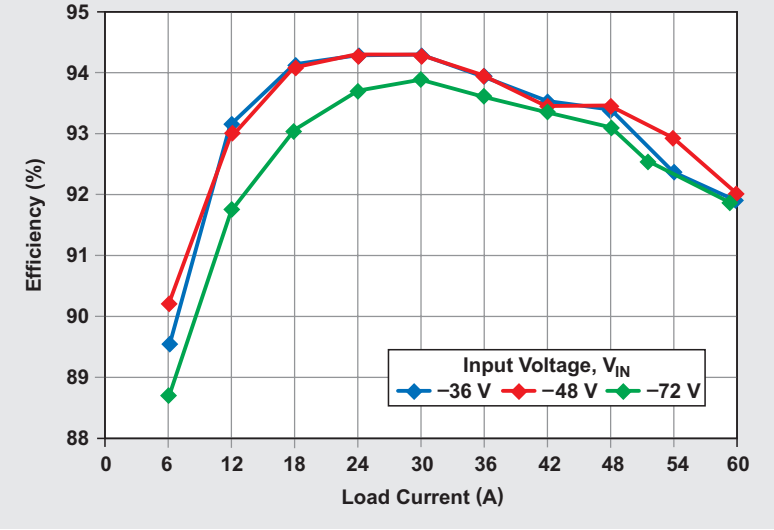
Figure 4. Synchronous rectification enables very high efficiency



Power MOSFET failures in mobile PMUs: Causes and design precautions

By Kern Wong
Principal Applications Engineer

Introduction

Power MOSFETs in automotive systems and in mobile devices being charged or operated in automobiles may be subjected to harsh operating environments and intense transients from power equipment and transmitters. Moreover, caustic contaminants in the atmosphere and on exposed conductive surfaces of circuit boards can induce low-impedance paths. Over time, these low-impedance paths and transient events like overloading, electromagnetic coupling, and inductively induced spikes from the operating environment can cause destructive electrical overstress (EOS) conditions. Such conditions may cause a large current to flow across a MOSFET power switch in a very short time.

This article addresses special design considerations and failure analysis of high-frequency switchers and regulators employing external feedback components for mobile and automotive applications. The goal is to help familiarize designers with various mechanisms and circumstances that may lead to destruction of on-chip power switches. Techniques for averting and eliminating the effects of EOS conditions are discussed to help improve end-user products and PCB designs. This article also presents tips for conducting lab tests and suggests good engineering practices to obviate potential problems from occurring in high-density/ultracompact mobile designs.[1, 2]

Case studies

In 2011, a designer reported a shorted NMOS switch in the step-down DC/DC converter of the Texas Instruments (TI) LM26484 PMU during in-house testing. This regulator was designed into a new instrumentation panel. The banks of LEDs powered by a buck converter were operating in light-load conditions. TI asked the designers to monitor the voltage at the supply pins around the clock for transients above 6 V. They confirmed that transient spikes were peaking at over 8 V for hundreds of nanoseconds, which occurred frequently. The device's absolute maximum limit on the supply pin is V_{IN} = 6 V!

It was suspected that a parasitic NPN (formed by n+ (S), p– (well), and n+ (D) as shown in Figure 1) may have turned on hard when the p– (well) base biased up the emitter from n+ (S), a classic EOS scenario in power devices. Figure 2 shows an equivalent-circuit model of a MOSFET device with parasitic components.

Figure 1. Cross-section of a typical MOSFET structure and relevant parasitic elements

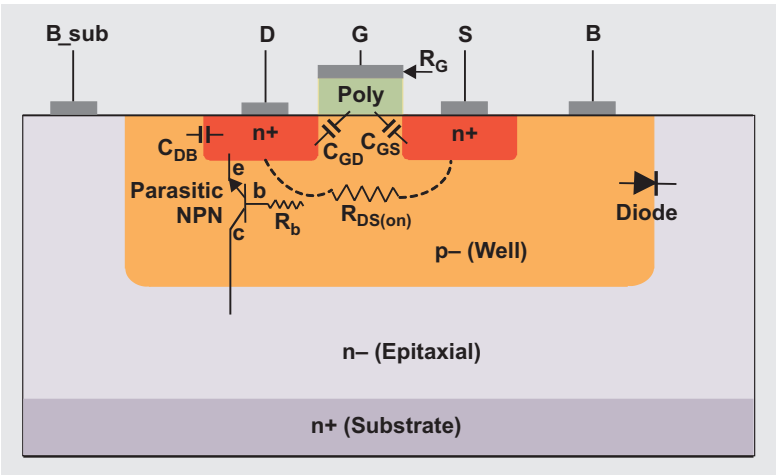
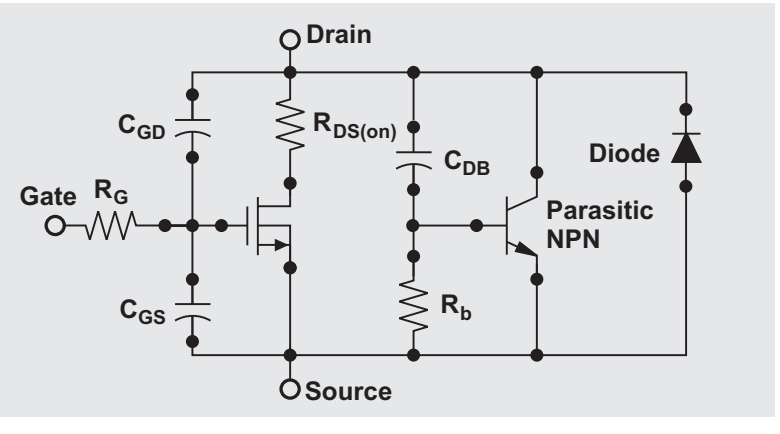


Figure 2. Model of a typical MOSFET with associated parasitic elements



Examining the PCB layout (Figure 3) revealed that the top traces of the power pins had a single via tapped into the power plane, and their longer tracks made the bypass capacitors ineffective. To prevent this situation from arising again, TI has suggested improved design guidelines. For example, adequately large bulk capacitors need to be added between the V_{IN} and ground planes. Also, local bypassing needs to be augmented with additional capacitors covering broader frequency bands. These precautions, shown implemented in Figure 4, will keep large transients from stressing the PMU's integrated circuit.

A more involved solution for eliminating EOS is to place the bypass capacitors closer to the power and ground pins, as shown in Figure 5. Note that the power-ground tracks have been widened and include liberal use of larger vias. This recommendation became a viable solution for the customer.

In 2012, another customer reported experiencing some failures with another PMU of the same family that had dual buck converters and dual LDOs. The buck-converter switches either shorted out or opened soon after the system left the factory. This PMU was powered from a stepped-down supply in an automotive application. With many infotainment and safety systems becoming standard equipment in cars starting in 2014, the PMU production rate is projected to increase by approximately tenfold, creating a concern for all parties involved. Although no anomalies have been discovered in the customer's rigorous testing for device- and board-level stress, some infrequent failures have occurred. In general, there are many known mechanisms and opportunities involved in vehicular applications that potentially could induce abnormal input-voltage transients, leading to device damage.

Figure 3. PCB with two LM26484s provides four buck converters and two LDOs

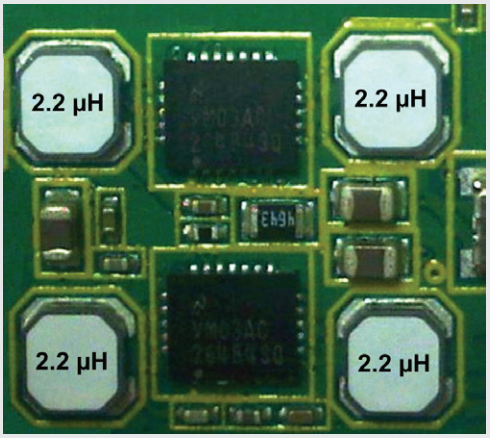


Figure 4. Example of a more robust line filter and bypass

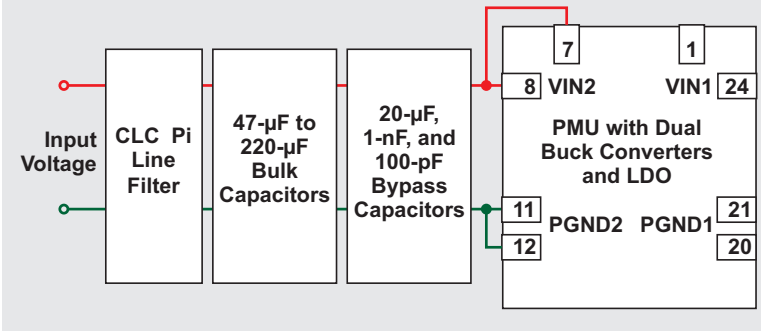
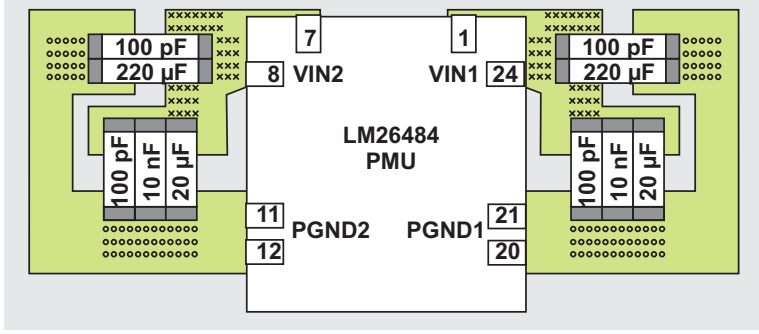


Figure 5. Improved layout with bypass capacitors closer to power and ground pins



Common causes of EOS

Many EOS conditions on PMUs arise from inadequate design considerations or overlooking subtle parasitics in some systems. This is especially true in industrial/automotive applications, wherein unusual ambient conditions or differences in the electromechanical layout can manifest reliability issues. EOS can also be related to the manufacturing process, testing, and component aging.

The following discussion presents some of the most common EOS culprits. Appropriate design tips and suggestions are included to help designers eliminate EOS problems. A typical means of identifying failure mechanisms is well-documented. It is strongly suggested that readers seeking more information also study the physics of failure via failure-mode mechanisms and effects analysis (FMMEA).

EOS caused by battery and wiring in automotive applications

Whenever a vehicle's 12-V battery voltage falls too low, as in cold weather and cranking operations, the onboard PMU's control, timing, and decision-making circuits may malfunction before undervoltage lockout (UVLO) comes to its rescue. As a result, undesirable effects such as shoot-through and disengaged clamping can stress the MOS switches and cause permanent damage over time.

High-voltage, fast edge-rate transients are another commonly encountered cause of instantaneous device damage. Another example, load dumping, is when the 12-V battery is momentarily removed from the alternator connection. Due to the inductive effect from the long wirings involved, the loads can experience a sudden increase in potential at over 100 V, which may last for hundreds of milliseconds before it decays to normal levels.

High-voltage spikes in fast transients can propagate from the MOSFET's drain terminal to the gate via terminal capacitance. This can rapidly bias up the gate, potentially leading to runaway conditions. Normally, slightly exceeding the recommended maximum operating supply voltage might not be a destructive event. However, when the suppply voltage exceeds the maximum level and sustains sufficient energy, it can cause the device to short-circuit in a few nanoseconds or lead to an avalanche breakdown. Moreover, loose or poorly secured battery-cable connections can manifest similar high-voltage transients if subjected to strong and abrupt mechanical vibrations.

Inadequate or poor power-supply bypassing

Inadequate supply bypassing can cause abnormal operation that may lead to shoot-through stress from timing issues. A proper bypass capacitor must have a voltage rating that adequately covers peak voltage transients. Leakage and parasitic inductance from traces are among the sources that cause the largest, most severe L(di/dt) overstress pulses created at the pulsing terminal of a switcher. These high-energy pulses can lead to device breakdown as previously described. Hence, taking proper precautions to eliminate unwanted inductive paths is imperative. For example, bypass capacitors should be placed as close as possible to the device rail pins. A thick metal trace should be used as much as is allowable on all high-transient paths to further cut down parasitic inductance. Finally, transient-suppressing elements or similar techniques should be used as appropriate to attenuate potentially destructive high-voltage spikes.

Shorted output from overloading and/or a defective load capacitor

When a switcher's output current (I_{OUT} load) exceeds the rated limit, built-in protection circuits usually prevent any immediate damage to the device. However, frequent overcurrent events can lead to accumulated EOS conditions, which over time may cause permanent device damage. Such damage is associated with the finite delay time, typically in the range of microseconds, required before the protection circuit kicks into action. Other than true loading shorts, a defective output capacitor can effect a low-impedance path that creates a dynamic short-circuit current in parallel with the maximum loading—thus producing another continuous EOS condition.

Temporary high-overcurrent operation with synchronous switches

The MOSFET body diode generally has a long reverse recovery time compared to that of the MOSFET switch itself. If the body diode of one MOSFET is still conducting when the opposing complementary device has switched on, then a short-circuit condition similar to shoot-through occurs. This can happen due to timing issues from parasitics or from the circuit or device design (see Figures 1 and 2). Furthermore, internal parasitic inductance and capacitance can store energy that, under certain conditions, additional current may freewheel through the body diodes of the FET switches as one turns off and the other turns on. This is the classic parasitic-capacitance mechanism, C(dv/dt), with high-speed switching that can lead to continuous high-peak-current transients with no dependence on load conditions.

This type of EOS increases dramatically when coupled with power-rail integrity issues as discussed before. The circumstance can be improved or eliminated with more accurate design and simulation of the power-train circuitry and/or by augmenting protective devices, such as a Schottky diode across the drain and source of the MOSFET. Using a Schottky diode is a proven technique to prevent the body diode from being turned on by the freewheeling current. Eliminating excessive undershooting below ground that could cause noise and turning on parasitic pn junctions also lends another benefit—the Schottky diodes may moderately increase switcher efficiency.

Device-failure verification and analysis

Failure analysis (FA) utilizes visual inspection, impedance measurements, X-rays, SAT.Sam, emission hot-spot OBIRCH analysis, SEM, and SCM tools and techniques, etc., to identify failure-mode mechanisms and root causes of device failure. Failure analysis also examines whether general oversights in a customer's design or manufacturing process may be the cause. When the cause is identified, TI issues relevant advisory and containment actions to internal and external customers to help prevent failure from reoccurring.

Failure-mode mechanisms

1. ***Electrostatic-discharge (ESD) destruction or gate surge:*** Device-junction or oxide-rupture damage (a short or leakage) can occur as a result of improper handling during assembly and testing of the device and system. These mechanisms introduce electrostatic charges onto the device and/or create external high-voltage surge events that reach the switch circuit.

   For example, an ESD event between a fingertip and the communication-port connectors of a cell phone or tablet may cause permanent system damage. As process-technology nodes continue to shrink, device-level ESD

protection becomes inadequate on a system level. A transorb, or a transient-voltage suppressor such as TI's TPD1E10B06 protection diode, is a good remedy.

2. Wear-and-tear mechanisms:

- A die fracture may occur in extreme temperature cycling
- Over time, high-voltage stress may induce dielectric breakdown that will become a gate-oxide short circuit
- Wire bond and metal routes can open due to EOS from current overload, etc.
- A voltage transient on the supply lines can cause damage to passive and active devices on the die

3. PCB elements and environment:

- A circuit failure may occur due to humidity, presence of a contaminant, or filaments becoming conductive
- A die fracture may occur due to shock, vibration, material fatigue, etc.
- Loss of polymer strength, known as glass transition failure, may occur under high-temperature stress
- Bypass and load capacitors may be leaky or shorted
- Inductor windings may short-circuit due to wear and tear of insulation under high-temperature stress or mechanical vibration

4. Component aging and inadequacy:

Because aging components may contribute to MOSFET failures even if they initially meet datasheet specifications,[1] manufacturing and product-engineering departments are encouraged to perform testing and burn-in of parts at ratings slightly above datasheet limits. This ensures that marginal devices with inherent wafer-defect density and random process-related issues are weeded out. It may be better to lose some yield at production than to be accountable for and spend valuable resources on field failures later on.

Failure-analysis results

In the 2012 case study mentioned earlier, where the switch's drain and source channels were fused together in an automotive application, the customer could not determine that the PMU IC, the circuit board, or the subsystem had a reliability problem. Each was rigorously tested and stressed beyond specification limits, and no failure ever surfaced. The culprit might have been the layout; the electrical plumbing; the system installation; and/or the operating conditions, such as cold cranking, a weak battery, or intermittent connection of long/loose power cabling.

Because the customer and its subcontractors were unable to reproduce the initial failure in their lab, they needed confirmation and sought assistance from TI. Examples of in-house failure-analysis results are depicted in Figures 6 and 7.

Figure 6. High-side pFET shorted to the VIN rails

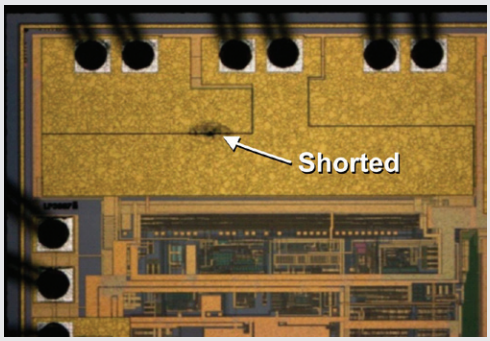
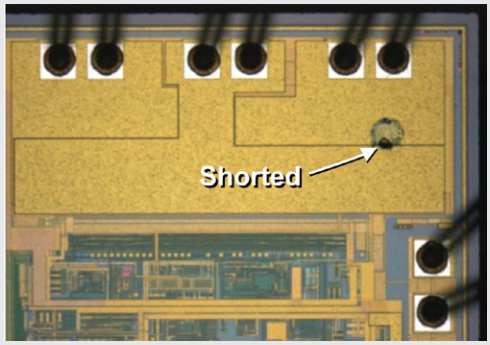


Figure 7. Low-side nFET shorted to ground



Failure analysis suggested that the burn marks reflected in the deprocessed dies were likely the consequence of EOS conditions. To validate this assumption, it was demonstrated that the failures could be induced in lab setups for (1) 5-V operation and (2) start-up conditions. By using a Keithley 2420 3-A source meter—a versatile power supply whose amplitude, frequency, and on/off times can be programmed—V_{IN} was programmed at 5 V and injected with a 50-ms pulse that repeated at 100-ms intervals. With loading at 200 mA and above, the pulse amplitude was increased at 0.5-V increments at 5-minute intervals until abnormal current was observed. The part was then decapped to visually confirm EOS. The results revealed that when the peak-to-peak pulse voltage reached approximately 7.5 V or more, the switches shorted out. Moreover, if pulses were to peak further to 9 V, the ESD structure might also be damaged.

Reproducing a short circuit from the switches during start-up was more challenging, however. With a bench supply cycling the buck converters on and off, V_{IN} issued relatively slow and smooth start-up transients and settled in at about 6 ms (Figure 8). Even with the supply set to slightly over 7 V, the switchers did not fail over days of stress testing.

In order to make the operation mimic in-vehicular conditions more closely, the cable length between the supply and the device was increased from about 30 cm to about 1.5 m. These longer wires, typically routed from the 12-V battery to the device, created more inductance. Furthermore, the soft power cycling from the power supply was replaced with a mechanical toggle switch such that the mechanical bounce and chatter behaved more like transients introduced by mechanical relay contacts (Figure 9).

The tests were conducted with the power-supply output set at 5.0 V, then the toggle switch was flip-flopped 20 times. If no overcurrent failure was detected, the supply voltage was increased by 0.2 V, the switch was again toggled on and off 20 times, and the process repeated until the part failed. The result was a stunning success! The buck converter's high- or low-side switch became shorted with the power-supply output at about 7.5 VDC. The V_{IN} pins monitored with a 10-pF probe exhibited faster turn-on transients, which caused an overshoot above 11 V in 20 µs. The actual L(di/dt) could have been a lot higher, creating a repeatable destructive EOS condition. The customer was elated that this bench setup replicated the same failures as in the field.

Figure 8. Power supply off/on ramping in ~6 ms

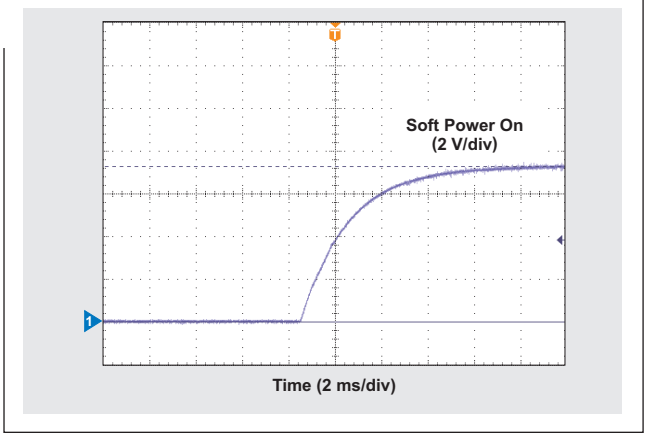
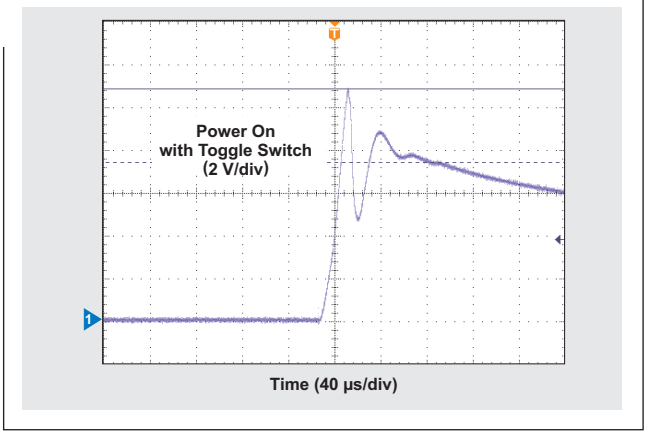


Figure 9. An 80-µs transient induced by switch and longer wire



Conclusion

This article has discussed common device-failure mechanisms related to MOSFET transistors in integrated power-management and voltage-regulator circuits. General precautions, specific PCB layout techniques, and component-selection tips have been presented to help mitigate and eliminate EOS concerns. It is hoped that this article will help system and PCB designers be aware of the EOS effects of seemingly benign parasitic elements that can be subjected to transients in the PMU operating environment. Product and field support personnel may also find this article useful for understanding the cause and effect of EOS to facilitate their interface with customers.

Acknowledgments

The author thanks Ann Cocannon, Steven Jacobson, ChiYoung Kim, Maxwell Goodman, Andy Strachan, and Gavin Kirihara for their valuable input and support.

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35-V, single-channel gate drivers for IGBT and MOSFET renewable-energy applications

By John Stevens
Systems Engineer, High-Performance Isolated Power

Introduction

The electronics market segment labeled as renewable energy is a complex and diverse arena for electric power conversion. In point-of-load applications, the switching power converter typically is non-isolated; power levels are fairly low (<200 W); and the power is usually converted from one DC voltage to another, such as from 12 V to 3.3 V. Further, the power-stage switches are integrated or capable of being driven by low-current controllers or transistors. Integration between the controller and power stage is being realized today. Silicon (Si) MOSFETs dominate this arena, where higher switching frequencies are preferred and can reach speeds of greater than 1 MHz. These power switches generally are driven by a 5- or 12-V IC gate driver or similar solution.

Challenges to efficiently managing renewable-energy systems

In the electronic power train from a wind or photovoltaic power generator, there are some unique performance challenges. Typical power levels for renewable energy can range from 1 to 3 kW for micro-inverters, 3 to 10 kW for string inverters, and 10 kW to 1 MW for large central-inverter stations. In addition to DC-to-DC conversion, DC-to-AC and AC-to-DC conversion can also be used, and sometimes a combination of the two.

Older wind turbines were tied directly to the power grid but had to run at the power-line frequency. This made them inefficient across the many operating points they experienced. Newer wind turbines (Figure 1) often convert AC to DC and then DC back to AC so that the wind-driven generator can run at variable speeds for maximum efficiency.

Conversely, photovoltaic cells produce DC voltage/current. Generally, the voltage is boosted higher and then sent through a DC-to-AC inverter before being tied to the grid.

Renewable-energy trends

For most countries, generating renewable energy from sources such as wind and solar power makes up only a small percentage of their total power portfolio. In recent history, growth has been consistent year by year. There are places where renewable energy makes up a large share of the available power. Denmark, for example, generated nearly 34% of its total electricity from wind power alone in the first half of 2012, according to the Danish Energy Agency. According to its parent agency, the Danish Ministry of Climate, Energy and Building, Denmark has committed to having 50% of its total power supply come from wind by 2020. When wind energy makes up that large a portion of a country's total power, reliability of the conversion system becomes critical. This—together with the high-power connection to the grid, isolation safety requirements, and the cost of large renewable-energy conversion systems—means that system reliability is always the design priority, followed by efficiency. Therefore, protection features and reliability are preferred at all levels, from the controller all the way down to the FET/IGBT driver itself.

Typical power-management configuration

High power levels lead to higher system voltages, and therefore higher standoff voltages, for the components used within the converter. For lower power loss at greater than 400 V, most circuit designers prefer to use insulated-gate bipolar transistors (IGBTs) or the latest silicon carbide (SiC) FETs. These devices can have standoff voltages of up to 1200 V, with lower ON resistance than equivalent Si MOSFETs. These complex power systems often are managed by a digital signal processor, a microcontroller, or a dedicated digital power controller. Thus, they usually require both power and signal isolation from the noisy switching environment of the power stage. Even during steady-state switching cycles, the circuit can see massive changes in both voltage and current that can create significant ground bouncing.

Figure 1. Simplified power flow from wind turbine to grid

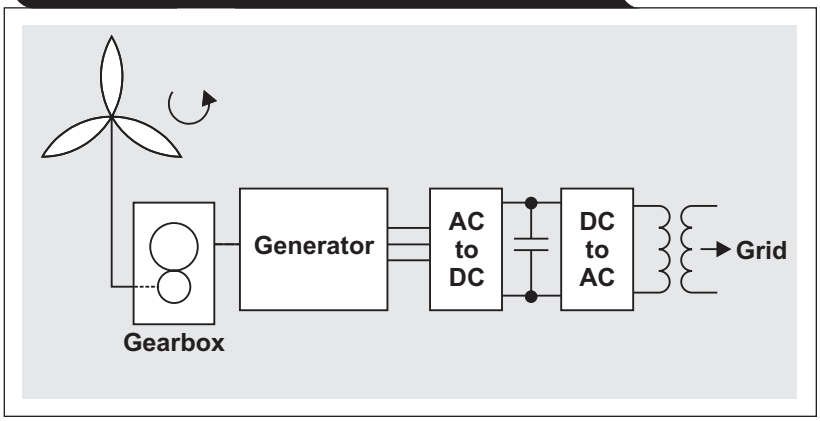


Figure 2. Basic structure of single-phase inverter

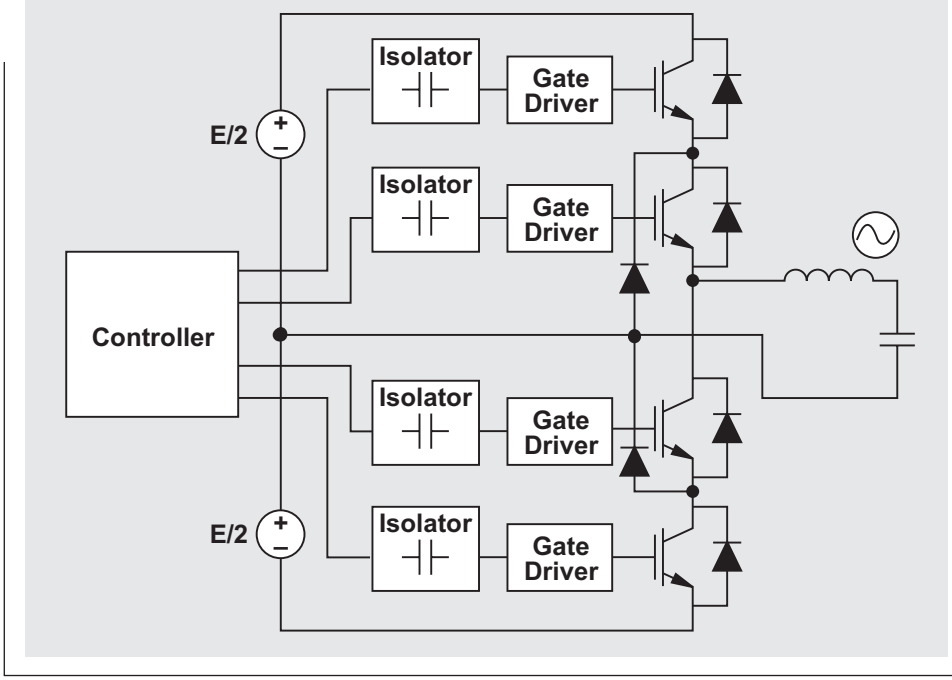
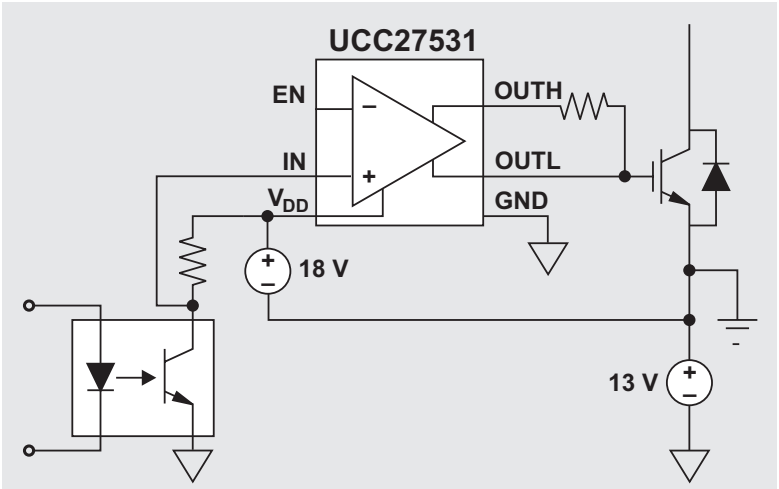


Figure 2 shows that even for a single-phase DC-to-AC inverter, there are many gate drivers needed to properly switch the IGBTs in the power stage. As a single-channel gate driver, the Texas Instruments UCC27531 can drive any of the switches in the switch bridge if it has the necessary signal and bias isolation. Signal isolation is achieved by using an optocoupler or digital isolator. For bias isolation, the designer can use a bootstrap circuit with a diode and a capacitor, or an isolated-bias supply. Another option is to connect the gate driver on the same side of the isolation as the controller, then drive the switch through a gate transformer after the gate driver itself. This option allows the driver to be biased with a non-isolated supply on the control side.

Figure 3. Driving a power switch with FET/IGBT single-gate drivers



Gate drivers in renewable energy

As a small, non-isolated gate driver, the single-channel UCC27531 is a good fit for the environment described. Its input signals to the IC are provided by an optocoupler or digital isolator. Its high supply/output-drive voltage range of 10 to 35 V makes it ideal for 12-V Si MOSFET applications as well as for IGBT/SiC FET applications. Here, a higher positive gate drive is typical, as well as a negative voltage pull-down on shutoff to prevent the power switch from false turn-on. Typically, SiC FETs are driven by a +20/–5-V gate driver relative to the source. Similarly, for IGBTs, system designers may use a +18/–13-V gate drive, for example (see Figure 3).

Since the UCC27531 is a rail-to-rail driver, OUTH pulls up the power-switch gate to its V_{DD} of 18 V relative to the emitter. OUTL pulls down the gate to the driver's GND of –13 V relative to the emitter. The driver effectively sees +18 to –13 V, or 31 V from V_{DD} relative to its own GND. Further, the 35-V rating provides a margin to prevent overvoltage failure of the IC due to noise and ringing.

The split output with both OUTH and OUTL permits the user to control the turn-on (sourcing) current and turn-off (sinking) current separately. This helps to maximize efficiency and maintain control of the switching times to

comply with requirements for noise and electromagnetic interference. Further, even with a split output, the single-gate driver maintains a minimum inductance on the output stage, preventing excessive ringing and overshoot. By having an asymmetrical drive (2.5-A turn-on and 5-A turn-off), the UCC27531 is optimized for average switch timing in high-power renewable-energy applications. Further, with the low pull-down impedance, this driver increases reliability by ensuring that the gate does not experience voltage spikes that could lead to false turn-on from the parasitic Miller-effect capacitance between the collector and gate for IGBTs and between the drain and gate for FETs. This internal capacitance can lead the gate to exceed the turn-on threshold voltage by pulling up on the gate when the collector/drain voltage rapidly increases during turn-off of the switch.

The input stage of the UCC27531 is also designed for high-reliability systems like renewable energy. It has a so-called TTL/CMOS input that is independent of the supply voltage, allowing for compatibility with standard TTL-level signals. It provides a higher hysteresis of about 1 V when compared to the usual 0.5-V hysteresis seen in classic TTL. If the input signal is lost and becomes floating for any reason, the output is pulled low. Also, with the large changes in voltage on the GND of the driver IC, it is possible for the input signals to appear negative if the GND bounces high during a switching edge. This driver addresses this concern by handling up to –5 V continuously on the input (IN) or enable (EN) during these events.

The UCC27531 comes in a 3 x 3-mm, industry-standard SOT-23 package, which is very competitive with a discrete two-transistor solution that has a discrete level shifter without negative-input capability or added protections. Beyond the obvious space savings, integrating the UCC27531's functions into a single IC package increases the system's overall reliability.

This single-channel driver is an attractive option because it can be located very close to the power-switch gate. Placement is more flexible than for a combination high-side/low-side gate driver in a single IC. This flexibility helps minimize the inductance between the driver and power switch and gives the designer better control of the switch's gate. Figure 2 shows how many high-power switches are in just a single phase of a DC-to-AC stage. Over a complete three-phase system with multiple conversions between DC and AC and back, and with boost stages of DC-to-DC conversion also needed in some applications, there becomes a need for many gate drivers. Each one must be strategically placed on the PCB to ensure a proper design.

Conclusion

In renewable-energy applications, conversion of power generated from solar arrays and wind turbines presents unique challenges to the system designer. These challenges include high voltages and power levels, meeting safety and reliability requirements, and the overall complexity of the completely interconnected system. Although gate drivers for power switches seem like a small part of the total system control and power flow, they are actually very important to the overall design performance.

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How to pick a linear regulator for noise-sensitive applications

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Marketing Engineer

Noise-sensitive applications require a power supply that generates low internal noise and rejects noise from the power source. These applications include test and measurement applications, medical equipment, communication equipment, base stations, and many others. A low-noise power supply is used to power a signal chain that includes data converters, amplifiers, clocks, jitter cleaners, PLLs, analog front ends and many other devices. A low-noise power solution is essential to preserving signal accuracy and integrity. This article addresses criteria and parameters to consider in designing such a power solution, including important specifications for picking a linear regulator.

The terms "power supply ripple rejection" (PSRR) and "linear regulator" often are used together. The linear regulator's high ripple rejection makes it an integral part of a power solution. PSRR is a measure of how well the regulator filters a circuit by rejecting noise or ripple coming from the power-supply input at various frequencies. In both low-dropout regulators (LDOs) and linear regulators, PSRR is a measure of output ripple compared to the input ripple over a frequency range.

Since PSRR is calculated as ripple rejection, it is expected to be a negative number. However, it is represented as a positive number in the datasheet so that a higher number denotes higher noise rejection. Mathematically, it is expressed in decibels as

$$PSRR = 20 \times \log\left(\frac{V_{IN\_ripple}}{V_{OUT\_ripple}}\right).$$

The PSRR of a linear regulator can be divided into three frequency-range regions. The first region extends from DC to the roll-off frequency. The ripple rejection in this region is mostly dominated by open-loop gain and the bandgap reference. The second region extends from the roll-off frequency to the unity-gain frequency. The PSRR in this region is usually higher than in the first region and is mainly dominated by the open-loop gain of the regulator. The third region's frequency range is above that of the unity-gain frequency. The output capacitor, along with the linear regulator's parasitics (in the V_{IN}-to-V_{OUT} path), dominates this region. Therefore, the values of the selected output capacitor and its equivalent series resistance are quite important. This information can be found in any datasheet.

In addition to V_{IN}, V_{OUT}, and system load requirements, an engineer needs to know the frequency range of ripple and noise in the system or power supply in order to select linear regulators with a good PSRR in that frequency range. For example, a switcher that switches at a frequency of 2 MHz may require a linear regulator that has a high PSRR at around 2 MHz. Figure 1 shows a linear regulator's high PSRR of about 55 dB at 2 MHz that helps to remove input noise. Also, when PSRR graphs in the regulator datasheets are evaluated, it is always good to note the dropout voltage at which the PSRR is measured. High dropout voltage leads to better PSRR but reduces the device's efficiency.

Figure 1. Plot of linear regulator's wide-bandwidth, high PSRR

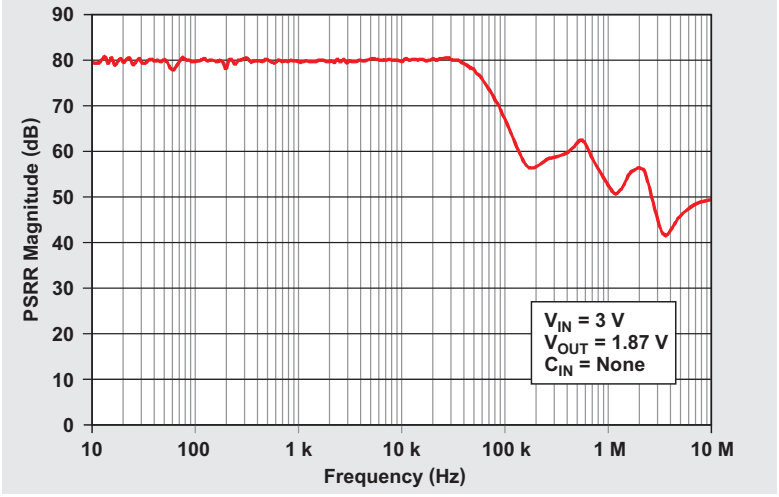


Figure 2 shows a switching regulator's spectral noise that is fed to a linear regulator. It can be seen that the switcher is operating at 500 kHz. Figure 3 shows the output spectrum of the Texas Instruments TPS7A4700 linear regulator. The spike caused by the switcher at 500 kHz has been attenuated. If the power solution is not designed for noise attenuation with high-PSRR linear regulators, the spike may show up at the output of the RF voltage-controlled oscillators, which after mixing affect the PA performance. The spike may also fold back into the audio band and create noise in an audio application.

Usually, noise and PSRR parameters are lumped together in a linear regulator's datasheet, which causes a lot of confusion because noise and PSRR are two very different characteristics. Noise is purely a physical phenomenon that occurs with transistors and resistors

Figure 2. Typical noise spectrum from a switching regulator

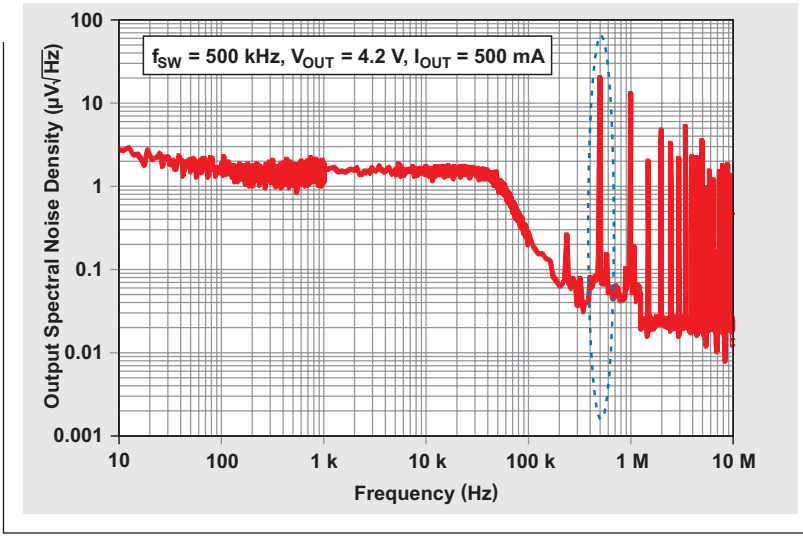
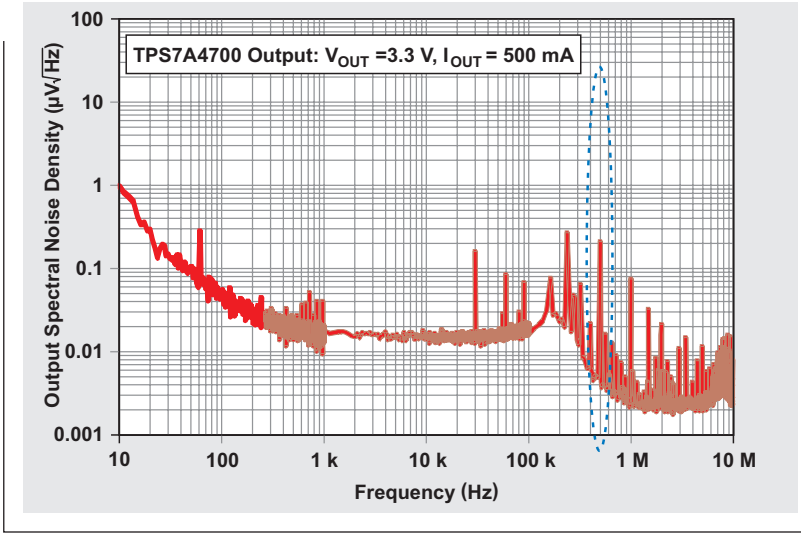


Figure 3. Output noise spectrum of TPS7A4700 linear regulator with attenuated 500-kHz spike



inside the linear regulator on a very fundamental level. This type of noise may include thermal, flicker, and shot noise. Noise is usually indicated as a curve showing spectral noise density (in $\mu V/\sqrt{Hz}$) versus frequency (Figure 4). Noise can also be indicated as integrated output noise (in μV_{RMS}), listed under the electrical characteristics table in the datasheet (Figure 5). The output noise (in μVR_{MS}) is the spectral noise density integrated over a certain frequency range and can be seen as the total noise in a specified frequency range.

The next obvious question is whether an engineer should look at spectral noise density or integrated output noise, or both. The answer depends purely on the engineer's application. For example, in RF applications where the signal does not have any dependency on the frequency, it makes more sense to look at the linear regulator's spectral noise density. However, in applications where the noise will be integrated by the system, such as powering DACs and ADCs, the engineer should look at the linear regulator's integrated output noise instead.

Conclusion

This article has discussed the important specifications that design engineers need to consider when picking a linear regulator. It has also covered the criteria and parameters to consider in designing a power solution for low-noise applications. Given these guidelines, engineers should be able to preserve signal accuracy and integrity in their applications.

Reference

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Figure 4. Spectral noise density for the TPS7A4700

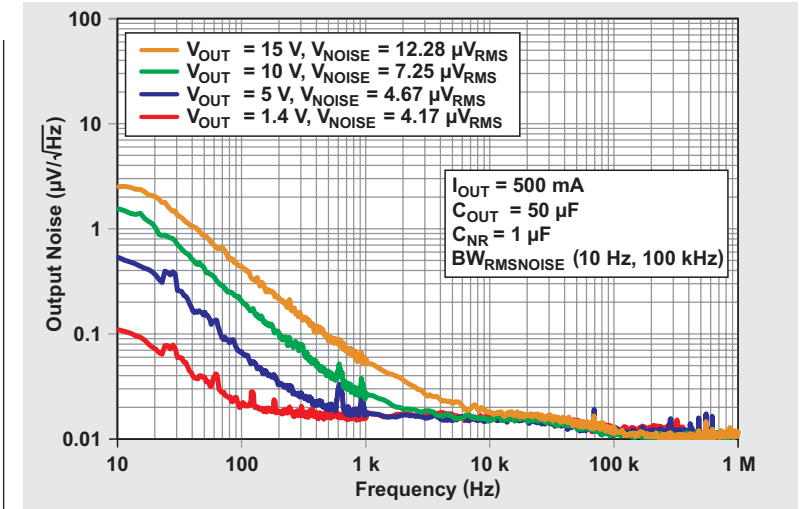

Figure 5. Excerpt from TPS7A4700 datasheet showing integrated output noise voltage

PARAMETER		TEST CONDITIONS	TYP	UNIT
V_{NOISE}	Output noise voltage	V_{IN} = 3 V, $V_{OUT(NOM)}$ = 1.4 V, C_{OUT} = 50 μF, C_{NR} = 1 μF, BW = 10 Hz to 100 kHz	4.17	μV_{RMS}
		V_{IN} = 6 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 50 μF, C_{NR} = 1 μF, BW = 10 Hz to 100 kHz	4.67	μV_{RMS}

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