High-Performance Analog Products

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Audio
- Amplifiers: Op Amps
- Low-Power RF
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Controlling switch-node ringing in synchronous buck converters

By Robert Taylor, *Applications Engineer,*
and Ryan Manack, *Field Applications Engineer*

Introduction

As power-supply efficiency becomes more important, faster switching speeds are necessary to reduce the losses. However, as switching speeds are increased, there are negative trade-offs that must be taken into account, such as a consequential increase in electromagnetic interference (EMI).

In a synchronous buck converter, fast-switching field-effect transistors (FETs) can experience significant voltage overshoots and ringing on the switch node. The magnitude of the ringing is a function of the high-side MOSFET's switching speed and the stray inductances in the layout and FET package. Proper techniques for circuit and layout design must be observed to keep the ringing below the absolute maximum rating of the synchronous FET.

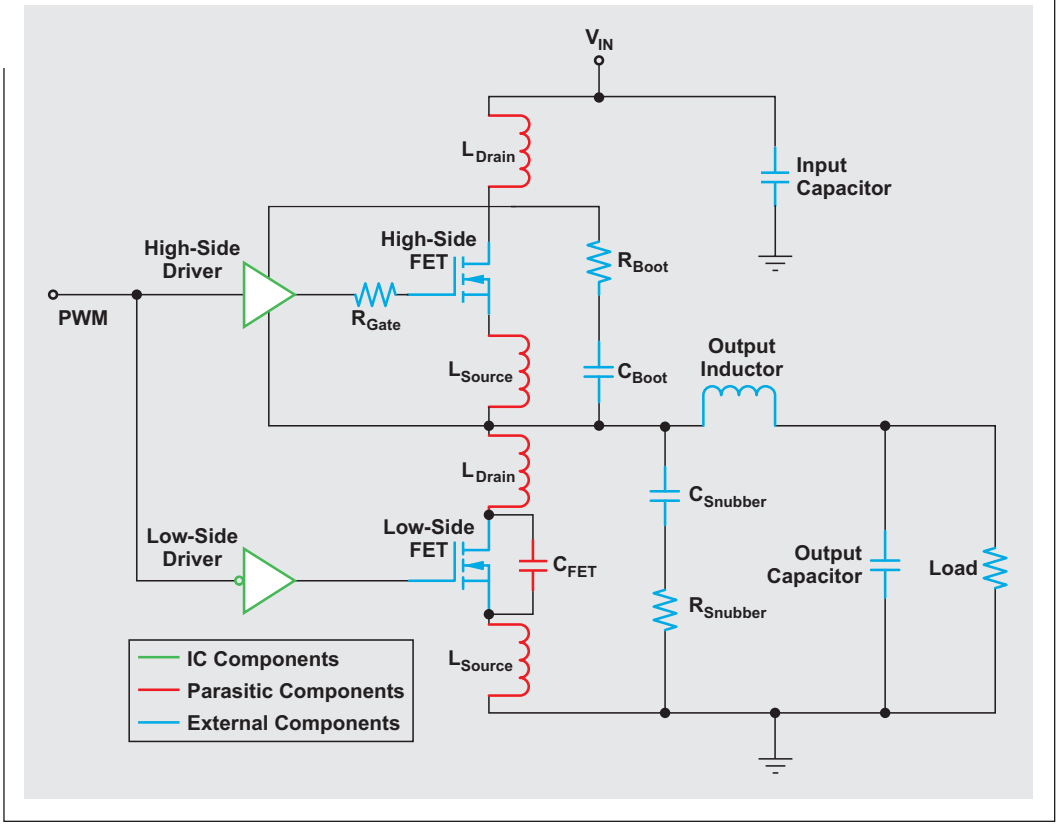
This article focuses on three circuit designs that control switch-node ringing with either a boot resistor, a high-side gate resistor, or a snubber. Data is presented for each approach, and the benefits of each are also discussed. These techniques can be nullified by poor power-supply layout, so it is important to take this into consideration as well. Please see Reference 1 for more information about layout.

Ringing caused by synchronous buck converter's parasitics

The circuit in Figure 1 shows the power-stage components for a synchronous buck converter. Included in this model are the parasitic inductances and capacitances responsible for switch-node ringing.

Assume that the converter is in steady state. During the portion of the switching cycle when the low-side FET is on, the power to the load is being provided only from the output inductance and capacitance. At this point, energy is being stored in the parasitic inductances of the low-side FET relative to $E = \frac{1}{2}L \times I^2$. At the end of the switching

Figure 1. Schematic showing parasitics of a buck converter

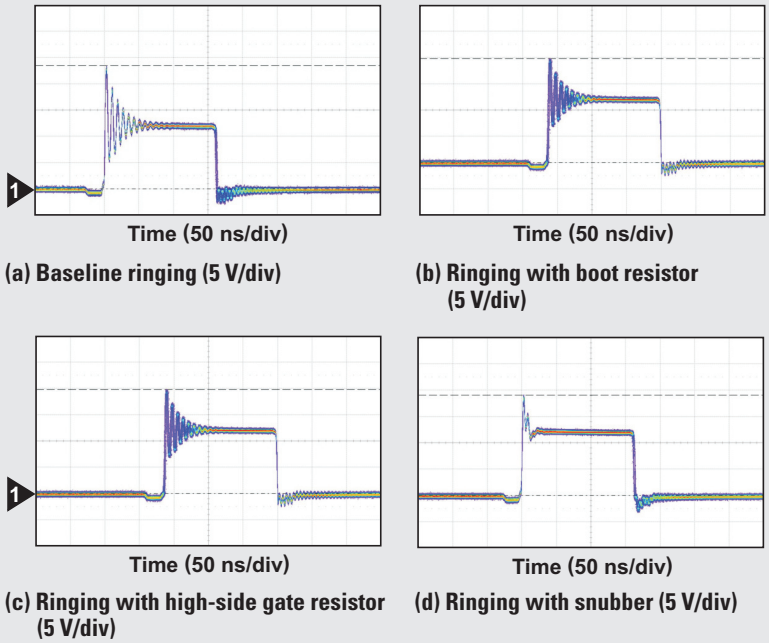


cycle, the converter prepares to switch the low-side FET off and the high-side FET back on to replenish power to the output L.

Strong gate drivers and a fast-switching FET allow the low-side FET to be turned off quickly. Assuming load conditions are sufficient to keep the inductor current flowing to the output, current is bypassed to the body diode of the low-side FET, and energy remains in the parasitic drain and source inductances of the low-side FET. After a fixed dead time, the high-side FET turns on, and the energy from the low-side and high-side FETs' parasitic inductances appears as an LC ringing waveform on the switch node.

The voltage magnitude of this ringing can exceed the absolute maximum drain-to-source voltage of the low-side MOSFET. Fast-switching MOSFETs such as the Texas Instruments (TI) CSD87350Q5D incorporate a stacked MOSFET pair that limits the parasitic inductances through innovative packaging techniques.

Figure 2. Waveforms of switch-node ringing with 12-V input



Reducing ringing

A test circuit with a 1.1-V/20-A buck converter was used to show the effects of switch-node ringing. This circuit used the TI TPS40304 600-kHz buck controller and the CSD87350Q5D fast-switching NexFET™ power block. The input-voltage range was 8 to 16 V. As a baseline reference, a switch-node waveform (Figure 2) and an efficiency plot (Figure 3) were generated without a boot resistor, high-side gate resistor, or snubber connected. The peak ringing with a 12-V input was 23.4 V. The efficiency at maximum load was 87.2%.

The boot resistor, high-side gate resistor, and snubber were optimized to reduce the overshoot to less than 20 V. This overshoot limit provided some margin to protect the FET, which had a 30-V maximum voltage rating. Figure 2 shows the overshoot for the baseline circuit and the reduced-ringing overshoot for the boot resistor, gate resistor, and snubber. The waveform for the gate resistor is very similar to that of the boot resistor. It is important to notice that only the magnitude of the ringing was affected by the boot-resistor and gate-resistor methods. The snubber method also changed the ringing frequency and damped out the ringing waveform. Figure 3 shows the measured efficiency for each of these conditions.

Using a boot resistor

The charge-pump circuit in Figure 1 uses C_{Boot} to boost the high-side gate supply above the supply voltage of the power stage. One way to reduce ringing is to include a boot resistor in series with the boot capacitor, which slows down the turn-on of the high-side FET. This allows more time for the parasitic network to discharge, ultimately limiting the ringing. The value of the boot resistor is determined by starting at 0 Ω and increasing the resistance until the desired ringing is achieved. To reduce the ringing for this design to below 20 V, a 6.8-Ω boot resistor was

Figure 3. Efficiency versus load current

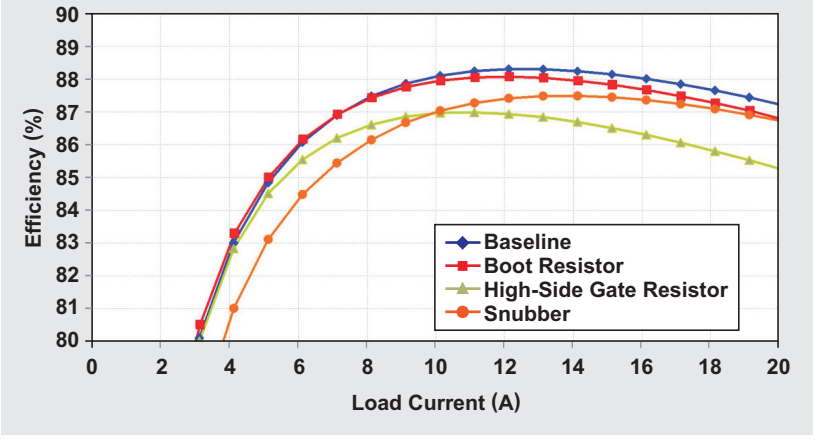


Table 1. Test data for three methods of reducing ringing

METHOD	RINGING (V)			FULL-LOAD EFFICIENCY (%)		
	V_{IN} = 8 V	V_{IN} = 12 V	V_{IN} = 16 V	V_{IN} = 8 V	V_{IN} = 12 V	V_{IN} = 16 V
Baseline	18.0	23.4	28.3	88.3	87.2	85.4
Boot Resistor	15.9	19.8	22.6	88.1	86.8	85.1
Gate Resistor	15.4	19.8	23.2	87.1	85.2	83.1
Snubber	14.2	19.1	23.7	88.1	86.7	84.7

required. It is interesting to note that the boot resistor affects only the turn-on of the high-side FET, making this method an efficient way to reduce ringing. However, if the boot resistor is made too large, the boot capacitor may not get fully charged in each cycle. In this case, the gate driver would not have sufficient voltage to keep the high-side FET on and could turn off in the middle of the cycle. This limits the amount of ringing that can be reduced with the boot-resistor method.

Using a high-side gate resistor

Using a resistor in series with the gate of the high-side FET is another effective way to reduce ringing. Similar to the boot-resistor method, this resistor slows down the turn-on of the high-side FET. However, because this resistor is in series with the gate, it is also in the discharge path, so it slows down the turn-off as well. To reduce the ringing for this design to below 20 V, a 6.8-Ω gate resistor was used. This method is the least efficient of the three choices.

Using a snubber

The third option to consider for reducing ringing is a snubber. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage and frequency and also reduces the number of ringing cycles. This helps to reduce the EMI emitted by the system.

The procedure for choosing the capacitor and resistor components starts with measuring the ringing frequency of the original circuit. Once the frequency is determined, a capacitor is put in parallel with the low-side FET to change the ringing frequency to half the original value. When the frequency is half the original value, the parallel capacitor is equal to three times the parasitic capacitance of the original circuit. With the capacitance and frequency known, the parasitic inductance can be calculated by using the formula $f = ½\pi\sqrt{LC}$, where f is the original ringing frequency and C is the parasitic capacitance. The resistor to critically damp the circuit is calculated from the equation $R = \sqrt{L/C}$. This resistor may or may not provide the necessary ringing reduction. Increasing the resistance results in an underdamped system, which allows more ringing but decreases power dissipation. Increasing the capacitance reduces the ringing but increases power dissipation. For the example, using a 2200-pF capacitor and a 1-Ω resistor reduced ringing to 19.1 V.

Conclusion

As MOSFET switching speeds continue to increase, controlling the switch-node ringing of a synchronous buck converter is critical. Doing so requires a good layout and proper analog-circuit design with a boot resistor, a high-side gate resistor, or a snubber. Table 1 shows the amount of ringing reduction achieved with the test circuit and the corresponding efficiency for each technique.

The boot resistor slows down the turn-on of the high-side FET without affecting the turn-off. In the design example, the boot resistor was the most efficient approach. However, if this method is used, proper care must be taken to prevent starving the gate. A resistor in series with the gate increases both the turn-on and turn-off times of the high-side MOSFET, which controls ringing on the rise and fall of the switch node. This approach burns the most power in the upper FET, reducing efficiency. An RC snubber reduces the frequency and overshoot of ringing, but it requires two extra components and has low efficiency at light loads.

Every power-supply design is unique, so each method should be inspected for its cost/benefit to the supply. Often, the best approach may even be a combination of all three circuits. The ultimate goal is to maintain a sufficient margin below the MOSFET's absolute maximum voltage rating while maintaining as much efficiency in the power stage as possible.

Reference

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

1. Robert Kollmann, "Constructing your power supply — layout considerations," 2004–05 TI Unitrode Design Seminar Series – SEM1600, Topic 4 . . . . . SLUP230

Related Web sites

power.ti.com
www.ti.com/nexfet
www.ti.com/product/CSD87350Q5D
www.ti.com/product/TPS40304

A solar-powered buck/boost battery charger

By Jeff Falin, *Factory Applications Engineer,*
and Wang Li, *Factory Applications Engineer*

Introduction

Charging batteries with solar power has become very popular. A solar cell's typical voltage is 0.7 V. Panels range from having one cell to several cells in series and are therefore capable of producing a wide range of voltages. Most battery chargers on the market today step down, or buck, their input voltages. Therefore, to charge a two-cell lithium-ion (Li-Ion) battery, for example, a solar panel capable of producing at least 8.4 V is needed. However, this same charger cannot be used to step up, or boost, its input voltage to charge a multicell Li-Ion battery used in a laptop or a 12-V lead-acid battery used in a solar lantern. It is possible to modify a buck battery charger into a battery charger that both bucks and boosts. This article identifies the key concerns of changing a buck battery charger into a buck/boost SEPIC charger and provides a design example using the Texas Instruments bq24650 battery charger controller for solar power.

Figure 1. Block diagram of battery charger controller

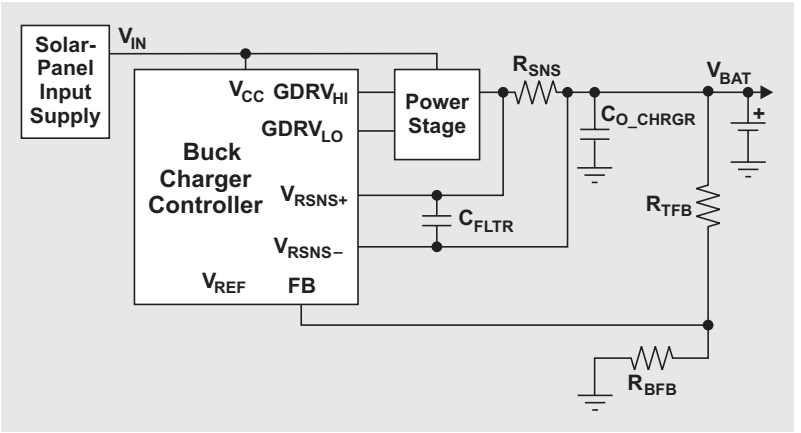
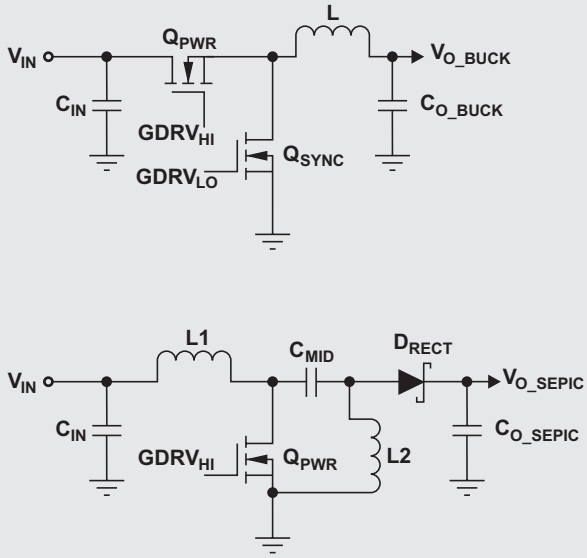


Figure 2. Buck power stage (top) versus SEPIC power stage (bottom)



SEPIC power stage versus buck power stage

Figure 1 shows a simplified block diagram of a battery charger controller. The charger controller IC monitors the charging current through R_{SNS} and the battery voltage through the feedback resistors (R_{TFB} and R_{BFB}) and adjusts the output of the power stage to meet the charging parameters. If the input source voltage can be both higher and lower than the maximum battery voltage, a SEPIC power stage capable of bucking and boosting can be used.

Figure 2 compares a synchronous buck power stage and a nonsynchronous SEPIC power stage. The buck controller's high-side gate drive ($GDRV_{HI}$) is used to drive the SEPIC converter's power FET (Q_{PWR}). However, a buck controller cannot be easily configured to drive a synchronous rectifying switch for a SEPIC converter. Therefore, Q_{SYNC} is replaced by diode D_{RECT}, and the low-side gate drive is not used. A buck converter also provides continuous inductor current, filtered by the capacitors C_{O_BUCK} and C_{O_CHRGR}, to the load, regardless of which switch is on. Unlike the buck converter, the SEPIC converter uses Q_{PWR} only to charge the inductor. During this time the output capacitor must supply the battery-charging current. When D_{RECT} turns on, the now charged inductor provides both the output capacitor recharging and battery-charging currents. Hence, the SEPIC converter's output-voltage ripple will always be

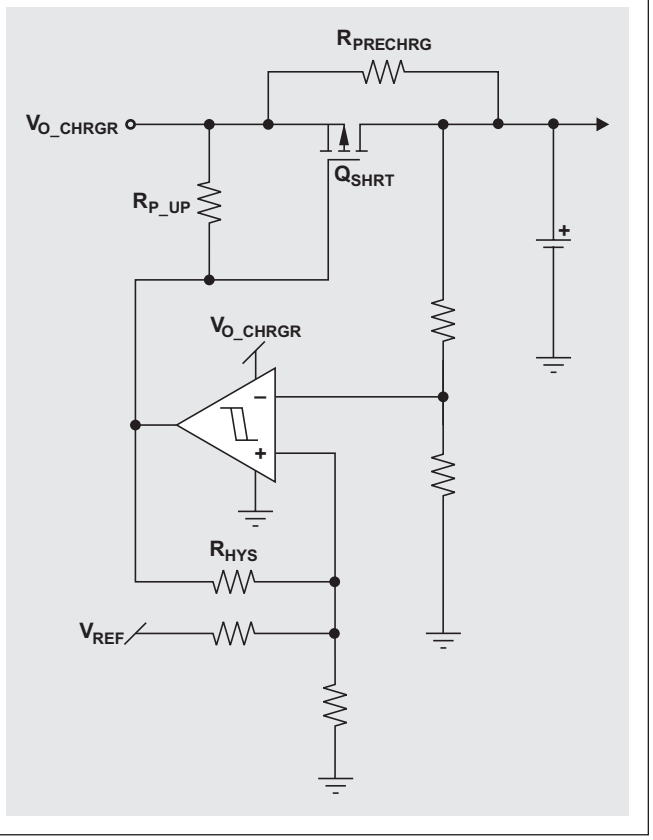
higher than that of a buck converter with the same inductor and output capacitance and same output power. This ripple can cause inaccurate current measurement across the current-sense resistor. As shown in Figure 1, a SEPIC charger requires a larger filtering capacitor (C_{FLTR}) and larger output capacitors (C_{O_SEPIC} and C_{O_CHRGR}) than does a buck charger.

Limiting precharge current when V_{BAT} << $V_{BAT(LOW)}$

With a deeply discharged battery, the battery voltage is below a predetermined $V_{BAT(LOW)}$ threshold. For battery safety, the charger should not provide full charge current to the battery. Therefore, a current-limiting resistor between the charger and battery is recommended to limit the charge current to a lower, precharging current value. Once the battery voltage exceeds the selected $V_{BAT(LOW)}$, this resistor can be shorted out with a FET to allow the controller to provide higher charge currents. Figure 3 shows how resistor $R_{PRECHRG}$, a FET (Q_{SHRT}), and a comparator can be used to implement this functionality.

$R_{PRECHRG}$ is sized so that the voltage drop from $I_{PRECHRG}$ flowing through $R_{PRECHRG}$, plus the deeply discharged battery voltage ($V_{BAT(LOW)}$), is higher than the charger's low-battery threshold (for example, V_{LOWV}), typically sensed by the V_{FB} pin. Q_{SHRT} is sized to accommodate the maximum battery voltage ($V_{BAT(MAX)}$) and the maximum charge current ($I_{CHRG(MAX)}$). The resistor across the comparator (R_{HYS}) provides hysteresis. Therefore, resistor dividers are needed on the sensed voltages fed to the comparator.

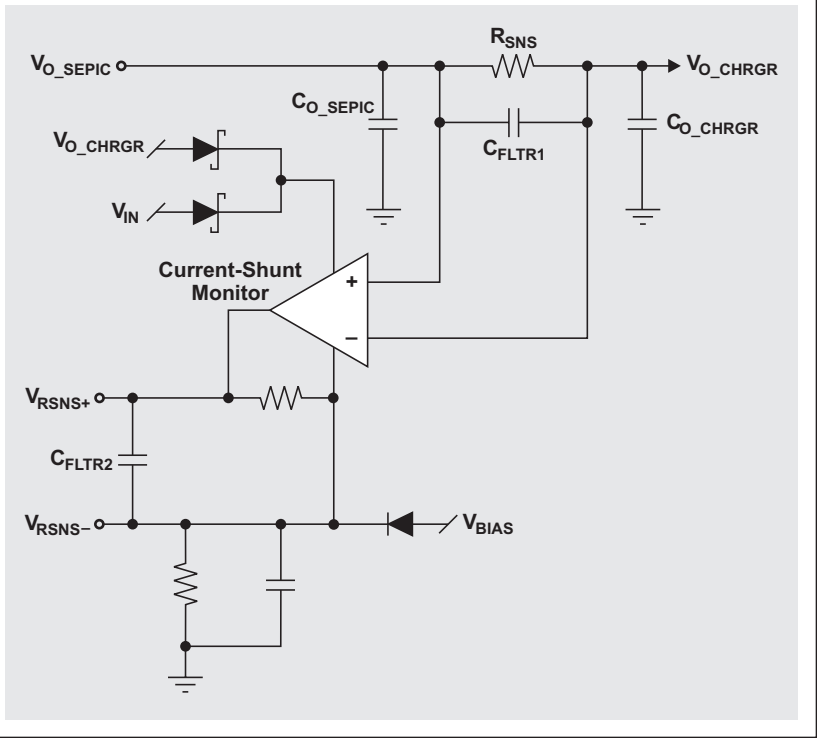
Figure 3. Precharge circuitry



Ensuring operation when $V_{BAT} > V_{IN}$ or when $V_{BAT} < V_{TH(BATSHORT)}$

A buck charger expects the battery voltage to always be less than its input voltage. In fact, many chargers have a feature that puts the charger into sleep mode if V_{BAT} is greater than V_{IN}. Alternatively, if V_{BAT} falls below a certain threshold, the IC may assume the battery is shorted and enter protection mode. If the current-sense pins (V_{RSNS+} and V_{RSNS-}) are used to determine the battery's state, the sensed voltages need to be level shifted. Figure 4 shows how to use an instrumentation amplifier configured as a current-shunt monitor to level shift the current information sensed across R_{SNS}. This circuit keeps the DC set point of the sensed voltages low enough that the IC does not enter sleep mode; it also keeps the voltages high enough so that the IC does not enter short-circuit protection. If the charger does not have its own reference voltage (V_{REF}), an external reference IC can be used.

Figure 4. Current-sense level-shift circuit



Computing the maximum charge current

A SEPIC converter's maximum charge current is a function of its available input power, both voltage and current. A simple way to estimate the maximum charge current is to compute a power balance where $P_{OUT}/P_{IN} = \eta_{EST}$, where η_{EST} is an estimate of the boost charger's efficiency in similar operating conditions. The following equation can be used to estimate the maximum charge current at a specific battery voltage:

$$I_{CHRG(MAX)} = \frac{V_{IN(MPP)} \times I_{IN(MPP)} \times \eta_{EST}}{V_{BAT}},$$

where $V_{IN(MPP)}$ is the solar panel's maximum power-point voltage, and $I_{IN(MPP)}$ is the solar panel's maximum power-point current.

R_{SNS} should be sized to provide $I_{CHRG(MAX)}$. Because capacitor C_{MID} between the inductors stays charged to the input voltage, Q_{PWR} must have a voltage rating slightly higher than $V_{IN(MAX)} + V_{BAT(MAX)}$. In a SEPIC converter, L1's peak current is the maximum input current ($I_{IN(MPP)}$) plus half the ripple current ($\Delta I_L/2$), and the peak current of L2 and diode D_{RECT} is the maximum output current ($I_{CHRG(MAX)}$) plus $\Delta I_L/2$. Q_{PWR} sees the sum of these peak currents when it is on, so it must have a current rating higher than $I_{IN(MPP)} + I_{CHRG(MAX)} + \Delta I_L$. The bq24650 charger controller can adjust the charge current to keep the solar-panel output at its maximum power point.

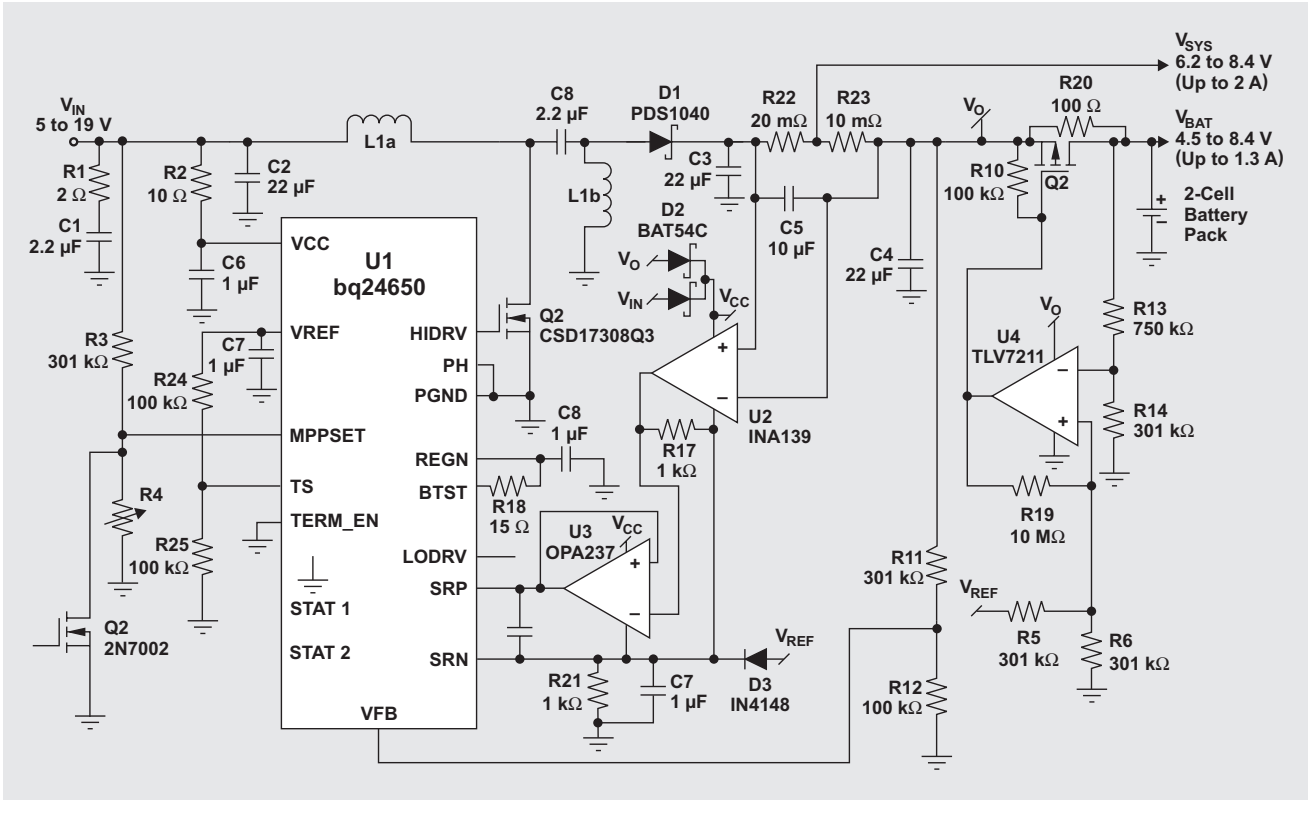
Design example of a solar-charged battery

Table 1 maps the functional pin names from Figure 1 to the corresponding bq24650 pin names in Figure 5. Figure 5 shows the charge controller configured to charge a two-cell Li-Ion battery with a maximum charge voltage of 8.4 V. The maximum charge current was limited to 1.3 A. The power NFET (Q2) and rectifying diode (D1) were sized using standard design guidelines for a SEPIC converter. The inductor and the output capacitors (C3 and C4) were sized to reduce inductor-current ripple and the resulting output-voltage ripple as well as to improve the small-signal control-loop phase margin. A coupled inductor, in the same footprint but only slightly taller than its single-inductor counterpart, was used instead of two separate inductors. The coupling effect allows the use of half the inductance that would have been necessary for the same current ripple

Table 1. Cross-reference for controller pin names

FIGURE 1 CONTROLLER PIN NAME	bq24650 PIN NAME
$GDRV_{HI}$	HIDRV
$GDRV_{LO}$	LODRV
V_{RSNS+}	SRP
V_{RSNS-}	SRN
FB	VFB

Figure 5. The bq24650 configured as a SEPIC charger



if two separate inductors had been used. R18 was used to slow down the fast turn-on of Q1. Also, the controller's PH pin was grounded to help provide the boosted output voltage. A 10-µF filter capacitor (C5) was necessary to reduce switching noise coupled into the current-shunt monitor (U2). To prevent the output of the current-shunt monitor (U2) from loading the SRP pin, a unity-gain buffer (U3), with ground shifted to match that of the current monitor, was necessary. With a discharged battery voltage of 4.5 V and the bq24650's V_{LOWV} = 1.55 V/2.1 V × 8.4 V = 6.2 V, a minimum precharge resistance ($R_{PRECHRG(MIN)}$) greater than

$$\frac{6.2\ \text{V} - 4.5\ \text{V}}{0.133\ \text{A}} = 13\ \Omega$$

was needed. A value of 100 Ω was selected for R20.

Figure 6 shows the efficiency of this charger. Although the bq24650 is internally compensated for a buck charger, when it is configured as a SEPIC charger its small-signal control loop is stable over a wide operating range, as shown in Figure 7. When using the bq24650 with a different power-stage inductor and different capacitors and batteries, the designer is responsible for confirming loop stability.

Figure 6. Efficiency of charger in Figure 5

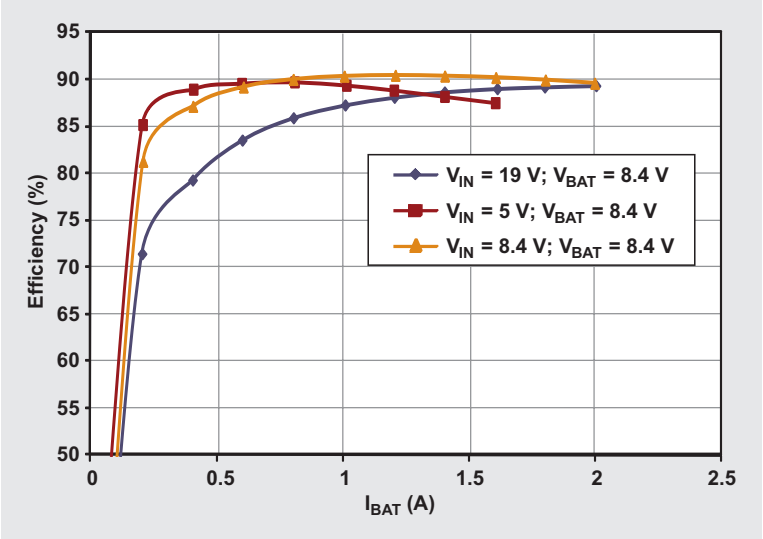
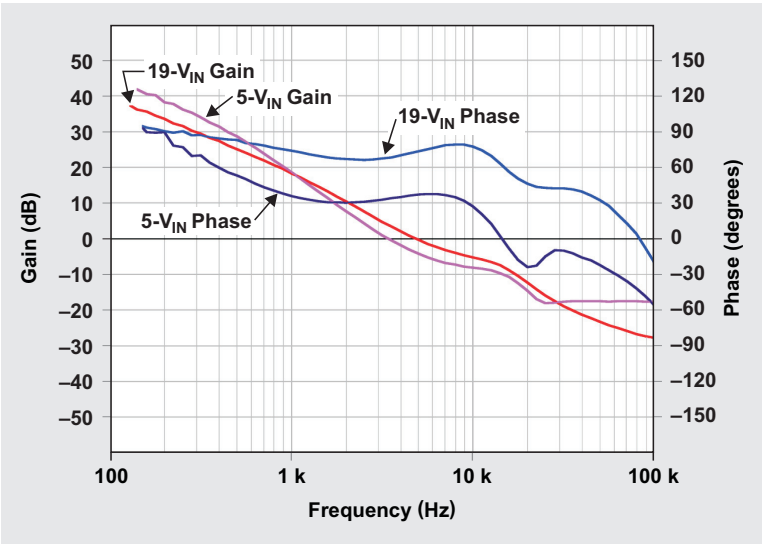


Figure 7. Bode plot of gain and phase with an open feedback loop at full charge current



Conclusion

The demand for a buck/boost battery charger is growing, especially as demand for charging from solar panels grows. By following the guidelines presented in this article and using the proposed additional circuitry, the designer can convert a buck charger controller like the bq24650 into a SEPIC charger. When converting a different buck charger into a buck/boost SEPIC charger, the designer is responsible for understanding how that charger operates in order to determine which additional circuitry is necessary and to confirm stable operation.

Related Web sites

power.ti.com
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Replace *partnumber* with bq24650, CSD17308Q3, INA139, OPA237, or TLV7211

Remote sensing for power supplies

By Tiger Zhou
Senior Applications Engineer

Remote sensing is widely used in telecommunication applications to meet the demanding accuracy requirements of critical ASICs and processors. This article discusses design considerations for remote sensing, including power-plane shortages, component placement, parasitic resistance, and potential oscillations. Also, a practical example demonstrates the effectiveness of a high-frequency bypass capacitor for mitigating oscillations associated with remote sensing.

In high-end telecommunication applications, the designer often faces the challenges of delivering power across large-scale printed circuit boards. To give precious real estate to critical ASICs and processors, the power supplies are often allocated to the corner or edge of the board. To compensate for the resistive drop of the power path, remote sensing is often used—especially for low-voltage, high-current applications. If not attended to, the dynamic nature of the load coupled with the parasitic resistance of the power path may affect the operation of the power supply.

Figure 1. Remote feedback to differential amplifier compensates for parasitic-resistance voltage drop

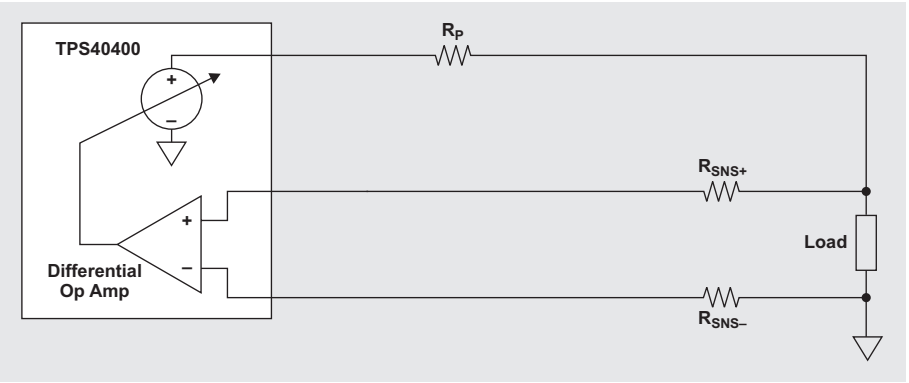
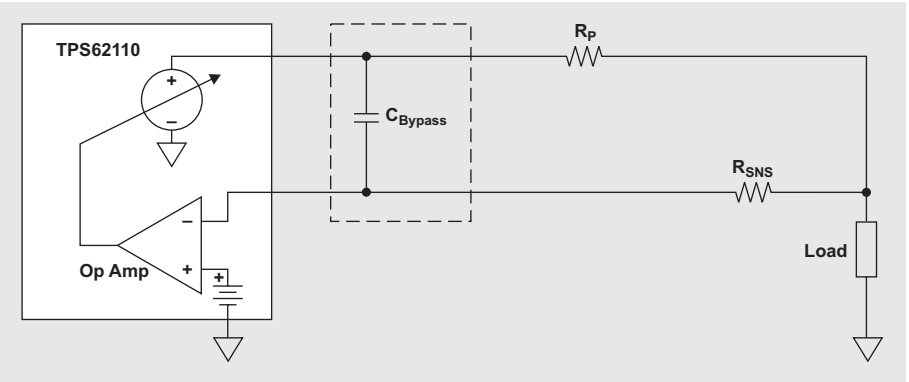


Figure 2. Remote sensing via resistor R_{SNS} regulates the output for R_P voltage drop



Reducing power-path impedance

The available power planes can be used to reduce the DC voltage gradient to within regulation tolerance. The power plane helps with DC-regulation accuracy and improves system efficiency by reducing the resistive drop along the power path.

Splitting the output capacitance

It is important for a dynamic load such as a gate driver to split the output capacitance between the supply and the remote load. The output capacitance at the remote load acts as a bypass capacitor for the dynamic load, reducing the ripple/noise current from the delivering path. It also stabilizes the output voltage at a remote sensing point, which makes both the monitoring and the sensing circuitry more accurate and reliable.

High-frequency bypass capacitor

Adding a high-frequency bypass capacitor at the local power supply is also beneficial. Modern converters are often equipped with a differential amplifier for remote sensing. Two sensing resistors are located near the remote side and connect the load voltage back to the controller by differential pairs. As shown in Figure 1, the Texas Instruments (TI) TPS40400 synchronous buck controller has a dedicated differential amplifier that compensates for the voltage drop across the power-path parasitic resistance (R_P).

If there is no dedicated differential amplifier, the power supply can still be remotely sensed. A remote sense resistor can connect the load voltage back to the converter, compare the load voltage to the reference voltage, and regulate the output voltage. Figure 2 shows the TI TPS62110 step-down converter configured to remotely

sense the load and regulate the output for any parasitic-resistance (R_P) voltage drop.

However, when a dynamic load is applied as illustrated in Figure 2, the remote sense line picks up the dynamic voltage and tries to compensate for the voltage drop across the parasitic resistance (R_P). This may result in a low-frequency oscillation due to the controller propagation delay. It appears as slight jittering on the switching waveform and causes elevated ripple on the output side. A high-frequency bypass capacitor (C_{Bypass}) can easily remedy the situation. It filters out the high-frequency dynamic voltage while keeping the characteristics of DC remote sensing.

A 7-V gate-drive power supply with a 1-µF bypass capacitor was tested with the TPS62110 step-down converter. Figure 3 shows an output ripple with 33-kHz oscillation that occurred when no bypass capacitor was used. Figure 4 shows that the addition of a 1-µF bypass capacitor clearly removed the 33-kHz oscillation from the output voltage and resulted in a low output ripple of 20 mV, which was 0.3% of the regulated voltage.

Related Web sites

power.ti.com
www.ti.com/product/TPS40400
www.ti.com/product/TPS62110

Figure 3. Original output ripple with 33-kHz oscillation

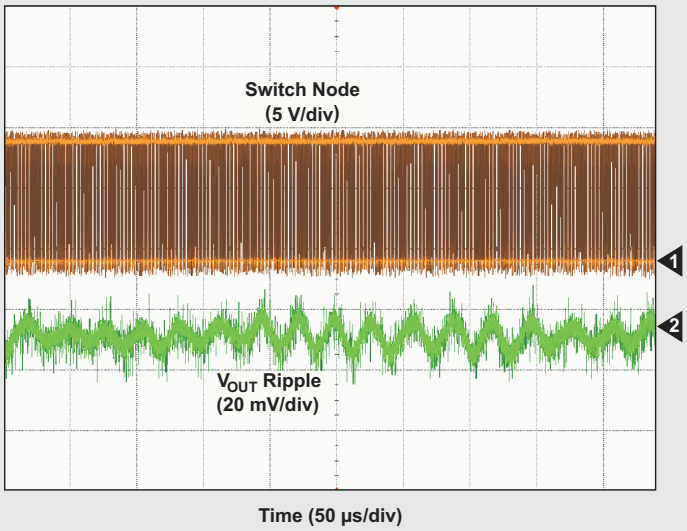
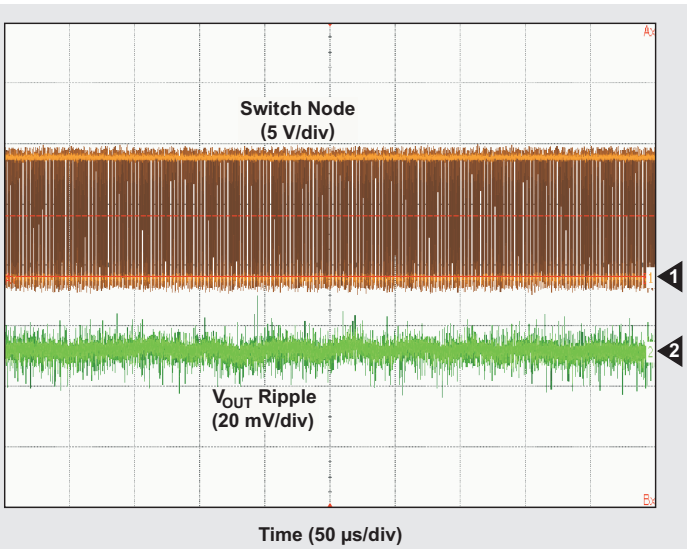


Figure 4. Low output ripple with oscillation removed by 1-µF bypass capacitor



Charging a three-cell nickel-based battery pack with a Li-Ion charger

By Charles Mauney
Senior Applications Engineer, Power Marketing

Introduction

One thing common to all portable devices is the need for a portable energy source to power the device. Many portable devices use lithium-ion (Li-Ion) polymer cells, which have a high energy density that allows them to be light and small in size. This has led to the design of numerous low-cost, highly integrated Li-Ion charger ICs to charge the batteries of such devices. For any device requiring high current, nickel-based cells are still very popular due to their low impedance, low cost, and availability. They are also considered safer than Li-Ion cells, which require many safety features.

Most systems require at least 3 V to operate, which dictates using one Li-Ion cell or three series (3S) nickel cells. Either type of cell chemistry can power portable devices, but each requires a different "fast-charge" method and thus a completely different charger IC. Due to the emphasis on Li-Ion cells and the need for nickel-charger ICs to have several external components, there are few modern, integrated, and easy-to-use nickel-charger ICs available today. This article shows the justification for using a highly integrated, low-cost, Li-Ion single-cell charger IC to charge nickel-cell packs and discusses the benefits and trade-offs.

Charge profiles of nickel and Li-Ion batteries

All nickel cells require a constant-current (CC) fast-charge rate greater than 0.3C and less than 3C to have a detectable termination signal. Discharging a full cell in one hour takes 1C of current. For example, a 2300-mAh cell is completely discharged if loaded at 2300 mA for one hour. The nickel-charger IC uses a peak-voltage-detection algorithm to monitor the nickel pack's voltage. When the pack reaches a peak voltage and then drops from that voltage by typically 3 to 6 mV per cell, the fast charge is terminated. Once the cell becomes full, the excess energy is dissipated as heat in the cell and the voltage drops, since the cell's internal impedance has decreased due to the increase in temperature. A very precise sampling circuit is required to detect the small voltage change that indicates fast-charge termination. Figure 1 is an example of a 3S NiMH-pack charge profile during one complete charge cycle at a 1-A (1C) constant-current (CC) fast charge.

Figure 1. Charge profile of 3S NiMH pack

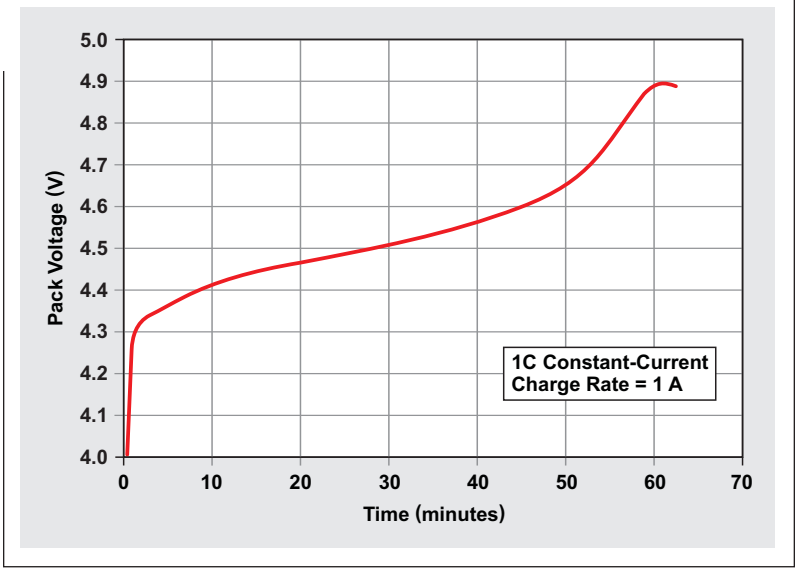
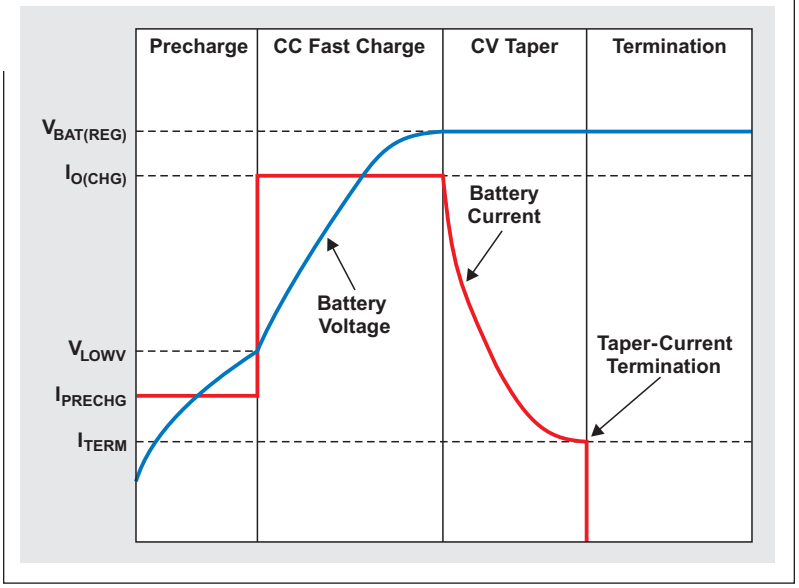


Figure 2. Charge profile of typical Li-Ion battery

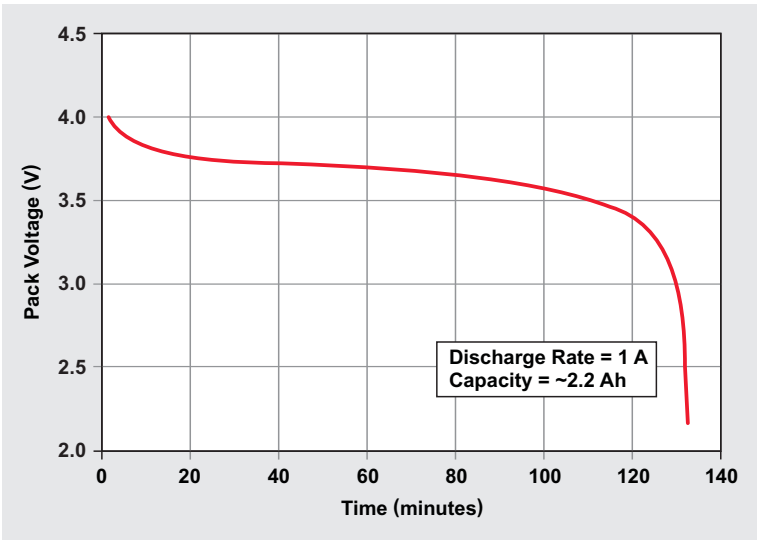


By contrast, a Li-Ion charger has a constant-current and constant-voltage (CC-CV) charge algorithm (Figure 2). During fast charge, the charge current is constant until

the pack voltage reaches 4.2 V. At this point, the voltage loop takes over and holds the voltage constant as the current tapers, typically to one-tenth of the fast-charge current. When the charge current decreases to this level, termination occurs. The precharge mode is a safety feature for Li-Ion cells with internal shorts and will be discussed later. The taper curve is nothing more than a slow RC time constant. The pack has internal resistance and capacitance. As the cell's voltage increases, the voltage drop across the cell's internal resistance decreases, which means less charge current.

A typical Li-Ion charger detects only the taper-current termination (I_{TERM}), which presents some design challenges when it is used as a nickel-cell charger. With the standard CC method, a typical NiMH cell charges up to ~1.55 V prior to termination. After termination, it relaxes to ~1.45 V. A NiCd cell terminates at ~1.45 V and relaxes to ~1.35 V. So the total voltage for a 3S NiMH pack is 4.65 V/4.35 V, and for a 3S NiCd pack, 4.35 V/4.05 V. Since the "relaxed" voltages are very close to the Li-Ion cell's termination point of 4.2 V, this article investigates using a Li-Ion single-cell charger to charge a 3S nickel pack. As the nickel cells charge to full capacity, the pack's voltage approaches 4.2 V, which causes the Li-Ion charger's current to taper to a very low level.

Figure 3. Discharge profile of 3S NiMH pack after traditional CC charging



Safety concerns

There are no real safety concerns with the Li-Ion CC-CV method of charging a 3S nickel pack up to 4.2 V, since the current naturally tapers toward 0 A as the pack reaches full capacity. Thus, there is little energy being applied to the pack once it is full. Termination of the Li-Ion charger should be disabled, since it is not necessary and reduces the charged capacity of the nickel cells if set too high. For example, with the Texas Instruments bq24040/50/90 families, the termination threshold can be programmed to a fairly low level if desired.

There is some possibility that one of the 3S nickel cells may become shorted and the fast charge may not reach voltage regulation where the current tapers toward zero. This concern can be addressed by placing a thermistor in the battery pack so the charger IC can monitor and limit the maximum temperature during this and other fault conditions. The Li-Ion charger's precharge mode is not needed or used for typical charging of a nickel pack. However, this mode can be a safety benefit that reduces the charge current if the pack voltage drops to the precharge threshold (2.5 to 3 V) due to a shorted pack. Another way to mitigate the risk of a shorted cell is to reduce the fast-charge current to C/5. This approach reduces the temperature rise at the expense of moderately increasing charging time.

Many designs for nickel chargers do have some inherent risks that are mitigated through circuitry that monitors the charging process, declares a fault condition, and stops the charge. In the typical CC fast-charge method, the IC looks for a –dV or dT/dt. One issue with this method is that after termination, if the device is removed and used for a minute and then reconnected to the charger, the pack will have to charge and heat up that much more to get a further dV drop or dT/dt increase. If the device is removed and replaced a few times, the impedance can drop only so much, and charging will not terminate. However, as previously stated, adding a thermistor will enable the charger IC to terminate the charge if the temperature fault threshold is reached. Using a Li-Ion charger does not have this recharging issue with the temperature unless a cell is shorted, which suggests an overall safer design.

Test results

A NiMH pack was charged and discharged to determine the difference in results between the CC and CC-CV charge profiles. Figure 3 shows the discharge profile and capacity of a typical 3S 2.3-Ah NiMH pack that was charged by the traditional CC method at 1C. The capacity measured ~2.2 Ah and was the reference point for judging the CC-CV charging method.

The first attempt at charging the pack with the CC-CV method yielded a surprise, since the termination was still set for 0.1C (230 mA). The battery did not charge long

before termination was reached, and the capacity was measured at 0.76 Ah. Figure 4 shows the discharge profile of the partially charged cell. Obviously, the cells were undercharged due to the 0.1C termination. The fast-charge termination threshold was similar to a 0.1C "trickle"-charge rate, which means that a much higher capacity could have been obtained if the trickle charge had been allowed to continue. In order to store more capacity in the cells, the next step was to disable termination and see how the capacity changed.

Figure 5 shows the charge profile of the pack when it was charged without termination. The profile plots current instead of voltage since the battery current was changing and the battery was in voltage regulation 99% of the charging time. CC mode was seen for a few minutes at the start of the charge. The current data was integrated over the

Figure 4. Discharge profile of 3S NiMH pack after CC-CV charging with 230-mA termination

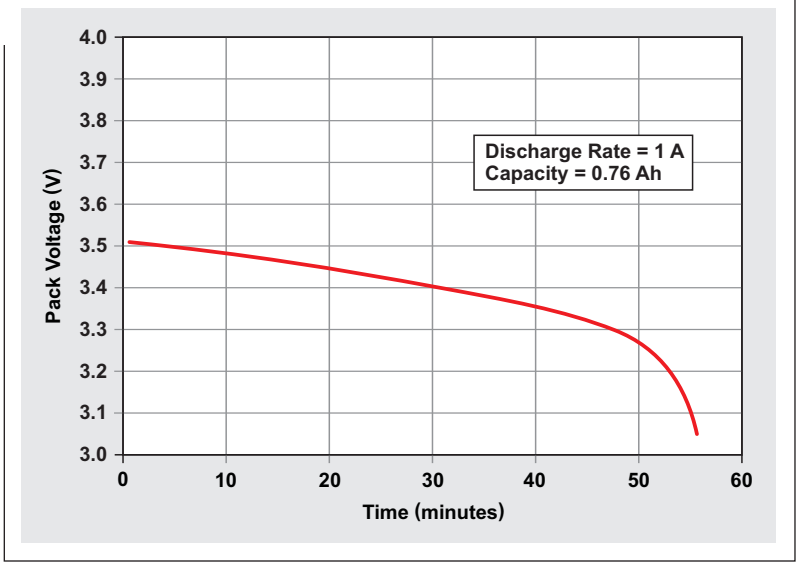
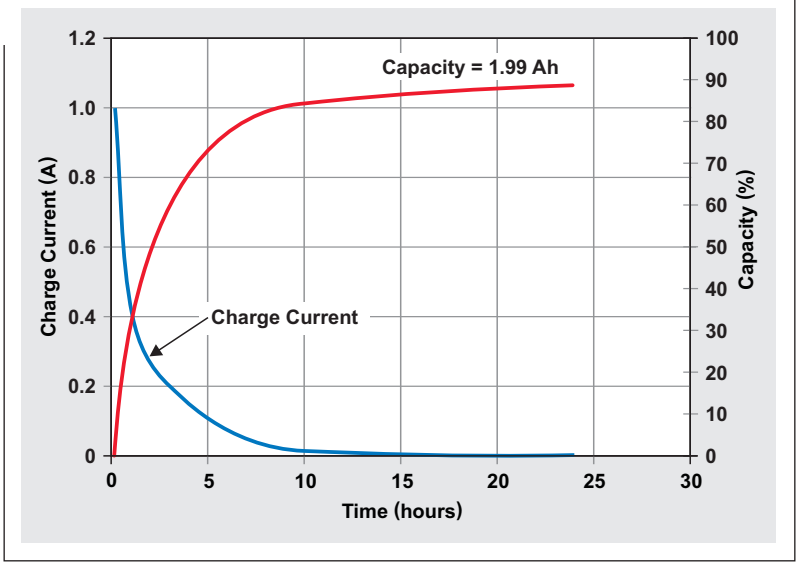


Figure 5. CC-CV charge profile of 3S NiMH pack with no charge termination



charging time and was used to determine that ~2 Ah were delivered to the cell. Figure 6 shows the discharge profile of the pack after it was charged without termination. The pack's measured capacity was 1.99 Ah.

As one can see, using the CC-CV method of charging a 3S NiMH pack results in charge capacity that approaches that of a standard CC fast charge, but the last 30% of that capacity takes longer to obtain.

Other applications

It is possible to apply the CC-CV method to a multicell Li-Ion charger to charge more than three series cells by adjusting the output voltage. If the regulation voltage is set by using the rule of thumb of 4.2 V/3 cells = 1.4 V per cell, this method should work fine. The design could be optimized by choosing a regulation voltage that is closer to the pack's full-capacity voltage with a 0.1C current level. This would give slightly more drive and would fully charge the pack quicker with a slightly higher capacity. The NiMH cells evaluated for this article had a pack voltage of 4.45 V at 0.1C (30°C) when full.

The CC-CV charging method can also be applied to a pack with NiCd chemistry. The NiCd pack has a specified voltage of 4.32 V at 0.1C (30°C) when full. The NiCd open-circuit voltage immediately after termination of a fast charge is ~1.4 V per cell times three, or 4.2 V, implying that the current goes to zero as the pack approaches full capacity.

When optimizing the maximum regulation voltage, the designer should take into account the characteristics of the cells to be used and whether or not they will be replaceable. To identify any system design issues, a charger application should always be tested over the full range of operation for all variables, plus a little more for some margin assurance.

The CC-CV charging method can be applied to adapters or USB sources, making the charging possibilities vast.

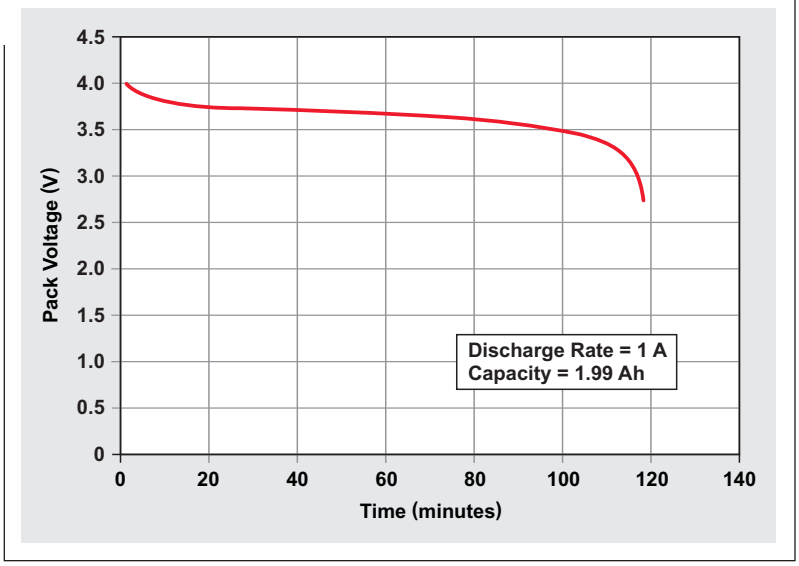
Conclusion

This article has shown that it is possible to charge a 3S NiMH pack safely and to nearly full capacity with a single-cell Li-Ion charger. The Li-Ion "nickel charger" can be classified as a hybrid fast/trickle charger, getting 70% of the bulk charge in 5 hours. The charge current tapers toward 0 A near the end of the charge, which reduces the chance of any thermal issues and possibly provides longer cell life. Most noteworthy is that the CC-CV method can be used to charge battery packs with either nickel-based or Li-Ion chemistry with no changes in hardware or firmware, making it a highly integrated solution at a low cost.

Related Web sites

www.ti.com/battery
www.ti.com/product/*partnumber*
Replace *partnumber* with bq24040, bq24050, or bq24090

Figure 6. Discharge profile of 3S NiMH pack after CC-CV charging for 119 minutes



Design considerations for a resistive feedback divider in a DC/DC converter

By Darwin Fernandez
Applications Engineer

Introduction

The resistive divider is the most common network in any DC/DC converter's feedback system. However, it is often misjudged as a circuit that simply sets the output voltage by scaling it down to a reference voltage. After computing the proper divider ratio, power-supply designers must make careful considerations when choosing the actual resistance values because they influence the overall performance of the converter. This article discusses the design considerations for the resistive divider in a feedback system and how the divider affects a converter's efficiency, output-voltage accuracy, noise sensitivity, and stability.

Efficiency

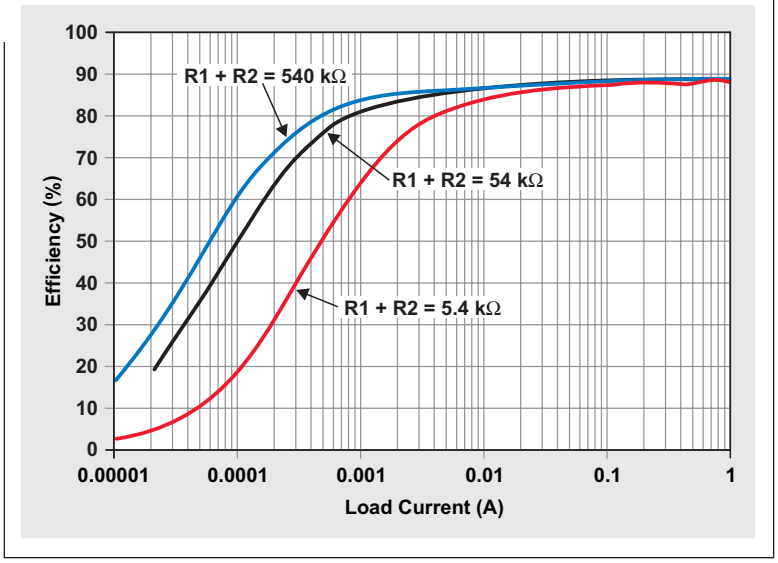
Switching DC/DC converters have relatively high efficiencies because they provide power transfer to a load through low-loss components such as capacitors, inductors, and switches. High efficiencies allow for a longer battery life and, consequently, an extended operational time for portable devices.

For low-power DC/DC converters, a typical design for resistive feedback requires the total resistance of the divider resistors (R1 + R2) to be very large (up to 1 MΩ). This minimizes the current through the feedback divider. This current is in addition to the load, which means that for lower feedback-divider resistances, the battery must supply more current and more power for the same load. Hence, efficiency is lowered. This is undesirable, especially in portable applications where battery life is important.

Design example 1

Figure 1 confirms that efficiency drops at low loads with lower feedback resistances. In this example, the Texas Instruments (TI) TPS62060EVM was used with V_{IN} = 5 V, V_{OUT} = 1.8 V, and power-save mode enabled. At high-load currents, the power dissipated by the load was much larger than the power dissipated by the resistive-feedback network. This is why the efficiencies for different R1 and R2 values converge at higher-load currents. However, at low-load currents, the differences in efficiency for different feedback resistances are more prominent. This is because the current through the divider dominated the current through the load. Therefore, to have higher efficiencies at light loads, it is good design practice to use the large feedback resistances recommended in the datasheet. If efficiency at light loads is not important in a given design, then smaller resistances can be used with essentially no impact on efficiency.

Figure 1. Efficiency of TPS62060 buck converter with different feedback-divider resistances



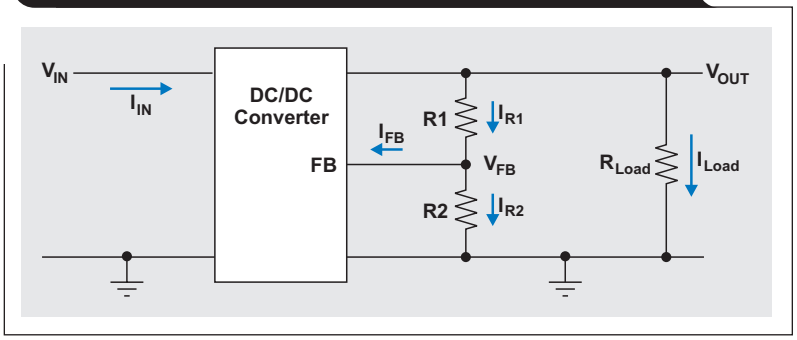
Output-voltage accuracy

Using large feedback resistances to increase efficiency was just discussed. However, choosing resistances that are too large affects the converter's output-voltage accuracy because of leakage current going into the converter's feedback pin. Figure 2 shows the current paths at the resistive feedback divider (R1 and R2). For a fixed feedback leakage current (I_{FB}), current through R1 (I_{R1}) decreases as the values of R1 and R2 increase. Therefore, an increase in divider resistance means that a larger percentage of I_{R1} leaks into the feedback pin, and the current through R2 (I_{R2}) decreases, causing a lower feedback-pin voltage (V_{FB}) than expected. Since V_{FB} is compared to an internal reference voltage to set the output voltage, any inaccuracies in the feedback voltage create inaccuracies in the output voltage. Equation 1 can be derived from Kirchhoff's Current Law, showing V_{FB} as a function of R1 and R2:

$$V_{FB} = R2 \times \frac{V_{OUT} - I_{FB}R1}{R1 + R2} \quad (1)$$

Note that I_{FB} is not fixed in a real system and can vary from device to device and over the operating conditions. To generate a worst-case estimate of the output-voltage change that is due to the leakage current, the specified maximum value of I_{FB} is used in the calculations.

Figure 2. Leakage current going into the feedback pin of a converter



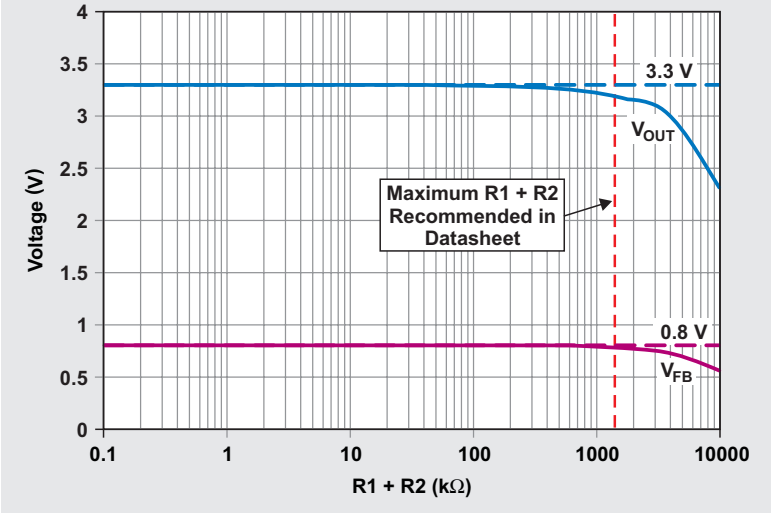
Design example 2

Equation 1 and the TI TPS62130 step-down converter were used to graph the feedback-pin voltage and the corresponding output voltage as functions of the feedback-divider resistance (Figure 3). The voltage graphs were based on the ideal resistances required to generate an output voltage of 3.3 V with a feedback-pin voltage of 0.8 V. The only error term considered was the maximum feedback leakage current of 100 nA specified in the datasheet.

Figure 3 shows that the feedback-pin voltage decreases as the feedback-divider resistance increases. Since the feedback-pin voltage is offset, the output of the converter is also offset. At low resistances, there is no offset from the feedback-pin voltage, and the output regulates at 3.3 V as designed.

When the recommended maximum value of 400 kΩ was used for resistor R2, resulting in a total divider resistance of 1650 kΩ, the leakage current caused only a minimal decrease in the output voltage. Keeping the output voltage within the datasheet's specified accuracy is typically the reason for the datasheet to specify a maximum value for one of the resistors.

Figure 3. TPS62130's V_{FB} and V_{OUT} as functions of feedback-divider resistance



Noise sensitivity

The resistive divider is one source of noise for a converter. This noise, known as thermal noise, is equal to $4K_BTR$, where K_B is Boltzmann's constant, T is the temperature in Kelvin, and R is the resistance. Using large resistance values for the divider increases this noise.

Additionally, large resistances allow more noise to couple into the converter. This noise comes from a multitude of sources, including AM and FM radio waves, cellular phone signals, and switching converters or RF transmitters on the PCB. Noise can even come from the switching DC/DC converter itself, especially if proper PCB-layout practices are not followed. Since the resistive divider is tied to the feedback pin, the noise is amplified by the closed-loop gain of the converter and is seen at the output. To reduce the susceptibility to other noise sources, a designer might use lower feedback resistances, better board layout, or shielding. Using lower feedback resistances does reduce the noise susceptibility, though at the cost of slightly lower efficiency.

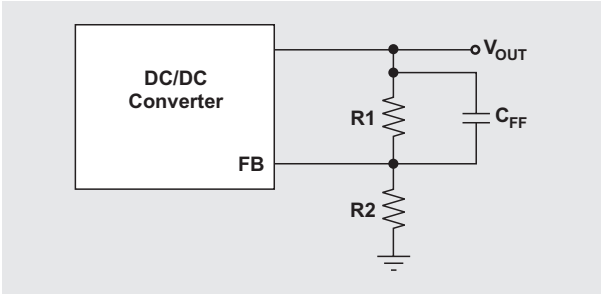
Control loop, transient response, and converter stability

A stable converter ideally has at least 45° of phase margin when measured with a network analyzer. This much phase margin gives less or no ringing on the output voltage, which prevents damage to voltage-sensitive loads during an input-voltage transient or load transient.

Depending on the control topology, the datasheet may require or recommend a feedforward capacitor (C_{FF}) to be used with the resistive feedback network. This setup is shown in Figure 4. Adding the feedforward capacitor to the resistive divider produces zero and pole frequencies that generate a phase boost capable of increasing the converter's phase margin and crossover frequency for a higher bandwidth and more stable system. Reference 2 describes this circuit in great detail. From the transfer function of the circuit in Figure 4, the zero frequency (f_z) and the pole frequency (f_p) are calculated with Equations 2 and 3, respectively:

$$f_z = \frac{1}{2\pi R1 \times C_{FF}} \quad (2)$$

Figure 4. Resistive feedback network with feedforward capacitor



$$f_p = \frac{1}{2\pi C_{FF} \times \frac{R1 \times R2}{R1 + R2}} \quad (3)$$

Clearly, the zero and pole frequencies are functions of the values used for the resistive divider and the feedforward capacitor. Therefore, increasing or decreasing the resistance values to optimize efficiency, voltage accuracy, or noise changes the frequency location of the phase boost and the overall loop of the system. To ensure stability, Equation 4 should be used to calculate a new C_{FF} value based on the previous zero frequency or the zero frequency recommended in the datasheet (whichever value is available):

$$C_{FF}(new) = \frac{1}{2\pi R1(new) \times f_z(recommended)} \text{ or } \frac{1}{2\pi R1(new) \times f_z(old)} \quad (4)$$

$$f_z(old) = \frac{1}{2\pi R1(old) \times C_{FF}(old)}$$

Design example 3

The effect of the resistive divider on converter stability is seen by using a buck converter. For example 3, the TI TPS62240 buck converter was used, with V_{IN} = 3.6 V, V_{OUT} = 1.8 V, L_{OUT} = 2.2 µH, C_{OUT} = 10 µF, and I_{Load} = 300 mA.

Figures 5 and 6 respectively show the closed-loop response and its corresponding transient response under three different resistive divider networks. A feedforward capacitor was used in each network to illustrate how changing the divider-network components changes the stability of the buck converter. When the values recommended in the datasheet for the divider-network components were used (R1 = 365 kΩ, R2 = 182 kΩ, and C_{FF} = 22 pF), the converter was stable, with a phase margin of 59°. Its transient response verified this with a slight output-voltage drop and no oscillations.

Figure 5. Buck converter's closed-loop frequency response with different R1, R2, and C_{FF} values

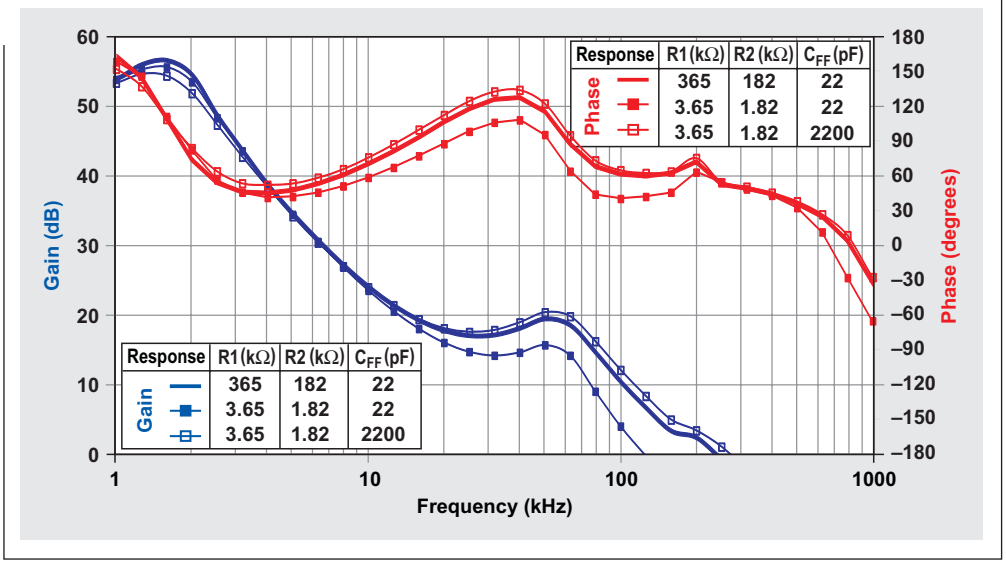
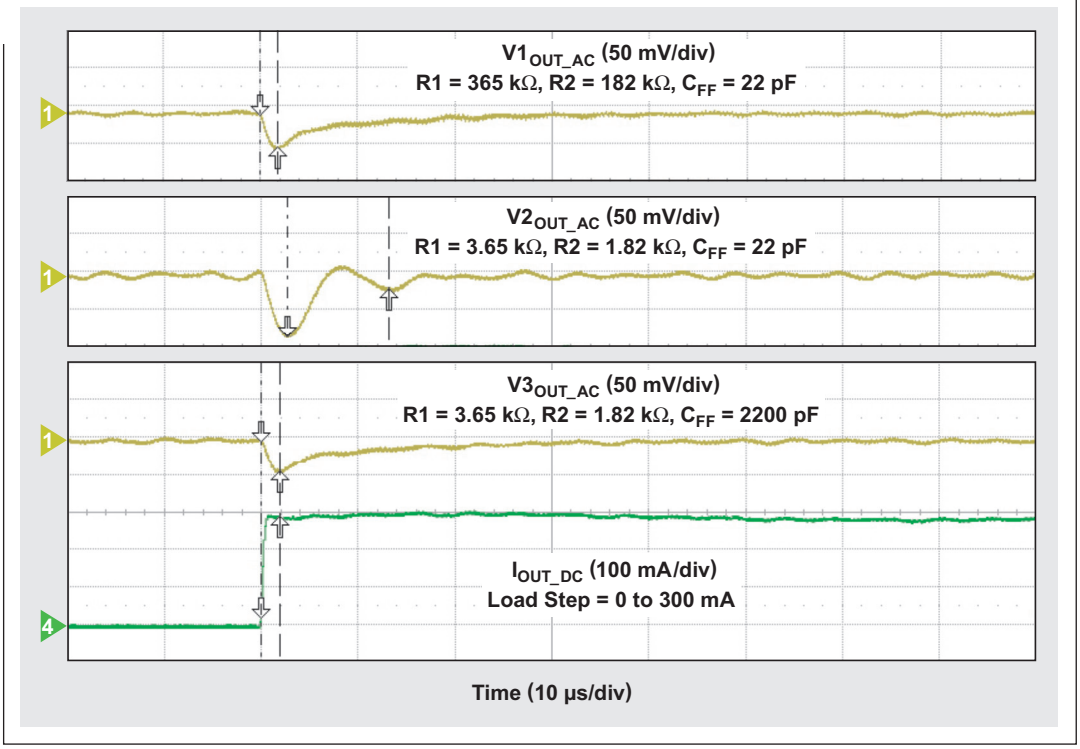


Figure 6. Buck converter's load-transient response with different R1, R2, and C_{FF} values



When the feedback-divider resistances were proportionally reduced to R1 = 3.65 kΩ and R2 = 1.82 kΩ, but the same feedforward capacitance (C_{FF} = 22 pF) was used, the change in the zero and pole frequencies of the feedback network moved the phase boost away from the crossover frequency of the loop. The frequency response showed that the converter was less stable, with a phase margin of 40°. The converter's transient response verified this with a larger output-voltage drop and more ringing. To maintain the original frequency response and stability, the C_{FF} value was recalculated for the new feedback-resistance values.

Using Equation 4 with the smaller resistance values yielded a new value for the feedforward capacitance of 2200 pF. This generated results similar to those of the first condition. The converter was stable with a phase margin of 56°, which its transient response verified with a slight output-voltage drop and no oscillation.

For a converter that utilizes a feedforward capacitor in its control topology, changing the values of the resistive divider can easily make the converter less stable. However, the example just given shows that changing these values maintains the same frequency response and transient response as long as the feedforward capacitance is adjusted appropriately.

Special-case designs

The internal compensation of some converters requires a specific C_{FF} value if a designer must use a feedforward capacitor to improve stability. For these cases, Equation 4 should not be used. Rather, the designer should use the datasheet's recommended design equations. For example, the TI TPS61070 has internal compensation across the high-side feedback resistor (R1). Its datasheet recommends using the following design equation for adding a capacitor in parallel to R1:

$$C_{FF} = 3\ \text{pF} \times \left(\frac{200\ \text{k}\Omega}{R2} - 1 \right) \quad \textbf{(5)}$$

Conclusion

The resistive feedback divider or network affects the efficiency, output-voltage accuracy, noise sensitivity, and stability of a DC/DC converter. To achieve the performance shown in a particular datasheet, it is important to use the datasheet's recommended values for feedback components. In other cases, system requirements may dictate departing from these recommendations to achieve some other design goal. By understanding the trade-offs between these different parameters, designers can choose larger or smaller resistances to meet their application needs.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Anthony Fagnani, "Optimizing resistor dividers at a comparator input," Application Report	SLVA450
2. Brian Butterfield, "Optimizing transient response of internally compensated dc-dc converters with feedforward capacitor," Application Report	SLVA289

Related Web sites

power.ti.com
www.ti.com/product/*partnumber*
Replace *partnumber* with TPS61070, TPS62060, TPS62130, or TPS62240

Source resistance and noise considerations in amplifiers

By Jorge Vega
Characterization Engineer

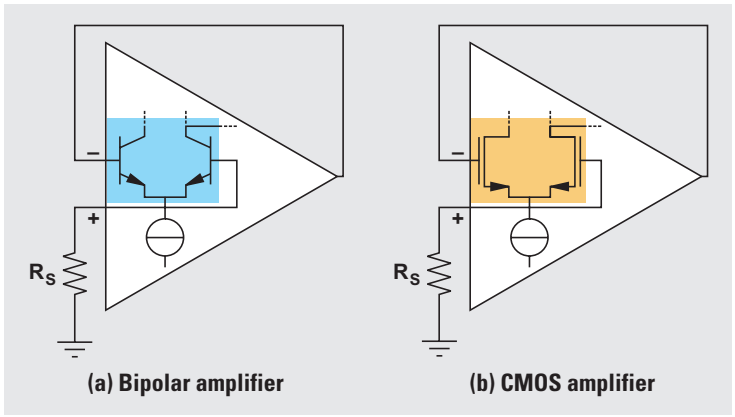
Introduction

In many applications it is critical to design for low noise. Different types of sensors, filters, and audio designs are common examples where low noise is critical. These applications can be modeled as a source resistance in series with a signal source. The source resistance has thermal noise and also converts current noise into voltage noise, increasing the amplifier's total output-voltage noise.

A common question is how to choose an amplifier that minimizes total output-voltage noise, even when a source resistance is modeled. This question is relevant because amplifiers can be fabricated in either bipolar or CMOS technology. Bipolar amplifiers have significant current noise but often have lower voltage noise than CMOS amplifiers for a given quiescent current. Current noise is most problematic when the source resistance is high. This article demonstrates how a CMOS amplifier is the best choice when a high source resistance is used and noise is the only concern. Knowing these facts along with the voltage-noise specifications of the amplifier is instrumental in making the right choice. For this analysis, it is assumed that the bipolar and CMOS amplifiers have comparable bandwidth, power, and intrinsic voltage noise. The trade-offs between the two amplifiers are also examined.

Figure 1 shows each amplifier in a buffer configuration with a modeled source resistance connected to the positive input and ground. The different noise contributions from the modeled source resistance, input-referred voltage noise, and input-referred current noise are taken into account. These models serve as reference examples for analyzing and comparing amplifier noise performance in a low-noise application where noise is the only parameter in play.

Figure 1. Buffer-configured amplifiers with source resistance attached to positive input and ground



Total voltage-noise contributions

The key to choosing the best amplifier is to understand how the amplifier's current noise, voltage noise, and resistor thermal noise combine to form the total output-voltage noise. Depending on the magnitude of the source resistance, sometimes low-current noise is the key specification. In other cases, low-voltage noise may be the key specification. To better understand this, the designer needs to have a grasp of the amplifier's total voltage-noise density, which is given by a root-mean-square (RMS) operation:[1]

$$E_O = \sqrt{(e_N)^2 + (i_N \times R_S)^2 + (4K_B T R_S)} \quad (1)$$

In Equation 1, E_O is the total voltage-noise density at the output of the amplifier. e_N and i_N are the voltage- and current-noise densities of the amplifier, respectively. R_S is the source resistance connected to the positive input. K_B is Boltzmann's constant, equal to 1.38×10^{-23} J/K, and T is absolute temperature in Kelvin units. At room temperature, T is equal to 300 K. For all the calculations in this article, it is assumed that T is at room temperature.

The three terms in Equation 1 account for the noise-density contributors at the output of the amplifier. The first term, e_N, is the intrinsic voltage-noise density of the amplifier, which is independent of the source resistance. The second term, $i_N \times R_S$, shows the voltage contribution from the current-noise density multiplied by the source resistance. The third term, $\sqrt{4K_B T R_S}$, corresponds to the thermal-noise density of the source resistance. The RMS sum of these three terms yields the total voltage-noise density of the amplifier in volts per square root of hertz.

In Equation 1, note that $i_N \times R_S$ increases faster than $\sqrt{4K_B T R_S}$ as the source resistance increases. This is significant because, for low source resistance, the thermal-noise density of the source resistance dominates. But there comes a point when the contribution from $i_N \times R_S$ becomes

significant and is thus the dominating noise source. Figure 2 presents a plot of these two noise contributors in a linear-linear scale.

Bipolar amplifiers have significant current-noise density, which the source resistance converts into voltage-noise density. CMOS amplifiers have a major advantage in this regard over bipolar amplifiers because their components have extremely low current-noise density. Even though both bipolar and CMOS amplifiers have all three noise contributors, the total noise density in a CMOS amplifier is primarily from only two noise contributors, e_N and $\sqrt{4K_BTR_S}$. This is because the current-noise density of $i_N \times R_S$ is very small and its impact on the total noise density can be neglected.

Datasheets for low-noise amplifiers present a typical graph showing the voltage- and current-noise densities versus frequency traces. Figure 3a shows this graph for a bipolar amplifier, and Figure 3b for a CMOS amplifier. Note that the trace for current-noise density is not shown in Figure 3b because it is extremely low, well into the femtoamperes range. This is in contrast to the bipolar amplifier's current-noise density, which is in the picoamperes range, or 1000 times greater than that of the CMOS amplifier.

To compare the noise contributors on both amplifiers, the voltage and current noise at 1 kHz can be used as the reference. This facilitates the explanation, since the thermal-noise region, not the flicker region, of the graphs is being examined. In Figure 3a,[2] the bipolar amplifier has a voltage-noise density of 3.3 nV/$\sqrt{\text{Hz}}$ and a current-noise density of 1 pA/$\sqrt{\text{Hz}}$. In Figure 3b,[3] the CMOS amplifier has a voltage-noise density of 4.5 nV/$\sqrt{\text{Hz}}$. With these values for intrinsic-noise density identified, the noise-density contributors can be quantified by using all three terms of Equation 1 for the bipolar

Figure 2. Voltage-noise density versus source resistance

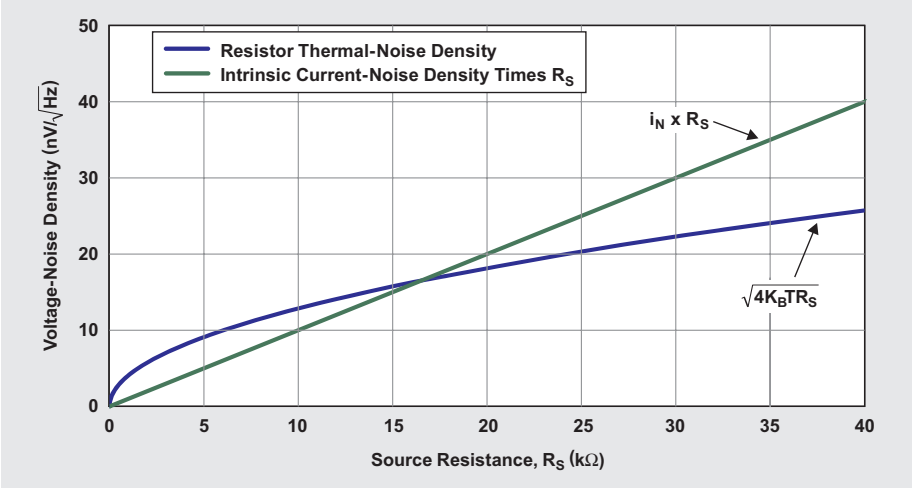
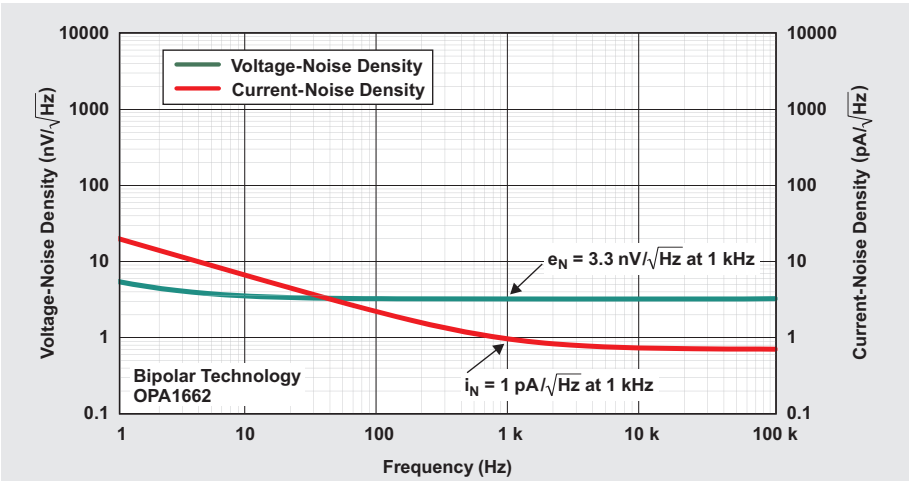
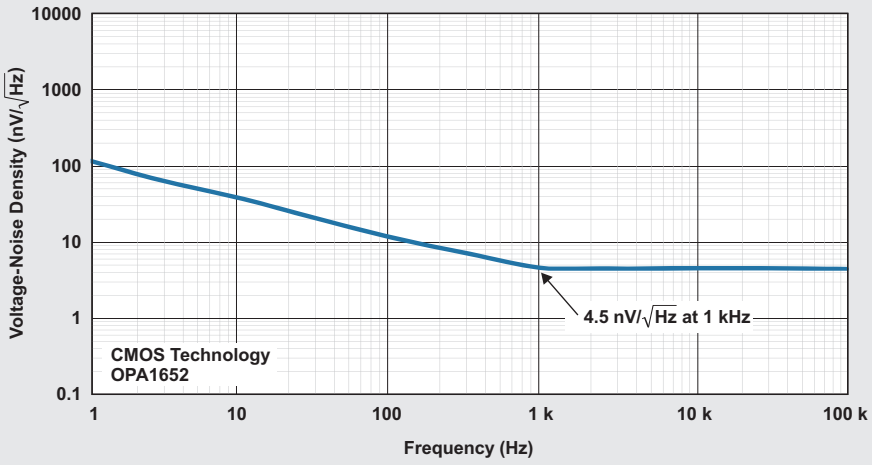


Figure 3. Noise density versus frequency on bipolar and CMOS amplifiers



(a) Voltage- and current-noise density for a bipolar amplifier



(b) Voltage-noise density for a CMOS amplifier

amplifier, and the first and third terms for the CMOS amplifier. The sweeping variable in Equation 1 is the source resistance. In other words, the voltage-noise density is calculated as a function of source resistance with voltage- and current-noise densities taken at 1 kHz. This is shown in Example 1 for a bipolar amplifier.

Example 1: Bipolar amplifier's noise contributors

$$e_N = 3.3\ nV/\sqrt{Hz}$$

$$i_N \times R_S = 1\ pA/\sqrt{Hz} \times R_S$$

$$\sqrt{4K_BTR_S} = \sqrt{4 \times \left(1.38 \times 10^{-23}\ J/K\right) \times \left(300\ K\right) \times \left(R_S\right)}$$

The second term of Equation 1 is not used for the CMOS amplifier because current-noise density is negligible in a CMOS amplifier. The calculation for the CMOS amplifier is shown in Example 2.

Example 2: CMOS amplifier's noise contributors

$$e_N = 4.5\ nV/\sqrt{Hz}$$

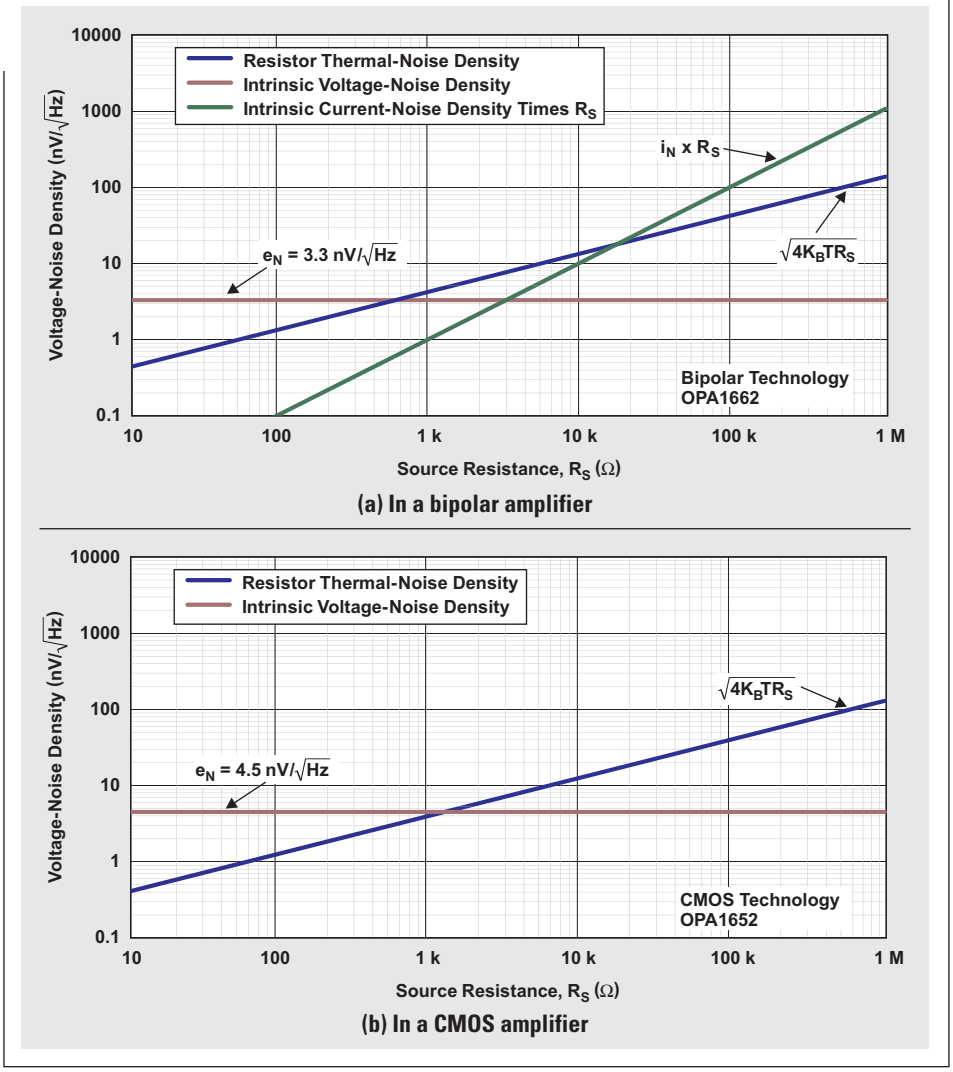
$$\sqrt{4K_BTR_S} = \sqrt{4 \times \left(1.38 \times 10^{-23}\ J/K\right) \times \left(300\ K\right) \times \left(R_S\right)}$$

Figure 4a plots the three noise-density contributors for the bipolar amplifier. The trace for intrinsic voltage-noise density (e_N) is constant and independent of the source resistance. As the source resistance increases, the value of $i_N \times R_S$, although small for low source resistance, increases faster than that of $\sqrt{4K_BTR_S}$, becoming the dominating noise source.

The noise-density contributors for the CMOS amplifier are plotted in Figure 4b.

For the bipolar amplifier, the total voltage-noise density (E_O) at 1 kHz can be obtained by using Equation 1. The

Figure 4. Voltage-noise density versus source resistance



total noise density for the CMOS amplifier is given by Equation 2:

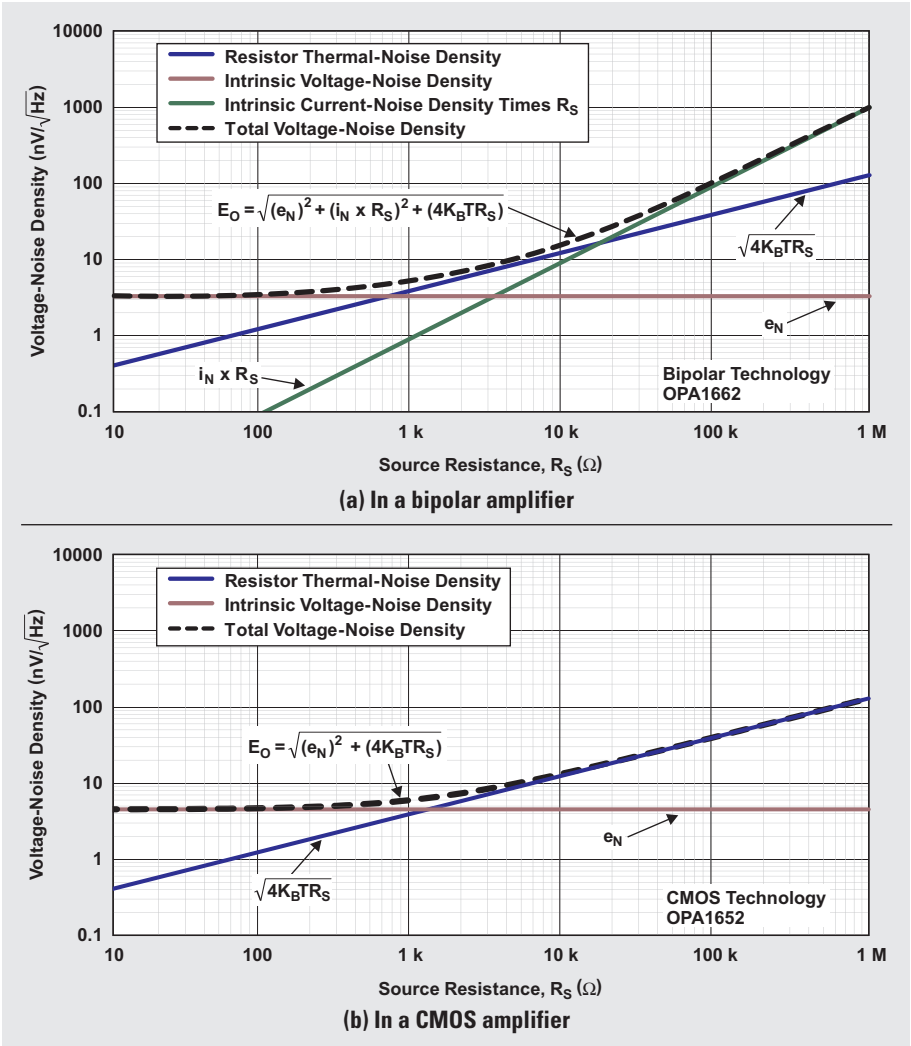
$$E_O = \sqrt{(e_N)^2 + (4K_BTR_S)} \quad \textbf{(2)}$$

Figures 5a and 5b respectively plot the total voltage-noise density for the bipolar amplifier and the CMOS amplifier.

Figure 5a shows that, on a bipolar amplifier using low source-resistance values, the total voltage-noise density (E_O) converges with the intrinsic voltage-noise density (e_N) of the amplifier. For midrange source-resistance values, E_O approaches the thermal-noise density of the source resistance $\left(\sqrt{4K_BTR_S}\right)$. For large source-resistance values, E_O converges with the product of the current-noise density and the source resistance $(i_N \times R_S)$. The current-noise density becomes a significant contributor towards the amplifier's total output-voltage-noise density as source resistance increases.

Figure 5b shows that, for low source resistance, the E_O of the CMOS amplifier, like that of the bipolar amplifier, converges with the amplifier's intrinsic voltage-noise density (e_N). The difference between the bipolar and the CMOS amplifier lies where the noise density converges for high source resistance. As already noted, the bipolar amplifier's E_O converges with $i_N \times R_S$ for large source resistance. However, as shown in Figure 5b, the CMOS amplifier's E_O converges with the thermal-noise density of the source resistance $\left(\sqrt{4K_BTR_S}\right)$.

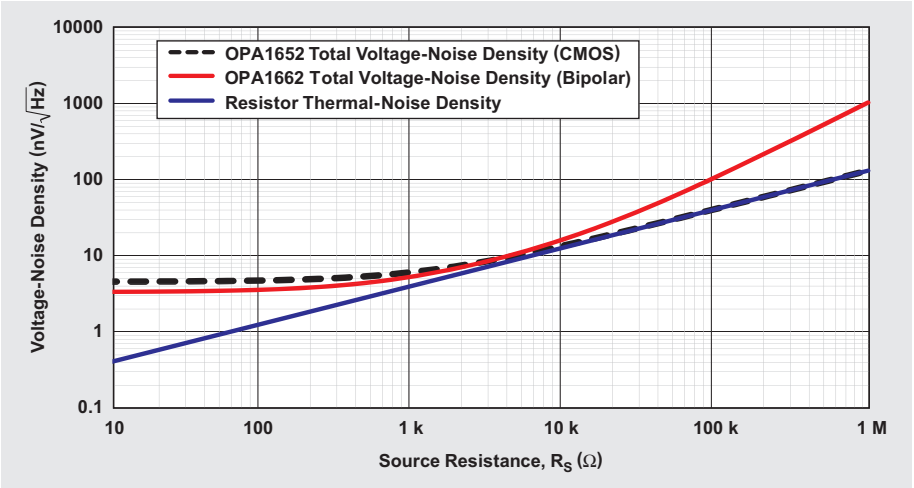
Figure 5. Total voltage-noise density versus source resistance



Noise analysis using different R_S values

Figure 6 shows the total voltage-noise density as a function of source resistance at 1 kHz for the bipolar and CMOS amplifiers. The thermal noise of the source resistance is included to serve as a reference. This graph may be found in the datasheets of low-noise amplifiers such as the Texas Instruments OPA1662[2] and OPA1652.[3] It helps the system engineer decide which type of amplifier is best to use, depending on the source resistance modeled. If the source-resistance curve is not available, the engineer can make point calculations by plugging values from the voltage-noise-density curves into Equations 1 and 2 to get an idea of what type of amplifier will yield the best noise characteristic.

Figure 6. Total voltage-noise density of bipolar and CMOS amplifiers compared to thermal-noise density of R_S



In Example 3, the bipolar amplifier (Figure 3a) has a voltage noise (e_N) of 3.3 nV/$\sqrt{\text{Hz}}$ at 1 kHz. The equivalent resistor value that generates this same amount of noise can be calculated by rearranging $e_N = \sqrt{4K_BTR_S}$ to solve for R_S.

Example 3: Calculations with $i_N \times R_S << \sqrt{4K_BTR_S}$ and a small R_S value

$$R_S = \frac{e_N^2}{4K_BT},$$

where e_N = 3.3 nV/$\sqrt{\text{Hz}}$, K_B = 1.38 × 10^{-23} J/K, and T = 300 K.

$$R_S = \frac{\left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right)^2}{4\times\left(1.38\times10^{-23}\ \text{J/K}\right)\times\left(300\ \text{K}\right)} \approx 660\ \Omega$$

Substituting 660 Ω for R_S yields the noise-density contributors:

$$e_N = 3.3\ \text{nV}/\sqrt{\text{Hz}}$$

$$i_N \times R_S = \left(1\ \text{pA}/\sqrt{\text{Hz}}\right)\times\left(660\ \Omega\right) = 0.66\ \text{nV}/\sqrt{\text{Hz}}$$

$$\sqrt{4K_BTR_S} = \sqrt{4\times\left(1.38\times10^{-23}\ \text{J/K}\right)\times\left(300\ \text{K}\right)\times\left(660\ \Omega\right)} = 3.3\ \text{nV}/\sqrt{\text{Hz}}$$

The total noise is

$$E_O = \sqrt{\left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(0.66\ \text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right)^2} = 4.71\ \text{nV}/\sqrt{\text{Hz}}.$$

Note that if the current-noise density is ignored, the following is obtained:

$$E_O = \sqrt{\left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right)^2} = 4.66\ \text{nV}/\sqrt{\text{Hz}}$$

Thus, ignoring this term for a source resistance of 660 Ω has little impact on the total voltage-noise density. Factoring yields a term of $\sqrt{2}$, or 3 dB:

$$E_O = \sqrt{2}\times\left(3.3\ \text{nV}/\sqrt{\text{Hz}}\right) \approx 4.7\ \text{nV}/\sqrt{\text{Hz}}$$

Thus, if a source resistance of 660 Ω is used, the increase in noise is approximately 4.7 nV/$\sqrt{\text{Hz}}$, or 3 dB. Beyond 660 Ω, the total noise starts to converge with the thermal noise of the source resistance.

Example 4: Calculations with $i_N \times R_S = \sqrt{4K_BTR_S}$ and a larger R_S value

Just like in Example 3, the current-noise density begins to become a major factor when $\sqrt{4K_BTR_S}$ becomes approximately equal to $i_N \times R_S$:

$$i_N \times R_S = \sqrt{4K_BTR_S}$$

$$R_S = \frac{4K_BT}{\left(i_N\right)^2},$$

where i_N = 1 pA/$\sqrt{\text{Hz}}$, K_B = 1.38 × 10^{-23} J/K, and T = 300 K.

$$R_S = \frac{4\times\left(1.38\times10^{-23}\ \text{J/K}\right)\times\left(300\ \text{K}\right)}{\left(1\ \text{pA}/\sqrt{\text{Hz}}\right)^2} \approx 16\ \text{k}\Omega$$

Substituting 16 kΩ for R_S yields the noise-density contributors:

$$e_N = 3.3\ \text{nV}/\sqrt{\text{Hz}}$$

$$i_N \times R_S = \left(1\ pA/\sqrt{Hz}\right) \times \left(16\ k\Omega\right) = 16\ nV/\sqrt{Hz}$$

$$\sqrt{4K_BTR_S} = \sqrt{4 \times \left(1.38 \times 10^{-23}\ J/K\right) \times \left(300\ K\right) \times \left(16\ k\Omega\right)}$$
$$= 16\ nV/\sqrt{Hz}$$

The total noise is

$$E_O = \sqrt{\left(3.3\ nV/\sqrt{Hz}\right)^2 + \left(16\ nV/\sqrt{Hz}\right)^2 + \left(16\ nV/\sqrt{Hz}\right)^2}$$
$$= 23.06\ nV/\sqrt{Hz}.$$

If the intrinsic voltage-noise density is ignored, the following is obtained:

$$E_O = \sqrt{\left(16\ nV/\sqrt{Hz}\right)^2 + \left(16\ nV/\sqrt{Hz}\right)^2} = \sqrt{2} \times \left(16\ nV/\sqrt{Hz}\right)$$
$$= 22.82\ nV/\sqrt{Hz}$$

Ignoring the intrinsic voltage-noise density for a source resistance of 16 kΩ has little impact on the total noise density because the amplifier is starting to be affected only by the current-noise density and the thermal-noise density of the source resistance. Beyond 16 kΩ, the total voltage-noise density begins to converge with $i_N \times R_S$. The bipolar amplifier provides the least noise of the two amplifiers at low source impedance, from approximately 660 Ω and below.

The CMOS amplifier shows the least amount of noise at high source resistance. The 3-dB point is when the thermal noise of the source resistance is equal to 4.5 $nV/\sqrt{Hz}$, which corresponds to 1.2 kΩ. Beyond this point, the output noise starts to converge with the thermal noise of the source resistance because the CMOS amplifier has negligible current noise.

Choosing the right amplifier

A quick rule of thumb can be used to decide if a bipolar or a CMOS amplifier is best: If e_N is larger than or equal to $i_N \times R_S$, a bipolar amplifier should be used; otherwise a CMOS amplifier should be used. For example, if data for the OPA1662 were used and R_S equaled 100 Ω, then e_N would be 3.3 $nV/\sqrt{Hz}$, and $i_N \times R_S$ would be 1 $pA/\sqrt{Hz}$ × 100 Ω, or 0.1 $nV/\sqrt{Hz}$. Since 3.3 $nV/\sqrt{Hz}$ > 0.1 $nV/\sqrt{Hz}$, using a bipolar amplifier would be best. If R_S equaled 100 kΩ, then $i_N \times R_S$ would be 1 $pA/\sqrt{Hz}$ × 100 kΩ, or 100 $nV/\sqrt{Hz}$. Since 3.3 $nV/\sqrt{Hz}$ < 100 $nV/\sqrt{Hz}$, the right choice would be a CMOS amplifier. This rule of thumb ignores the thermal noise of the source resistance, which will be present regardless of the amplifier chosen. Figure 6 validates this rule of thumb.

If the application calls for a midrange source resistance of about 4 kΩ, what amplifier should be used according to Figure 6? When the gain bandwidth, power, and DC specifications are comparable, a bipolar amplifier can be almost twice the price of a CMOS amplifier. So the choice would be the CMOS amplifier because it yields noise characteristics that are approximately equal to those of the bipolar amplifier for this source resistance.

The choice of source resistance also plays a role in the amplifier's total harmonic distortion plus noise (THD+N). The THD+N in bipolar amplifiers gets worse with increasing source resistance, whereas the CMOS amplifier has negligible current noise to increase the total distortion.[4] In a low-noise, low-distortion application with a large source resistance, a CMOS amplifier would be a better choice.

Coincidentally, the measurement of current noise in bipolar amplifiers is done with the choice of a source resistance whose value for thermal noise is lower than $i_N \times R_S$. The voltage noise due to $i_N \times R_S$ is intentionally made bigger than the thermal voltage noise of the source resistance so it can be easily measured.

Conclusion

Low-noise applications that demand the use of source resistance require an amplifier that minimizes the total output-voltage noise. This article has discussed the different voltage-noise contributors on a bipolar and a CMOS amplifier that have comparable bandwidth, power, and intrinsic voltage noise. It has been shown that the bipolar amplifier is a poor choice for use with high source resistance because the voltage-noise contribution from $i_N \times R_S$ becomes increasingly dominant. The CMOS amplifier is a better choice since its current noise is negligible. With this information in hand, the system designer is better equipped when choosing between a bipolar or a CMOS amplifier for a low-noise application when noise is the only concern.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. David Johns and Kenneth W. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1997.	
2. "SoundPlus™ low-power, low noise and distortion, bipolar-input audio operational amplifiers," OPA1662/64 Datasheet	SBOS489
3. "SoundPlus™ low noise and distortion, general-purpose, FET-input audio operational amplifiers," OPA1652/54 Datasheet	SBOS477
4. Jorge Vega and Raj Ramanathan. "Harmonic distortion: Part I – Understanding harmonic distortion vs. frequency measurements in op amps." *EN-genius Network: analogZONE: acquisitionZONE* [Online]. Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_013012	

Related Web sites

amplifier.ti.com
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Industrial flow meters/flow transmitters

By Deepa Kalyanaraman
Business Development Manager, End-Equipment Solutions

Introduction

Flow meters are an integral tool for measuring the flow of liquid, gas, or a mixture of both in applications used in the food and beverage industry, oil and gas plants, and chemical/pharmaceutical factories. There are many different types of flow meters available on the market. Fluid characteristics (single or double phase, viscosity, turbidity, etc.), flow profile (laminar, transitional, or turbulent, etc.), flow range, and the need for accurate measurements are key factors for determining the right flow meter for a particular application. Additional considerations such as mechanical restrictions and output-connectivity options also impact this choice. The overall accuracy of a flow meter depends to some extent on the circumstances of the application. The effects of pressure, temperature, fluid, and dynamic influences can potentially alter the measurement being taken.

Industrial flow meters are used in environments where noise and sources of high-voltage surges proliferate. This means that the analog front end (AFE) needs to operate at high common-mode voltages and have extremely good noise performance, in addition to processing small electrical signals with high precision and repeatability. The 4- to 20-mA loop is the most common interface between flow transmitters and flow-control equipment such as programmable logic controllers. Flow transmitters can either be powered by this loop or have a dedicated power line. Flow transmitters designed to use the loop have extremely stringent power constraints, as all of the electronics for signal acquisition/processing and transmission may need to operate solely off the 4- to 20-mA loop. Ultra-low-power processors such as the Texas Instruments MSP430™ and TMS320C5000™ DSP families, in conjunction with high-precision, low-power AFE solutions, are commonly used in loop-powered transmitters. Transmitters with digital-connectivity features such as a process field bus (PROFIBUS), I/O links, and/or wireless connectivity are increasingly popular, as they reduce start-up times and provide continuous monitoring and fault diagnostics. All these factors greatly improve productivity and efficiency of the automation loop.

This article provides an overview of the working operation of the four most common flow meters: differential-pressure, electromagnetic (magmeter), Coriolis, and ultrasonic, the last of which includes Doppler-shift and transit-time flow meters. The key uses of these meters are presented along with their advantages/disadvantages and system considerations.

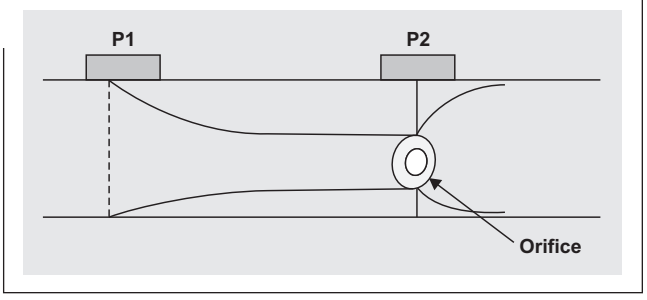
Differential-pressure flow meter

This meter operates based on Bernoulli's principle. It measures the differential-pressure drop across a constriction in the flow's path to infer the flow velocity. Common types of differential-pressure flow meters are the orifice, the pitot tube, and the venturi tube. An orifice flow meter (Figure 1) is used to create a constriction in the flow path. As the fluid flows through the hole in the orifice plate, in accordance with the law of conservation of mass, the velocity of the fluid that leaves the orifice is more than the velocity of the fluid as it approaches the orifice. By Bernoulli's principle, this means that the pressure on the inlet side is higher than the pressure on the outlet side. Measuring this differential pressure gives a direct measure of the flow velocity from which the volumetric flow can easily be calculated.

System considerations for differential-pressure flow meters

- Robust and mature technology with easy maintenance (no moving parts)
- Suitable for turbulent flow
- Poor accuracy for low-flow measurements
- Uses extractive flow-measurement technique, so there is always a permanent pressure loss that must be overcome with extra pumping energy
- Requires strict placement of pipe fittings, elbows, and bends for downstream and upstream constriction taps

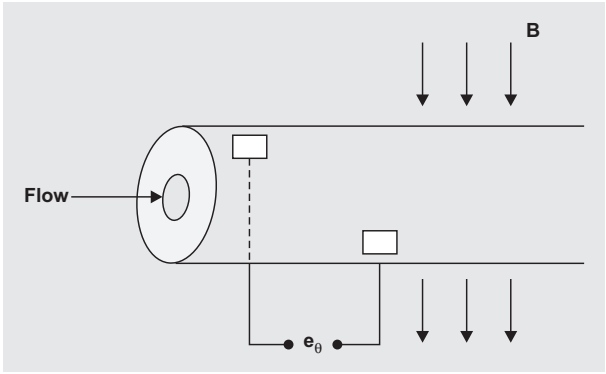
Figure 1. Differential-pressure orifice flow meter



Electromagnetic flow meter (magmeter)

The electromagnetic flow meter, also known as a magmeter, is based on Faraday's law of electromagnetism and can be used to measure the flow only of conductive fluids. Two field coil magnets are used to create a strong magnetic field across a pipe (Figure 2). Per Faraday's law, as the liquid flows through the pipe, a small electric voltage is induced. This voltage is picked up by two sensor electrodes located across the pipe. The rate of fluid flow is directly proportional to the amplitude of the electric voltage induced.

Figure 2. Electromagnetic flow meter



e_θ (voltage) = $-d\Phi B/dt$ B = Magnetic field

The coils used to create the magnetic field can be excited with AC or DC power sources. In AC excitation, the coils are excited with a 50-Hz AC signal. This has the advantage of drawing a smaller current from the system than the DC excitation technique. However, the AC excitation method is susceptible to interference from nearby power cables and line transformers. Thus, it can introduce errors into the signals measured. Furthermore, null drifting is a common problem for AC-powered systems and cannot be calibrated out. Pulsed DC excitation, where the polarity of the current applied to the field coils is periodically reversed, is commonly employed as a method to reduce the current demand and mitigate the problems seen with AC-powered systems.

System considerations for electromagnetic flow meters (magmeters)

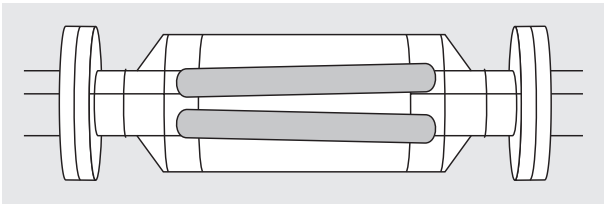
- Can measure only fluids with conductivity greater than 10 µS/cm, eliminating their use in the petroleum, oil, and gas industries, since hydrocarbons have poor conductivity
- Sensor-electrode choices change depending on fluid conductivity, pipe construction, and type of installation
- No losses in system pressure, which may be critical in applications that cannot tolerate pressure drops, such as applications with low-velocity flow
- Ideal for corrosive and dirty fluids, slurries, etc., provided the liquid phase has sufficient conductivity, since the flow meter has no internal parts
- High accuracy to within ±1% of indicated flow
- Higher cost

Coriolis flow meter

This popular flow meter directly measures mass flow rate. The installation can include a single straight tube or, as shown in Figure 3, a dual curved tube. The architecture with a single straight tube is easier to construct and maintain because it is subject to fewer stress forces, but it is susceptible to interference and noise. The architecture with dual curved tubes cancels out any noise picked up because the two tubes oscillate in counterphase.

In Coriolis meters, the tubes through which the fluid flows are made to oscillate at a particular resonant frequency by forcing a strong magnetic field on the

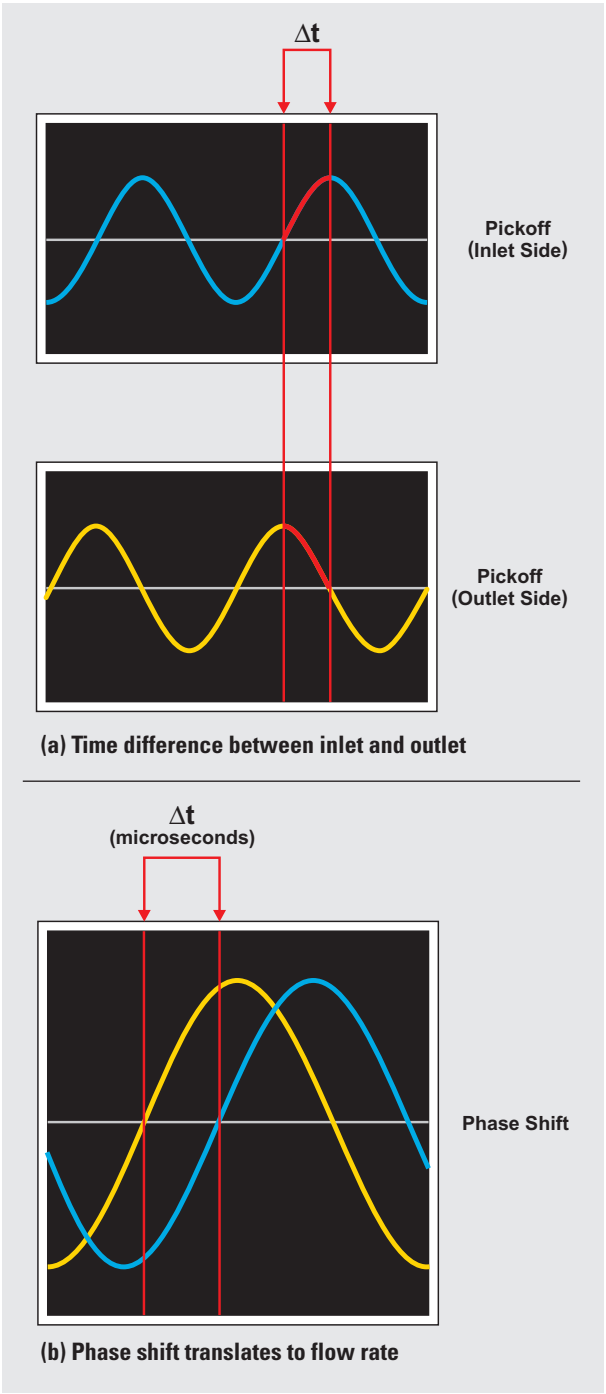
Figure 3. Coriolis flow meter



F_C (Coriolis force) = $2m\omega v_r$ ω = Speed of rotation
m = Moving mass v_r = Radial velocity

tubes. When the fluid starts flowing through the tubes, it is subject to Coriolis force. The oscillatory motion of the tubes superimposes on the linear motion of the fluid, exerting twisting forces on the tubes. This twisting is due to Coriolis acceleration acting in opposite directions on either side of the tubes and the fluid's resistance to the vertical motion. Sensor electrodes placed on both the inlet and outlet sides pick up the time difference caused by this motion. This phase shift due to the twisting forces is a direct measurement of mass flow rate. Figure 4 shows typical detection results.

Figure 4. Signals detected by sensor in Coriolis flow meter



System considerations for Coriolis flow meters

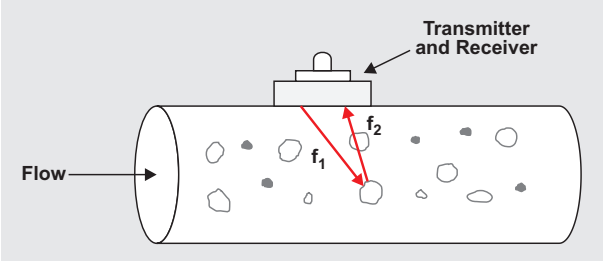
- Direct measurement of mass flow rate eliminates effects of temperature, pressure, and flow profile on the measurement
- High accuracy
- Sensor can make simultaneous measurements of flow rate and density because the basic oscillating frequency of the tube(s) depends on the density of the fluid flowing inside
- Cannot measure flow rate of fluids with entrained particles (liquids with gas or solid particles; gas with liquid bubbles; etc.) because such particles dampen the tube's oscillations, making it difficult to take accurate measurements

Ultrasonic flow meter

Doppler-shift meter

The Doppler-shift ultrasonic meter, as the name suggests, is based on the Doppler effect. This meter (Figure 5) consists of transmit- and receive-node sensors. The transmit node propagates an ultrasound wave of 0.5 to 10 MHz into the fluid, which is moving at a velocity v. It is assumed that the particles or bubbles in the fluid are moving at the same velocity. These particles reflect the propagated wave to the receiver with a frequency shift. The difference in frequency between the transmitted and received ultrasound wave is a measure of the flow velocity. Because this type of ultrasound flow meter requires sufficient reflecting particles in the fluid, it does not work for extremely pure single-phase fluids.

Figure 5. Doppler-shift ultrasonic flow meter



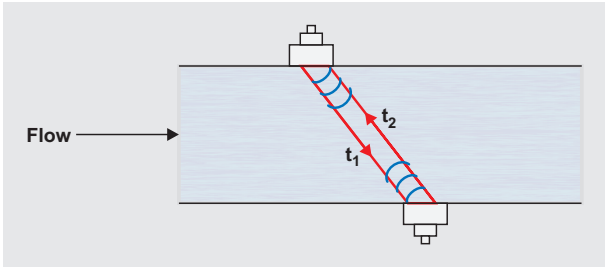
Q (volumetric flow rate) = $K\Delta(f_1, f_2)$
f_1 and f_2 = Incident and reflected frequencies, respectively
K = A constant that is a function of angle of incidence/reflection, reflective-particle position, cross section

Transit-time meter

On the contrary, the transit-time ultrasonic meter can be used for measuring only extremely clean liquids or gases. It consists of a pair of ultrasound transducers mounted along an axis aligned at an angle with respect to the fluid-flow axis (Figure 6). These transducers, each consisting of a transmitter/receiver pair, alternately transmit to each other. Fluid flowing through the pipe causes a difference between the transit times of beams traveling upstream and downstream. Measuring this difference in transit time gives flow velocity.

The difference in transit time is typically on the order of nanoseconds. Hence, precise electronics are needed to make this measurement, whether the time is measured directly or a conversion corresponding to frequency difference is made. The latter is more popular and involves an FFT analysis of the difference in frequency between waves received in and against the flow direction.

Figure 6. Transit-time ultrasonic flow meter



Q (volumetric flow rate) = $K \times (t_1 - t_2)/(t_1 \times t_2)$
K = A constant that is a function of acoustic-path length, ratio between the radial and axial distances from the sensors, velocity distribution (flow-velocity profile), cross section
t_1 = Transit time for downstream path
t_2 = Transit time for upstream path

System considerations for ultrasonic flow meters

- The Doppler-shift flow meter is relatively inexpensive
- The transit-time flow meter provides one of the few techniques for measuring nonconductive slurries and corrosive fluids
- The ultrasonic flow meter is externally clamped onto existing pipes, allowing installation without cutting or breaking pipes, which minimizes personal exposure to hazardous liquids and reduces possible system contamination
- The ultrasonic flow meter's most significant disadvantage is its dependence on the fluid's flow profile; for the same average flow velocity, the meter could give different output readings for different flow profiles

Conclusion

This article has discussed the working operation of the four most common flow meters. Their key uses and design considerations, summarized in Table 1, were also discussed.

There is a wide range of solutions available for flow meters, including interfaces for industrial field-bus transceivers, a variety of AFEs, and low-power processing solutions. Selecting the right flow meter for an application from the various different technologies and designs available on the market can be rather challenging. By understanding the properties of the fluid being used, knowing the application's flow rates and required measurement accuracy, and being aware of physical constraints and operating conditions, the designer can narrow down the choices faster.

Related Web site

www.ti.com/solution/flow_meter

Table 1. Characteristics of the four most common flow meters

FEATURE	DIFFERENTIAL-PRESSURE	ELECTROMAGNETIC	CORIOLIS	ULTRASONIC
Volume/mass measurement	Volume	Volume	Mass	Volume
Fluid/flow rate	Not suitable for gases with low flow rate	Not suitable for gas flow	Not suitable for very high flow rates (>20,000 l/min)	Not suitable for gas flow
Particulate flow/slurries	Conditionally suitable	Suitable	Conditionally suitable	Conditionally suitable
Liquid/gas mixture	Not suitable	Conditionally suitable	Conditionally suitable	Conditionally suitable
Liquid conductivity	Suitable for all	Only conductive liquids	Suitable for all	Suitable for all
Food and beverage (consumable liquids)	Not suitable	Suitable	Suitable	Most suitable for non-intrusive measurement
Installation/maintenance	Easy installation; periodic cleaning required	Moderate installation effort; minimal maintenance	Installation outlay can be considerable; relatively maintenance-free	Easy installation and maintenance
Typical accuracy	0.6 to 2% of full scale	0.2 to 1% of reading	0.1 to 0.5% of reading	Doppler-shift meter: 1% of reading to 2% of full scale
				Transit-time meter: 0.35% of reading to 2% of full scale

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