High-Performance Analog Products

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High-performance mobile computers with turbo-mode CPUs have peak power demands that could require an AC adapter with a significantly higher power rating than standard CPUs. Instead of a higher-cost adapter, a high-efficiency, turbo-boost charger can be used to manage the power from the battery and adapter to meet the excessive power demands when the CPU operates in turbo mode. This article discusses the operation of a typical turbo-boost charger and presents efficiency analysis of its two modes of operation.

Benefits of a multiphase buck converter 8

Single-phase, low-voltage buck converters work well at up to about 25 A; but at higher currents, multi-phase buck converters offer several performance advantages. These include higher efficiency due to lower transitional losses; lower output ripple; better transient performance; and lower ripple-current-power dissipation in the input capacitor, FETs, and inductors. This article discusses these advantages, shows waveforms from a typical application, and provides a performance analysis and tips for board layout.

Downslope compensation for buck converters when the duty cycle exceeds 50%. 14

Current-mode control in a PWM forward converter with a duty cycle greater than 50% has the potential of going into subharmonic oscillations. This article presents as an example a three-switch forward converter that provides improved stability with downslope compensation and extends the maximum duty cycle to 67%. Included are typical waveforms and calculations to determine the value of the current-sensing resistor.

High-efficiency AC adapters for USB charging 18

Battery chargers with USB outlets are becoming a universal standard for 10- to 25-W chargers. This article explores the advantages of using a synchronous rectifier to increase efficiency and satisfy the push towards high-density, small-form-factor adapters. Included are typical waveforms and efficiency plots comparing the performance of a Schottky diode to that of a synchronous rectifier.

Amplifiers: Op Amps

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This article describes a new methodology that has proven to be effective in making settling-time measurements for modern op amps. Detailed is a relatively inexpensive and simple way to measure settling time that bases accuracy and precision on the relative speed of the waveform generator and the sample-and-hold circuit. Included with a description of the test setup are typical waveforms and settling-time plots.

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Audio
- Amplifiers: Op Amps
- Low-Power RF
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

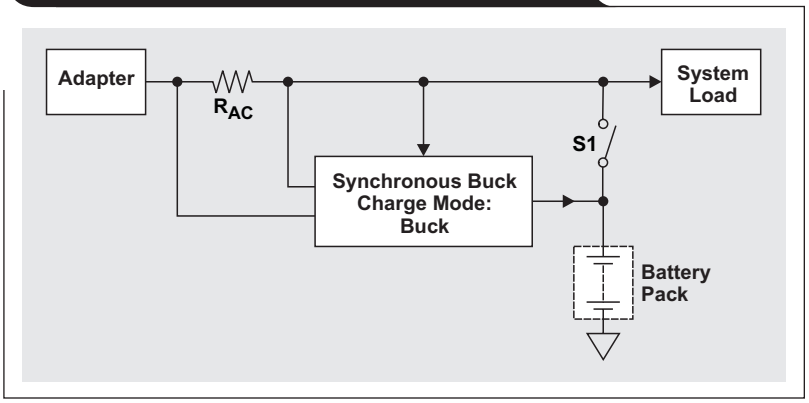
Turbo-boost charger supports CPU turbo mode

By Jinrong Qian, *Product Line Manager,*
and Suheng Chen, *Design Engineer*

Introduction

To continuously improve a CPU's dynamic performance for fast processing of multiple complicated tasks in mobile computers, it is essential to increase the CPU frequency with full utilization of the CPU's thermal capability in a short time period. This could cause the total power required by the system to exceed the power delivered from a power source like an AC adapter, which may result in crashing the adapter. One possible solution is to increase the adapter's power rating, but at a higher cost. This article discusses the turbo-boost charger, which allows the adapter and battery to power the system simultaneously to meet instantaneous and excessive power demands from a notebook computer system operating in CPU turbo mode.

Figure 1. Adapter and battery-charger system



In traditional mobile computer systems, an AC adapter provides the power, and any power not needed by the system is used to charge the battery. When an AC adapter is not available, the battery provides power to the system by turning on switch S1 (see Figure 1). The adapter can be used to power the system and charge the battery simultaneously, which may require it to have a high power rating, increasing both its size and its cost without active control. Dynamic power management (DPM) typically is used to accurately monitor the total power drawn from the adapter, which gives high priority to powering the system.

Once the adapter's power limit is reached, the DPM control system regulates the input current (power) by reducing the charge current, providing power directly from the adapter to the system without power conversion for optimum efficiency. With the heaviest system load, all the adapter power is used to power the system without charging the battery at all. Therefore, the main design criterion is to make sure that the adapter's power rating is high enough to support peak CPU power and other system power.

To meet the increasing demand for improved system performance in processing complicated tasks fast with multiple CPU cores and enhanced graphics processor units (GPUs), Intel developed its turbo-boost technology in the Sandy Bridge processors. This technology allows processors to burst their power above the thermal design power (TDP) for a short time period in the range from a few tens of milliseconds to tens of seconds. However, an AC adapter is designed to provide the power just above the demand from the processors and platform at a TDP level considering the design tolerance. When a charger system detects that the adapter has reached its input power rating after its charge current has been reduced to zero through DPM, the simplest way to avoid crashing the AC adapter is to achieve CPU throttling by reducing the CPU frequency, which compromises system performance. How can the CPU be operated faster at above the TDP level for a short time period without crashing the adapter or increasing its power rating?

Turbo-boost battery charger

When the total power required by the system load and battery charger reaches the adapter's power limit, DPM starts to reduce the battery's charge current. The battery charger stops charging, and its charge current is reduced to zero when the system load alone reaches the AC adapter's power limit. As the system continues to increase its load during the CPU turbo mode, the battery charger, which is usually a synchronous buck converter, is idle, as no remaining power is available to charge the battery. The synchronous buck converter is actually a bidirectional DC/DC converter that can operate in either buck or boost mode, depending on the operating conditions. If the battery has enough capacity, the battery charger can operate in boost mode to provide power to the system in addition

to the power from the AC adapter. Figure 2 shows a block diagram of a turbo-boost battery charger.

When and how does the battery charger start to transition from buck charge mode to boost discharge mode? The system can enter CPU turbo mode at any time, and it is usually too late to inform the charger to initiate this transition through an SMBus. The charger should automatically detect which operating mode is needed. It is also critical that the system be designed to achieve a fast transition from buck to boost mode and vice versa. A DC/DC converter needs a soft-start time of a few hundred microseconds to a few milliseconds to minimize the inrush current. The adapter should have a strong overloading capability to support the whole system's peak power before the charger transitions into boost discharge mode. Most of the AC adapters currently available can hold their output voltage over a few milliseconds.

Figure 2. Turbo-boost battery charger in CPU turbo mode

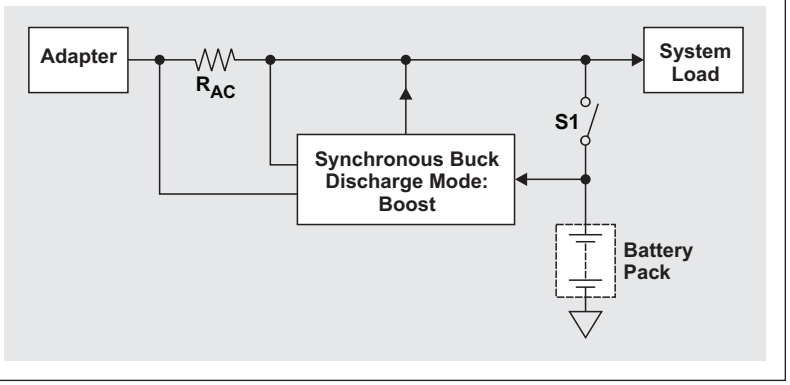
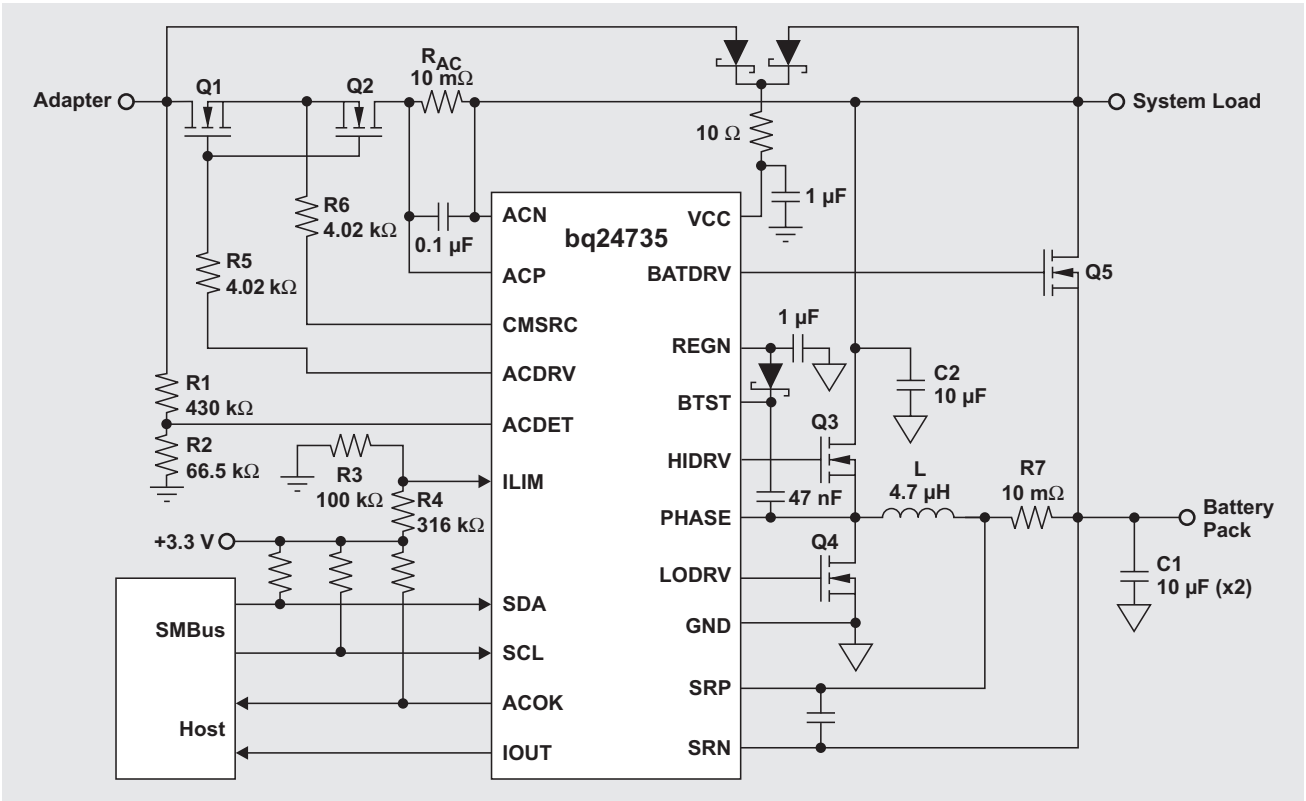


Figure 3 shows an application circuit for a turbo-boost battery charger supporting CPU turbo mode. The R_{AC} current-sense resistor is used to detect the AC adapter current for the DPM function and to determine whether the battery charger is operating in buck charge mode or boost discharge mode. Current-sense resistor R7 is used to sense the battery charge current programmed from the host through the SMBus based on the battery conditions. The total power drawn by both the charger and the system can be monitored through the I_{OUT} output, which is 20 times the voltage drop across sense resistor R_{AC} for achieving CPU throttling, if needed. Through SMBus control registers, the battery's boost discharge mode can be enabled or disabled based on the battery's state of charge and temperature conditions. In boost discharge mode, the circuit provides additional cycle-by-cycle current-limit protection by monitoring the voltage drop across the

Figure 3. Application circuit for turbo-boost battery charger



low-side MOSFET, Q4. To achieve a small form factor for a notebook computer like Intel's Ultrabook™, the switching frequency can be programmed at 615, 750, or 885 kHz. This minimizes the inductor size and the number of output capacitors. To further reduce the number of external components, the charger's controller chip fully integrates the loop compensators for the charge current, the charge voltage, and the input-current regulation loops. The power-source selector MOSFET controller is also integrated in the charger. Furthermore, the charger system uses all n-channel MOSFETs for cost reduction instead of the p-channel power MOSFETs used in traditional charge solutions. Another benefit of this turbo-boost charger system is that it can be used for either function without changing the bill of materials. System designers can do a quick system-performance evaluation without additional hardware-design effort.

Figure 4 shows the switching waveforms that occur during the transition from buck charge mode to boost discharge mode. When the input current reaches the adapter's maximum power limit due to a system-load increase, the battery charger stops charging and the battery transitions into boost mode to provide additional power to the system.

Figure 5 shows the efficiency of the turbo-boost charger. It can be seen that over 94% efficiency is achieved for charging and discharging a 3-cell or 4-cell battery pack. If the battery is removed or the battery's remaining capacity is not high enough, it is necessary to throttle the CPU to avoid the adapter crash.

Now the battery can be discharged even when the adapter is connected. However, one possible concern is the battery cycle life. Since the boost discharge mode lasts from only tens of milliseconds to tens of seconds, the impact on battery cycle life will be minimal. Battery degradation is proportional to the battery-cell voltage; so the higher this voltage is, the faster the battery will degrade and the shorter its cycle life will be. Discharging the battery in the boost discharge mode results in a lower battery-cell voltage, reducing the degradation of the battery and lengthening its cycle life.

Figure 4. Waveforms between buck charge mode and boost discharge mode

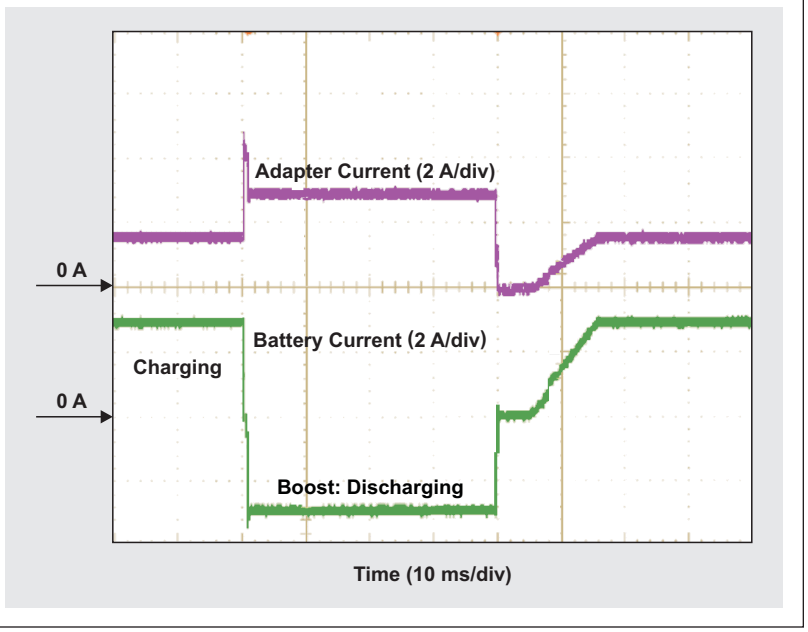
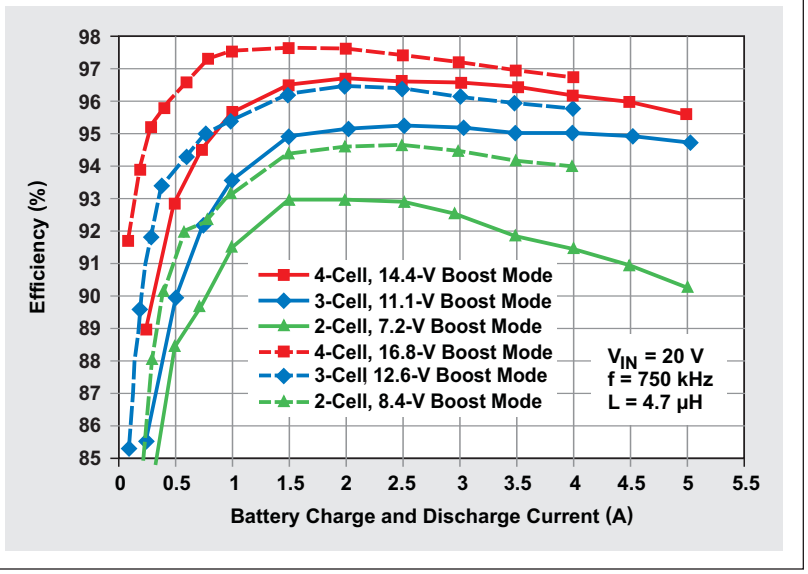


Figure 5. Efficiency of turbo-boost charger



Conclusion

A turbo-boost charger is a simple and cost-effective way for a battery to supplement AC adapter power for short periods when an AC adapter and battery simultaneously power the system. This topology supports CPU turbo mode while ensuring the lowest system cost without the need for upgrading to an AC adapter rated for peak system power. The test results show that the turbo-boost charger is a practical solution in real mobile-computer designs.

Related Web sites

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Benefits of a multiphase buck converter

By David Baba
Applications Engineering Manager

Introduction

Single-phase buck controllers work well for low-voltage converter applications with currents of up to approximately 25 A, but power dissipation and efficiency start to become an issue at higher currents. One suitable approach is to use a multiphase buck controller. This article briefly discusses the benefits of using a multiphase buck converter versus a single-phase converter and the value a multiphase buck converter can provide when implemented.

Figure 1 shows a two-phase circuit. From this circuit's waveforms, shown in Figure 2, it is clear that the phases are interleaved. Interleaving reduces ripple currents at the input and output. It also reduces hot spots on a printed circuit board or a particular component. In effect, a two-phase buck converter reduces the RMS-current power dissipation in the FETs and inductors by half. Interleaving also reduces transitional losses.

Output-filter consideration

The output-filter requirements decrease in a multiphase implementation due to the reduced current in the power stage for each phase. For a 40-A, two-phase solution, an average current of only 20 A is delivered to each inductor. Compared to a 40-A single-phase approach, the inductance and inductor size are drastically reduced because of lower average current and lower saturation current.

Output ripple voltage

Ripple-current cancellation in the output-filter stage results in a reduced ripple voltage across the output capacitor compared to a single-phase converter. This is another reason why a multiphase converter is preferred. Equations 1 and 2 calculate the percentage of ripple current canceled in each inductor.

$$m = D \times Phases \quad (1)$$

and

$$I_{Rip\_norm}(D) = Phases \times \frac{\left[D - \frac{mp(D)}{Phases}\right] \times \left[\frac{1 + mp(D)}{Phases} - D\right]}{(1 - D) \times D}, \quad (2)$$

Figure 1. Two-phase buck converter

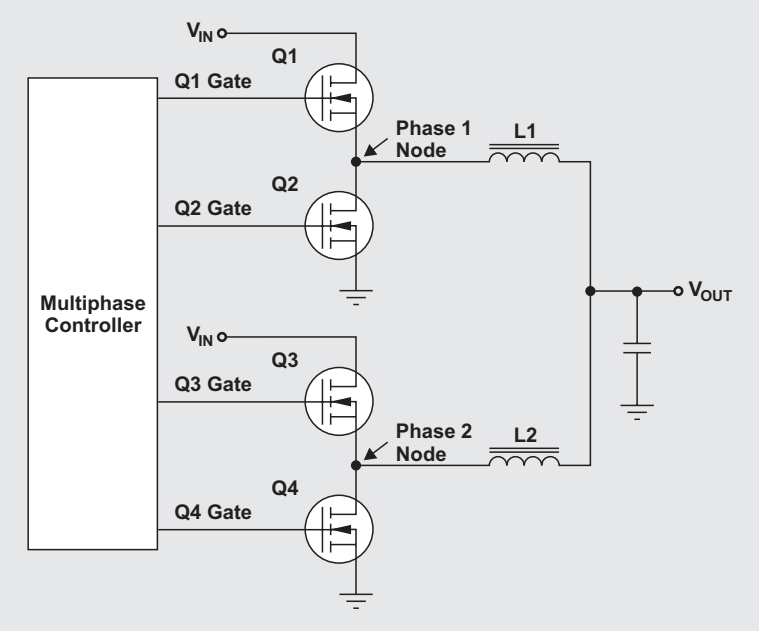
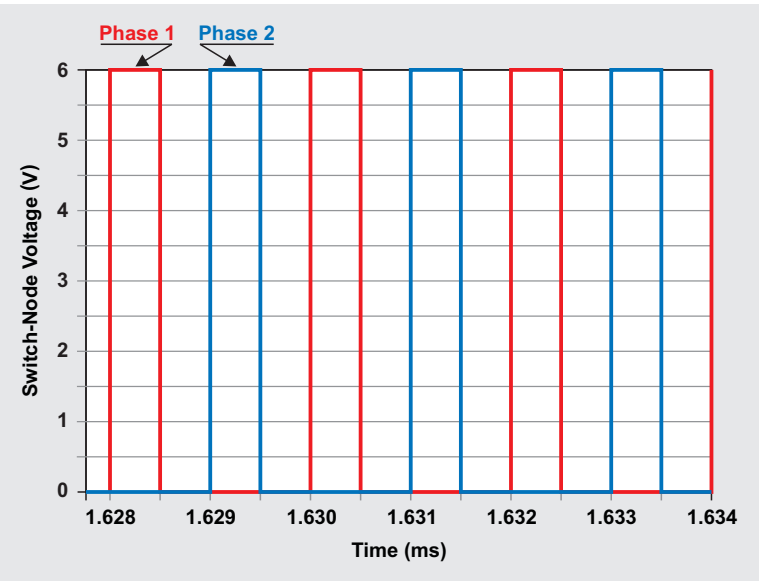


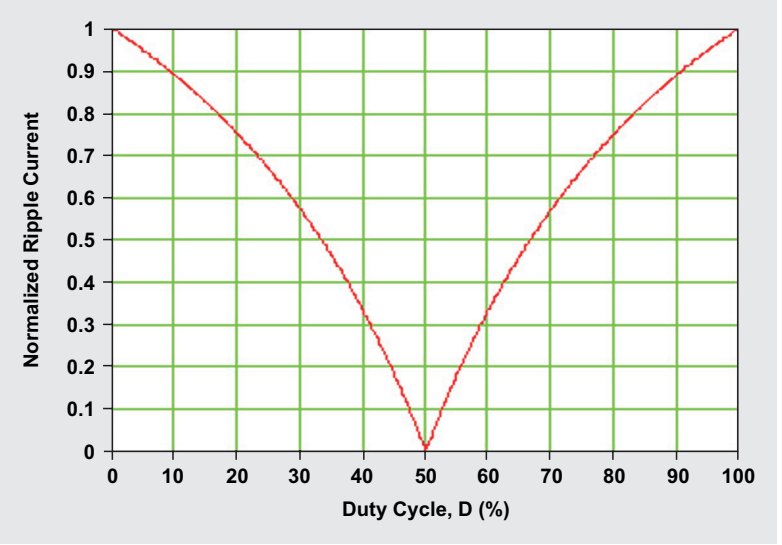
Figure 2. Node waveforms of phases 1 and 2



where D is the duty cycle, I_{Rip_norm} is the normalized ripple current as a function of D, and mp is the integer of m. Figure 3 plots these equations. For example, using two phases at a 20% duty cycle (D) yields a 25% reduction in ripple current. The amount of ripple voltage the capacitor must tolerate is calculated by multiplying the ripple current by the capacitor's equivalent series resistance. Clearly, both maximum current and voltage requirements are reduced.

Figure 4 shows the simulation results for a two-phase buck converter at a duty cycle of 25%. The inductor ripple current is 2.2 A, but the output capacitor sees only 1.5 A due to ripple-current cancellation. With a duty cycle of 50% and two phases, the capacitor sees no ripple current at all.

Figure 3. Normalized capacitor ripple current as a function of duty cycle



Load-transient performance

Load-transient performance is improved due to the reduction of energy stored in each output inductor. The reduction in ripple voltage as a result of current cancellation contributes to minimal output-voltage overshoot and undershoot because many cycles will pass before the loop responds. The lower the ripple current is, the less the perturbation will be.

Cancellation of input RMS ripple current

The input capacitors supply all the input current to the buck converter if the input wire to the converter is inductive. These capacitors should be carefully selected to satisfy the RMS-ripple-current requirements to ensure that they

Figure 4. Cancellation of inductor ripple current with D = 25%

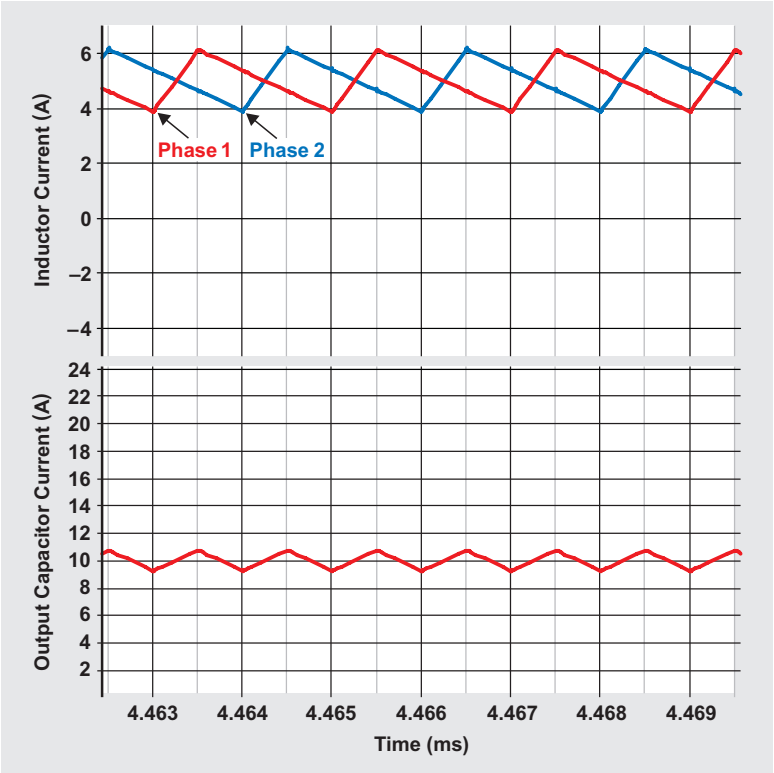
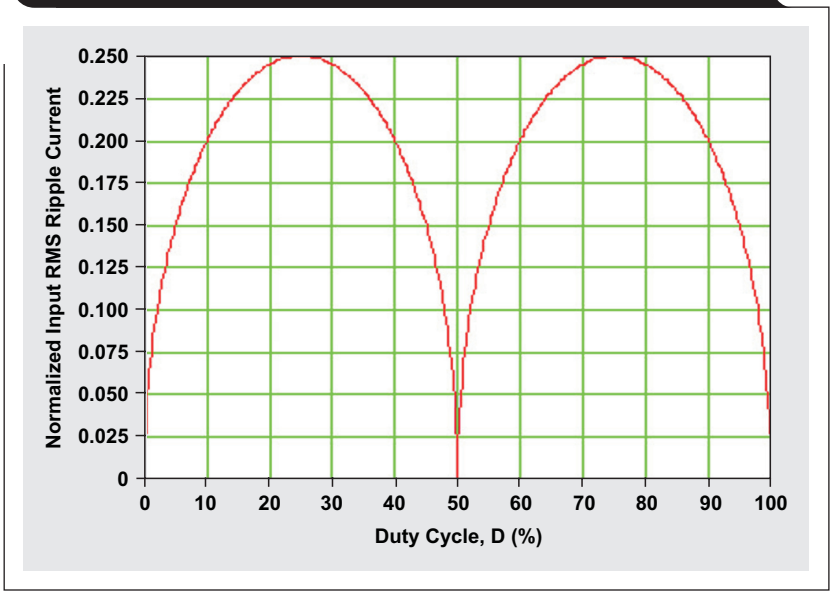


Figure 5. Normalized input RMS ripple current as a function of duty cycle



do not overheat. It is well understood that, for a single-phase converter with a duty cycle of 50%, the worst-case input RMS ripple current is typically rated at 50% of the output current. Figure 5 and Equation 3 indicate that, for a two-phase solution, the worst-case RMS ripple current occurs at duty cycles of 25 and 75% and is only 25% of the output current.

$$I_{Input\_norm}(D) = \sqrt{\left[D - \frac{mp(D)}{Phases}\right] \times \left[\frac{mp(D)+1}{Phases} - D\right]} \quad (3)$$

The value of a multiphase solution as compared to a single-phase solution is clear. Less input capacitance can be used to satisfy the RMS-ripple-current demands of the buck stage.

Application example

The LM3754 high-power-density evaluation board delivers 1.2 V at 40 A from a 12-V input supply. The board is 2 × 2 inches, and the area covered by the components is 1.4 × 1.3 inches. The switching frequency of each phase is set to 300 kHz. Table 1 provides a summary of these and other operating conditions. The components are placed on a 4-layer board, with 1 oz. of copper on all layers. Additional pins are included on this board for remote sensing, and a pin is used for margining the output voltage.

Because the LM3754 evaluation board is designed to operate in high-power-density configurations, it utilizes the optimized input capacitors to provide the reduced RMS ripple current that is required. The evaluation board also has a low ripple voltage and good transient performance. The board layout shown in the LM3754 application note[1] should be followed as closely as possible. However, if this is not possible, close attention should be paid to these considerations. Several more layout considerations will now be described, followed by the test results from a test board using the LM3754. These results are presented in Figures 6–11 on pages 12–13. They are typical of what one can expect to achieve or even improve upon in making the necessary modifications.

Table 1. Operating conditions of LM3754 evaluation board

Input voltage	10.8 to 13.2 V
Output voltage	1.2 V ± 1%
Output current	40 A (max)
Switching frequency	300 kHz
Module size	2 × 2 inches
Circuit area	1.4 × 1.3 inches
Module height	0.5 inches
Air flow	200 LFM
Number of phases	2

Layout considerations

High-current traces require enough copper to minimize voltage drops and temperature rises. The general rule of using a minimum of 7 mils per ampere was applied for the 2 oz. of copper used, and 14 mils per ampere for the inner layers for the 1 oz. of copper used. The input capacitors of each phase were placed as close as possible to the top MOSFET drain and the bottom MOSFET source to ensure minimal ground "bounce."

Signal components connected to the IC

All small-signal components that connected to the IC were placed as close to it as possible. Decoupling capacitors for V_{REF} and V_{CC} were also placed as close as possible to the IC. The signal ground (SGND) was configured to ensure a low-impedance path from the ground of the signal components to the ground of the IC.

SGND and PGND connections

Good layout techniques include a dedicated ground plane; this board dedicated as much of inner-layer 2 as possible for the ground plane. Vias and signal lines were strategically placed to avoid high-impedance points that could pinch off wide copper areas. The power ground (PGND) and SGND were kept separate, only connected to each other at the ground plane (inner layer 2).

Gate drive

The designer should ensure that a differential pair of traces is connected from the high-gate output to the top MOSFET gate and the return, which is the switch node. The distance between the controller and the MOSFET should be as short as possible. The same procedure should be followed for the LG and GND pins when the traces for the low-side MOSFET are routed.

A differential pair of traces must also be routed from the CSM and CS2 pins to the RC network located across the output inductor. Notice in the layout in Reference 1 that, in order to provide additional noise suppression, the filter capacitor is split into two capacitors—one positioned by the inductor and the other close to the IC. These sense lines should not be run for long lengths in close proximity to the switch node. If possible, they should be shielded by using a ground plane.

Minimizing the switch node

To follow the common rules of keeping the switch-node area as small as possible but large enough to carry high currents, the switch node was built on multiple layers. Because the small evaluation board essentially folds back on itself from input to output, the switch node naturally sits on the outer layer, and the IC sits directly underneath the switch node. Therefore, it is essential to keep the switch node well away from the sense lines and also from the IC. Hence, the switch node was strategically placed facing outwards toward the edge of the board.

Conclusion

There are a number of benefits to using multiphase buck converters, such as higher efficiency from lower transitional losses; lower output ripple voltage; better transient performance; and lower ripple-current-rating requirements for the input capacitor. Some examples of multiphase buck converters that can deliver the full benefits described herein are the LM3754, LM5119, and LM25119 families.

Reference

1. Robert Sheehan and Michael Null, “LM3753/54 evaluation board,” National Semiconductor Corp., Application Note 2021, Dec. 15, 2009 [Online]. Available: http://www.national.com/an/AN/AN-2021.pdf

Related Web sites

power.ti.com
www.ti.com/product/*partnumber*
Replace *partnumber* with LM3754, LM5119, or LM25119

Test results

Figure 6. Efficiency plot with 12-V input

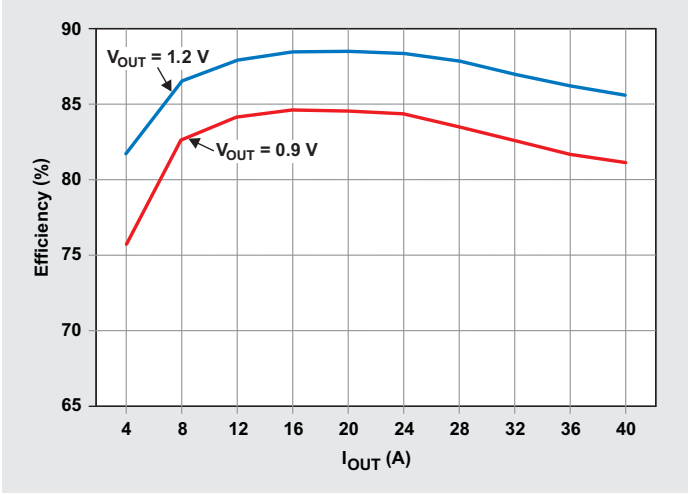


Figure 7. Power loss with 12-V input

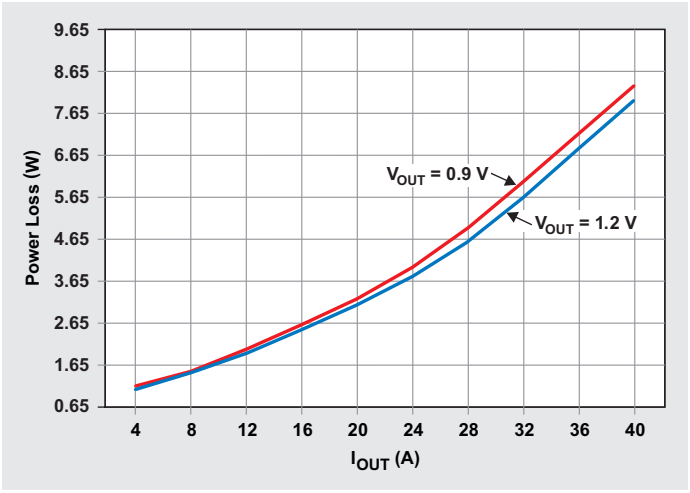
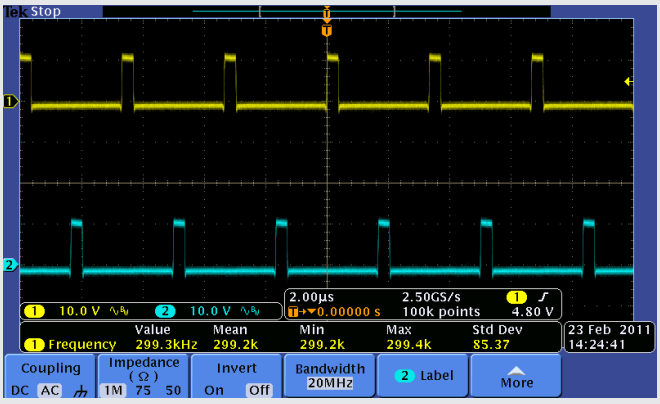
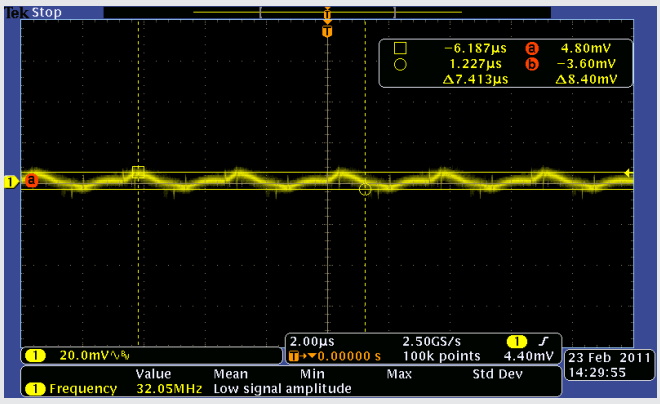


Figure 8. Switch-node voltages



V_{IN} = 12 V, V_{OUT} = 1.2 V at 40 A

Figure 9. Output voltage ripple



V_{IN} = 12 V, V_{OUT} = 1.2 V at 40 A

Figure 10. Transient response: 20 µs with 10-A load step (undershoot/overshoot ~ 27 mV)

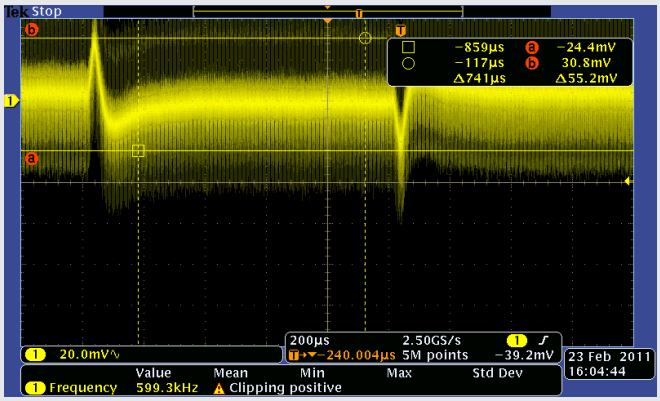
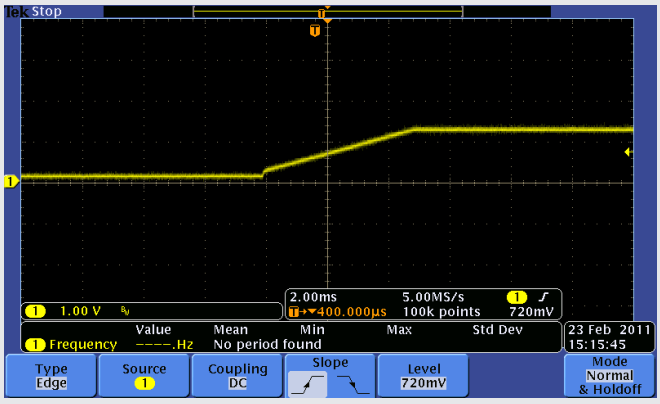


Figure 11. V_{OUT} start-up for 1.2-V output with 40-A load



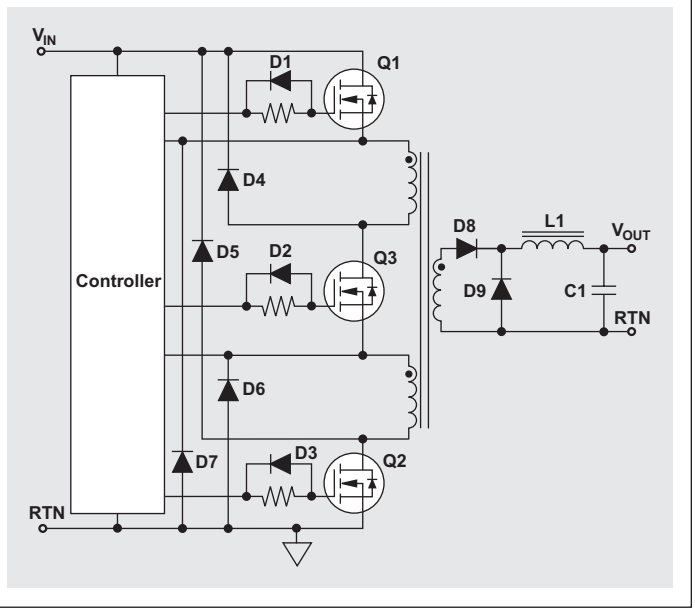
Downslope compensation for buck converters when the duty cycle exceeds 50%

By John Bottrill
Senior Applications Engineer

Current-mode control (CMC) in a pulse-width-modulated (PWM) buck converter with a duty cycle greater than 50% has the potential of going into subharmonic oscillations. Lloyd H Dixon, Jr., discusses this in detail in Reference 1. According to Dixon, the solution is to add to the current-sensing signal a ramp that is equal to the downslope of the output inductor current. This additional voltage needs to be added into the required calculation in order to select the current-sensing resistor.

A push-pull converter, a phase-shifted full-bridge converter, or any forward converter with duty cycles greater than 50% at the output inductor are topologies that require this compensation. However, for demonstration purposes, the topology selected for this discussion is one that is relatively unknown: a three-switch forward converter. See a basic schematic of the power section in Figure 1. This topology, though patented by Texas Instruments (TI), is licensed to the public when a TI control IC is used in the circuit.

Figure 1. Three-switch forward topology



This topology has several advantages, particularly when the input-voltage range is that which is normally considered the telephone-battery range of 36 to 72 V. The topology limits the maximum duty cycle to 67%, which limits the design to a maximum duty cycle at a minimum input voltage of 67%. At the same time, the voltage on the main switches when they turn off is limited to the input voltage of the power rail. This means that low-voltage FETs can be used with their corresponding lower $R_{DS(on)}$ resistance. This topology also provides a means of recovering the magnetizing energy in the power transformer and in the primary-side leakage inductance, thereby removing the need for wasteful snubbers.

The converter design, in most other respects, is typical of any buck topology, with the exception that the duty cycle must be limited to 67% to avoid transformer saturation. This limit can be accomplished by selecting a control IC where the maximum duty cycle can be programmed, such as the UCC2807-1 (see Reference 2). Because this controller has the required duty-cycle-limiting feature, it is perfect for this application. Therefore, it was used in this study along with its characteristics for the analysis.

The following analysis assumes a theoretical switching supply with a 3.3-V output at 100 W. The supply has a maximum peak-to-peak ripple current through the output inductor equal to 10% of the maximum output DC load current of 30 A, and the input voltage is expected to be between 36 and 78 V. It is also assumed that synchronous rectifiers with a forward voltage drop, V_{fd}, of 0.5 V will be used for the output. The first step is to determine the turns ratio of the transformer. At the minimum input voltage, the duty cycle will be at the maximum limit (67%). The voltage needed at the output of the transformer can be determined by the equation

$$\frac{V_{OUT} + V_{fd}}{D_{max}} = \frac{3.3\ V + 0.5\ V}{0.67} = 5.672\ V. \quad \textbf{(1)}$$

If 36 V across the transformer primary windings is assumed, the turns ratio (N_p) will be 6.147, so a primary with six turns will be used. The primary is divided into two sections of three turns each (see Figure 1). As is standard practice, the secondary is sandwiched between the primary sections, and Q3 is placed between the two primary sections. With the input at 78 V, the transformer output voltage is 12.3 V, which will yield a minimum duty cycle, D_{min}, of about 31%. Therefore, the maximum OFF time equals

$$\frac{1 - D_{min}}{f_{sw}},$$

where f_{sw} is the planned switching frequency of 200 kHz. The minimum output inductance (L1 in Figure 1) to achieve the desired peak-to-peak ripple current of 10% is thus defined as

$$L_{OUT} = \frac{(V_{OUT} + V_{fd}) \times (1 - D_{min}) / f_{sw}}{I_{OUT} \times 0.1}. \quad \textbf{(2)}$$

The output inductor in Equation 2 was determined to be 4.33 µH. For design purposes, 4.5 µH will be used. From this value, the current downslope, I_{ds}, of the output inductor can be calculated:

$$I_{ds} = \frac{V_{OUT} + V_{fd}}{L_{OUT}} \quad (3)$$

The inductor's downslope current (I_{ds}) is determined to be 0.844 A/µs.

It can also be determined that the peak current through the output inductor at maximum input voltage is

$$I_{OUT} + 0.5 \times (I_{OUT} \times 0.1),$$

because the maximum peak-to-peak ripple current was defined as being 10% of the output current, and that current is balanced about the nominal DC output. The peak current that results is 31.884 A.

For the minimum input voltage, it is possible to determine the differential voltage across L_{OUT}. From that, the rate of change in the output inductor can be determined to be 0.489 A/µs. Knowing the duty cycle and frequency permits calculation of the time that the current is increasing in the output inductor, making it possible to determine the ripple current under these conditions. Finally, the peak current under the minimum input voltage is found to be 31.122 A. The waveforms are shown in Figure 2. These values are almost equal, but if the downslope is added, they change—and in a surprising way. The downslope current that must be added to the peak current for the maximum input voltage is

$$\frac{I_{ds} \times D_{min}}{f_{sw}} = 1.306 \text{ A},$$

and the downslope current that needs to be added to the peak current for the minimum input voltage is

$$\frac{I_{ds} \times D_{max}}{f_{sw}} = 2.829 \text{ A}.$$

See Figure 3, where the effective downslope current is added to the currents shown in Figure 2. The result is that

Figure 2. Output inductor ripple at maximum load for $V_{IN(min)}$ and $V_{IN(max)}$

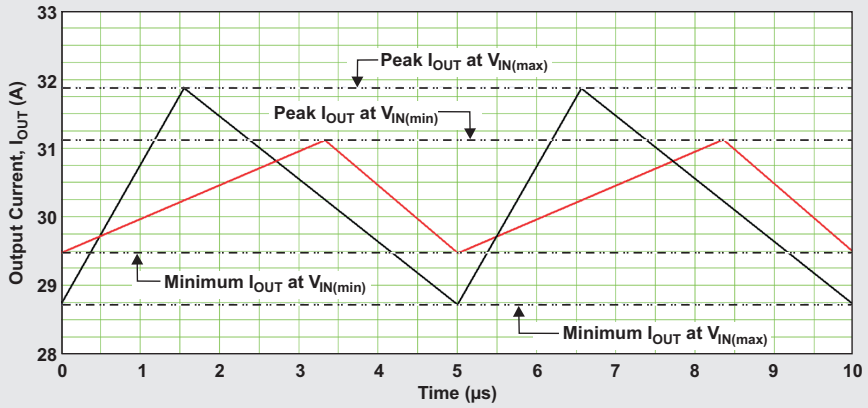


Figure 3. Secondary currents plus effective downslope current

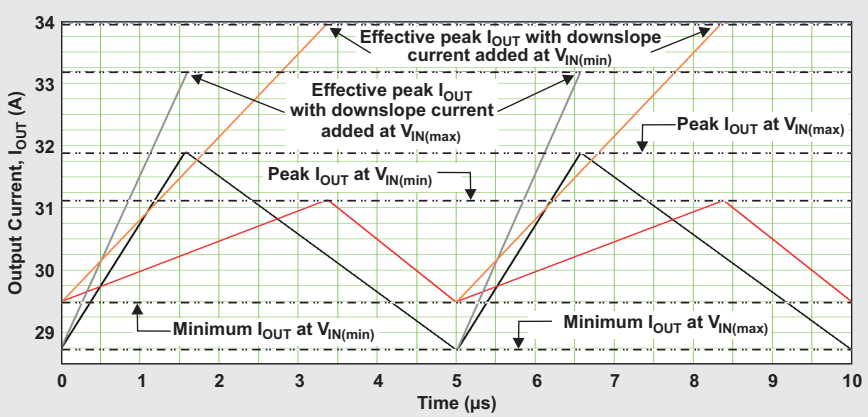
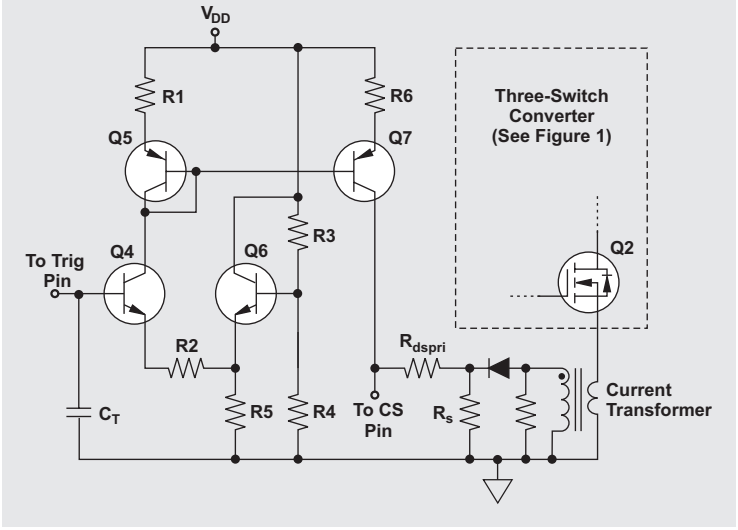


Figure 4. Circuit used to generate the desired current through R_{dspri}



the effective peak current for the minimum input voltage is higher than the effective peak current for the maximum input voltage, even though the real peaks were the reverse. The effective maximum current, including downslope at the minimum input voltage, has a peak of 33.9 A, which is the value that must be used to set the current-sensing resistor, Rs. This current, including the downslope current translated to the primary, is 5.658 A.

The IC chosen as the controller has a typical current-trip level of 1.0 V, but the tolerance is between 0.9 and 1.1 V. To make certain that all units can provide the required power, the lower limit is used, and the value of R_s is set so that the voltage across it at 5.658 A will be 95% of the 0.9-V minimum. This gives a 5% safety margin for transients and sets R_s at 0.15 Ω. Of course, there will be about 5 W of power loss, which most likely would be replaced by a current transformer. With a 100:1 transformer, R_s would increase to 15 Ω. The remaining discussion assumes that such a transformer is used.

In reality, the downslope current (I_{ds}) does not go through either the current transformer or the power transformer, but the effect needs to be accounted for and added to the voltage on resistor R_s. To do this, a resistor R_{dspri} is added between resistor R_s and the IC's current-sensing pin. At the IC's current-sensing pin, a current ramp is injected into the circuit. This current ramp is such that the ramp voltage developed across resistor R_{dspri} between the IC's current-sensing pin and resistor R_s is equivalent to the voltage that would be developed across resistor R_s by the I_{ds} translated to the primary. It is assumed that an equivalent downslope current is flowing through resistor R_s, taking into account both the power-transformer and the current-transformer winding ratios. For this case, resistor R_{dspri} is set at 1 kΩ for ease of calculation and because it is much larger than resistor R_s.

The next step is to determine the dv/dt required across R_{dspri}:

$$V_{dspri} = \frac{I_{ds} \times R_s}{N_p \times 100} = 21 \text{ V/ms} \quad \textbf{(4)}$$

From this result, the current ramp needed through the 1-kΩ resistor can be determined:

$$I_{dspri} = \frac{V_{dspri}}{R_{dspri}} = 21.1 \text{ µA/µs} \quad \textbf{(5)}$$

This current times the maximum ON time gives a peak current of 70.7 µA.

With a programmable, maximum-duty-cycle PWM controller like the UCC2807, it is relatively simple to set the maximum duty cycle to 67% by setting the two timing resistors to the same value, as shown in the datasheet. Also, the specification for the part states that the valley and peak voltages on the timing capacitor equal ⅓ V_{CC} and ⅔ V_{CC}, respectively. This gives a voltage-ramp amplitude of ⅓ V_{CC}. With this information, a circuit can now be designed to generate a ramp current that can be injected into the current-sensing circuit to provide the current downslope to the current signal.

A circuit to generate the desired current is shown in Figure 4. This circuit is based on the UCC2807-1 control IC, with V_{DD} set at 11 V. The valley and peak voltages of the Trig ramp are 3.667 V minimum and 7.33 V maximum, and the time from minimum to maximum is equal to the maximum ON time. In this circuit, R3 is equal to twice R4. This sets the voltage at the base of Q6 equal to ⅓ V_{CC},

which is the valley of the Trig voltage. As the voltage on the Trig pin swings from the valley to the peak (⅔ V_{CC}), the voltage across R2 goes from 0 to ⅓ V_{CC} in a linear manner. By choosing a value for R2 that gives a current of 70.7 µA with 3.667 V (51.8 kΩ) across it and then having the unity current mirror formed by Q5/R1 and Q7/R6, the designer can develop and add to the current-sensing signal the needed current with the correct shape and timing for the 1-kΩ resistor.

Conclusion

The three-switch forward converter offers unique advantages in energy recovery by returning the magnetizing energy and primary-side leakage energy to the source, preventing the need for snubbers and reducing the electromagnetic interference common with normal forward converters. It also offers the advantage over a two-switch forward topology of a duty cycle greater than 50%. This article has shown an example of the calculations necessary to determine the value of the current-sensing resistor and the impact of the downslope necessary for stability in a buck converter operating at a duty cycle greater than 50%. It has also shown a method of adding in the downslope in a converter.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Lloyd H. Dixon, Jr., "Current-mode control of switching power supplies," 1985 Texas Instruments Power Supply Design Seminar (SEM400)	SLUP075
2. "Programmable maximum duty cycle PWM controller," UCC1807-x/2807-x/3807-x Datasheet	SLUS163

Related Web sites

power.ti.com
www.ti.com/product/UCC2807-1

High-efficiency AC adapters for USB charging

By Adnaan Lokhandwala
Product Manager

USB charging for electronic gadgets

Universal serial bus (USB) charging has become a common means for powering electronic gadgets. The AC power adapter/battery charger for many new consumer devices like smartphones, tablets, and e-readers is in the 5- to 25-W power range and presents a USB Standard-A receptacle. The adapter output voltage of 5 V has become the preferred choice for compatibility with PC/desktop-port charging and communication. The current dominant interface is via a standard (mini or Micro-B) USB cable or, in some cases, a nonstandard connector. With battery charging gaining consumer attention, the odd "wall wart" is transforming into a "cool," light, sleek, green charger. Beyond meeting standard regulatory requirements, original equipment manufacturers are pushing the performance envelope on adapter efficiency and no-load power, which is also known as vampire power. For example, leading manufacturers of mobile-phone chargers have agreed to a five-star (<30 mW of no-load power) charger-rating system. This makes it easy for consumers to compare and choose the most energy-efficient chargers.

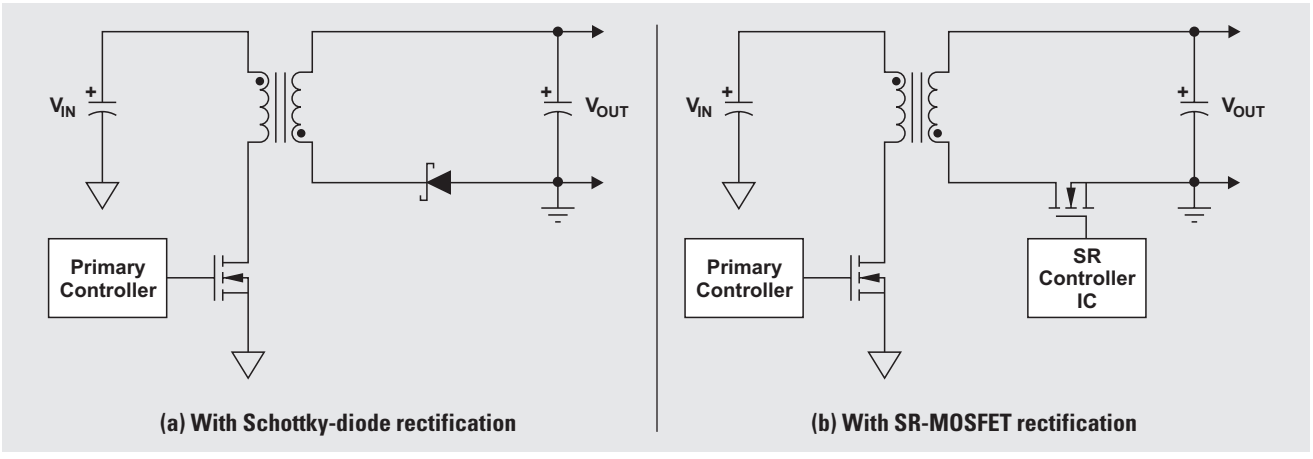
Recently, there has been much talk about standardizing the input to mobile phones and creating a universal charger to charge any cell phone. In 2006, China issued a new regulation aimed at standardizing the wall charger and its connecting cable. Similarly, the GSM Association (GSMA) is now leading the Universal Charging Solution adapter initiative for powering mobile phones with a micro USB connector. The common charger is required to provide 5 V ± 5%, a minimum of 850 mA, and <150 mW of no-load power. It must also comply with the USB Implementers Forum (USB-IF) Battery Charging Specification 1.1 (BC1.1).* Besides providing ease of use for consumers, the standardized charger could potentially eliminate a multitude of duplicate chargers. Additionally, AC adapters with multiple USB outlets offer consumers the convenience of charging multiple devices without the need for a dedicated charger for each gadget. Chargers with higher output current also allow the possibility of fast battery charging, a key advantage over standard USB 2.0 ports that are limited to 500 mA. The increasing demand for these improvements, along with the continued push towards adapter designs with a smaller form factor, makes thermal management in this "black box" a huge challenge for power-supply designers.

Power-supply architecture

For the power levels under consideration here, the flyback topology shown in Figure 1 is the preferred choice today due to its simplicity and low cost. The conduction loss on the secondary-side Schottky-diode rectifier (Figure 1a) becomes a limiting factor in achieving high-efficiency, compact adapter designs. For instance, in a typical 5-V/3-A adapter, the power loss in the diode rectifier alone at full load can be 30 to 40% of the total system losses (neglecting the compounding effect of secondary losses on increased primary-side losses). Implementing a synchronous rectifier (SR) for the output (Figure 1b) can increase the overall efficiency of the converter and, because much less heat is generated (fundamentally important in adapter designs), ease system thermal management.

*USB-IF BC1.2 extends the charging-current range from 1.5 A to 5 A.

Figure 1. Simplified flyback topology



The conceptually simple change of adding an SR to the classic flyback topology can significantly reduce overall system power losses. The power level at which such a modification is practical has been decreasing with the rapid advancement in power MOSFET technology. Hence, synchronous rectification is now applicable to an ever-growing range of products. The lower power dissipation of an SR allows designers to take advantage of smaller components that have less heat sinking, thus increasing power density while lowering assembly costs, product size, and shipping weight.

Note that if the SR MOSFET is allowed to switch during no-load/standby conditions, the system power performance could be compromised. The SR-MOSFET switching losses, in addition to the quiescent power required by the SR controller IC, can be limiting factors in achieving the best possible system no-load performance.

Green output rectification: Full load to no load

This article will now discuss how an IC such as the Texas Instruments (TI) UCC24610 Green Rectifier™ controller can simplify USB charger designs and enable high system efficiency across the full load range. Simplified system waveforms for a flyback converter with and without synchronous rectification are shown in Figure 2. The waveforms are the results of a control scheme that directly senses the MOSFET drain-to-source voltage (V_{DS}). This control method is widely adopted today instead of other implementation choices such as primary-side synchronization or synchronous control from a secondary-side current transformer. Having the SR controller's turn-off threshold (V_{THOFF}) as close as possible to zero in this control scheme allows maximum conduction time in the MOSFET channel.

Flyback converters can be designed to operate in different modes depending on the end-application requirements. For designs operating in continuous-conduction mode (CCM), the current in the transformer secondary does not fall to zero before the primary-side MOSFET is turned on, which results in a period of cross-conduction. When synchronous rectification is implemented in such converters, it is imperative that the SR MOSFET be turned off as soon as the primary-side switch turns on. This prevents reverse conduction and limits additional power losses and device stresses. Instead of waiting for the V_{THOFF} threshold detection, the synchronizing function in the Green Rectifier detects the primary-side turn-on transition and turns off the SR MOSFET. Figure 3 illustrates how the SR-gate turn-off transition is now controlled by a synchronizing signal from the primary side and not by V_{DS} sensing.

Figure 2. Simplified flyback waveforms with Schottky-diode and SR-MOSFET output rectification

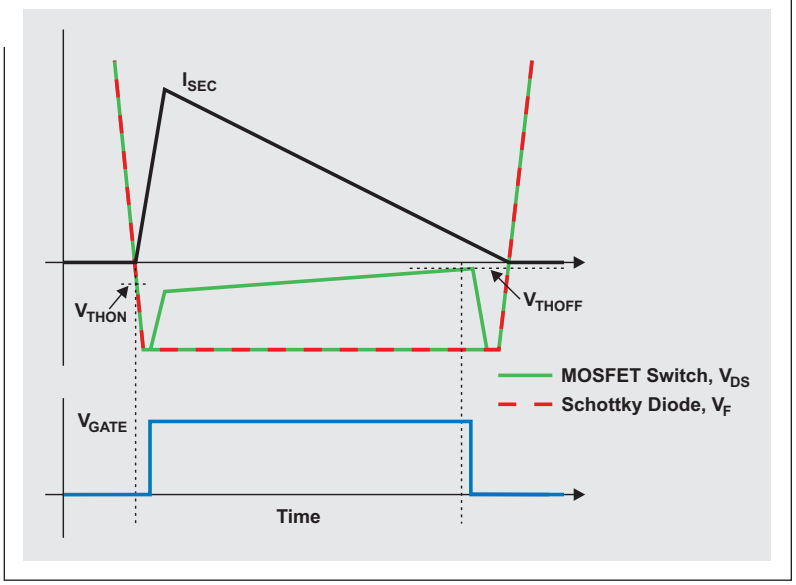
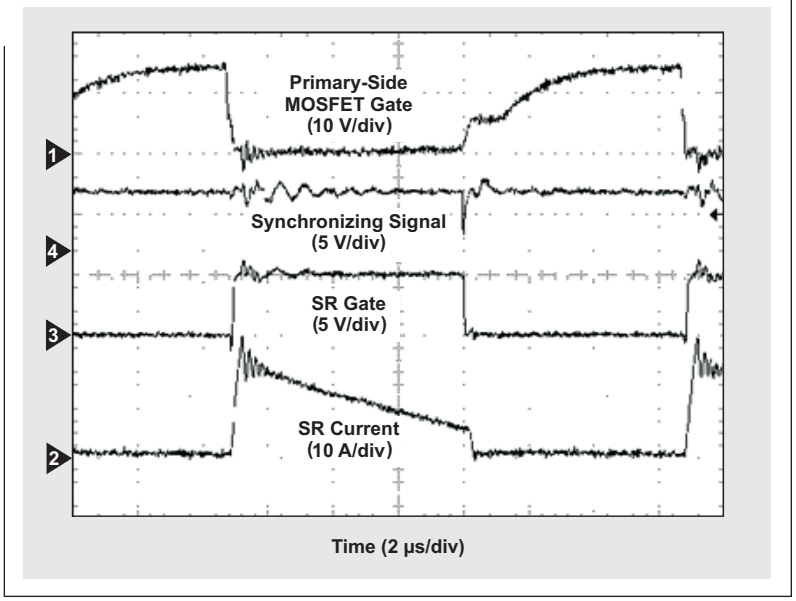


Figure 3. Typical CCM flyback waveforms with primary-side synchronization



As described earlier, implementing synchronous rectification could possibly compromise light-load efficiency and no-load power consumption. The major contributors to loss at light or no load are SR-MOSFET switching and SR controller-IC bias. The Green Rectifier overcomes these issues with (1) an automatic light-load-detection circuit that disables gate switching of the SR MOSFET when its conduction time falls below a certain threshold, and (2) an EN function to put the IC in sleep mode and disable

quiescent power loss. The light-load-detection circuit compares the SR conduction time and the programmed minimum ON time (MOT) for every switching cycle. When the load decreases, the secondary conduction time becomes shorter than the MOT, and the next SR gate pulse is disabled. Further reduction in no-load power can be achieved by using the EN function of the controller IC. A simple averaging circuit on the MOSFET drain voltage can be used to put the IC in sleep mode at a no-load condition that limits the IC's bias-current consumption to 100 µA. An additional 10 mW of no-load power consumption can be saved with this approach. The last gasp in improving no-load performance is to add a low-current Schottky diode in parallel with the SR MOSFET.

As an example, a USB charger with a 3-A current rating was designed using two controller chipsets, TI's UCC28610 and UCC24610, for a tablet-PC end application. The reference design for this charger, the PMP4305, can be seen at the Web site listed at the end of this article. The UCC24610 is good for applications with a 5-V flyback switch-mode power supply and can operate within the specified USB voltage range of 4.75 to 5.25 V. Hence, this SR controller was biased directly from the converter output, eliminating the need for an auxiliary winding on the main power transformer. The controller also allowed external programming of two blanking timers to prevent SR false triggering from V_{DS} ringing sensed during the turn-on and turn-off transitions. Figure 4 shows typical power-stage waveforms of the PMP4305 at full load. The IC control scheme was not affected by the severe ringing on the V_{DS} signal at turn-on because the programmable MOT timer disabled the V_{THOFF} comparator during this period.

A comparison of the efficiency of SR-MOSFET versus Schottky-diode output rectification at 115- and 230-V AC line conditions is shown in Figure 5. Implementing synchronous rectification enables over 80% efficiency from full load down to about 25% of full load. Additionally, for this load range, an SR configuration can achieve a three- to five-point improvement in efficiency over Schottky-diode rectification.

Figure 4. Full-load waveforms from PMP4305

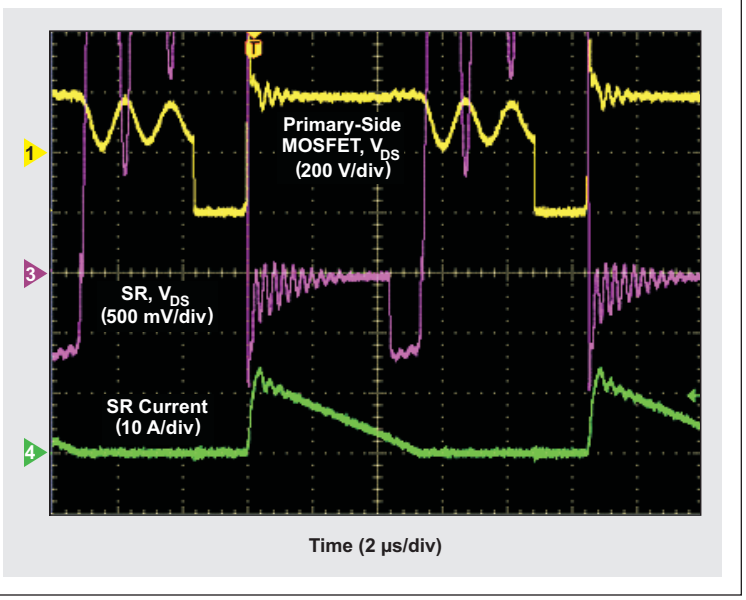
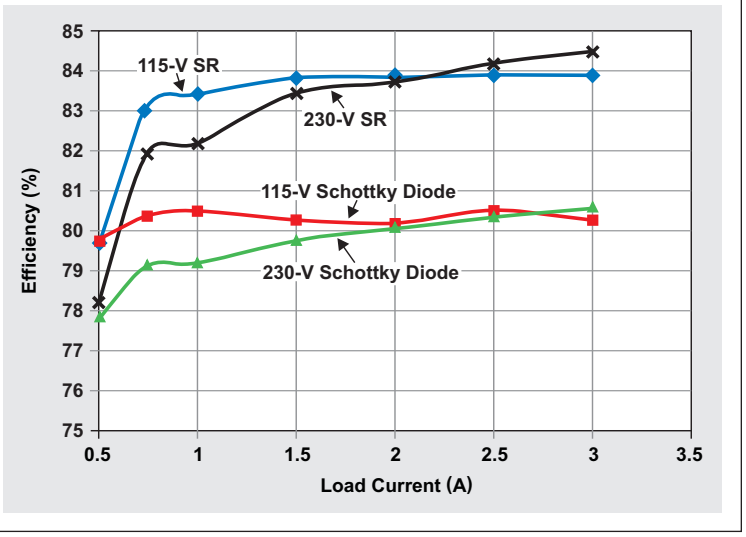


Figure 5. Comparison of system efficiency with Schottky diode versus synchronous rectifier (SR)



Conclusion

USB power charging for consumer devices is gaining traction. A universal standard for 10- to 25-W chargers with USB outlets that power multiple devices eliminates the need for a new wall charger with every new gadget purchase. High-efficiency AC/DC converters are needed to satisfy the push towards high-density, small-form-factor adapters. Devices like the UCC24610 Green Rectifier can help improve AC/DC converter efficiency and enable the high-density USB-charger designs.

Related Web sites

power.ti.com
www.ti.com/product/UCC24610
www.ti.com/product/UCC28610

Reference design for tablet-PC charger:
www.ti.com/tool/PMP4305

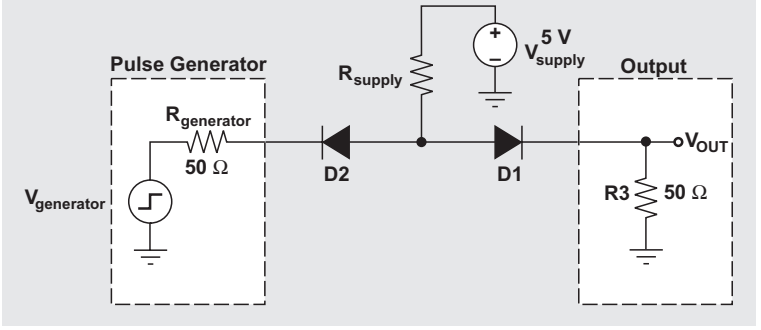
Measuring op amp settling time by using sample-and-hold technique

By Roger Liang, *Systems Engineer,*
and Xavier Ramus, *System Engineer, High-Speed Amplifiers*

Introduction

Modern high-speed operational amplifiers (op amps) are designed with settling time in the range of nanoseconds. This time is so brief that measuring it within a reasonable error band presents a challenging task not only on automatic test equipment (ATE) but also on the bench. In today's op amp datasheets, settling time is usually given as a simulated value due to the cost and challenges associated with implementing additional hardware to test it on the bench. Traditional high-speed oscilloscopes have only a 10-bit analog-to-digital converter, which limits any measurement resolution to a maximum of 0.1%.

Figure 1. Flat-bottom pulse generator (FBPG)



This article describes a new methodology that has proven to be effective in making these measurements. Detailed is a relatively inexpensive and simple way to measure settling time that bases accuracy and precision on the relative speed of the waveform generator and the sample-and-hold circuit.

Step input for the device under test

In this article, settling time refers to the time that elapses from the application of an ideal step input to the time at which the device under test (DUT) enters and remains within a specified error band that is symmetrical about the final value. An ideal step input is easily generated in simulation, but there are no instruments that can produce an ideal step waveform in any lab setting. Even under ideal conditions, the output of overdamped and critically damped instruments would take a few RC time constants to monotonically settle to within tenths of a percent of the final value.

For underdamped systems, a step waveform can overshoot the final value, and ringing may occur. In practice, even critically damped systems have underdamped behaviors. Generally, the faster the fall time of the step waveform, the more overshoot and ringing one observes. This non-ideality is then propagated into the measured output waveform of the DUT. Fortunately, with the aid of computer-logged records of input and output data, the output can be normalized by lining up the two and subtracting the input from the output (with the DUT in a non-inverting unity-gain configuration).

Flat-bottom pulse generator

When the falling edge of a waveform generator is used as the input to the DUT, a flat-bottom pulse generator (FBPG) can be used to clean up the low-voltage level of the generated signal. The FBPG clamps the falling voltage to ground at the cost of a bigger overshoot. This gives test engineers some control over trade-offs in the test setup. Similarly, a flat-top pulse generator can be used to clean up the high-voltage level.

Figure 1 illustrates two back-to-back high-speed Zener diodes, each with a separate, adjustable power supply. As a rule of thumb, the setup should be started as follows: The R_{supply} should be adjusted to obtain 5 V at the D1/D2 connection, and the $V_{generator}$ output voltage should be adjusted to swing between a 2-V high and a –5-V low. This should bias the output at 2 V_{PP} and the low-voltage level at 0 V. When $V_{generator}$ is high, D2 is turned off and D1 is turned on. During this time, the output voltage becomes a function of D1's forward voltage (V_{supply}) and of the amount of current that flows through R_{supply} and D1. When the input is low, D1 is turned off and D2 is turned on. During this time, the output voltage swings to ground, and its slew rate is proportional to the amount of current that flows into the matching resistor, R3. The transient response is a function of the diode's capacitance, reverse recovery time, and forward recovery voltage.

Because of the diodes' nonlinearity, it does not make sense to derive rigorous equations to determine the DC levels and transient response of the FBPG. Instead, the equations can be simulated in software such as TINA-TI™ from Texas Instruments. Assuming that the pulse generator is very fast, the fall time and overshoot of the output waveform become functions of the diodes' speed and recovery time, as well as of the parasitic capacitance and inductance of the printed circuit board (PCB) on which the FBPG is built. In other words, the designer should pick the fastest, most robust diode and follow guidelines for

good PCB layout when using FBPG for generating high-speed waveforms.

Sample-and-hold methodology for measuring settling time

For the example presented here, the TI OPA615 (see Figure 2) was chosen to implement the sample-and-hold (S/H) functions of settling-time measurement because of its wideband operational transconductance amplifier (OTA), which is optimized for low input-bias current, and its fast and precise sampling OTA (SOTA), which also serves as a comparator and buffer. The analog input (V_{IN}) is sampled by the SOTA onto the capacitor (C_{HOLD}) when the Hold-Control pin is high. The voltage on C_{HOLD} is held and reflected at the output (V_{OUT}) when the Hold-Control pin swings low. During sampling, the voltage on C_{HOLD} is adjusted to the real-time voltage level on the input. If there is a large voltage difference between the input and C_{HOLD} and there are only a few nanoseconds of sampling time, then fast slewing is required. During holding, the voltage on C_{HOLD} invariably charges/discharges due to its leakage current and any biasing current needed for the OTA. The current-feedback loop ensures that the SOTA slews fast enough to capture the correct voltage level at V_{IN}.

Figure 3 shows an example of a S/H output of a 100-kHz sine-wave input. A waveform generator can be used to produce the input step function for the DUT and to synchronize a S/H signal to that step function. A S/H circuit can be used to capture points on the DUT's output waveform. Any arbitrary waveform generator should work if it has a marker output that synchronizes with the output, thus creating a very convenient Hold-Control signal. The example test used a Tektronix AWG610, which has a sampling time of 2.6 Gbps and a minimum marker step of 100 ps, making it fast enough for most measurements of high-speed op amp settling time.

Figure 4 shows how to capture points on a curve by using a S/H circuit with the marker as the Hold-Control signal. The designer can capture sequential points on the curve by moving the marker position. After all the points

Figure 2. Sample-and-hold (S/H) circuit

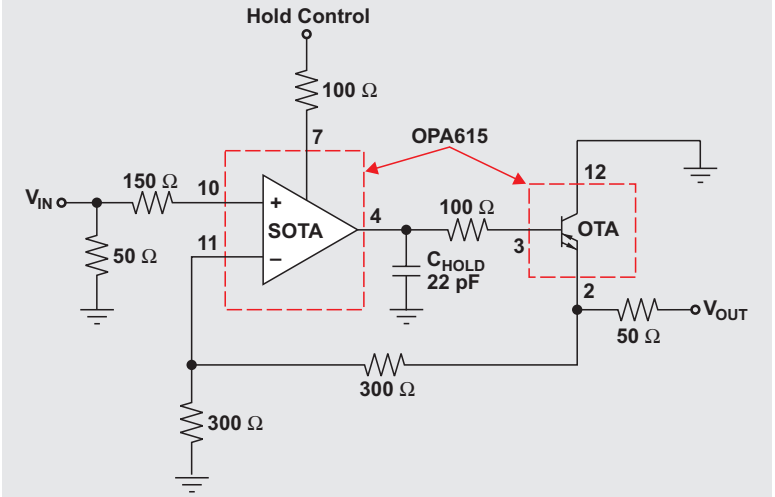


Figure 3. Example 1-MHz S/H output of a 100-kHz sine wave

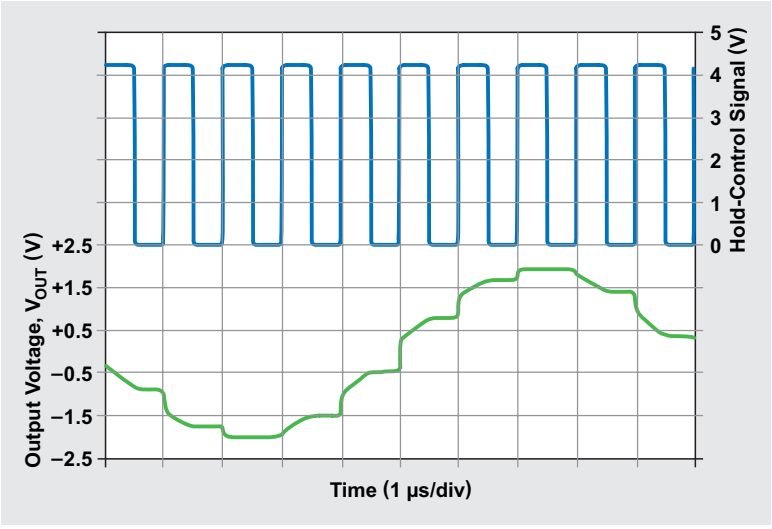
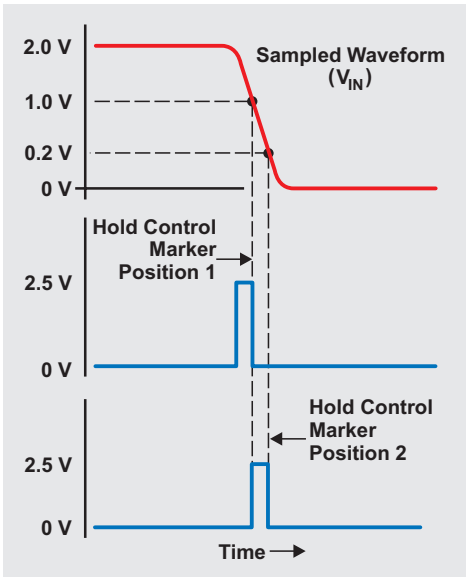


Figure 4. Example of AWG610 output and marker synchronization



have been recorded, the S/H curve can be plotted and analyzed. Programming the waveform generator with software like MATLAB® or LabVIEW™ makes changing the marker and recording the results very simple. With the marker set in position 1, the S/H circuit tracks the V_{IN} voltage level when the marker is high and holds that value when the marker is low. At position 1, the output is held at 1 V. At position 2, the output is held at 0.2 V.

Figure 5 shows the test setup for measuring settling time where the AWG610 and OPA615 were used for the S/H functions. All signal lines were matched at 50 Ω. The output of the waveform generator was used as the test signal with two S/H circuits: One measured the input of the DUT (OPA656), and the other measured the DUT output. Digital multimeters (DMMs) were used to record the held values.

As an example of this method, take measuring a settling time of up to 100 ns. Assume that the waveform generator is programmed to continually output a square wave with a duty cycle of 50% and a period of 200 ns. The marker is initially set at the beginning of the falling edge of the waveform generator's output. The generator runs continually (executes many cycles of sampling and holding), and the S/H circuit integrates its output voltage to a steady DC value. This value is then recorded by the DMM, and the test engineer moves the marker to the next position, repeating this cycle until data for 100 ns has been recorded.

Figure 6 shows the plotted waveforms that resulted when the test setup in Figure 5 was used. To obtain a settling-time error waveform, the DC error was offset, and the output was normalized to the input. The result is shown in Figure 7.

Limitations and challenges

There are some limitations to the setup described here that should be kept in mind. When in doubt, the designer should always use the following equation:

$$I = C_{HOLD} \times dv/dt$$

For this equation, the size of the initial C_{HOLD} should be chosen based on three factors:

1. During the holding time, the OTA biasing current will flow in or out of the capacitor, thus affecting the accuracy of the voltage held.
2. Since a voltage droop will occur on the capacitor due to the biasing current, a delta voltage should be chosen based on the percentage of error within which the measurement should stay.
3. Delta time is the duration for which the sampled voltage is held and should be no longer than the planned settling time to be measured.

For example, C_{HOLD} should be no less than 50 pF under the following conditions: The biasing current of the OTA is 0.5 µA; an error of less than 0.1% of a 1-V_{PP} signal is to be achieved; and the duration to be measured is 100 ns.

Figure 5. Test setup for measuring settling time

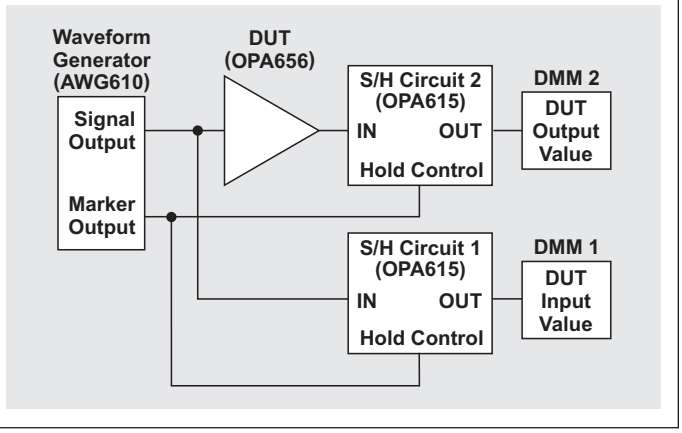


Figure 6. Step waveforms of op amp's input and output

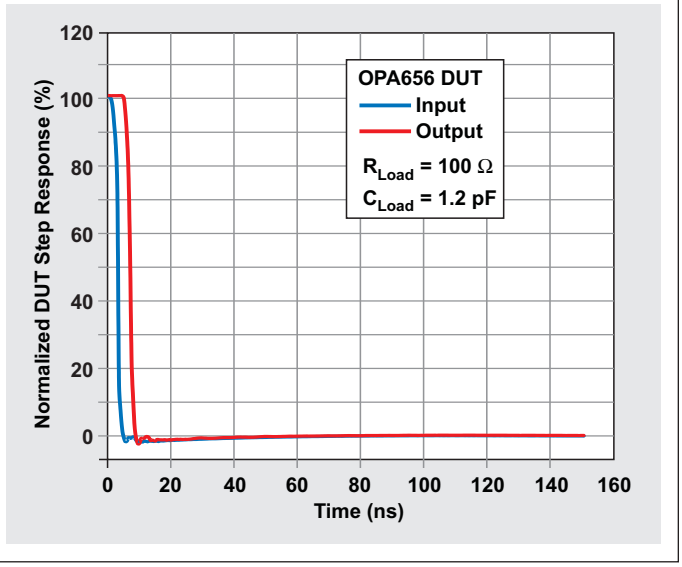


Figure 7. Op amp's normalized settling error

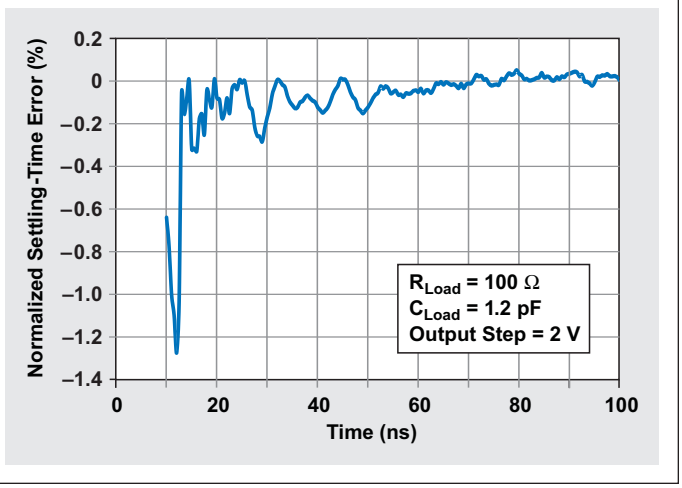
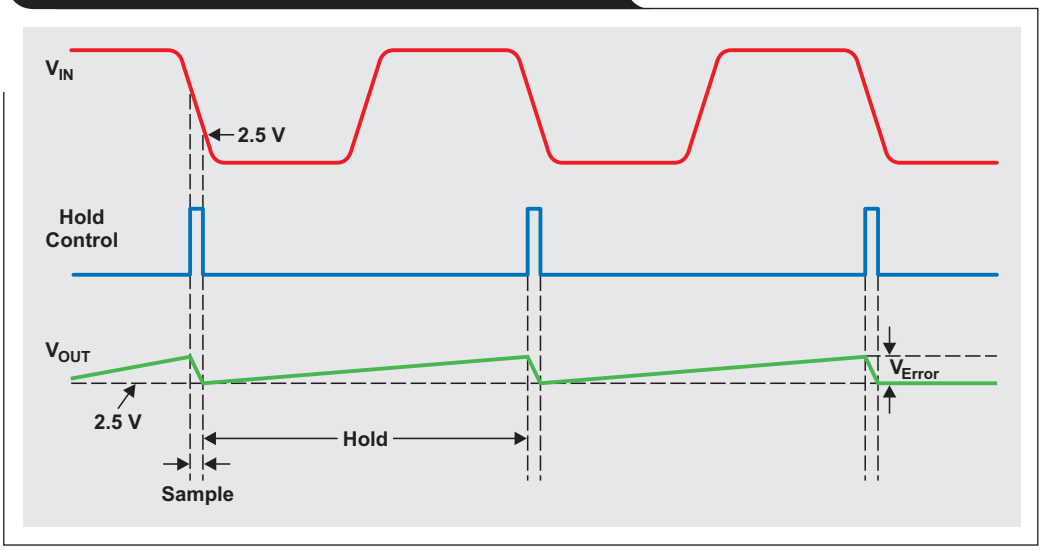


Figure 8. Charge leakage on sampling capacitor



Other considerations

The duration of the sampling time could greatly affect the result of the measurement. During holding, the voltage on the sampling capacitor invariably strays from the supposed DC value because the OTA demands a biasing current. This voltage is then readjusted back to the expected DC value during sampling. The DMM that is reading the output of the S/H circuit is thus essentially taking an average value of this triangle waveform. This phenomenon is shown in Figure 8. To reduce this error, the holding time should be minimized and the capacitor size maximized. It should be kept in mind that the bigger the sampling capacitor is, the more S/H cycles (integration time) will be needed for the charges to integrate to a steady DC value.

Of course, increasing the sampling time does not mitigate the leakage problem. A minimum sampling time should be used that still guarantees the SOTA's holding-time delay and ensures enough time for the sampling capacitor's charge/discharge while it is tracking the S/H circuit's input. Figure 9 shows the recorded values of the op amp's settling time when different sampling times were used with the same holding and integration times. The results were measured against the same waveform taken from a 6-GHz, 10-bit oscilloscope, which showed a maximum overshoot of –60 mV. The measurement using a 20-ns sampling time matched that from the oscilloscope, but at the cost of applying a significant filter over the result. Conversely, the measurement using 6 ns applied a smaller filter but produced a bigger overshoot, which is an artifact of the measurement.

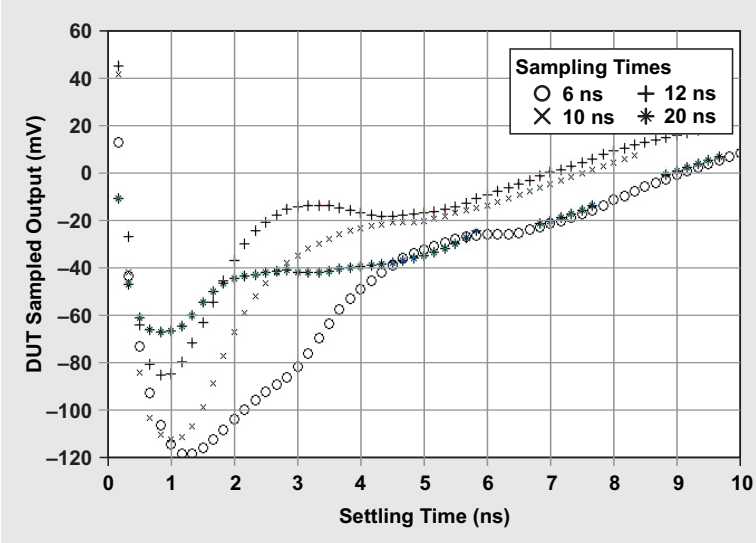
Conclusion

Numerous techniques exist for measuring settling time. This article has introduced a simple yet accurate technique that uses a relatively fast waveform generator and a S/H circuit. Knowing the limitations of this method, the user should be able to adjust any measurement parameters necessary to obtain the best results for a given settling-time range and expected accuracy.

Related Web sites

amplifier.ti.com
www.ti.com/product/OPA615
www.ti.com/product/OPA656
www.ti.com/tinati-ca

Figure 9. Settling time measured with different sampling times



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