# Computing power going "Platinum"

## By Michael O'Loughlin
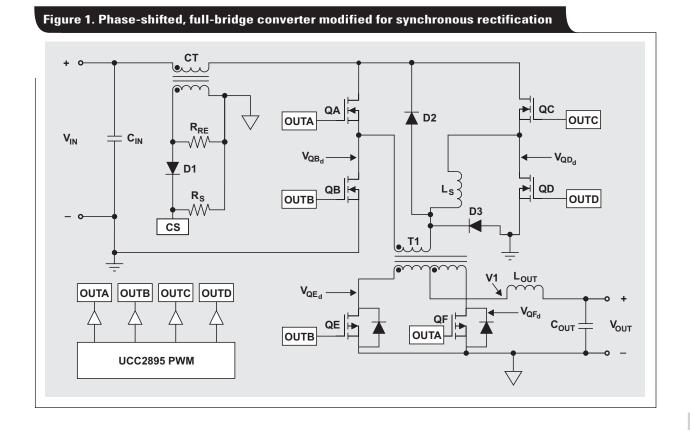*Senior Applications Engineer*

## Introduction

The 80 PLUS™ and Climate Savers Computing™ initiatives have set a very aggressive efficiency standard for computer power supplies. The "Platinum" level of these standards specifies that computer power supplies must have an efficiency of 90% at 20% of rated load, 94% at 50% load, and 91% at 100% load. To meet these standards, some power-supply designers have chosen to use a phase-shifted, full-bridge DC/DC converter with synchronous rectification. This topology is a good choice because it can achieve zero voltage switching (ZVS) on the primary FETs. A popular way to drive the synchronous rectifiers is with signals that are already present driving the primary FETs. The only problem with doing this is that dead times on these primary FETs are required to achieve ZVS. This results in both synchronous rectifiers being off simultaneously during the freewheeling period, allowing excessive body-diode conduction and reducing system efficiency. The purpose of this article is to propose different timing for driving these synchronous rectifiers to reduce body-diode conduction and improve overall system efficiency.

There are a few pulse-width modulators (PWMs) on the market that were developed for controlling a phase-shifted, full-bridge converter but were not set up for driving synchronous rectifiers (QE and QF). To use these controllers in this application, engineers have found they can control the synchronous FETs with control signals OUTA and OUTB from the PWM controller. Figure 1 shows a functional schematic of one of these converters.

## The problem

The PWM controllers help achieve ZVS in these converters by delaying the turn-on of the FETs in the H bridge (QA, QB, QC, QD). The delay ($t_{Delay}$) between the turn-on and turn-off transitions of FETs QA and QB will cause synchronous FETs QE and QF to be off simultaneously, allowing their body diodes to conduct as already stated. The following equation is a good estimate of the body-diode conduction losses in QE and QF during the freewheeling period:

$$P_{Diode} = \frac{P_{OUT}}{V_{OUT}} \times V_D \times t_{Delay} \times f_s,$$

**Figure 1. Phase-shifted, full-bridge converter modified for synchronous rectification**
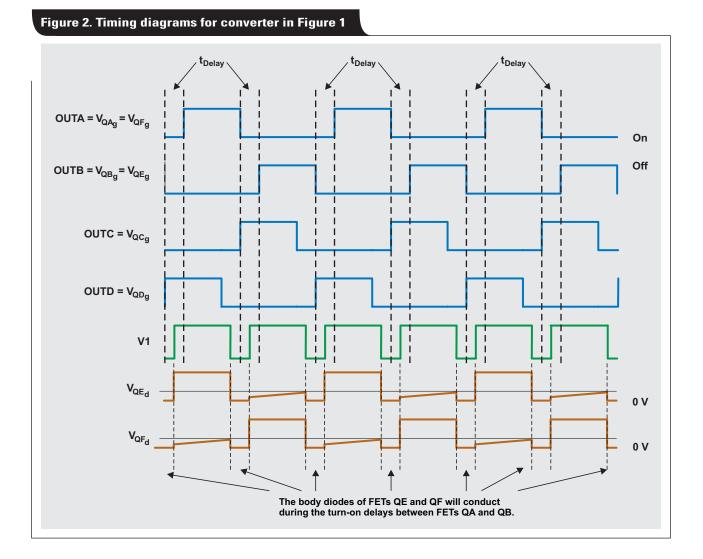
where $P_{OUT}$ is the output power, $V_{OUT}$ is the output voltage, $V_D$ is the forward voltage drop of the body diode, and $f_s$ is the inductor switching frequency.

The excessive body-diode conduction losses of QE and QF ($P_{Diode}$) could cause the design not to meet the Platinum standard. Please refer to Figures 1 and 2 for details. As shown, OUTA drives FETs QA and QF, while OUTB drives FETs QB and QE. V1 is the voltage presented to the input of the $L_{OUT}$ and $C_{OUT}$ filter network, and

$V_{QE_d}$ and $V_{QF_d}$ are the voltages across the respective synchronous rectifiers QE and QF.
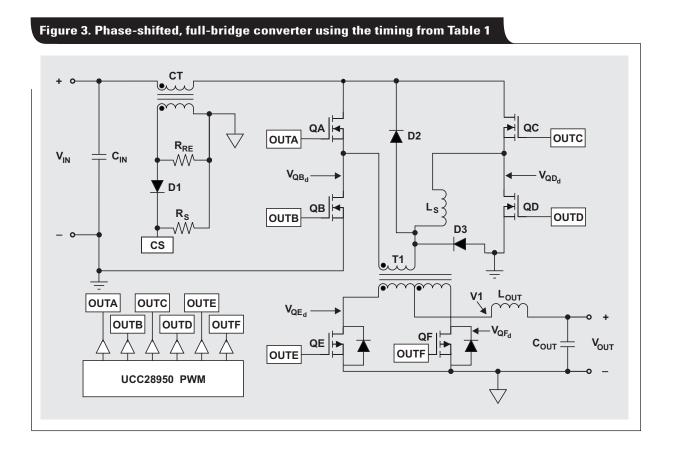
## The solution

To reduce QE and QF body-diode conduction, it would be better to have these synchronous rectifiers on during the QA and QB delay periods ($t_{Delay}$). To accomplish this, FETs QE and QF would have to be driven with their own outputs where the ON times would overlap instead of the OFF

**Figure 2. Timing diagrams for converter in Figure 1**



The body diodes of FETs QE and QF will conduct during the turn-on delays between FETs QA and QB.

times being simultaneous. Figure 3 shows a functional schematic of the phase-shifted, full-bridge converter with six separate drive signals (OUTA through OUTF). The signals for QE (OUTE) and QF (OUTF) can be generated by turning OUTE and OUTF on and off based on the edges of QA through QD. The timing needed to accomplish this

**Table 1. OUTE and OUTF on/off transitions**

| OUTE | Turns on when OUTC turns on | Turns off when OUTB turns off |
|------|------------------------------|--------------------------------|
| OUTF | Turns on when OUTD turns on | Turns off when OUTA turns off |

**Figure 3. Phase-shifted, full-bridge converter using the timing from Table 1**

is presented in Table 1 and Figure 4. The theoretical waveforms in Figure 4 show that this technique removes the body-diode conduction that would be present if both gate drives were off during $t_{Delay}$ with the gate-drive signals presented in Figure 2.

### Experimental results

To see how well this technique worked for reducing body-diode conduction, a 390- to 12-V phase-shifted, full-bridge converter was modified to drive the FETs with the signals shown in Figures 2 and 4.

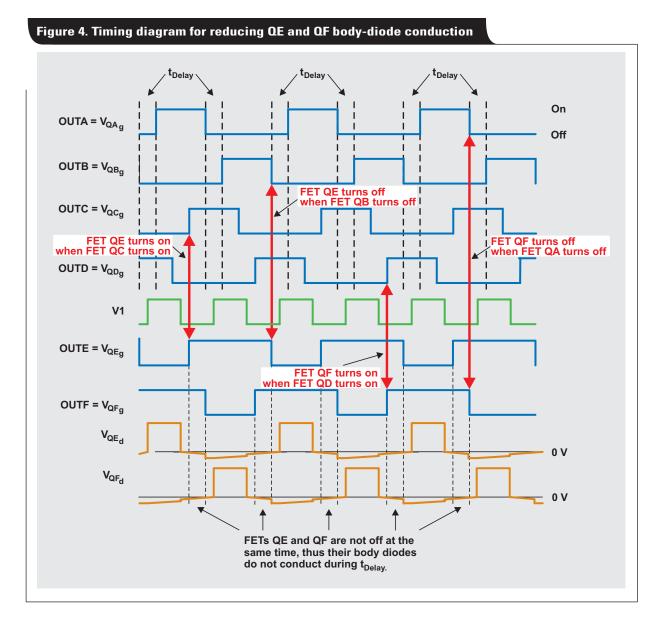**Figure 4. Timing diagram for reducing QE and QF body-diode conduction**

Figure 5 shows a scope plot of the gates of the synchronous FETs (QE and QF) while they were driven with the OUTA and OUTB PWM outputs. In this figure, body conduction can be observed during the delay times ($t_{Delay}$) between OUTA and OUTB.

Figure 6 on the next page shows a scope plot of the gates of the synchronous FETs (QE and QF) while they were driven with the OUTE and OUTF signals presented in Figure 3. These signals were generated from TI's new UCC28950 phase-shifted, full-bridge controller. Figure 6 shows that the body diodes did not conduct when FETs QE and QF were on at the same time. Some body-diode conduction is still visible, but there is not as much as in Figure 5.
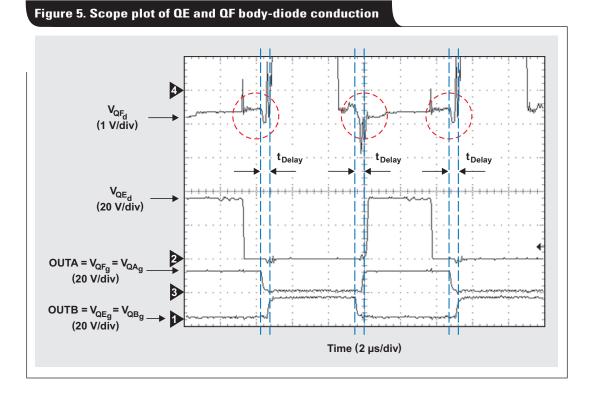
The 600-W DC/DC converter's efficiency was measured for both drive schemes—OUTA and OUTB versus OUTE and OUTF—from 20% to full load. The efficiency data of the converter for these two drive schemes is presented in Figure 7 on the next page. It can be observed that using OUTE and OUTF was roughly 0.4% more efficient at a 50 to 100% load than using OUTA and OUTB. A 0.4% efficiency gain may not seem like a lot but could make a difference when the designer is trying to achieve the Platinum standard.
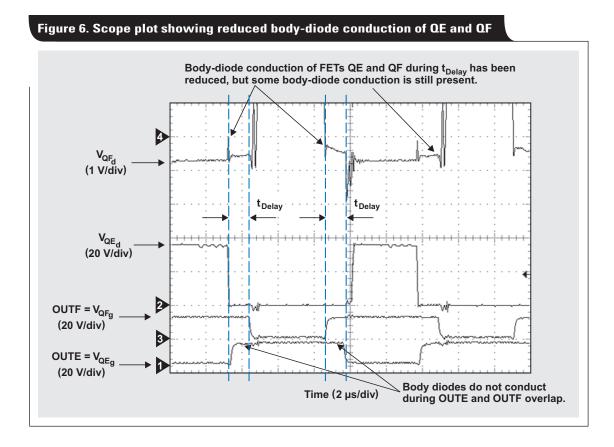
## Conclusion

Even though it is possible to control a phase-shifted, full-bridge converter that has synchronous rectifiers with a phase-shifted, full-bridge controller that was not designed for synchronous rectification (OUTA and OUTB drive scheme), the turn-on delay between OUTA and OUTB required to achieve ZVS causes both synchronous FETs to be off at the same time ($t_{Delay}$). This delay results in excessive body-diode conduction during the FET's freewheeling period. This article has shown that it is more efficient to overlap the ON time of the synchronous rectifiers during the freewheeling time so that the body diodes do not conduct. Even though the body-diode conduction is not completely removed with this technique, it is drastically reduced, improving overall system efficiency and making the Platinum efficiency standard easier to meet.

## Related Web sites

**power.ti.com**
**www.ti.com/sc/device/UCC2895**
**www.ti.com/sc/device/UCC28950**

### Figure 5. Scope plot of QE and QF body-diode conduction

**Figure 6. Scope plot showing reduced body-diode conduction of QE and QF**



Body-diode conduction of FETs QE and QF during $t_{Delay}$ has been reduced, but some body-diode conduction is still present.

$V_{QF_d}$ (1 V/div)

$t_{Delay}$        $t_{Delay}$

$V_{QE_d}$ (20 V/div)

OUTF = $V_{QF_g}$ (20 V/div)

OUTE = $V_{QE_g}$ (20 V/div)

Time (2 μs/div)

Body diodes do not conduct during OUTE and OUTF overlap.

**Figure 7. Efficiency of 600-W DC/DC converter with different QE and QF drive schemes**



OUTE and OUTF Controlling QE and QF

OUTA and OUTB Controlling QE and QF

Efficiency (%)

Power Output, $P_{OUT}$ (%)

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