How the voltage reference affects ADC performance, Part 1

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Introduction

When designing a mixed-signal system, many designers have a tendency to examine and optimize each component separately. This myopic approach can go only so far if the goal is to have a working design at the end of the day. Given the array of different components in a system, designers must have a complete understanding of not only the individual components but also their impact on the overall system performance. When a design has an analog-to-digital converter (ADC), it is critical to understand how this device interacts with the voltage reference and voltage-reference buffer.

This article is the first of a three-part series. Parts 2 and 3 will appear in future issues of the *Analog Applications Journal*. Part 1 looks at the fundamental operation of an ADC independently, exactly as many designers do, and then at the performance characteristics that have an impact on the accuracy and repeatability of the system. Part 2 will delve into the voltage-reference device, once again examining its fundamental operation and then the details of its impact on the performance of the ADC. Part 3 will investigate the impact of the voltage-reference buffer and the capacitors that follow it, and will discuss how to ensure that the amplifier is stable. Assumptions and conclusions will be compared to measurement results. The interplay between the driving amplifier, voltage reference, and converter will be briefly analyzed, followed by an investigation of the sources of error in the ADC's conversion results.

The fundamentals of ADCs

Figure 1 shows the voltage-reference system for the successive-approximation-register (SAR) ADC that will be examined in this three-part series. As the name suggests, the ADC converts an analog voltage to a digital code. The overall system accuracy and repeatability depend on how effectively the converter executes this process. The accuracy of this conversion can be defined with static specifications, and the repeatability with dynamic specifications. Generally, the ADC static specifications are offset-voltage error, gain error, and transition noise. The ADC dynamic specifications are signal-to-noise ratio (SNR), total harmonic distortion (THD), and spurious-free dynamic range (SFDR).

Static performance

Figure 2 shows an ideal and an actual (or non-ideal) transfer function of a 3-bit ADC. The actual transfer function has an offset-voltage error and a gain error. In the example application circuit, only the ADC gain error, transition noise, and SNR are of concern.

Figure 1. Voltage-reference system for SAR ADC

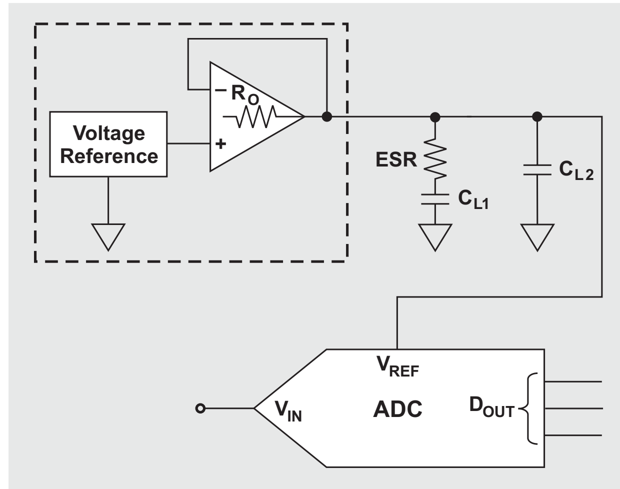


Figure 2. Ideal and actual ADC transfer functions with offset and gain errors

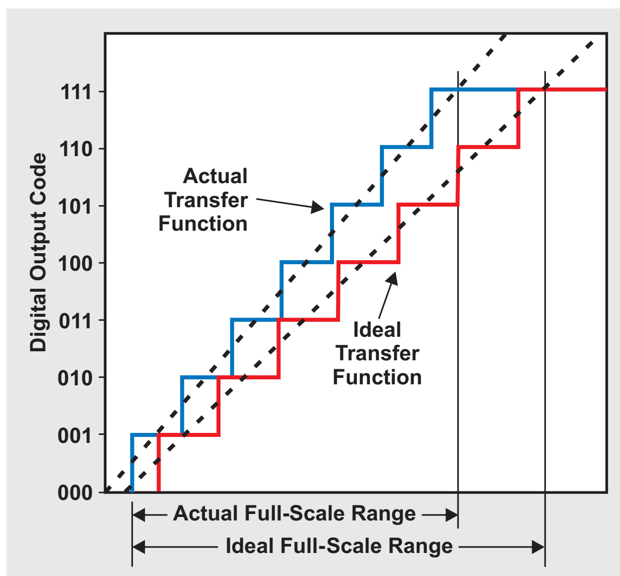
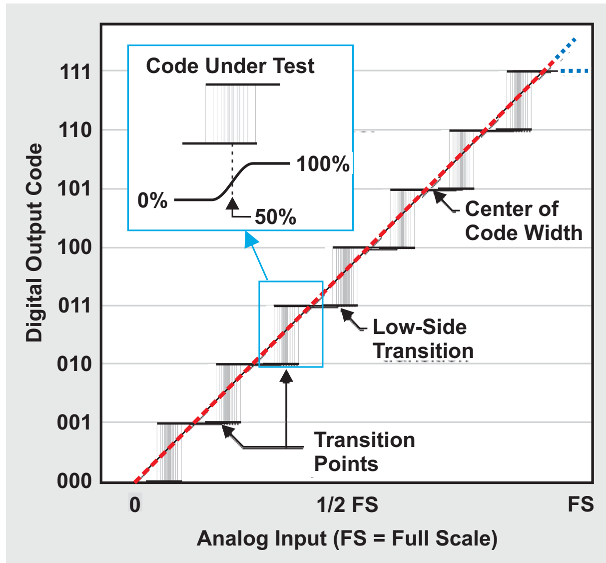


Figure 3. Transition noise with a 3-bit ADC



Equation 1 describes the typical transfer function of the ideal (error-free) ADC:

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}}, \tag{1}$$

where "Code" is the ADC output code in decimal form, V_{IN} is the analog input voltage (in volts), n is the resolution of the ADC (or number of output-code bits), and V_{REF} is the analog value of the voltage reference (in volts). This equation demonstrates that the ADC output code is directly proportional to the analog input voltage and inversely proportional to the voltage reference. Equation 1 also shows that the output code depends on the number of bits (the converter resolution).

The DC errors of non-ideal ADCs are offset-voltage error and gain error. If the offset-voltage error is introduced into the transfer function, Equation 1 can be rewritten as

$$\text{Code} = \left(V_{IN} - V_{OS\_ADC}\right) \times \frac{2^n}{V_{REF}}, \tag{2}$$

where V_{OS_ADC} is the input offset voltage of the ADC. Gain error is equal to the difference between the ideal slope from zero to full scale and the actual slope from zero to full scale. The notation for gain error is a decimal or percentage. If the impact of only the gain error (no offset-voltage error) on an ADC is considered, Equation 1 can be rewritten as

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)}, \tag{3}$$

where GE_{ADC} is the gain error in decimal form, expressed as

$$GE_{ADC} = \frac{\text{Actual Gain} - \text{Ideal Gain}}{\text{Actual Gain}}.$$

From Equation 3 it can be seen that the gain-error factor adds to the initial accuracy of V_{REF}. The output code is inversely proportional to the combination of the voltage reference plus the gain error. The DC error caused by noise from the voltage-reference chip inversely impacts the gain accuracy of the ADC. Part 2 of this series will specifically show the impact of the voltage reference's errors.

Equations 2 and 3 can be combined to show the final transfer function:

$$\text{Code} = \left(V_{IN} - V_{OS\_ADC}\right) \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)} \tag{4}$$

To analyze ADC transition noise, the code transition points in the ADC's transfer curve can be examined. These are the points where the digital output switches from one code to the next as a result of a changing analog input voltage. The transition point from code to code is not a single threshold but a small region of uncertainty. Figure 3 shows the uncertainty at these transitions that results from internal converter noise. The region of uncertainty is defined by measuring repetitive code transitions from code to code.

An ADC's transition noise has a direct effect on the signal-to-noise ratio (SNR) of the converter. Since it is important to understand this phenomenon, Part 2 of this series will look more closely at voltage-reference noise characteristics.

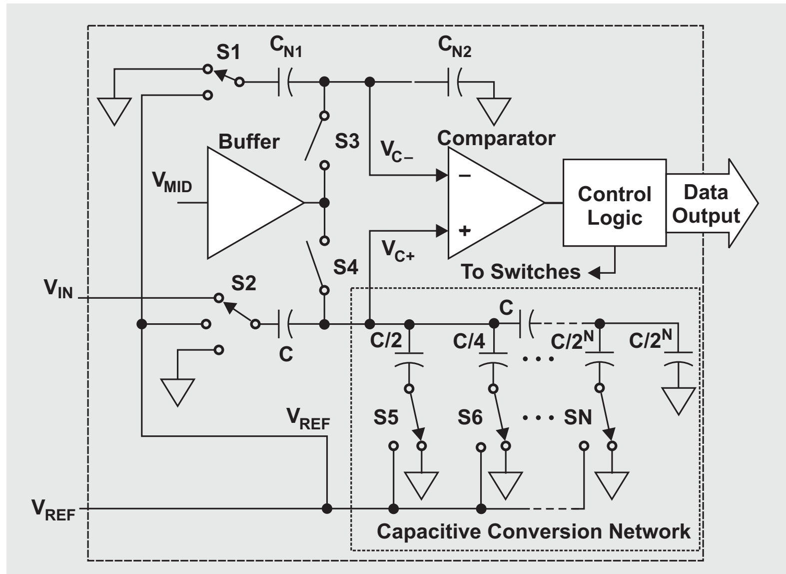
Dynamic performance

The total system noise from the circuit in Figure 1 is a combination of the inherent ADC noise, the noise from the analog input-buffer circuitry, and the reference input-voltage noise. Figure 4 shows a simplified internal circuit of a SAR ADC.

To determine the dynamic performance of an ADC, a fast Fourier transform (FFT) plot of the converter's output data can be used. An FFT plot can be calculated from a consistent clocked series of converter outputs. The FFT plot provides the SNR, the noise-floor level, and the spurious-free dynamic range (SFDR). In the example application circuit, only the SNR specification is of interest. Figure 5 provides an FFT plot of these specifications.

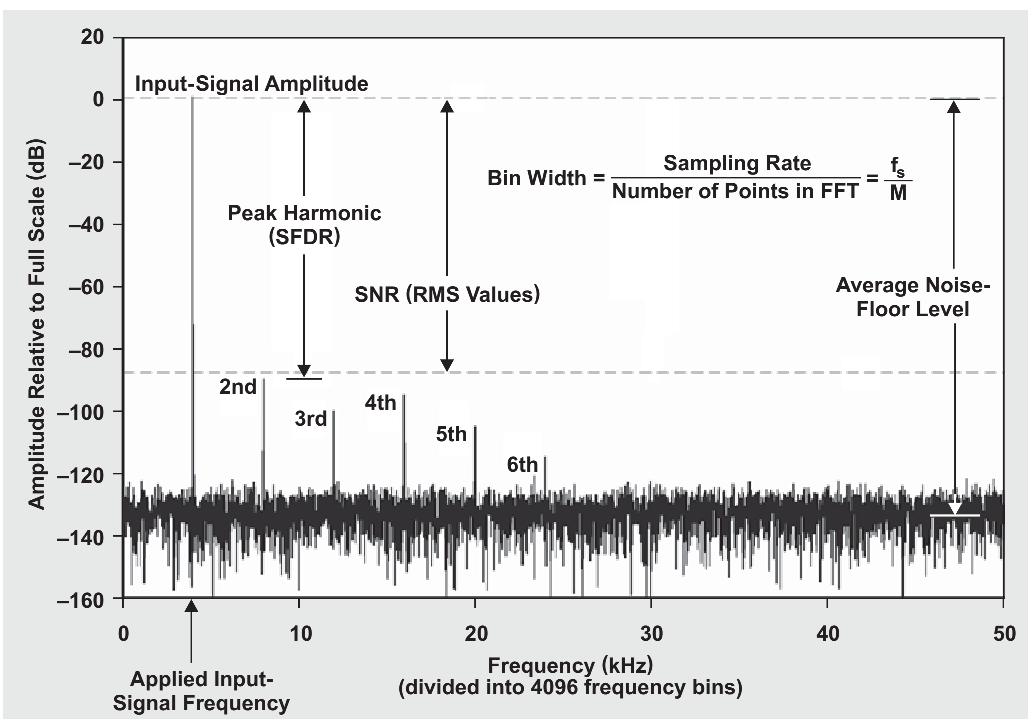
A useful way of determining noise in an ADC circuit is to examine the SNR (see Figure 5). The SNR is the ratio of the root mean square (RMS) of the signal power to the RMS of the noise power. The SNR of the FFT calculation is a combination of several noise sources, which may include the ADC quantization error and the ADC internal noise. Externally, the voltage reference and the reference driving amplifier contribute to the overall system noise. The theoretical limit of the SNR is equal to 6.02n + 1.76 dB, where n is the number of ADC bits.

Figure 4. Simplified topology of a SAR ADC



The total harmonic distortion (THD) quantifies the amount of distortion in the system. THD is the ratio of the root sum square (RSS) of the powers of the harmonic components (spurs) to the input-signal power. For example, in Figure 5, the harmonic components are labeled "2nd" through "6th." An RSS calculation is also known as the

Figure 5. FFT plot with 8192 data samples from a 16-bit converter



square root of the sum of the squares of several values. Spurs resulting from the nonlinearity of the ADC appear at whole-number multiples of the input signal's frequency (the fundamental frequency). Most manufacturers use the first six to nine harmonic components in their THD calculations.

If the ADC creates spikes in the FFT plot, it is probable that the converter has some integral nonlinearity errors. Additionally, spurs can come from the input signal through the signal source or from the reference driving amplifier. If the driving amplifier is the culprit, the amplifier may have crossover distortion; or it may be marginally stable, slew-rate-limited, bandwidth-limited, or unable to drive the ADC. Injected noise from other places in the circuit, such as digital-clock sources or the frequency of the mains, can also contribute spurs to the FFT result.

The combination of the converter's SNR and THD can be used to determine the signal to noise and distortion (SINAD) of the device. Many engineers refer to SINAD as "THD plus noise" or "total distortion." SINAD is an RSS calculation of the SNR and THD; i.e., it is the ratio of the fundamental input signal's RMS amplitude to the RMS sum of all other spectral components below half the sampling frequency (excluding DC). While the SAR converter's theoretical minimum for SINAD is equal to the ideal SNR, or 6.02n + 1.76 dB, the working SINAD is

$$\text{SINAD (dB)} = -20\log\sqrt{10^{-\text{SNR}/10} + 10^{\text{THD}/10}}. \qquad \textbf{(5)}$$

SINAD is an important figure of merit because it provides the effective number of bits (ENOB) with a simple calculation:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\ \text{dB}}{6.02} \qquad \textbf{(6)}$$

In an FFT representation of converter data, the average noise floor (see Figure 5) is an RSS combination of all the bins within the FFT plot, excluding the input signal and signal harmonics. The number of samples versus the number of ADC bits can be chosen so that the noise floor is below any spurs of interest. With these considerations, the theoretical average FFT noise floor (in decibels) is

$$\text{FFT Noise Floor} = 6.02\text{n} + 10\ \log\left(\frac{3\text{M}}{\pi \times \text{ENBW}}\right),$$

where M is the number of data points in the FFT, and ENBW is the equivalent noise bandwidth of the FFT window function. A reasonable number of samples for the FFT of a 12-bit converter is 4096, which will result in a theoretical noise floor of –107 dB.

Conclusion

The ADC specifications that impact the application circuit in Figure 1 are gain error, transition noise, and SNR. Part 2 will examine the voltage reference's DC accuracy and noise contribution to the system performance.

References

For more information related to this article, you can download an Acrobat® Reader® file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

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