High-Performance Analog Products

Analog Applications Journal

Third Quarter, 2008

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Contents

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

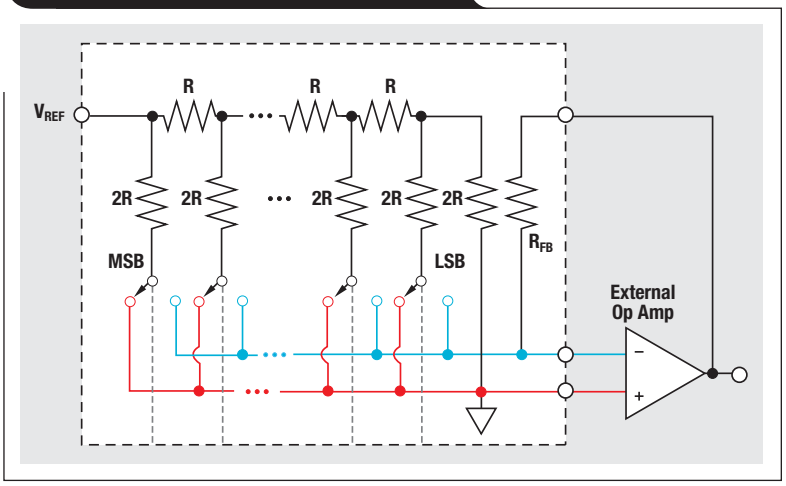
A DAC for all precision occasions

By Bonnie C. Baker, *Senior Applications Engineer*

Introduction

Analog-to-digital converters (ADC) routinely convert analog signals such as temperature, pressure, sound, or images to a precise digital representation. Microcontrollers and microprocessors store, massage, and transmit this digital information throughout a system. There are also times when precision digital-to-analog converters (DAC) convert the digital representation of these real-world events back into the analog domain. Three of the DAC topologies that achieve this feat are the R-2R MDAC, R-2R backDAC, and the string DAC. These three topologies service applications such as automatic test equipment, instrumentation, portable equipment, and digitally controlled calibration.

Figure 1. An R-2R multiplying DAC



The R-2R MDAC

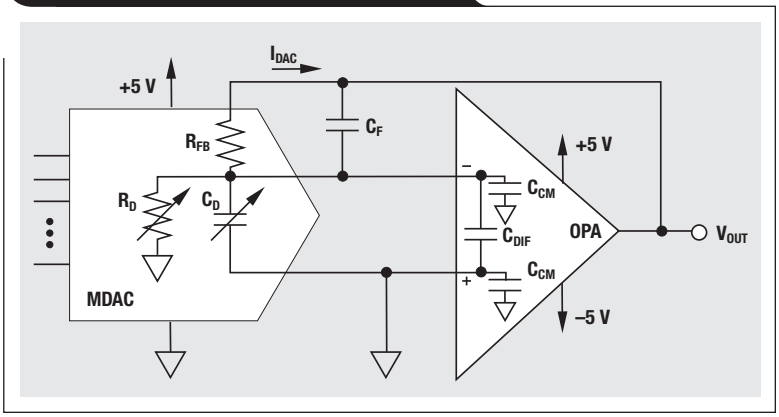
Automatic test equipment or instrumentation typically uses the R-2R multiplying DAC (MDAC, Figure 1). The external operational amplifier augments the DAC function by providing the opportunity for differing supply voltages and high output currents. MDAC manufacturers are able to design high resolution devices (16 bit) with ±1 LSB integral non-linearity (INL) and differential non-linearity (DNL) specifications. With an appropriate external amplifier, the MDAC exhibits fast settling time (< 0.3 ms) with a multiplying bandwidth that can be greater than 10 MHz.

The MDAC generates a current that is proportional to an input digital code. The external amplifier, along with R_{FB} (internal in the MDAC), converts the DAC's current-output signal to a usable voltage level. It would seem that a simple current-to-voltage conversion is easy to implement with a DAC, an amplifier, and a resistor. However, this application circuit has a set of stability issues.

The output model of the MDAC contains a current source, variable resistor, and variable capacitor (Figure 2a). The output resistance and capacitance of the MDAC is dependent on the input code to the DAC. Programming the MDAC to zero causes the output resistance (R_D) to be near infinite. If you program the MDAC to full scale or all ones, R_D is equal to R_{FB}. The output capacitance (C_D) changes according to the number of internal gate-source junctions across the MDAC output. At full scale, the MDAC output capacitance is equal to the data sheet specification. When programmed to zero scale, the MDAC output capacitance is equal to approximately half the full-scale value. As we calculate the worst-case stability condition, we will use the full-scale output values of R_D and C_D.

To maintain precision, most MDACs have a feedback resistor (R_{FB}) on-chip. The feedback capacitor, C_F, is external and discrete. The unity gain bandwidth (f_U) of

Figure 2a. MDAC model



the operational amplifier, as well as the input-differential capacitance (C_{DIF}) and common-mode capacitance (C_{CM}), directly affect the stability of this circuit.

At the input of the amplifier, the total capacitance in this system is equal to $C_{IN} = C_D + C_{DIF} + C_{CM}$. The pole and zero in the feedback loop of the amplifier are equal to (see Figure 2b and c):

$$f_1 = \frac{1}{2\pi(C_{IN} + C_F) \times (R_D \parallel R_F)} \quad \text{[feedback circuit zero]}$$

$$f_2 = \frac{1}{2\pi(C_{IN} + C_F)} \quad \text{[feedback circuit pole]}$$

You determine the system stability by keeping the difference of the rate of change of the operational amplifier open-loop gain curve and the closed-loop gain curve at 20 dB/decade. You can do this by selecting an amplifier with unity gain bandwidth (f_U) less than f_1 or higher than f_2 (Figure 2b and c).

From here, it is easy to design a stable circuit. If f_1 is higher than the unity gain crossing of the amplifier f_U, the following formula applies to this design.

$$C_F \geq \frac{1 + \sqrt{1 + 8\pi C_{IN} R_F f_U}}{2\pi R_F f_U}$$

If f_2 is lower than the intersection of the open-loop gain curve and the closed-loop gain curve, use this formula.

$$C_F \leq \frac{1}{2\pi(R_D \parallel R_F) f_U} - C_{IN}$$

These calculated values of C_F are a starting point. As you test your circuit, parasitics, device manufacturing variations, etc. can prompt you to modify the value of C_F.

Making the MDAC analog voltage signal stable is critical. However, there are other issues to take into account. At the risk of covering this topic too briefly, consider issues such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy.

The MDAC is a low-noise solution for a variety of applications. The voltage-reference, current-output change with digital codes to the MDAC is constant. The trade-off for this advantage is varying ground currents with digital input codes. Typically, you will find MDACs in digital gain and attenuation control circuits as well as waveform generators.

The R-2R back-DAC

You usually use the R-2R back-DAC (Figure 3) in industrial applications. Some other applications for the R-2R back-DAC include instrumentation and digitally controlled calibration. With the R-2R back-DAC, each new update switches the 2R legs to either the voltage reference high (VREF-H) or the voltage reference low (VREF-L). Notice that the arrangement of the R-2R ladder is upside down as compared to the MDAC. This is where the name "back-DAC" came from. This architecture is simple to manufacture, assuming the resistors for each current source can be properly adjusted.

Gate-switch timing skews manifest themselves at the output of the MDAC and back-DAC as glitches. The glitch is most prevalent during the MSB transition, when bits are

Figure 2b. Model's frequency response with a high-bandwidth amplifier

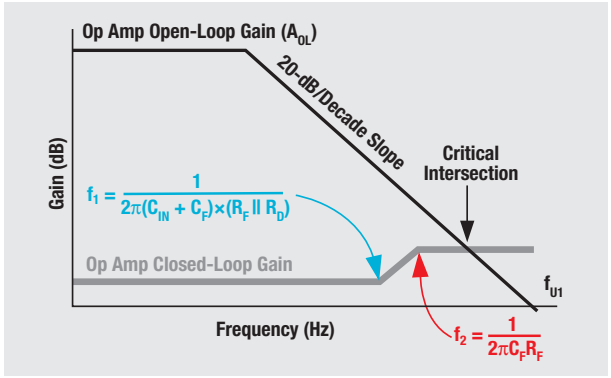


Figure 2c. Model's frequency response with a low-bandwidth amplifier

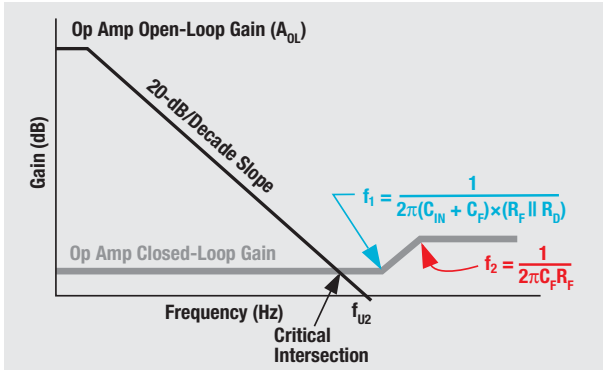


Figure 3. An R-2R Back-DAC

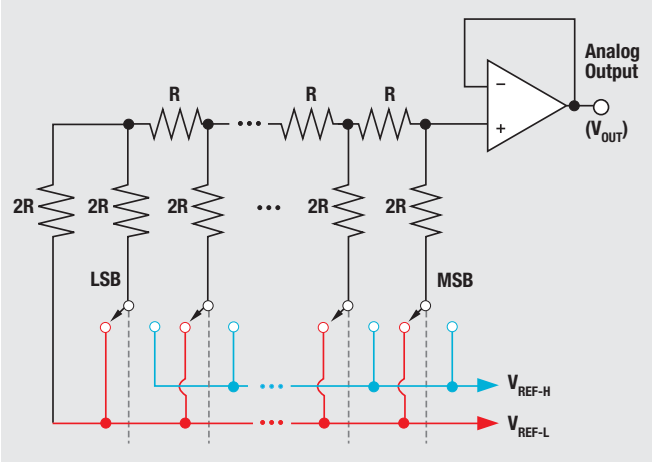


Figure 4a. Glitch impulse of a DAC producing two regions of code transition error

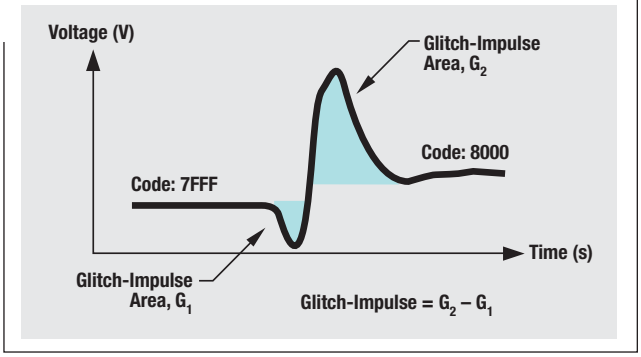
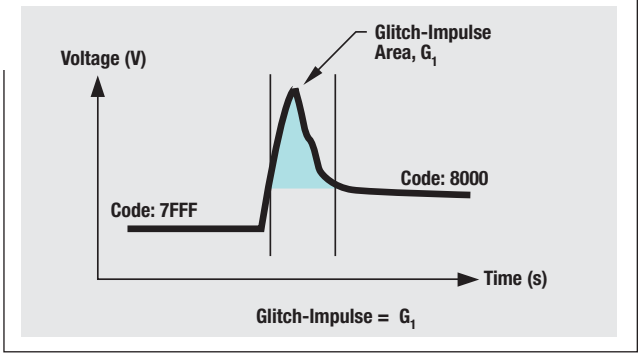


Figure 4b. Glitch impulse of DAC producing one region of overshoot



switching from 7FFFh to 8000h (for a 16-bit DAC). The R-2R back-DAC, like the MDAC, typically has excellent low noise, INL, and DNL performance, with medium settling-time capability.

DAC glitches result from capacitive-charge injection from the internal, asynchronous gate switching. The DAC glitch for R-2R DACs typically has two lobes (Figure 4a), while string topologies typically have a single-lobe glitch impulse (Figure 4b).

The units of a glitch impulse is volts/seconds. Glitch impulses are most dramatic between consecutive codes where a major code transition occurs. In Figure 4a the total glitch impulse equals G_2 minus G_1, where G_1 and G_2 are the calculated areas. In Figure 4b the total glitch impulse equals the shaded area of G_1. In most systems, you can ignore the glitches that occur at the output of a DAC during code transition; however, in a control loop, glitch impulses are typically undesirable. In a control system, the DAC glitch impulse from a one-bit code transition, where the MSB is switching, confuses the loop by momentarily sending an erroneous output-voltage signal.

The glitch-impulse area in Figure 4a occurs during the DAC's output-voltage transition region as it switches from one code to another. As the 16-bit DAC switches from 8000h to 7FFFh (or half the full-scale output voltage), the output glitch impulse becomes noticeable to the extent that it appears as if the DAC is momentarily non-monotonic. Secondary glitches occur around the one-fourth full-scale and three-fourths full-scale voltages. If the control system is fast enough to respond to this glitch, the circuit may oscillate.

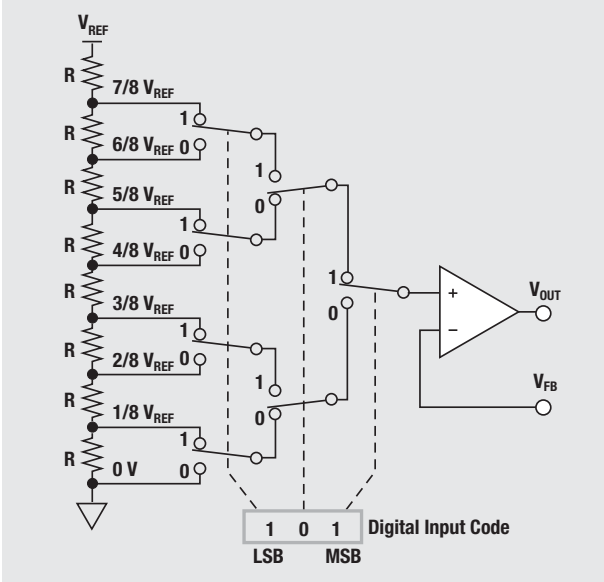
You can try to reduce the impact of this glitch impulse by using a low-pass filter at the output of the DAC. However, while a low-pass filter reduces the glitch-impulse amplitude, it increases the glitch time. For example, consider a glitch-impulse response of the 16-bit DAC is equal to 96 nV-s, with a peak voltage of 60 mV and duration of 1.6 µs. You can filter this glitch impulse so that the peak voltage is 30 mV with duration of 3.2 µs. You can also add sampling circuitry on the output of the DAC and time it with DAC conversions. This technique may work for lower resolution, slow DACs; however, the sampling mechanism may create more problems by adding to the analog errors and conversion time. The best way to overcome larger glitch impulses is to select a string DAC with lower glitch-impulse errors from the start.

The R-2R back-DAC has medium settling time capability; however, you can build high-performance circuits with its superior INL and DNL performance. Texas Instruments achieves higher accuracy specifications with final test trimming. The R-2R ladder also facilitates low-noise performance from the DAC.

String DAC topology

The string DAC is best suited for portable instrumentation, closed-loop servo control, and process control. Figure 5 shows a model of a 3-bit string DAC. In this figure, the digital input code 101b is decoded to 5/8 V_{REF}. The string DAC's output-stage amplifier isolates the internal resistive elements from output loads. The string DAC is a low-power solution that guarantees monotonicity

Figure 5. String DAC topology



with good DNL performance across the entire input code range. The glitch energy is typically lower than other types of DACs; however, the INL performance is generally larger and dependent on resistive, on-chip matching. On the other hand, a DAC in a control loop lessens the impact of high linearity. The noise of string DACs is also relatively high because of the resistive string-array impedance.

The string DAC operates with low power and very low glitch energy. An on-chip output buffer simplifies the interface to this device.

DAC calibration

With any of the three DACs in this article, you may see a need to calibrate the analog output for higher precision results. If you calibrate any DAC, you initially determine the code-to-voltage error at one-third of the output range and again at two-thirds of the output range. The range between one-third full scale (FS) and two-thirds FS avoids the output amplifier errors near the power supply rails. You achieve the calibration of the offset and gain errors with the formula $V_{OUT} = a + bV_{IN}$ ("a" is the offset error and "b" is the gain error). You can calibrate your DAC in the digital domain with the help of an ADC that is more accurate than the target specifications of a DAC.

A more challenging DAC calibration activity is to adjust the linearity of the converter's entire output range. Once again, you will require an ADC that has four times the resolution of the DAC. You can calibrate every DAC code with 8, 10, or 12 bits of resolution. In this environment there are fewer DAC codes to calibrate and the memory requirements are lower. The accuracy of the calibrating low-bit ADC is not as demanding, allowing faster ADC conversion times. For DACs with resolution of 14+ bits, the total number of codes becomes unmanageable in terms of processor memory. Additionally, you will need to use a slower ADC with higher accuracy, such as a delta-sigma converter. Higher cost and slower speeds will encourage you to consider alternative DAC calibration strategies.

An effective alternative to linearizing every DAC code is to select several small groups of codes. The plot in Figure 6a shows an example of the integral non-linearity of a 16-bit string DAC. The universal formula for calculating any DAC correction code is

$$DAC_{COR} = INL_V + (INL_V - INL_W) \times \frac{v - x}{v - w},$$

where INL_V and INL_W are the INL error of the v and w code. x is a code between codes v and w. If (v – w) is equal to an integer that is a power of two, you can implement the division with right shifts, reducing the processor calculation time and complexity. Figure 6b illustrates the benefit of this linearization technique using 1024 code groupings, 64 codes per group.

This technique is best suited for DACs that are monotonic, with INL error in excess of ±8 LSB. Additionally, you must exercise care when selecting the size of the code sets. If there are large, sudden jumps from one code to the next, as may be with R-2R architectures, this technique may prove to be counterproductive instead of an improvement in DAC performance. The string DAC topology is best suited for this calibration technique because it is inherently monotonic (a requirement for this technique) and jumps from one code to the next are relatively small as compared to other DAC topologies.

Figure 6a. INL of a 16-bit string DAC

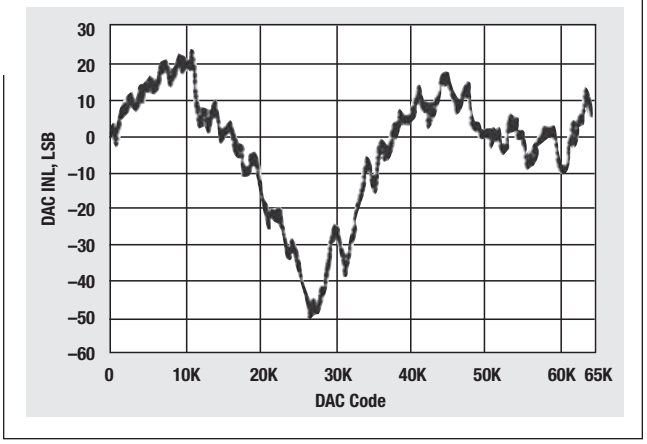
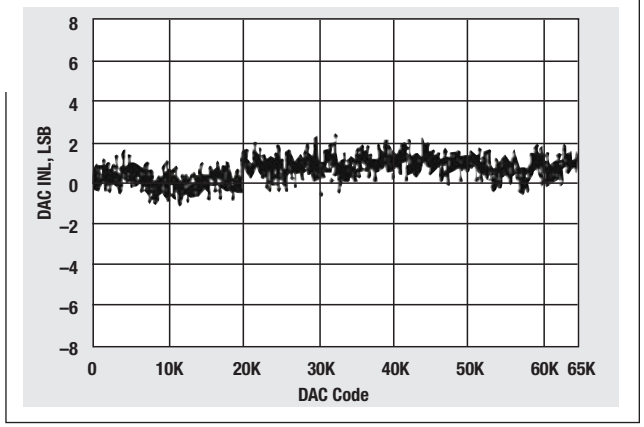


Figure 6b. A correction step of 64 LSB (1024 out of the 65,536 points) reduces the INL error to less than ± 3 LSB



Conclusion

A precision DAC uses a limited number of discrete digital input codes to produce a corresponding number of discrete analog output values. For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. The MDAC, R-2R back-DAC, and string DAC architectures do not encompass all of the possible DAC topologies, but if you know about these topologies you will have a good start on knowing the basics.

Related Web sites

dataconverter.ti.com

New current-mode PWM controllers support boost, flyback, SEPIC and LED-driver applications

By Jürgen Schneider, *Systems Engineer Power Solutions*

Introduction

With their wide input voltage range, the TPS40210 and TPS40211 PWM controllers are targeted for isolated and non-isolated power converters used in industrial, automotive, and battery-powered applications. The full freedom in selecting the power stage and its compensation—as well as the advanced features, such as programmable soft start, adjustable/synchronizable oscillator frequency and internal slope compensation—supports the use of the devices in many applications. The basic converter architecture can provide different power levels by simply changing the power stage. While the TPS40210 is designed for general-purpose applications, the TPS40211 is tailored for driving high-brightness LEDs.

Features

- Input voltage: 4.5 to 52 V
- Current-mode architecture
- Switching frequency: 35-kHz to 1-MHz (programmable and synchronizable)
- Programmable soft start (closed loop)
- Reference voltage: 700 mV for TPS40210 and 260 mV for TPS40211
- Internal slope compensation
- Threshold for overcurrent detection: 150 mV
- Internal 8-V regulator and N-channel MOSFET driver
- Quiescent current when disabled: 10 µA
- MSOP10 PowerPAD™ and 3-mm x 3-mm SON package

Boost converter application

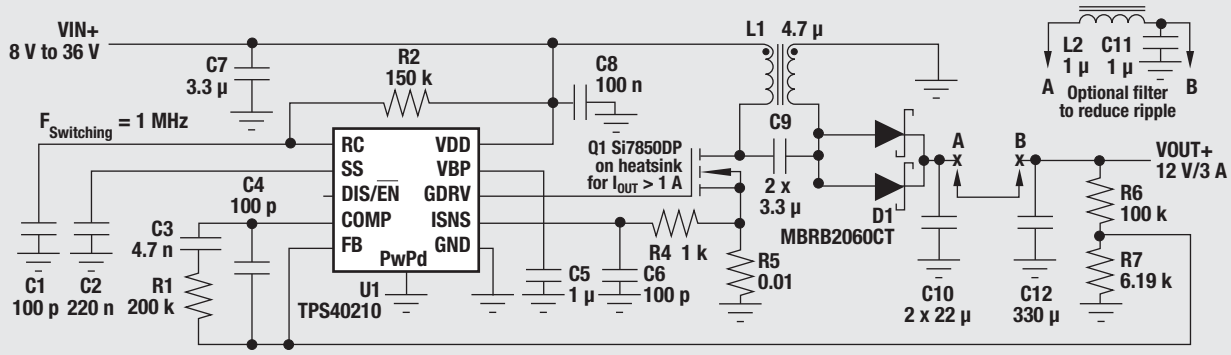
The devices and their basic configuration are described in detail in Reference 1.

SEPIC converter application

The SEPIC-converter shown in Figure 1 allows the input voltage to be smaller, larger, or equal to the targeted output voltage. The topology requires two single inductors or one coupled inductor, L1, and a capacitor C9, which is responsible for the energy transfer. The filter formed by L2 and C11 is optional. It reduces the output ripple voltage to 50 mV_{p-p} in the example shown. When operating the converter at 1 MHz, the size of the power stage (inductors/capacitors) can be minimized. However, due to the increased switching loss at this high frequency, a greater than 1-A continuous output current requires Q1 to be mounted on a heat sink. Operation without a heat sink is possible at a reduced switching frequency and/or reduced maximum input voltage.

With a 2-A current output and a 1-MHz switching frequency, converter efficiency was measured as follows: 90% with a 12-V source, 88% with a 24-V source, and 85% with a 36-V source.

Figure 1. SEPIC 1-MHz converter with 8- to 36-V input and 12-V/3-A output



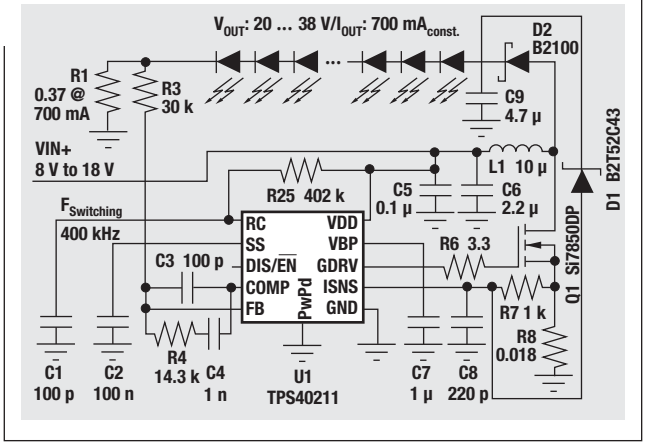
Flyback converter application

Figure 2 shows the TPS40210 controller configured in a flyback-converter topology for a dual-output isolated supply. Key components include the transformer (T1), the snubbers (R5, C7, D1, R8, C9, R10, R11, C12 and C13), the optocoupler (U2), the secondary-side reference and error amplifier (U3), the bias resistor (R15) belonging to U3, the loop compensation (C19, C20 and R16), the output-voltage divider (R17 and R18), and the secondary-side soft-start and overshoot control (D5, R14 and C18). The circuit shown directly controls the positive output rail (V_{OUT}+) only. Negative-rail regulation is based on the cross regulation between the two secondary windings of T1. When the negative output does not have a load, R12 and D4 provide a basic load.

High-brightness LED-driver application

DC/DC regulators are usually designed to provide a constant-voltage output; however, LED applications require a constant-current output. In Figure 3, R1 is used to sense the LED current. The losses in R1 are minimized with the TPS40211 because of its low 250-mV reference voltage. D1 protects against output overvoltage in the event of an LED-string open circuit. The brightness can be programmed by altering R1, current injection into the FB pin, or by PWM dimming. See Reference 1 for more information.

Figure 3. 700-mA high-brightness LED driver



References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "TPS40210/211" data sheet	slus772

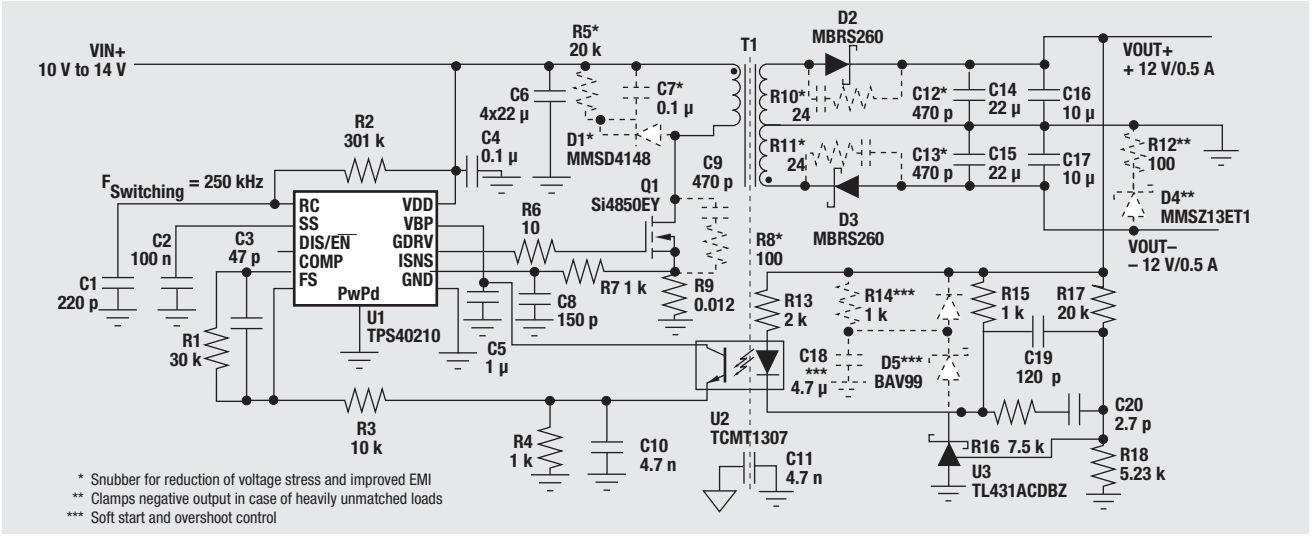
Related device

TPS40200—4.5- to 52-V wide input range step-down converter
www.ti.com/sc/device/TPS40200

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS40210

Figure 2. Isolated flyback converter with a 10- to 14-V input and ±12-V/0.5-A output



When good grounds turn bad—isolate!

By Thomas Kugelstadt
Senior Applications Engineer

Industrial communication via fieldbus-transceiver systems often requires long transmission lines. Designers, unaware of the large ground-potential differences (GPDs) between remote bus locations, either rely on the local earth ground as a reliable signal return path or directly connect remote grounds to each other—thus creating noisy ground loops. In both cases the integrity of the transmission signal is compromised, which can lead to system lockup and, at worst, destroy the bus transceivers.

To make designers aware of these design pitfalls, this article explains where GPDs originate in the electrical installation, how ground loops are created unintentionally, and how isolation circumvents both conditions to yield a robust data-transmission system.

Linking grounds

The link between the direct-current (DC) ground of a local electronic circuit and the earth reference potential of the mains is usually provided by the local power supply converting the line voltage into the required DC output. Figure 1 shows a simplified block diagram of a low-cost switched-mode power supply (SMPS) typically used in personal computers, laser printers, and other equipment. Here the DC ground of the SMPS output is referenced to the protective earth (PE) conductor of the mains via the SMPS chassis. This direct link, therefore, acts as a sense conductor, establishing the PE voltage as the local DC ground potential.

Linear and nonlinear loads

Large office and industrial buildings operate a vast number of nonlinear loads such as PCs, laser printers, solid-state heater controls, fluorescent tubes, uninterruptible power supplies, and variable-speed drives. In comparison to linear loads such as incandescent lamps, whose phase currents maintain a sinusoidal waveform, nonlinear loads distort phase currents, introducing large harmonic content (see Figure 2).

Figure 1. Simplified block diagram of an SMPS

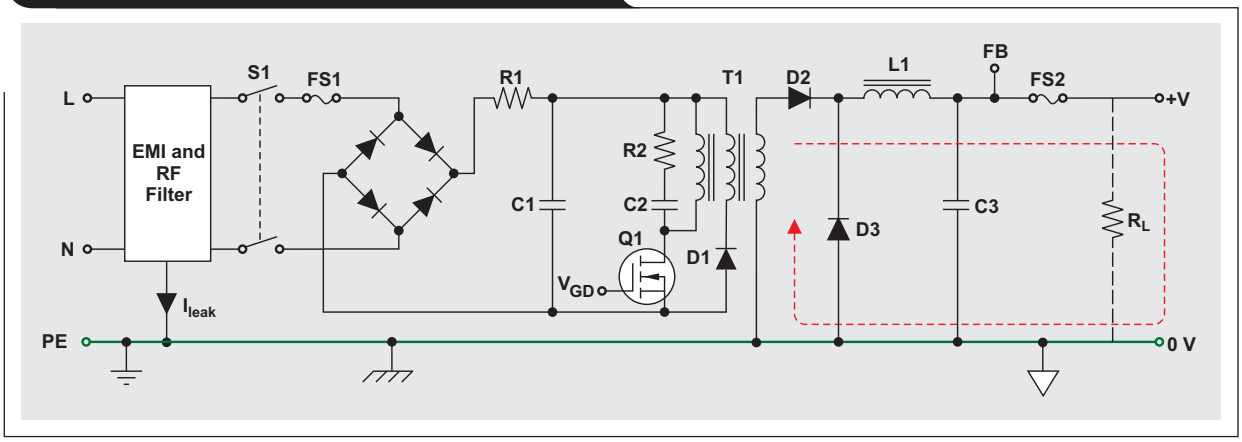


Figure 2. Distorted phase current and its frequency components

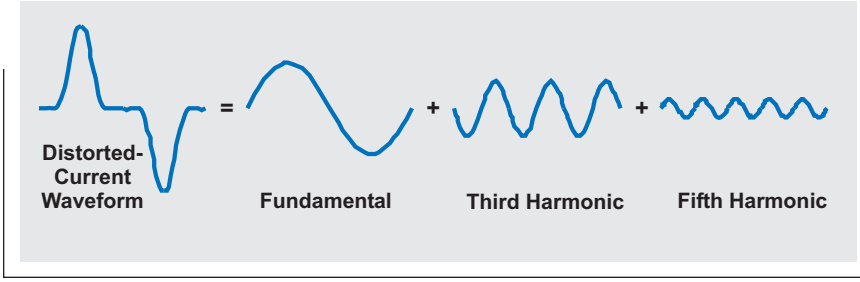


Figure 3. Multiphase currents with a linear load

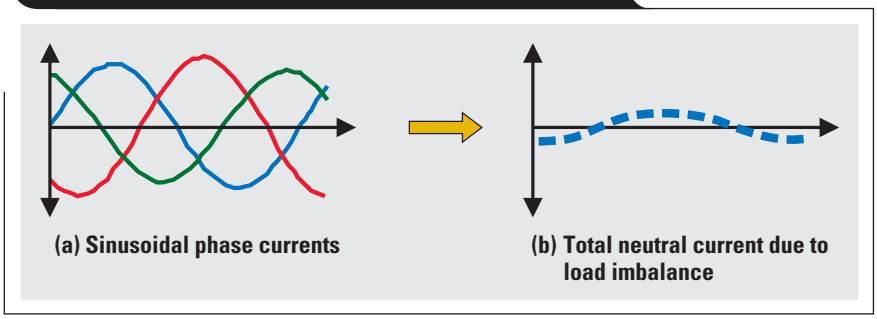
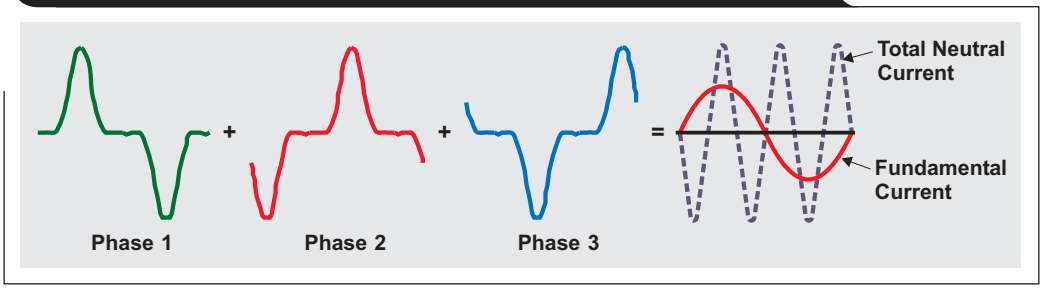


Figure 4. Total neutral current consists mainly of third harmonics



While the third and fifth harmonics of the fundamental 60-Hz line frequency make up the lion's share of the harmonic content, the vector sum of all frequency components (including the 60-Hz fundamental) can reach peak values that exceed the amplitude of the fundamental phase current by more than 100%.

All neutral conductors merge into one neutral conductor of large diameter within the distribution panel, running towards the transformer (Figure 5). In the case of linear loads, the neutral currents of multiphase systems cancel each other to a certain extent. Only a fraction of the total neutral current remains due to loading imbalance (Figure 3).

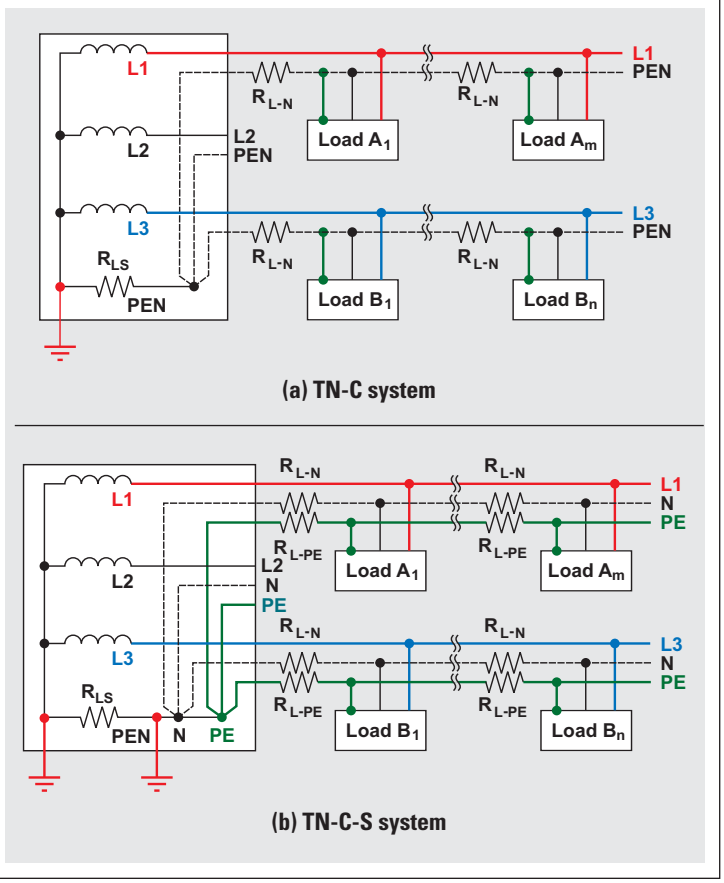
For nonlinear loads, however, the individual currents add up to a total neutral current consisting primarily of third harmonics (Figure 4). The large neutral currents of nonlinear loads, therefore, cause significantly higher voltage drops across the line resistance of the electrical installation than those of linear loads.

Earthing systems

Most electrical installations use either the TN-C or the TN-C-S earthing system, both shown in Figure 5.

"TN" means the neutral is grounded to earth (French *terre*) at the transformer. The letter "C" indicates the combined use of PE and neutral lines via one conductor, designated as "PEN." The PEN runs through the entire system up to a distribution point (i.e., a subpanel) close to the loads, where it is split into separate PE and neutral conductors that directly connect to the loads.

Figure 5. TN-C system (a) with typically higher GPDs than TN-C-S system (b)



Although TN-C represents an old earthing system, it has regained interest because it is less costly than a system requiring an additional PE conductor. The TN-C method, however, has a major drawback. Because the split into PE and neutral lines occurs close to a load, the voltage potential at the local PE connection includes the large voltage drops across the line resistance, $R_{L\text{-}N}$, of long neutral conductors. These voltage drops are caused by high neutral currents from nonlinear loads. The TN-C system, therefore, has the potential to cause large GPDs between remote grounds in the tens of volts.

The TN-C-S system reduces GPDs by starting an extra PE conductor within the distribution panel. Additionally, the star connection of the system's neutral and PE conductors receives a second grounding to earth, reducing the equipotential at this point and counteracting the otherwise large voltage drop at the PEN across the source line resistance, R_{LS}.

According to the United States National Electrical Code (NEC), the PE conductor is supposed to be currentless under normal operation. However, most nonlinear loads leak currents in the lower milliamperes into the PE conductor. This amount, although small for one circuit, easily reaches amperes when hundreds of circuits contribute into the same line.

Although negligible in comparison with neutral currents, leakage currents do create potential differences between remote ground locations due to the voltage drops across the line resistance of the PE conductors. These GPDs, however, are in the millivolts range or lower and are thus significantly lower than in TN-C systems.

GPDs are not a problem for an electronic circuit limited to operation from only one local supply. GPDs do become of concern in the design of a communication link between two remote circuits (i.e., fieldbus-transceiver stations), each operating from a different supply.

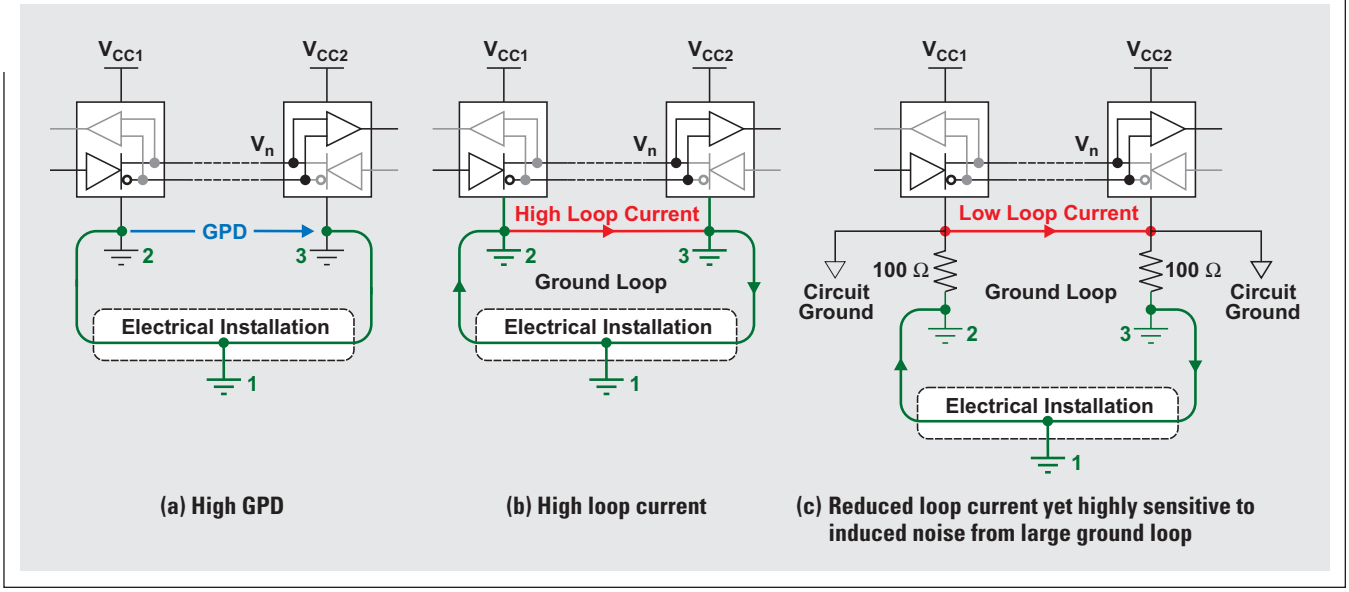
Designing a remote data link

When designing a remote data link, the designer must assume GPDs exist. These voltages add as common-mode noise, V_n, to the transmitter output. Even if the total superimposed signal is within the receiver's input common-mode range, relying on the local earth ground as a reliable path for the return current remains dangerous (see Figure 6a). This applies even to "super" RS-485 transceivers such as the Texas Instruments SN65HVD2x family, whose input common-mode range stretches from –20 V to +25 V.

Any modifications of the electrical installation (i.e., during regular maintenance work) are out of the designer's control. The modifications can increase the GPD to the extent that the receiver's input common-mode range is either sporadically or permanently exceeded. Thus, a data link that works perfectly today might cease operation sometime in the future.

Removing the GPD by directly connecting remote grounds through a ground wire is also not recommended (Figure 6b). Bear in mind that the electrical installation constitutes a highly complex resistance network consisting

Figure 6. Design pitfalls



of multiple cross-connected line and grounding resistances caused by multiphase systems, different cable lengths, and various grounding electrode paths (Figure 7).

A direct connection between remote grounds shunts this network while creating a current loop. The initial GPD tries to compensate its collapse by driving a large loop current through the low-impedance ground wire. The loop current couples to the data-line circuit and generates noise voltage that is superimposed on the transmission (common-mode) signal. This again carries the risk of a highly unreliable data-transmission system.

To allow for a direct connection of remote grounds, the RS-485 standard recommends the separation of the device ground and the local system ground via the insertion of resistors (Figure 6c). While this approach reduces loop current, the existence of a large ground loop keeps the data link sensitive to noise generated somewhere else along the loop. Thus, a robust data link still has not yet been established. The most robust RS-485 data link over a long distance, withstanding GPDs of up to hundreds and thousands of volts, is via galvanic isolation of the signal and supply lines of a bus transceiver from its local signal and supply sources (Figure 8).

Supply isolators such as isolated DC/DC converters, and signal isolators such as digital capacitive isolators, avoid the creation of current loops and prevent current flow between remote system grounds with GPDs of up to several thousand volts.

Without a reference to ground, the bus transceivers would be operating from a floating supply. Thus, current or voltage surges caused by lightning, ground faults, or other noisy environments would be able to lift the floating bus common to dangerously high levels. These events won't destroy components connected to the bus, as their signal and supply levels are referenced to the bus common and ride on the varying common reference potential. However, where the transmission wires connect to PCB connectors at the various transceiver nodes, the high voltages, if not removed, can lead to arcing and destroy PCB components close to the connector. To suppress current and voltage transients on the bus common, it is necessary to reference the bus common at one point to the system ground. This location usually is at a non-isolated transceiver node, which provides the single-ground reference for the entire bus system.

Figure 7. Example of resistance complexity of grounding paths

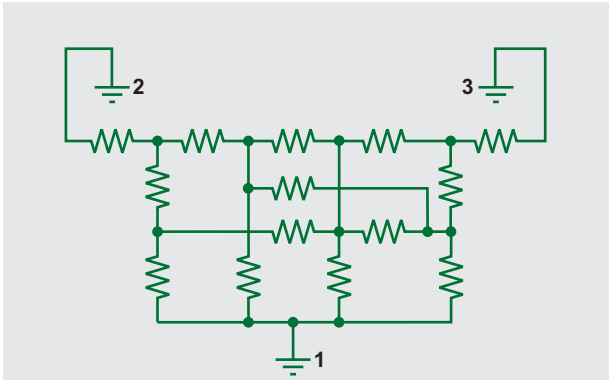


Figure 8. Isolation of two remote transceiver stations with single-ground reference

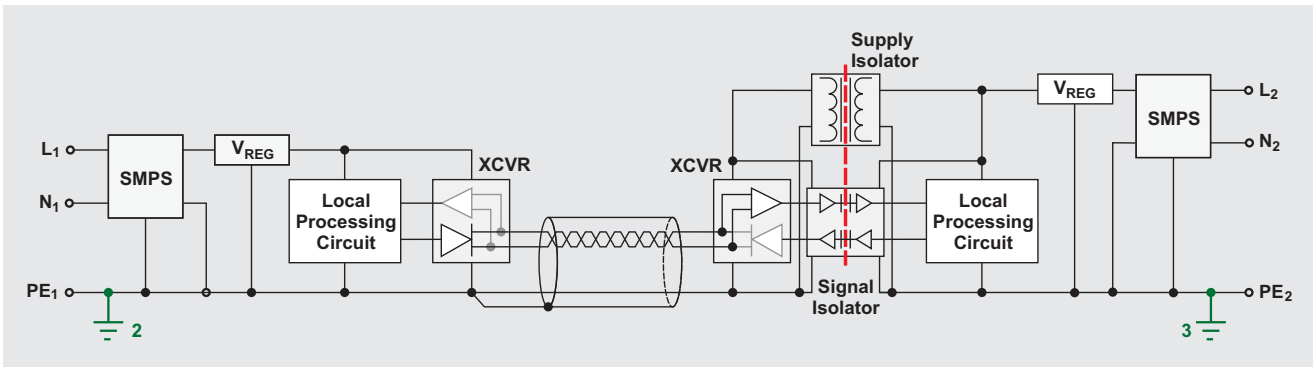
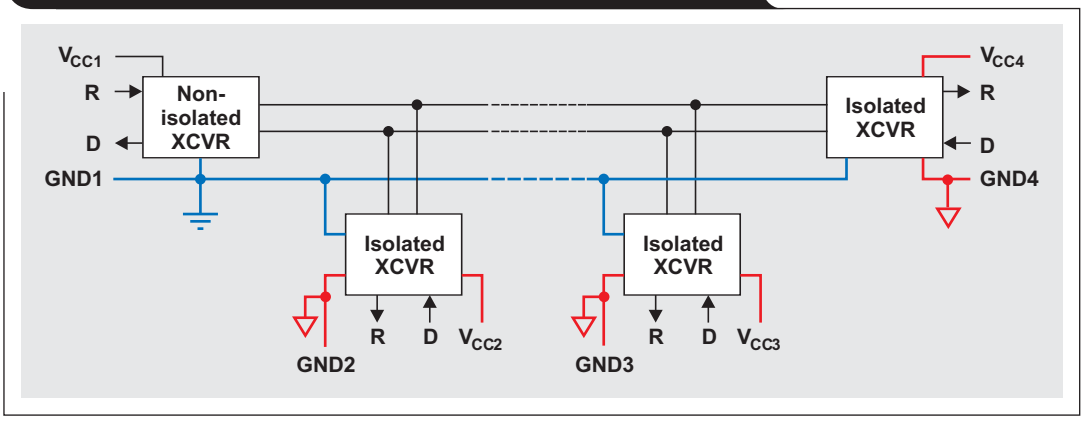


Figure 9. Isolation of multiple fieldbus-transceiver stations



While Figure 8 shows the detailed connection of two remote transceiver nodes, Figure 9 shows an example of an isolated data-transmission system using multiple transceivers. Here all but one transceiver connect to the bus via isolation. The non-isolated transceiver on the left provides the single-ground reference for the entire bus.

Conclusion

Designing remote data links requires the isolation of supply and signal lines of fieldbus-transceiver stations to circumvent the detrimental effects of GPDs and ground loops on the signal integrity and the components.

While some of the figures in this article illustrate differential data transmission, the principles discussed also hold true for single-ended transmission systems such as the RS-232.

Related Web site

interface.ti.com

Cascading of input serializers boosts channel density for digital inputs

By Frank Dehmelt, *Systems Engineer Analog Products*

Introduction

Programmable logic controllers (PLCs) play an integral role in industrial automation. They allow inputs from digital as well as analog sensors and provide outputs to drive actuators. The digital inputs represent a significant share of those I/Os, accepting inputs from end switches, proximity switches, fuel sensors, light barriers, over-temperature sensors and many others.

The traditional approach

There are several types of digital inputs; the IEC-61131-2-standard defines those most commonly used.

Traditionally, digital inputs used discrete components and required a parallel processor interface. Current limitation was achieved by a series of high-power resistors. Resistor-capacitor (RC) filters reduced bouncing of mechanical switches, while a per-channel optocoupler connected to the parallel processor interface. This design, however, requires bulky components, many isolation channels, and a large footprint host controller to allow for the parallel inputs. It also creates significant power dissipation.

With a typical resistor chain providing about 2.2 kΩ, the current at the nominal 24 V rises to 11 mA and results in power consumptions of 260 mW or 400 mW at 30 V. Considering that this dissipation may occur simultaneously for all input channels — along with the bulky components and the processor interface — it severely limits channel density.

A new approach

TI's SN65HVS88x product family addresses these limitations and more. The digital input serializer (as the name implies) serializes the inputs into a single SPI data stream and reduces the number of isolators by 50%.

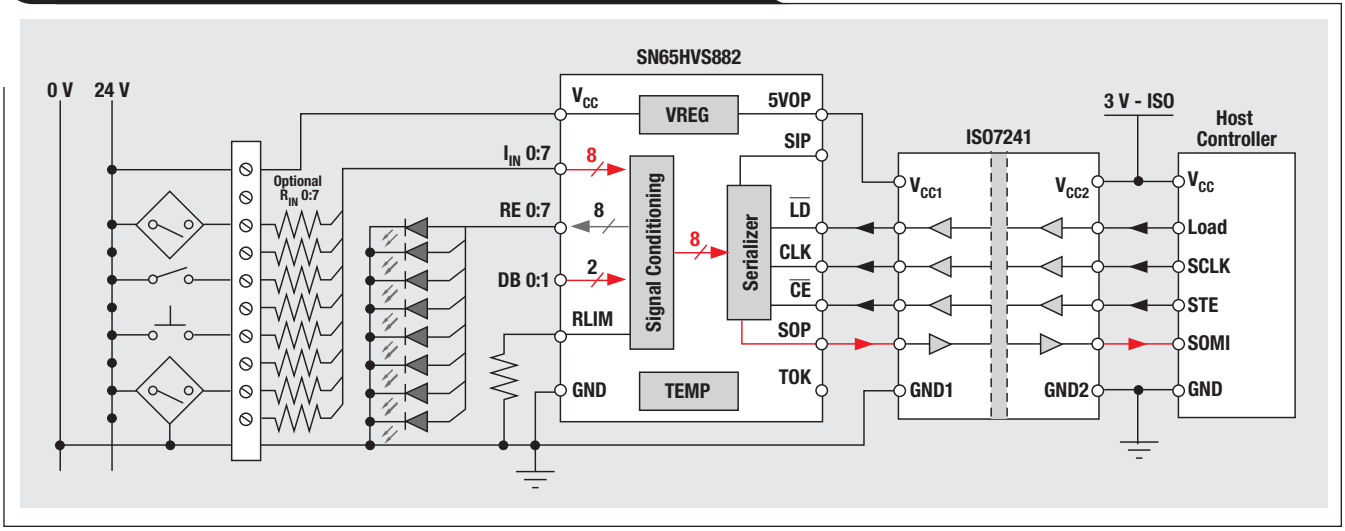
The resistors and LEDs shown in Figure 1 are required by the IEC-61131-2-standard; they can be omitted for inputs that do not require conformance with this standard. Regardless, the integrated current limit allows use of a lower power resistor.

The input current is fed to an output pin, which allows to drive an external LED to indicate the current state of the input. Without the LED, this pin simply connects to ground.

The HVS88x family allows for the cascading of several devices, all sharing the same SPI interface. For a 32-channel input, it still provides a four-channel isolation, saving 87% of ISO channels.

And what about power dissipation with a 32-channel interface? We previously calculated a worst-case dissipation of 400 mW/channel totaling almost 13 W: this is too much for a PLC slice which is about the size of a deck of cards. The HVS88x family allows the designer to set current limitation anywhere between 200 µA and 5.2 mA. For a type-1 or type-3 switch, choose a limit in the 3-mA range, limiting the per-channel dissipation to 90 mW at 30 V. This reduces power dissipation by more than 75% vs. a discrete approach.

Figure 1. 8-channel digital input using HVS882 and ISO7241



The designer can further reduce the number of external components by using the integrated debounce filter, set to filter pulses of less than 3 ms or 1 ms in duration. For the fastest acquisition of glitch-free switches, bypass the filter as well.

The parts operate from the 24-V nominal field supply and generate the internally used 5 V themselves. This supply is also available to drive external circuitry such as the field side of the isolation barrier on the SPI interface.

The HVS88x family allows high-density digital inputs by serialization, cascading, a significant reduction of power dissipation, and elimination of external components. Production material, samples, and evaluation boards are available.

Related device

ISO721 – High-speed digital isolator
www.ti.com/iso721

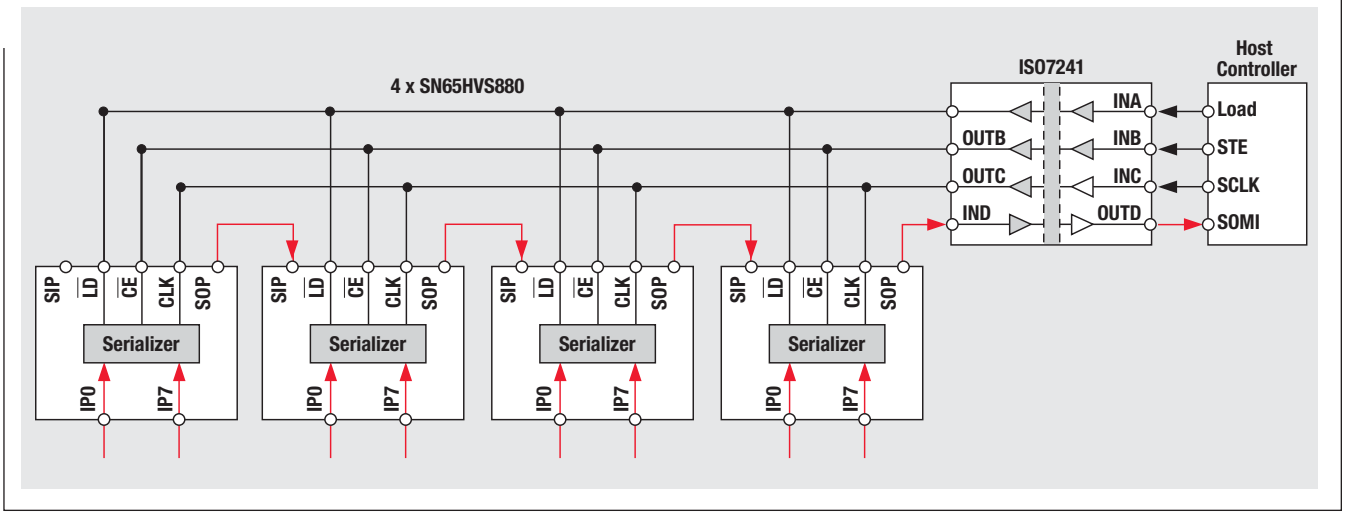
Related Web sites

interface.ti.com
www.ti.com/sn65hvs882

Table 1. The SN65HVS88x digital input serializer family digital isolator

PARAMETER	SN65HVS880	SN65HVS882
Serialization	Yes	Yes
Cascading	Yes	Yes
Current Limitation	Yes (0.2 to 5.2 mA)	Yes (0.2 to 5.2 mA)
Debounce Filter	Yes (0 ms, 1 ms, 3 ms)	Yes (0 ms, 1 ms, 3 ms)
V_{CC}	18 V to 30 V	10 V to 34 V
Undervoltage Indicator	Yes (~15 V)	No
5-V Output	Yes	Yes
Input Voltage Range	0 V to 30 V	0 V to 34 V
Temperature Range	–40°C to 85°C	–40°C to 125°C
Over-Temperature Protection	Yes	Yes

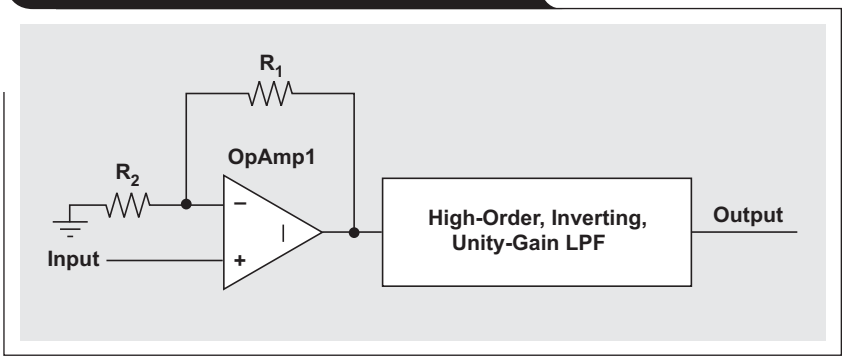
Figure 2. Simplified 32-channel digital input with cascading, using four HVS88x serializers and one ISO7241 digital isolator



A new filter topology for analog high-pass filters

By Mark Fortunato
Analog Field Applications Manager

Figure 1. Gain block with high-order LPF



The analog circuit designer today has literally dozens of circuit topologies available to implement filters, from the venerable Sallen-Key (SK) filter, in use for well over fifty years,[1] to more esoteric and hard-to-pronounce filters such as the Mikhael-Bhattacharyya (MB) filter or the Padukone-Mulawka-Ghausi (PMG) filter.[2] Each of these filters has advantages and disadvantages relative to its cousins. Nearly all of the filter topologies used today were developed in the 1950s, '60s, and '70s.[2–6]. Can we come up with a filter topology that has an advantage over all the many topologies that have been in use for decades? For some specific needs, the new topology presented here has some unique advantages.

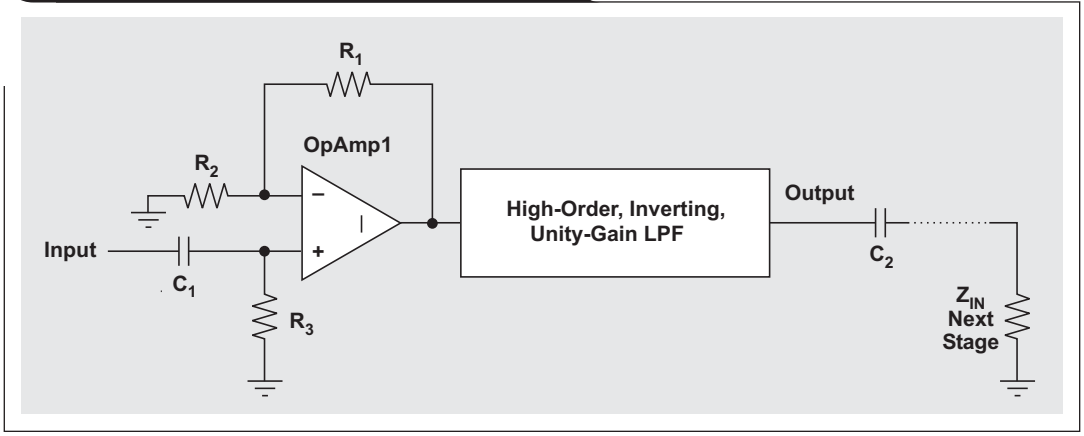
Almost all the common high-pass filters (HPFs) tend to have one thing in common—capacitors in series with the forward signal path. For most applications, having capacitors in the signal path is not a problem. However, there are applications where such capacitors can be problematic. For example, in broadband low-noise circuits such as many audio circuits, there is a need to keep resistance values, and thus noise, low. These applications also often call for high-pass functions that roll off at low frequencies, below 10 Hz in some audio applications. These cases can thus call for very large capacitor values. Large-value capacitors tend to be very expensive or have voltage coefficients and other non-idealities that can ruin the fidelity of the signals being passed through them.

Another limitation of the HPFs commonly used is that the entire filter circuit is implemented separately and placed either before or after another circuit functional block. Sometimes a filter in front and one after a block is needed. The technique we will discuss here allows an engineer to design a circuit without consideration of the high-pass function required. After the circuit is designed, another circuit can be "wrapped around" the original one that will cause the overall circuit to have a high-pass function without affecting the operation of the original circuit at frequencies above the high-pass rolloff.

Adding a high-pass function to block DC offsets

Figure 1 is a simplified schematic of a circuit with a gain block driving a high-order low-pass filter (LPF) in a signal-processing application. In this example there is an offset in the input signal and an offset caused by the filter, both of which must be removed. Typically a designer would place a capacitor in series with the input and the output as shown in Figure 2. For many applications this approach is just fine; but for some applications, this simple AC-coupling scheme can cause problems. Besides the reasons already

Figure 2. Adding simple AC-coupling stages



discussed, the characteristics of these high-pass stages may adversely affect the signal-processing function that is the primary purpose of the overall circuit. Each of these AC-coupling stages creates a single real (i.e., simple) pole at the frequency determined by the applicable RC time constant. Especially as the number of AC-coupling stages in the signal chain increases, the composite high-pass function is unlikely to be the optimal one for the full circuit and system. More commonly, a filter with complex pole pairs is necessary to optimize the HPF response.

Using servo feedback rather than blocking capacitors

In our example, let's assume that the input signal presents the largest of the offsets and that the filter's output offset, though small, is objectionable for the latter stages. Let's further assume that the desirable HPF function is that of a single pole. If we eliminate the input AC-coupling filter, the output filter will certainly remove all DC offsets for the subsequent stages; but then that input offset will cause the signal applied to and processed by the filter to be significantly shifted "off center," which can cause significant distortion.

An old technique referred to as "servo feedback" is often used in cases like this. This technique provides AC coupling, removing all offsets at the output of the circuit without putting any circuitry in series with the amplifier/filter chain of Figure 1. Servo feedback is fully covered in Reference 7.

The feedback path added in Figure 3 is an inverting integrator. The integrator output is fed to the inverting terminal of the input amplifier so that the overall loop has negative feedback. Assuming that the rolloff of the LPF is at least a decade above the desired high-pass rolloff, we can treat the LPF as a flat gain block for the purposes of calculating the high-pass response. A simple analysis shows that we have added a high-pass function with the transfer function

$$\frac{V_{OUT}}{V_{IN}} = -G_{LPF}\frac{R_1+R_2}{R_2}\frac{S\dfrac{R_2R_3C_1}{R_1G_{LPF}}}{1+S\dfrac{R_2R_3C_1}{R_1G_{LPF}}}, \qquad (1)$$

where G_{LPF} is the absolute value of the LPF gain. G_{LPF} is a high-pass function with a 3-dB (pole) frequency of

$$f = \frac{\dfrac{R_1}{R_2}G_{LPF}}{2\pi R_3C_1}. \qquad (2)$$

Since the LPF in this circuit has a gain of –1, we get the frequency response shown in Figure 3 with a pole frequency of 15.92 Hz.

This servo technique solves the problem of putting capacitors in series with the signal path, eliminates the need for multiple high-pass stages, and allows a designer to add a high-pass function to a gain/low-pass block without modifying the block itself. However, this technique is capable of implementing only simple poles and thus does

Figure 3. Single-pole HPF using servo feedback

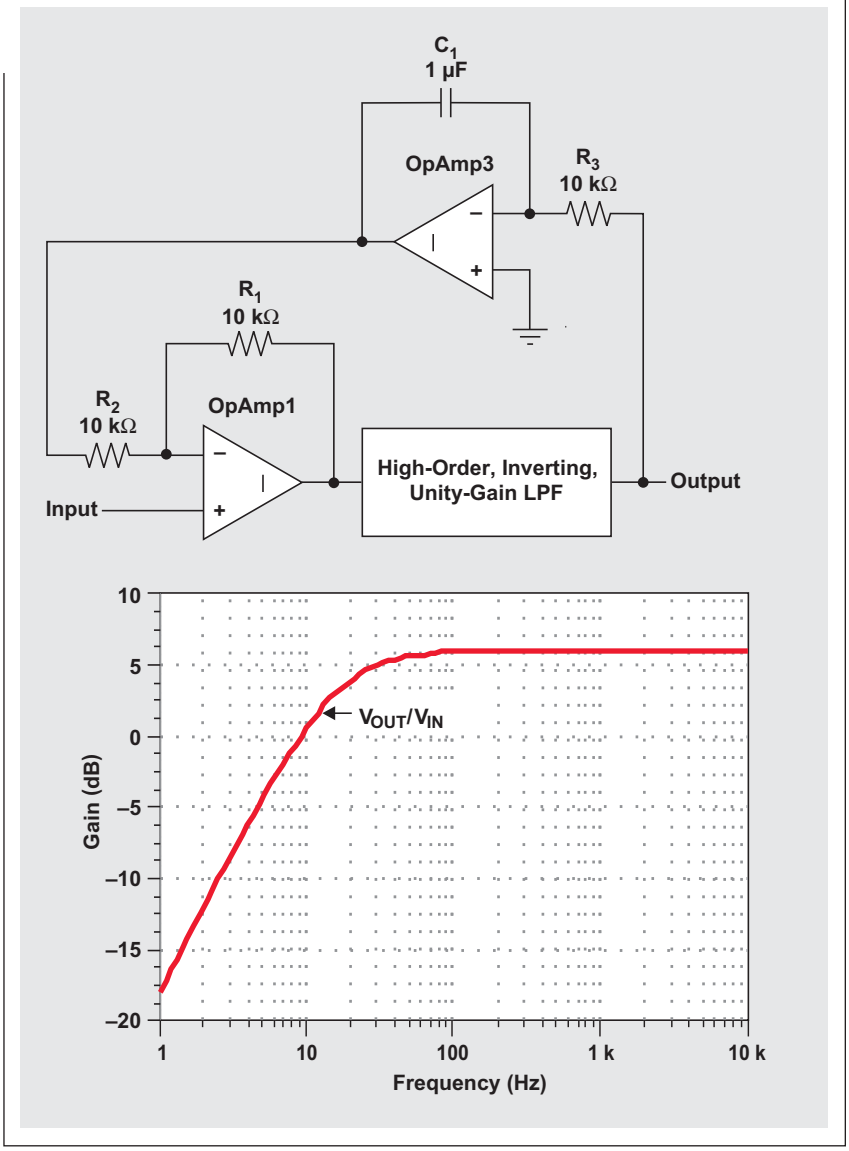
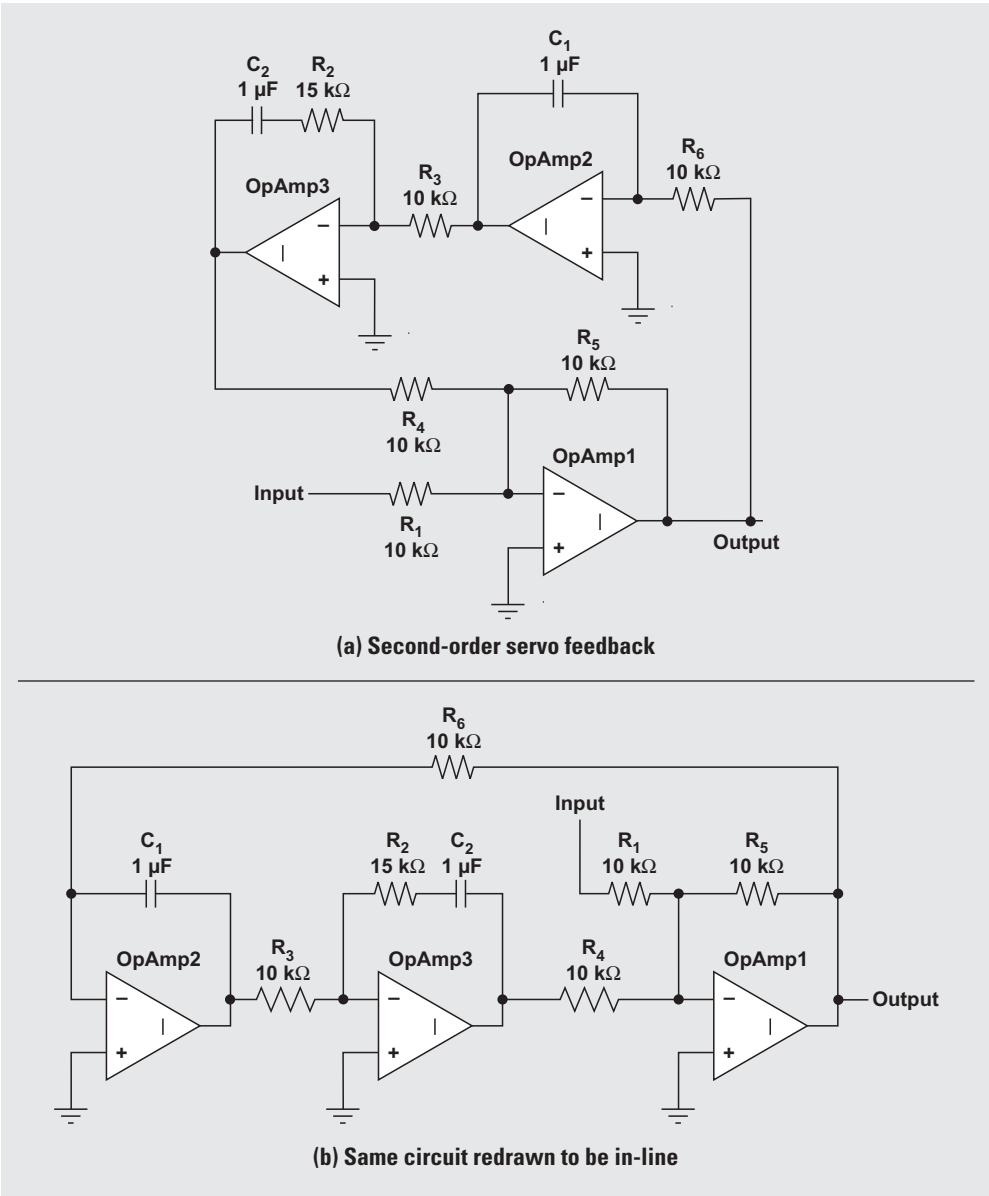


Figure 4. New second-order high-pass topology



not allow us to create complex pole pairs. Therefore we need a similar technique that will provide a complex second-order function.

A new circuit topology implements a complex pole pair

Figure 4 shows just such a circuit, drawn two different ways. Figure 4a shows a gain block with the frequency-dependent part of the circuit wrapped around it like the first-order servo filter discussed earlier. Figure 4a is very similar to the previous schematics except that there are two integrators in the feedback path, one of which has an added resistor included to set the Q of the second-order function. Figure 4b shows the identical circuit just shifted around to be in-line. Anyone familiar with three-op-amp biquad circuits such as the Kerwin-Huelsman-Newcomb (KHN) and Tow-Thomas (TT) filters will see a distinct similarity. In fact, this topology is the same as the TT filter except that, rather than having a resistor in parallel with C_1, it has R_2 in series with C_2.

The end result of this subtle change from the TT filter is that, whereas the TT filter implements an LPF and a band-pass filter (BPF) but no HPF, this circuit can implement an HPF and a BPF but no LPF. In our new circuit the HPF

output is the node labeled "Output" in both Figures 4 and 5. Figure 5 identifies the BPF output as "BPF_{OUT}."

The transfer function, pole frequency, and Q for our new HPF are respectively given by

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_5}{R_1}\frac{S^2C_1C_2R_3R_6\frac{R_4}{R_5}}{S^2C_1C_2R_3R_6\frac{R_4}{R_5}+SC_2R_2+1}, \quad (3)$$

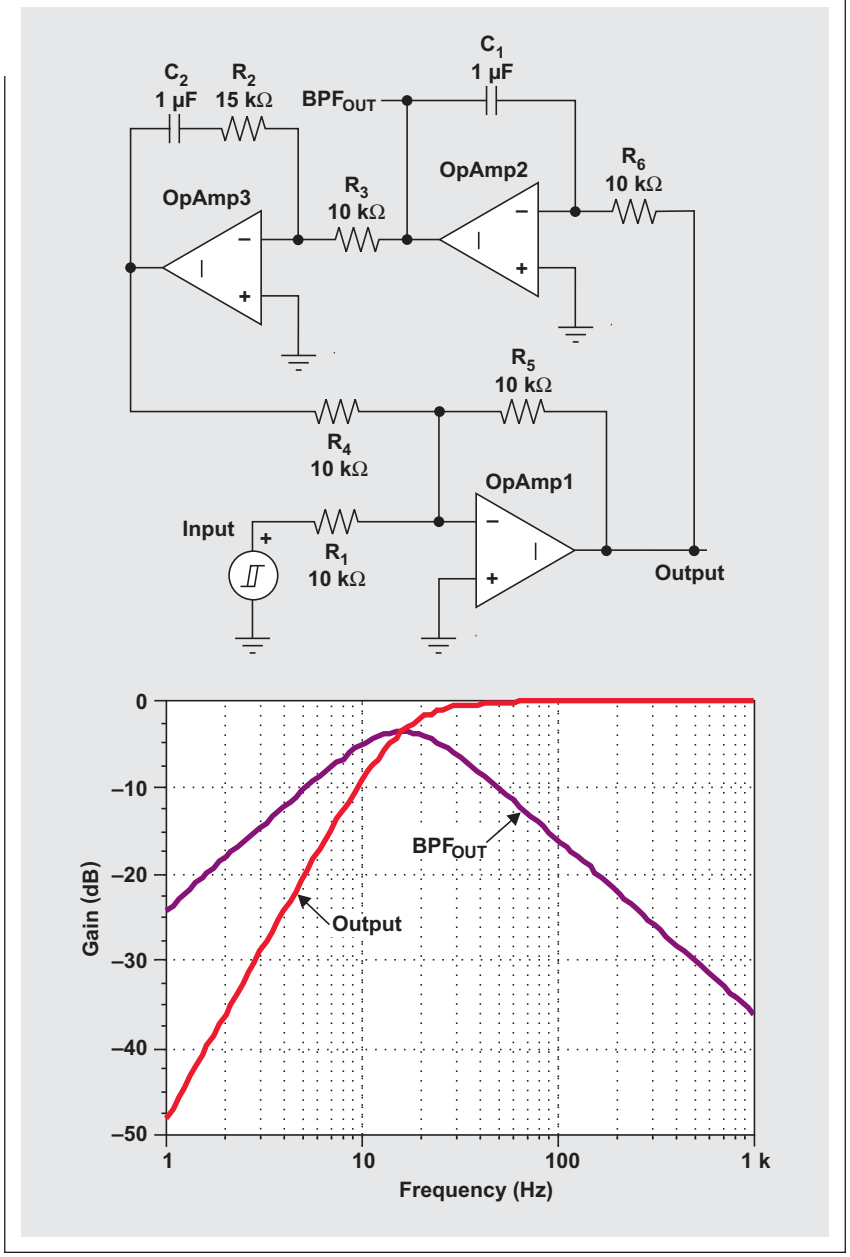
$$f_0 = \frac{1}{2\pi\sqrt{C_1C_2R_3R_6\frac{R_4}{R_5}}}, \quad (4)$$

$$\text{and } Q = \frac{1}{R_2}\sqrt{\frac{R_4}{R_5}R_3R_6\frac{C_1}{C_2}}. \quad (5)$$

Using sensitivity analysis as covered in References 2, 5, 6, and 8, we find that, as with the KHN and TT filters, all sensitivities of f_0 or Q to the passive components are 1 or lower. It is quite difficult to get lower sensitivities.

Of course, this filter could be used as a separate filter block like any other HPF topology. In the first example given earlier, we could add a three-op-amp circuit like this to the front of the gain block/filter section and another following the filter. In this case, our new HPF topology would have no real advantage over the KHN filter, and the only

Figure 5. Transfer functions for the new filter



advantage it would have over any other common topology is that it can implement an HPF with no capacitors in the forward signal path.

The unique feature that this filter provides is that it is easily applied around a gain block to add a high-pass function without putting any additional circuitry in the forward signal path. Later we will see that there is a variation of this circuit that works with an inverting amplifier while feeding back to the non-inverting terminal, and that there are other variations that work with non-inverting gain blocks. All of these variations feed back to only one input.

Applying this technique to a non-inverting amplifier

If the gain block to which we want to add a high-pass function is non-inverting, we can use the variation of the topology shown in Figure 6.

The transfer function for this circuit, Equation 6, is identical to that of the circuit in Figure 5, except that the gain term is $(R_4 + R_5)/R_4$ rather than $-R_5/R_1$:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_4 + R_5}{R_4} \frac{S^2 C_1 C_2 R_3 R_6 \frac{R_4}{R_5}}{S^2 C_1 C_2 R_3 R_6 \frac{R_4}{R_5} + S C_2 R_2 + 1} \quad (6)$$

Since the rest of Equation 6 is the same as Equation 3, the pole frequency and Q for this HPF variation are also given by Equations 4 and 5.

Maintaining gain-bandwidth product with an inverting amplifier

In Figure 5 we demonstrated this filter technique for an inverting amplifier. Note that both the input signal and the feedback signal are applied to the inverting terminal via R_1 and R_4, respectively. While the addition of R_4 to add the HPF feedback has no effect on the nominal forward gain for the gain block, it does increase the division ratio of the feedback path of the gain block from

$$\frac{R_1}{R_1 + R_5} \text{ to } \frac{R_1 \| R_4}{R_1 \| R_4 + R_5}, \quad (7)$$

where $R_1 \| R_4$ represents that R_1 is parallel to R_4. This change in local feedback around op amp 1 has the effect of decreasing the effective gain-bandwidth product (GBWP) of the op amp by the same amount. In our case, $R_1 = R_4$, which means the GBWP will be decreased by 33%.

For an inverting amplifier, rather than feeding back to the inverting terminal as in Figure 5, we can feed back to the non-inverting terminal, thus avoiding decreasing the effective GBWP of the op amp. Figure 7 shows this variation.

Notice that R_2 is missing in this configuration. Recall that R_2 was needed to add a zero to the feedback path, which allowed the Q to be set to a reasonable value; without R2, the Q of the circuit would always be very high. In this circuit we get a zero by reconfiguring the op amp 3 stage from inverting to non-inverting. This reconfiguration was

Figure 6. Applying the technique to a non-inverting amplifier

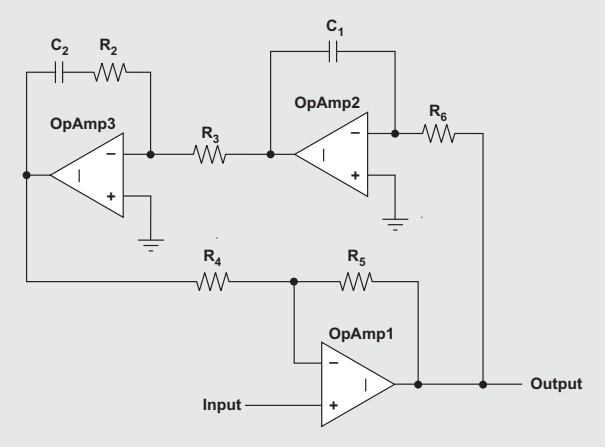
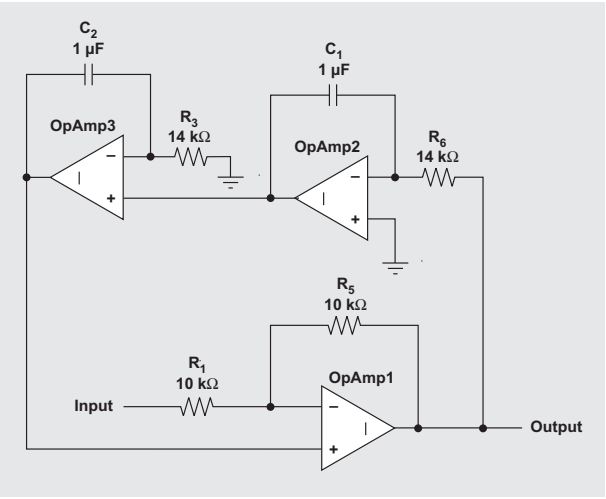


Figure 7. Inverting amplifier with feedback to non-inverting terminal



necessary to keep the feedback negative. The resulting transfer function, along with the pole frequency and Q, are respectively given by

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_5}{R_1} \frac{S^2 C_1 C_2 R_3 R_6 \frac{R_1}{R_5 + R_1}}{S^2 C_1 C_2 R_3 R_6 \frac{R_1}{R_5 + R_1} + S C_2 R_3 + 1}, \quad (8)$$

$$f_0 = \frac{1}{2\pi \sqrt{C_1 C_2 R_3 R_6 \frac{R_1}{R_5 + R_1}}}, \quad (9)$$

$$\text{and } Q = \sqrt{\frac{R_1}{R_1 + R_5} \frac{R_3}{R_6} \frac{C_1}{C_2}}. \quad (10)$$

With this configuration there is no component that can independently set the Q. Also, since R_1 and R_5 set the gain of the forward amplifier, we cannot use them to set the pole frequency or the Q. Instead, C_1, C_2, R_3, and R_6 have to be manipulated to set both the pole frequency and the Q. Fortunately, f_0 is a function of the product of these four component values, while Q is a function of the ratio of the resistors and the ratio of the capacitors. These mathematical relationships make it fairly easy to choose the right component values. We can simply set $R_3 = R_6$ and $C_1 = C_2$, then choose their values to set f_0. Then the desired Q can be set by altering the ratio of the resistors and/or the capacitors while keeping their products constant.

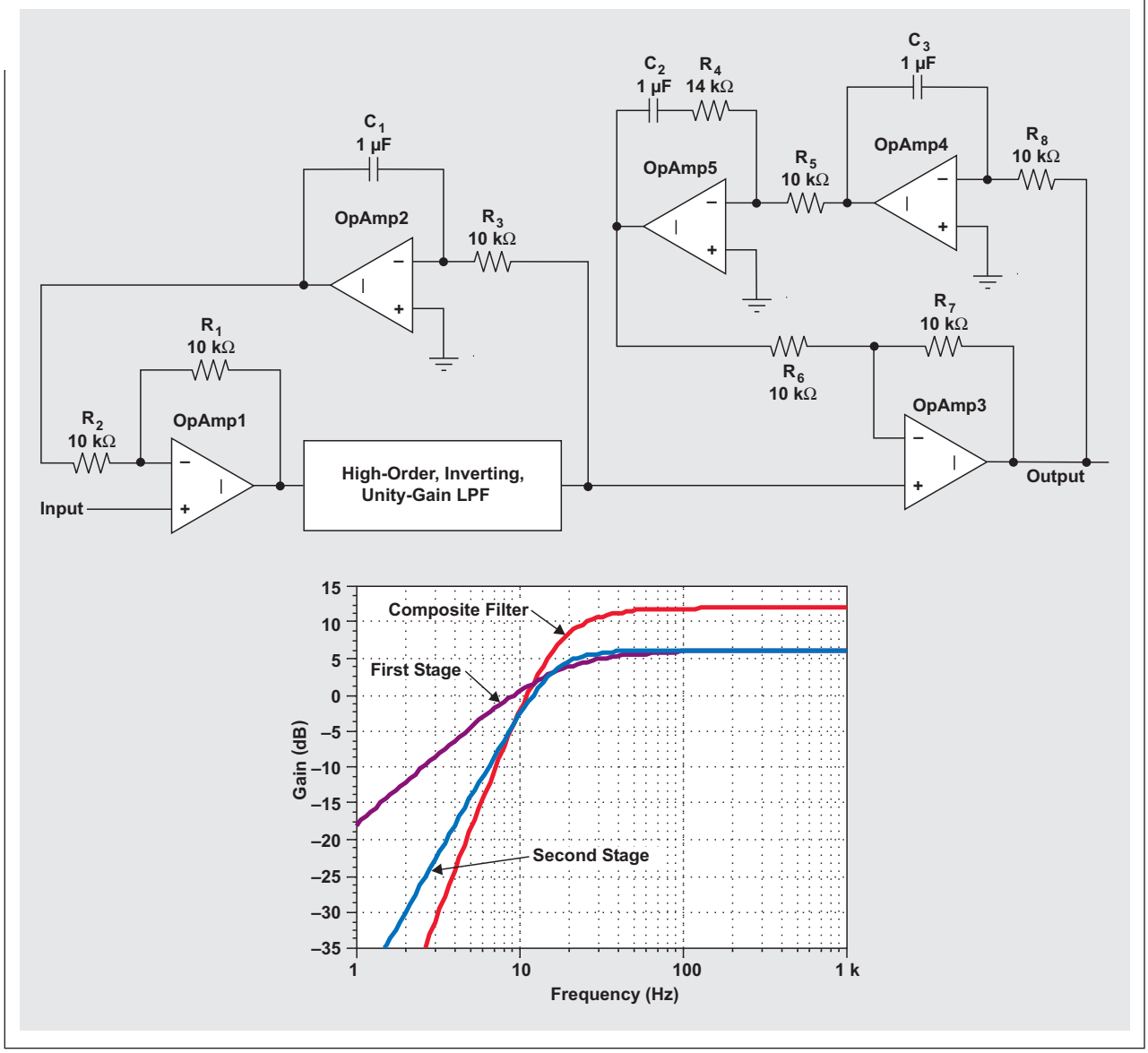
Implementing higher-order HPF functions

Since the new second-order filter topology and the older first-order servo technique can both be used to wrap a high-pass function around a gain block and/or an LPF function, we can use any number of these in a signal chain to create a composite HPF function of any practical order we want.

Figure 8 shows how we have created a third-order filter by combining the first-order servo feedback HPF function from Figure 5 with the second-order circuit from Figure 7.

While many DC-blocking applications can be readily handled with the insertion of capacitors in the signal path, and many others can be satisfied with older circuit topolo-

Figure 8. Combining two sections for a third-order HPF



gies, the first-order servo feedback HPF and the new second-order HPF we have described can provide a great advantage in some applications due to their unique features. These features include the ease of adding to gain/LPF blocks without adding circuitry in the signal path or modifying the gain/LPF blocks, and the ability to implement HPF functions without capacitors in the signal path. The combination of the two topologies provides the ability to implement HPFs of higher orders while maintaining these advantages.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
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