Accurately Measuring ADC Driving Circuit Settling Time

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ABSTRACT

Many modern data acquisition systems consist of highspeed, high-resolution ADCs.(1) CMOS-switched, capacitorbased ADCs are often chosen for such designs due to their low cost and low power dissipation. These ADCs use an unbuffered front end directly coupled to the sampling network. To effectively minimize noise and signal distortion, it is necessary to drive the ADC with a high-speed, lownoise, low-distortion operational amplifier.(2) To achieve minimal distortion it is important for the op amp output to settle to the desired accuracy within the acquisition time of the ADC. Normally the op amp settling time is either calculated from the frequency response specified in the datasheet or measured by probing the output with an oscilloscope that has a limitation on resolution. Sometimes the difference between the op amp input and output is amplified to achieve better accuracy. These methods are limited by the oscilloscope resolution or circuit parasitic. Moreover, the settling time of the op amp is affected by the parasitic capacitance and inductance introduced by the oscilloscope probe. In another method, the difference between output and input is amplified to increase the resolution of the measurement. None of these methods includes the parasitic capacitance and inductance present in the ADC sampling circuit and package.

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1 Definition of Settling Time

Settling time is the time elapsed from the application of an ideal instantaneous step input to the time at which the closed-loop amplifier output has entered and remained within a specified symmetrical error band. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slewing, and finally settle to within the specified error. For high-resolution ADCs, the specified error band is usually one fourth of one least significant bit (LSB) of the ADC.

2 Basic Setup

The ADC used here is the Texas Instruments (TI) ADS8411, which is a 16-bit, 2-MSPS successive approximation register (SAR) ADC. The driver op amp is the TI THS4031. Figure 1 shows the evaluation setup.

The instantaneous step input is generated with an analog multiplexer (MUX) (the TI TS5A3159) by switching its two channels. A dc voltage, V, is applied to channel 2, and channel 1 is connected to ground; so this setup can produce a step input rising to V from 0 or falling to 0 from V. Alternatively, the step input can be generated from any step generator. The step generator should settle much faster than the op amp settling time.

2.1 Explanation

Step 1

ADC samples channel 1 (connected to ground) first. A long sampling time is provided to make sure that the input capacitor of the ADC is fully discharged.

Step 2

The analog MUX is switched to channel 2 from channel 1 at instant A in Figure 2. This diagram shows the voltage at point S (Figure 1) when the MUX switches over to channel 2 from channel 1. The settling time of the MUX is denoted by ts. It is assumed that ts is much shorter than the op amp settling time.

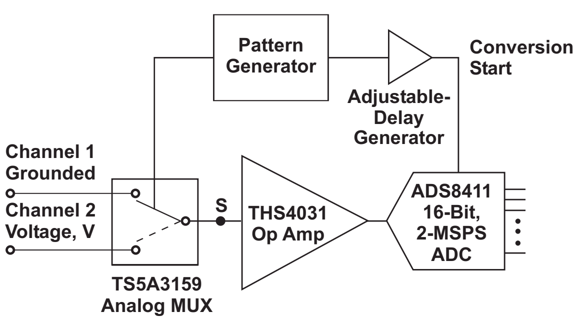

Figure 1. Settling Time Evaluation Setup

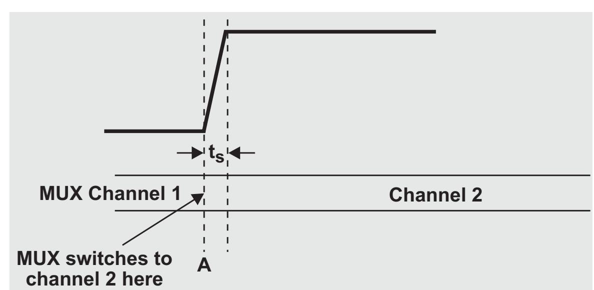

Figure 2. Settling Time for MUX Channel Change

Step 3

Once the analog MUX is switched at instant A, the input of the op amp starts changing. The output of the op amp starts changing after a very brief propagation delay after instant A. The op amp settling time (tideal) is approximately calculated from the slew rate and bandwidth specified in the op amp datasheet. The method proposed here plots the op amp output from instant A to instant B (Figure 3). The time difference between instant B and instant A is $2t_{ideal}$.

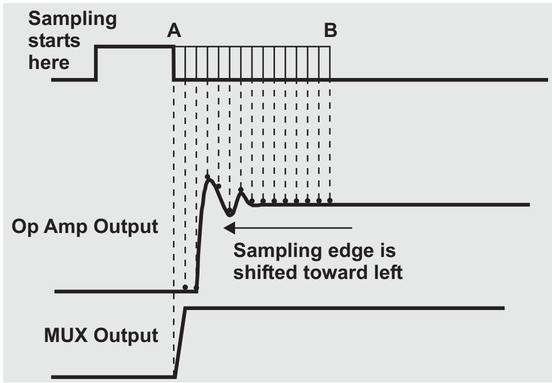

Figure 3. Averaging n Samples from B to A Increases Accuracy

Step 4

The first ADC sampling edge appears at instant B, and n number of readings (digital outputs from the ADC) are taken. The n number of readings are averaged for better accuracy (discussed later). Next the sampling edge is shifted to the left by 1 ns (Figure 3) with the help of a pattern generator and an adjustable-delay generator (Figure 1), and again n number of readings are taken. This way the sampling edge is shifted toward the left from instant B to instant A in 1-ns steps. At each sampling edge the average is stored in an element of an array. The array is plotted against the time to get the true picture of the op amp output settling (Figure 3).

2.2 Averaging to Achieve Better Resolution

Input of an n-bit ADC should settle to at least n+2 bits, but measured output is an n-bit digital code from the ADC. The resolution can be increased by repeatedly sampling the same input and taking multiple (n) readings from the ADC. Finally an average is taken on the n digital output codes. It can be shown that for each additional bit of resolution, the number of readings should be 4, so w extra bits of resolution require 4^w readings.

For each additional bit, the signal-to-noise ratio (SNR) increases by 6.02 dB. In this case the 16-bit ADC should settle with at least 18-bit accuracy.

$$SNR = 6.02 \times N + 1.76,$$

where N is the ADC resolution. SNR is 110.08 dB for 18-bit accuracy, so an extra bit (w) of resolution required is:

$$110.08 – 86^* / 6.02 = 4$$

* Typical SNR specification of ADS8411

The number of samples (n) needed for each reading is 44 = 256.

2.3 Results

An RC filter is used at the output of the op amp to filter the external noise. An ADC sampling circuit always consists of another RC (R′, C′), as shown in Figure 4.

Figure 5 shows the settling behavior when three different values of an external capacitor are used for RC filtering.

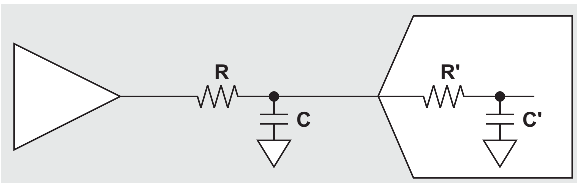

Figure 4. Typical Noise Filter

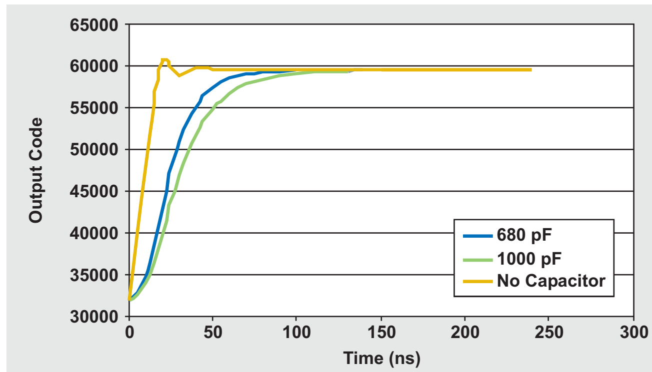

Figure 5. Input Settling Time With an External Capacitor

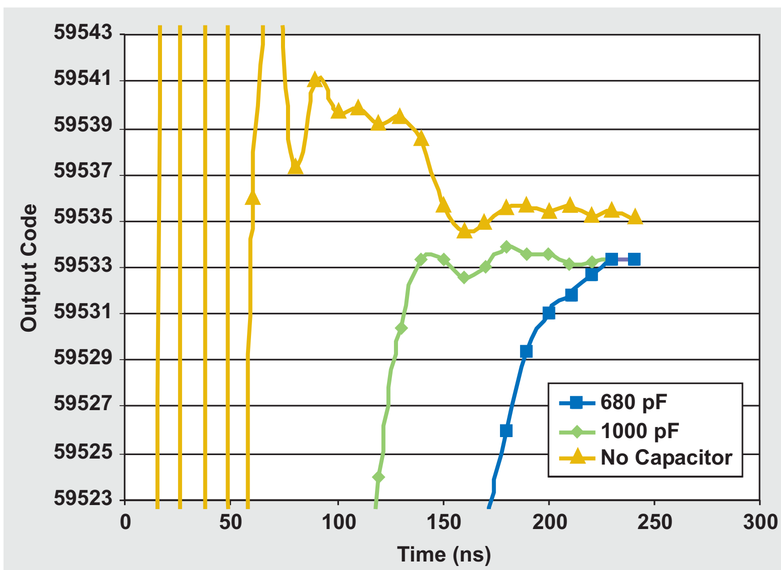

Figure 6. Expanded Scale Magnifies Settling-Time Behavior Shown in Figure 5

Figure 6 is a zoomed-in version of Figure 5 to show the settling more accurately. While the output code is based on 16-bit sampling, the resolution of the measurement is more than 16-bit because 65536 samples were captured and averaged for each reading. The result shows significant ringing and underdamping of the system when no capacitor was used. Also note that use of a bigger (1000-pF) capacitor significantly increases the settling time.

A summary of these results is shown in Table 1. Averaging the output data can improve the resolution of the result beyond 16-bit.

Table 1. Comparison of Edge-Shift Method Versus Traditional Method

Method		Capacitor, C (pF)	Accuracy* (%)	Settling Time (ns)
Datasheet Specification	10-Bit	No Spec	0.1	45
	13-Bit		0.01	80
Edge-Shift Method (R = 20 Ω)		25	0.1	55
			0.01	140
			0.0015	150
		680	0.1	109
			0.01	130
			0.0015	140
		1000	0.1	152
			0.01	195
			0.0015	220

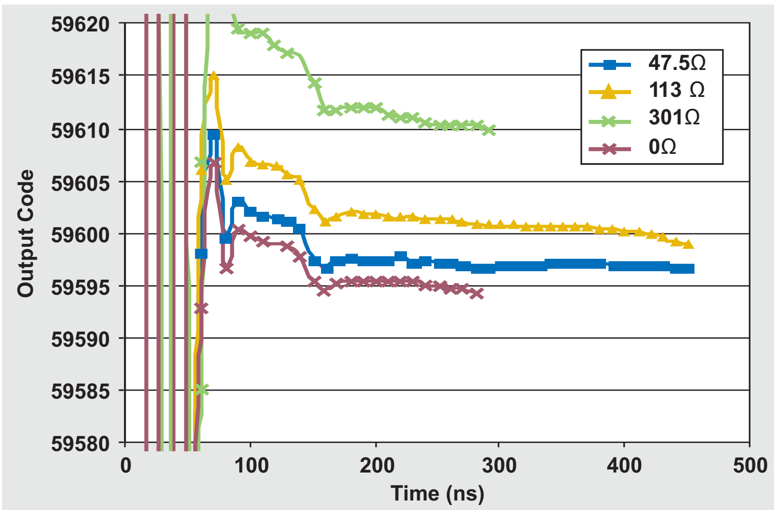

Figure 7. Effects of Changing Feedback Resistors

3 Measurement of Bias Current

Figure 7 shows op amp settling behavior with different values of feedback resistors. The difference between the settled voltages indicates the offset voltage shift caused by bias current. From this the bias current can be calculated as 3 µA, which matches the typical specification of the THS4031. This experiment validates the correctness of this setup.

4 Bias Current Calculation

The settled value with 0 Ω in the feedback is 59595. The settled value with 301 Ω in the feedback is 59610.

Delta (offset voltage) = bias current × resistor

(used in the feedback).

$$\text{Delta (Offset Voltage)} = \frac{(59610 \times 59595) \times 4.096}{65536} = 938\ \mu\text{V}$$

$$\text{Bias Current} = \frac{938}{301} = 3.12\ \mu\text{A}$$

(compared to the datasheet typical specification of 3 μA).

5 Conclusion

This is a practical and simple method to accurately measure the settling time of an ADC driving circuit. The settling behavior is unaffected by the measurement, because no additional component is used for the setup. This method can be implemented as a built-in self-test (BIST) in the future. The averaging of multiple readings improves the accuracy of the result.

6 References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace "litnumber" with the TI Lit. # for the materials listed below.

6.1 Document Title

1. Kevin M. Daugherty, Analog to Digital Conversion: A Practical Approach (McGraw-Hill Companies, 1993).
2. Ron Mancini, ed., "Op Amps for Everyone," Design Reference (Rev B) (SLOD006)

6.2 Related Web sites

amplifier.ti.com

http://www.ti.com/product/*partnumber*

Replace partnumber with ADS8411, THS4031, or TS5A3159.

Revision History

Changes from Original (Month Year) to A Revision	Page
• Changed document format to current application reports standard.	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.