User's Guide

SLWU052A – December 2007 – Revised September 2008

TSW4100EVM

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1 Introduction

The TSW4100 contains a signal chain consisting of an ADC, DDC, DUC, and DAC to create a repeater application. The design has a clock distribution solution, and an interface for programming and reading programmable devices on the TSW4100 with a PC. In addition to the interfaces, the TSW4100 provides test connectors, which can be used to monitor the RX outputs or provide inputs to the TX portion of the chain.

The TSW4100 requires only a single 5-6 V DC power source at 3 A to operate.

The block diagram of the TSW4100 is shown in Figure 1.

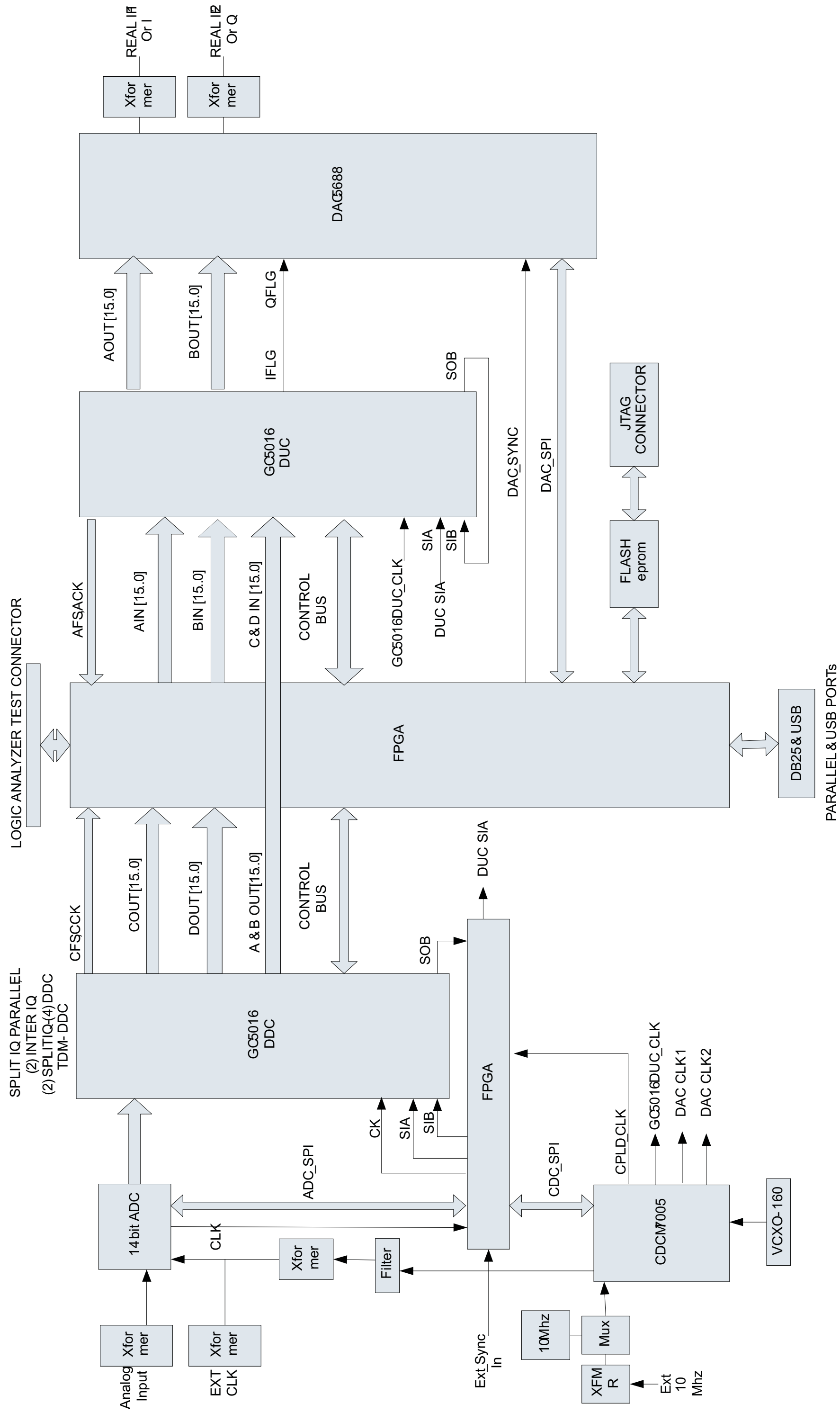


Figure 1. TSW4100 Block Diagram

2 TSW4100 Interfaces

2.1 USB Port J26

USB port connector J26 provides a PC interface to allow writes and reads between a PC/Laptop and the FPGA and the two GC5016 (SLWS142) devices. This interface helps program the two GC5016 devices with existing software provided by TI. The parallel port connector provides the same functionality when configured. The default TSW4100 configuration has the USB port enabled and leaves the parallel port disabled.

2.2 USB Connector J25

USB connector J25 provides a PC interface to allow writes and reads between a PC/Laptop and the DAC5688 and the CDCM7005 (SCAS793) devices. There is an option to allow this interface to write to the ADS5545 (SLWS180) device when configured for serial interface, but the board has this part configured for parallel interface mode. With this configuration, the part operation is determined by jumpers.

3 Hardware Configuration

By using the provided software and on-board jumpers, the TSW4100 can be set up in a variety of configurations to accommodate a specific operation mode. Before starting evaluation, the user should decide on the configuration and make the appropriate connections and load the appropriate parameters for the GC5016's, DAC5688, ADS5545, and CDCM7005 devices.

3.1 Power Requirements

The TSW4100 requires 5V-6V DC at approximately 3.0 Amps. The board contains several on-board regulators that generate the necessary voltages from the 5V-6V DC source The board provides banana jacks J4 (red) and J5 (black) for use with a separate power supply. When using this mode, connect 5V-6V DC to J4 and the return to J5.

3.2 Jumper Settings

The board jumper description and default settings are shown in Tables 1, 2, and 3. Details of the software operation modes can be found in the software section of this document. Table 1, Table 2, and Table 3 explain the functionality of the board jumpers.

Table 1. Two Pin Jumper List

Jumper	Function	Installed	Removed	Default
J7	DUC clock input test point	N/A	N/A	N/A
J10	DDC clock input test point	N/A	N/A	N/A
J18	Sets Parallel port J2 interface device drive mode	Open drain	Totem pole	Removed
J19	Used to disable VCXO U19 when providing external oscillator at J20	Enables U19	Disables U19	Installed

Table 2. Three Pin Jumper List

Jumper	Function	Location: Pins 1-2	Location: Pins 2-3	Default
JP7	CDCM7005 reference select	Reference clock provided by J21	Reference clock provided by Y1 or Y2	2-3
JP5	CDCM7005 complimentary clock	input select Clock provided from VCXO U19	Input connected to VBB of CDCM7005	1-2
JP6	CDCM7005 clock input select	Clock provided from VCXO U19	Input clock provided from J20	1-2
JP1	ADS5545 output enable	Output enabled	Output disabled	1-2
SJP3	ADS5545 output clock direction	Sends output clock to DDC	Sends output clock to FPGA	1-2

Table 2. Three Pin Jumper List (continued)

Jumper	Function	Location: Pins 1-2	Location: Pins 2-3	Default
SJP11	ADC input clock select	Provides clock from CDCM7005 to T5	Provides clock from SMA connector J13	removed
JP4	ADC clock buffer enable	Disables ADC clock buffer U14	Enables ADC clock buffer U14	2-3
J17	Selects cable side operation voltage of U6 for parallel port J2	Sets VCAB to +3.3V	Sets VCAB to +5V	2-3
JP12	Selects signal path for DAC5688 CLK1B Connects	CDCM7005 output Y1A to DAC CLK1CB	Connects DAC CLK1CB to LED D9.	1-2
JP13	Selects signal path for DAC5688 CLK1	Connects CDCM7005 output Y1B to DAC CLK1C	Connects DAC CLK1C to FPGA.	1-2
SJP9	DDC input clock select	ADC output clock to DDC	FPGA output clock to DDC	1-2
SJP8	DUC input clock select	FPGA output clock to DUC	CDCM7705 output clock to DUC	1-2
SJP1	Selects +5V source for USB controller U24	+5V sourced from board.	+5V sourced from USB cable.	1-2
SJP2	Selects +5V source for USB controller U21	+5V sourced from board.	+5V sourced from USB cable.	1-2

Table 3. Jumper J15 List

Jumper	Function	Location = +3.3V	Location = GND	Default
PLL_VDD	Sets logic value of SYNC pin of DAC5688	Sets SYNC to GND	Sets SYNC to +3.3V	1-2
Sleep	N/A	N/A	N/A	Not Used
EXT_LO	Sets logic value of EXTLO pin of DAC5688	Sets EXTLO to GND	Sets EXTLO to +3.3V	7-8
TXENABLE	Sets logic value of TXENABLE pin of DAC5688	Sets TXENABLE to GND	Sets TXENABLE to +3.3V	11-12
CDC_PD	Sets logic value of Power Down pin of CDCM7005	Sets $\overline{PD}$ to GND	Sets $\overline{PD}$ to +3.3V	14-15

3.3 Apply Power to Board

The TSW4100 contains an Altera EP2C8 Cyclone II™ FPGA (U10) and an Altera EPCS4™ reprogrammable serial configuration PROM. The EPCS4 is pre-programmed to a default configuration. To prepare the board for operation:

1. Plug in the provided power supply to connector J3 and the other end to +110 VAC.
2. Press the DAC RESET switch SW5 on the TSW4100 board.
3. Ensure the FPGA is configured by verifying the D2 LED is on.
4. Verify the CDCM7005 VCXO and reference clock are present (D4 and D5 LEDs are on).

4 Software Installation

This section describes the software installation procedures needed to operate the TSW4100:

- Section 4.1 Installing the TSW4100 interface to the GC5016 CDC and DAC Software
- Section 4.2 Installing the USB Driver Software
- Section 4.3 Installing the MATLAB Runtime Engine
- Section 4.4 Installing the TSW4100GUI Software

4.1 Installing the TSW4100 Interface to GC5016 CDC and DAC Software

The TSW4100 uses a modified version of the existing DAC5688 EVM LabView software program for writing and reading to the DAC5688 and CDCM7005. This software is separate from the TSW4100 software used to design and load GC5016 filter configurations.

Note: Once all software is loaded, TI recommends the host computer be restarted. This software has been verified to be functional for the Windows 2000 and Windows XP operating systems.

1. Copy the folder **TSW4100_DAC_CDC_Installer** found on the TSW4100 Installation CD-ROM to a temporary directory on the host PC.
2. Double-click the **setup.exe** filename found under this directory.
3. Follow the standard Windows Installation procedure that includes accepting the License Agreement and using the default installation directory.

CAUTION

Do not start the software after completing the installation.

4.2 Installing the USB Driver Software

The USB interface adapter provides an additional, dedicated PC IP address to connect to the TSW4100 IP address. To install this adapter:

1. Plug in one of the USB cables between J25 of the TSW4100 board and a PC. The software should recognize the connection and ask for drivers.
2. After the *Welcome to the Found New Hardware Wizard* message displays, select the *No, not at this Time* option.
3. Select the *Install from a list or specific location (advanced)* option.
4. If asked, click on the *Don't' search. I will choose the driver to install* option.
5. If a window opens with the following driver name *Texas Instruments TSW4100 DAC and CDC Controller*, select this then click next. If this does not appear, navigate to the **C:\Program Files\TSW4100_DAC_CDC\TSW4100 Drivers** directory.
6. Click *Open*.
7. The software loads the drivers in this directory. When prompted, select the *Continue anyways* option.
8. Complete the USB driver installation. If the driver cannot be found, click on the option *Don't search. I will choose the driver to install*. Click *Next*.
9. A new widow should open with a couple of options to choose from. Select *TSW4100 DAC and CDC Controller*. Click *Next*.
10. Repeat steps 6 and 7. This completes the TSW4100 DAC and CDC driver installation.
11. Copy the folder **TSW4100_GC5016 Drivers** found on the *TSW4100 Installation CD-ROM* to a temporary directory on the host PC.
12. Plug in the other USB cable between J26 of the TSW4100 board and a PC. The software should recognize the connection and ask for drivers.
13. After the *Welcome to the Found New Hardware Wizard* message displays, select the *No, not at this Time* option.
14. Select the *Install from a list or specific location (advanced)* option.
15. Navigate to the **TSW4100_GC5016 Drivers** directory.
16. Click *Open*.
17. The software loads the drivers in this directory. When prompted, select the *Continue anyways* option.
18. Complete the USB driver installation.

4.3 Installing the MATLAB Runtime Engine

This section helps you install the MATLAB Runtime engine which is used to run the provide MATLAB executable code.

1. Double-click on the *MCRInstaller.exe* file located on the TSW4100 installation CD. The Choose Setup Language (Figure 2) displays. Click *OK* for English (United States).

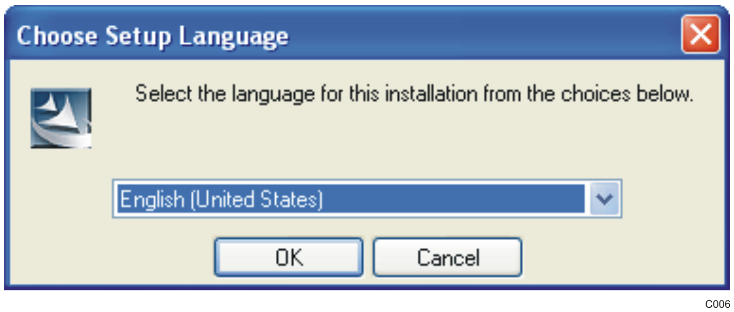


Figure 2. Choose Setup Language

2. When the *MATLAB Component Runtime 7.5* screen (Figure 3) displays, click *Next*.

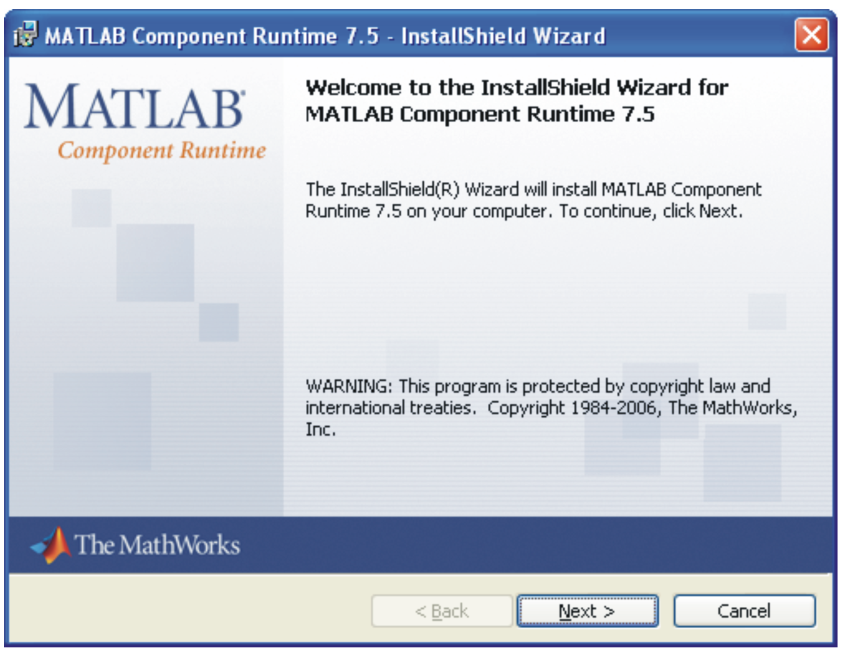
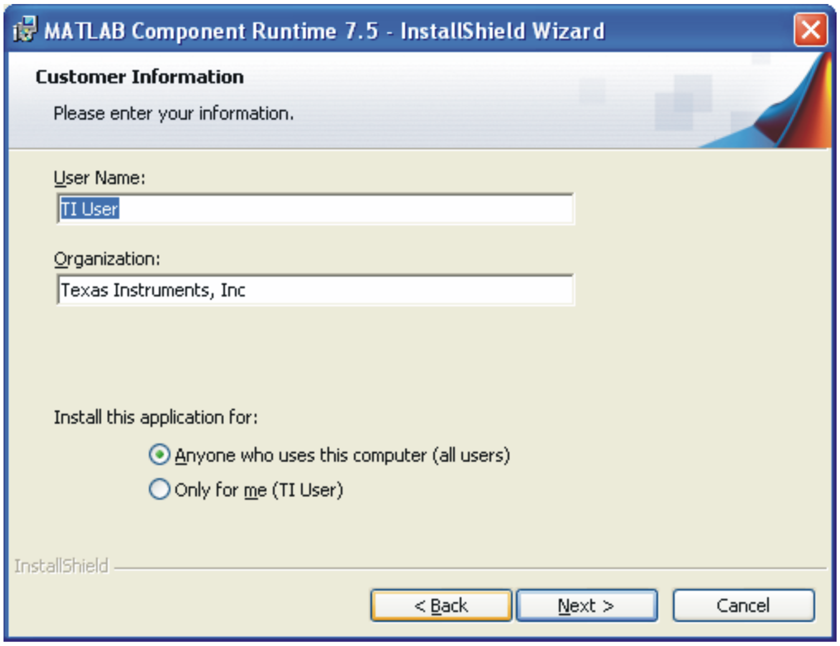


Figure 3. MATLAB Welcome Screen

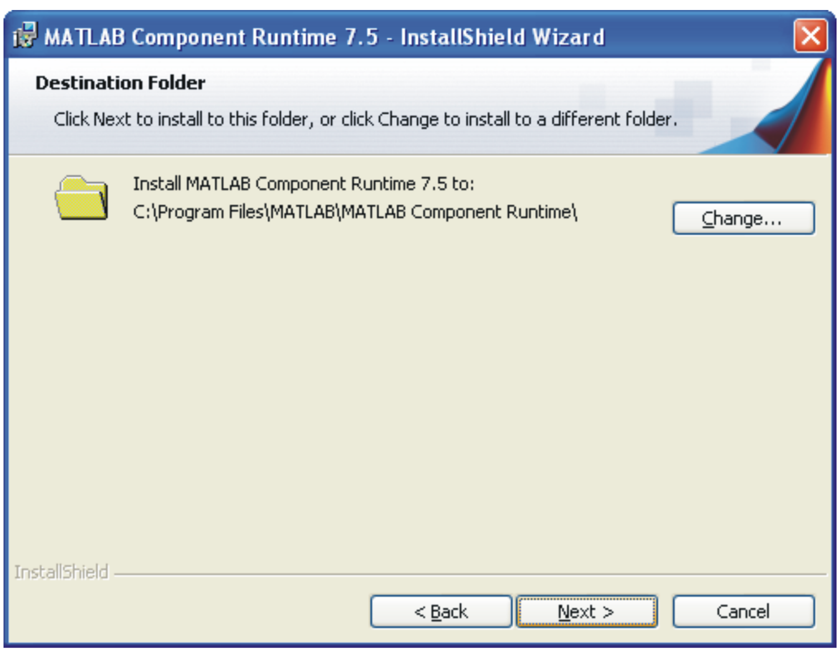
3. For the *Customer Information* (Figure 4) screen, specify the *User Name*, *Organization*, select the desired user option button, and click *Next*.



C008

Figure 4. Customer Information

4. When the *Destination Folder* screen (Figure 5) displays, click *Next* to install the MATLAB software in the default directory.



C009

Figure 5. Destination Folder

5. When the *Ready to Install the Program* screen (Figure 6) displays, click *Install* to begin the installation. The installation lasts approximately five minutes.

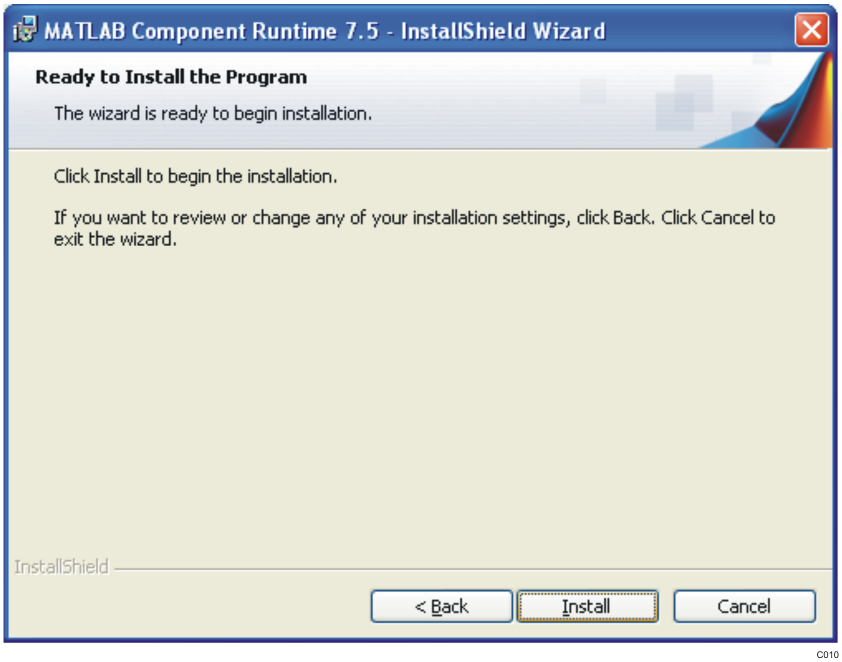


Figure 6. Ready to Install the Program

6. Click *Finish* once the *InstallShield Wizard Completed* screen (Figure 7) displays.

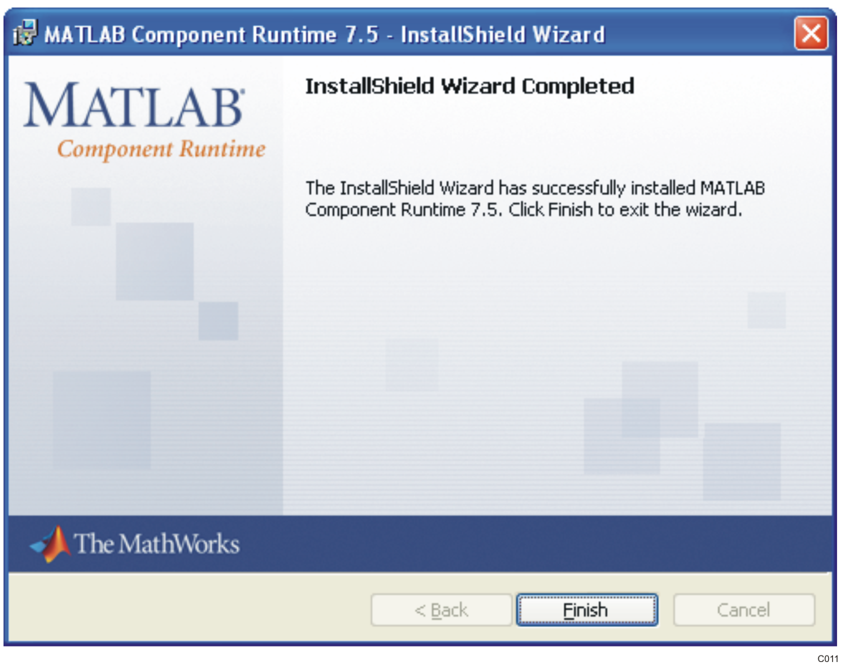


Figure 7. InstallShield Wizard Completed

4.4 Installing the TSW4100GUI Software

1. Double-click the *TSW4100GUIInstaller.exe* filename found in the top-level folder of the TSW4100 Installation CD-ROM. The TSW4100 Installation Wizard (Figure 8) displays. Click *Next*.

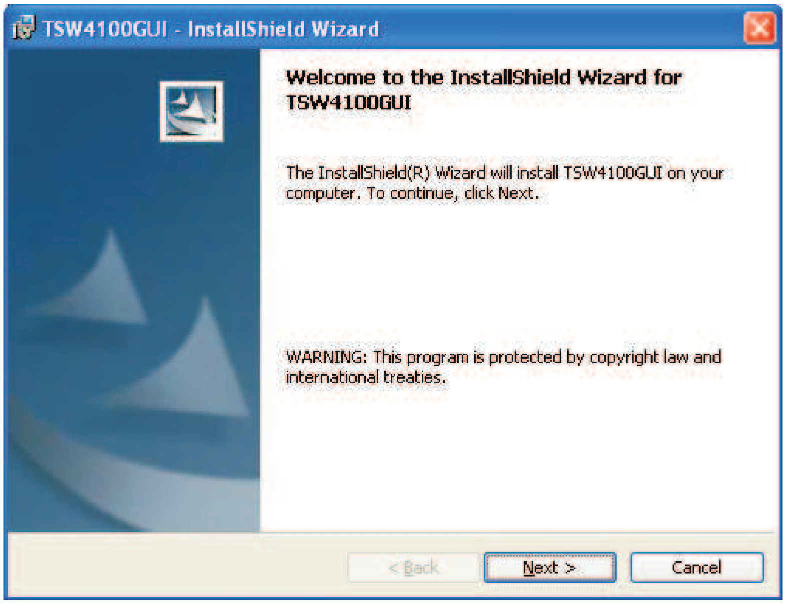


Figure 8. TSW4100 Installation Welcome

2. When the License Agreement (Figure 9) displays, select the *I accept the terms in the License agreement* option and click *Next* to accept the TSW4100 Software License Agreement.

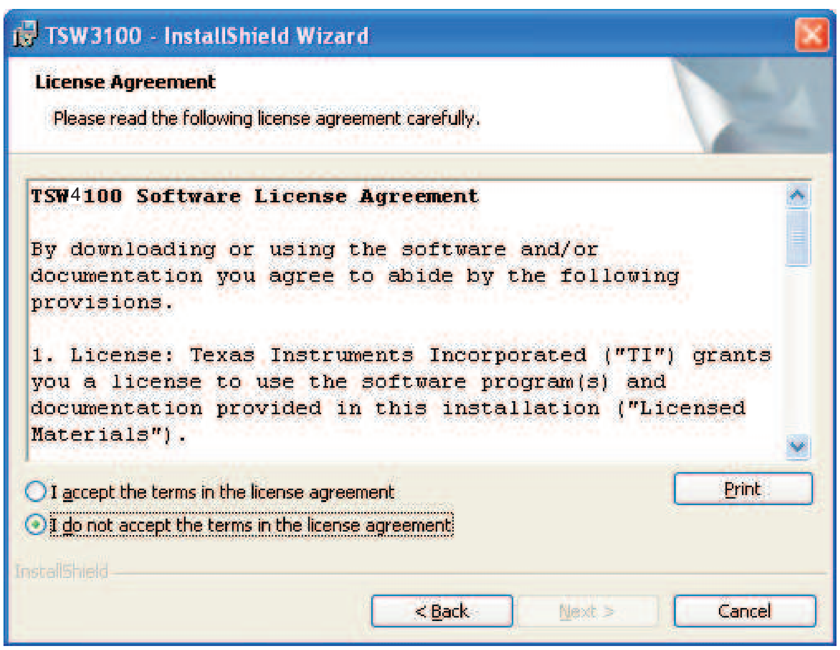


Figure 9. TSW4100 License Agreement

3. On the Customer Information (Figure 10) screen, provide *User Name*, *Organization* information, and select the appropriate *Install this Application for* option. Click *Next*.

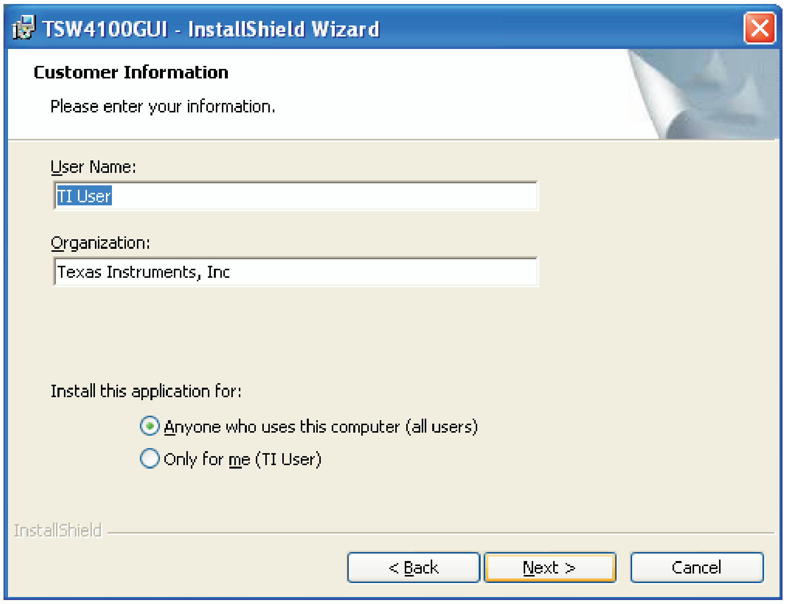


Figure 10. Customer Information

4. On the Setup Type (Figure 11) display, select the *Complete* Setup Type option and click *Next*.

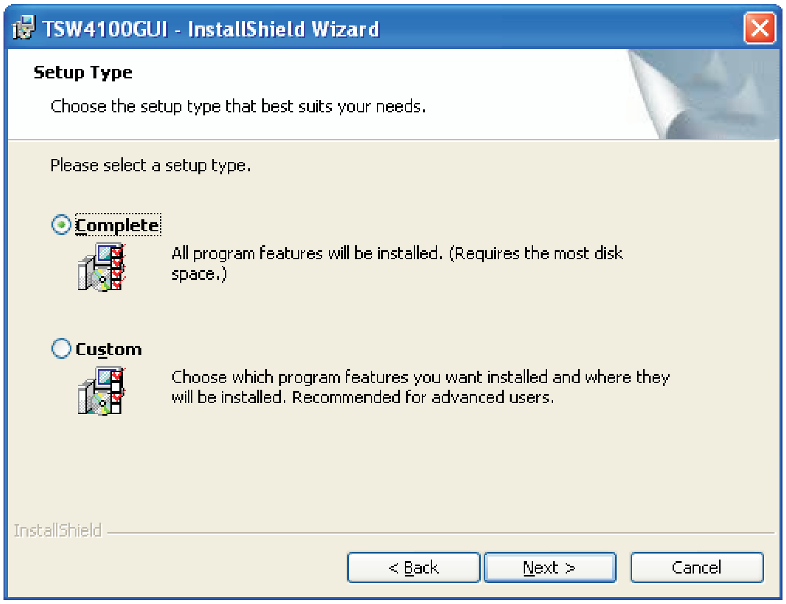


Figure 11. Setup Type

5. On the Ready to Install the Program (Figure 12) display, click *Install*. The installation takes between one and three minutes to complete.

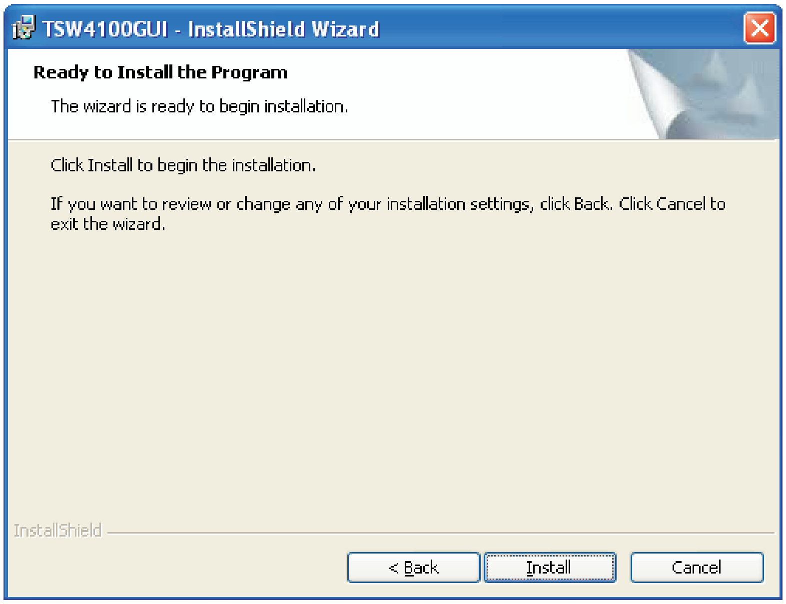


Figure 12. Ready to Install the Program

6. Click *Finish* once the InstallShield Wizard Completed screen (Figure 13) displays.

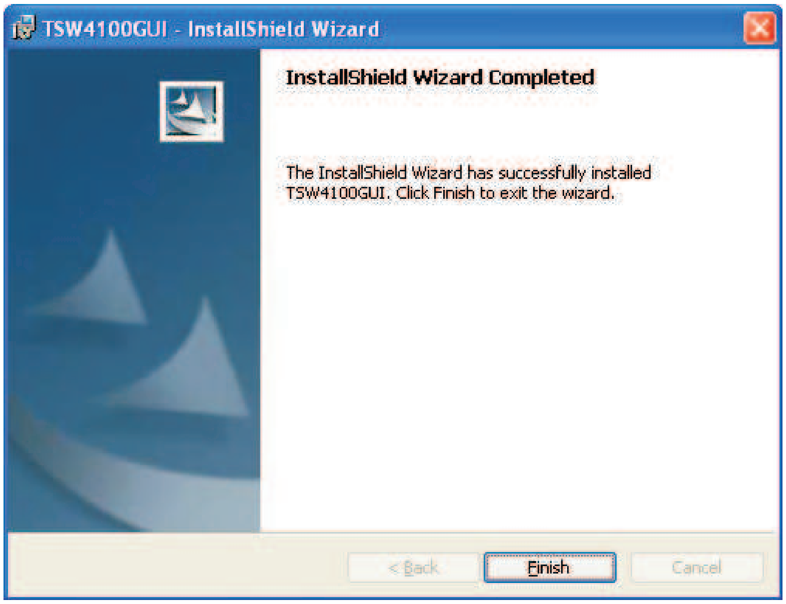


Figure 13. InstallShield Wizard Completed

5 Running the TSW4100 CDC and DAC Interface

5.1 *Starting the TSW4100 Interface*

The TSW4100 software is now ready to use. To start the application program, click the Windows menu sequence **start** → **All Programs** → **Texas Instruments TSW4100 DAC and CDC Control** → **TSW4100 DAC and CDC Control** (Figure 14).

Note: Click *OK* if a warning message about Internet connections is received. This provides a link for the current TSW4100 data sheets on the TI Internet Site. Unplug and plug the USB connector if necessary. The user may need to click the *USB Reset* button (on the left side of the GUI) to reinitialize the USB connection.

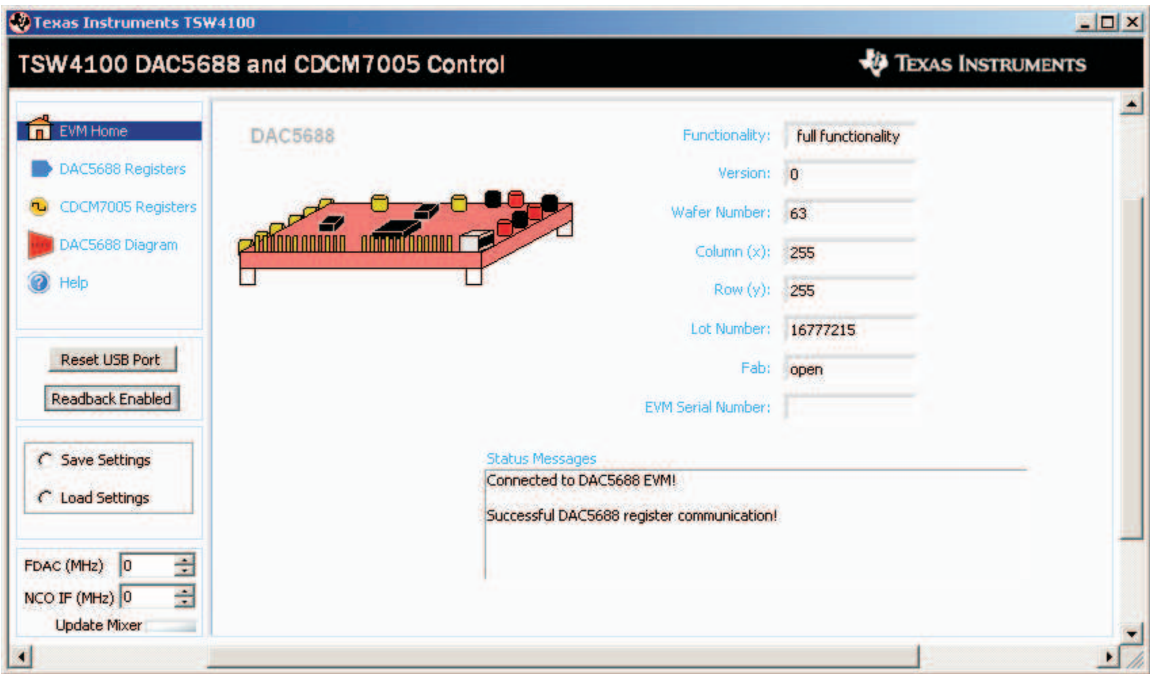
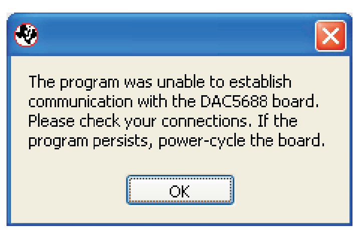


Figure 14. TSW4100 CDC/DAC Graphical User Interface



If the error message *DAC5688 EVM not detected* is displayed, indicating that the host is unable to communicate with the DAC5688, perform these actions:

1. Press the DAC RESET switch SW5 on the TSW4100 board.
2. Click the *Read All* button on the *DAC5688 Registers* window.
3. Click *Reset USB* button on the left side of the TSW4100 DAC CDC GUI.
4. If this does not fix the problem, reboot the host computer. If the problem still exists, uninstall the software and any other TI software such as the DAC5688 or TSW3003 if it exists on the computer. Re-install the TSW4100 DAC CDC software.

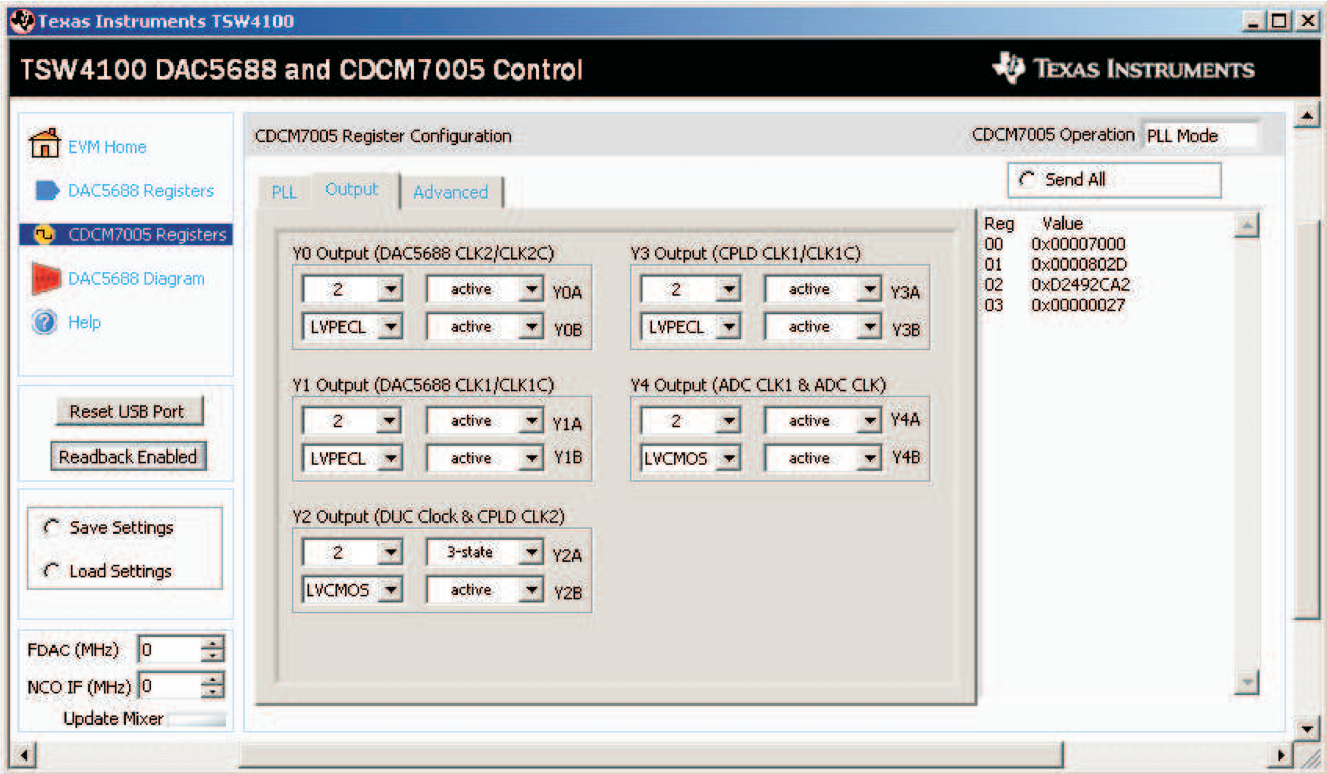


Figure 15. CDCM7005 Interface

5.2 Loading the CDCM7005 with Default Values

By using the provided CDCM7005 serial peripheral interface (SPI) software, the user can load settings to the CDCM7005 internal registers. This must be performed every time power is applied to the TSW4100 EVM. The CDCM7005 device has default settings that are loaded at powerup and are different than the settings needed to operate the TSW4100.

To load the CDCM7005 with the TSW4100 default values:

1. Open the TSW4100 DAC CDC GUI. Upon opening, the GUI will automatically send the TSW4100 default values to the CDCM7005. LED D6 should now be illuminated indicating the CDCM7005 is locked to the internal 10MHz reference.
2. Click on *Reset USB Port*. After this, If no changes are going to be made to the CDCM7005, the user can skip steps 2-10 and go the *Loading the DAC5688* section.
3. To make changes to the CDCM7005, click the *CDCM7005 Registers* option in the top, left-hand corner. The CDCM7005 interface (Figure 15) displays.
4. The *PLL tab* goes to another window which allows the user to change the VCXO, reference, and output frequency. The current default values are set to match the VCXO and reference oscillator that are installed on the TSW4100.
5. The *Output tab* allows the user to set the divide ratio, output drive standard, and output mode for all of the outputs. The current default values are what is required for the TSW4100 to operate with.
6. The *Advanced tab* allows the user to change several parameters used by the internal PLL of the CDCM7005 along with other parameters. Consult the CDCM7005 data sheet for more information on these controls.
7. After making any changes to any of these settings, click the *SEND All* button to load the CDCM7005 registers with the new values.
8. The default values are also stored in a file provided by TI. To load the stored settings, click the *Load Settings* button on the lower left side of the GUI.

9. Navigate to the directory (**C:\Program Files\Texas Instruments\TSW4100GUI\CDCandDACregisters**) for the default register settings and select the file TSW4100_DAC_CDC_example_1.txt. This file is also located on the provided CD as well.
10. Click *OK* to load the CDCM7005 registers with default values.
11. To save a custom configuration, click on the *Save Settings* button and provide a file name. This file will then save all of the current settings for both the DAC5688 and CDCM7005.

The TSW4100 uses differential and single-ended clocks from the CDCM7005:

- Y0A and Y0B to drive the DAC5688 CLK2 inputs.
- Y1A and Y1B to drive the DAC5688 CLK1 inputs.
- Y2A provides an option to drive the DUC. This is currently not used and the output is 3-stated.
- Y2B to drive the single-ended FPGA input clock.
- Y3A and Y3B to drive the FPGA differential input clock.
- Y4A provides an option to drive the ADS5545 along with Y4B and bypass the transformer. This is currently not used and the output is 3-stated.
- Y4B to drive the crystal filter and transformer which generate the ADS5545 differential input clock.

This default configuration generates a:

- 320 MHz clock for CLK2 inputs of the DAC5688.
- 160 MHz clock for CLK1 inputs of the DAC5688.
- Two 160 MHz clocks for the FPGA.
- 160 MHz clock input for the ADS5545.

5.3 Loading the DAC5688

The default values for the DAC5688 and CDCM7005 are stored in a file provided by TI. To load the stored settings, click the *Load Settings* button on the lower left side of the GUI.

Navigate to the directory (**C:\Program Files\Texas Instruments\TSW4100GUI\CDCandDACregisters**) and select the file **TSW4100_DAC_CDC_example_1.txt.** The GUI loads both the DAC5688 and CDCM7005 with the settings contained in this file every time the *Load Settings* function is used. After the DAC5688 is configured, the user must make sure the internal PLL is locked. To verify this, click on the *DAC5688 Registers* button in the top, left-hand corner of the GUI. Click on the *PLL* tab. The GUI shall now look as shown in Figure 16. If the PLL Lock indicator is **Green**, the DAC5688 has been loaded properly and is ready for operation. If the indicator is **Red**, indicating the PLL is not locked, press the DAC5688 reset switch SW5, then click on the *Auto-Sync* button on the top right side of the GUI. If PLL Lock indicator still does not turn **Green**, press the DAC Reset button SW5 on the TSW4100 and reload the DAC and CDC settings. The PLL Lock Indicator must be **Green** for the DAC5688 to be working properly

To make changes to the DAC5688, do the following:

1. Click the *DAC5688 Registers* button in the top, left-hand corner of the GUI.
2. The GUI should now be displaying the Input tab settings, as shown in Figure 17. In this window, the user can change the Input Formats, MUX options, Output path, and Fixed Data settings.
3. Click on the *Digital* tab. The GUI display shall now look as shown in Figure 18. In this window, the user can change the DAC interpolation rate, FIFO settings, Mixer settings, Quadrature Modulation Correction settings, and Offset adjustments.
4. Click on the *Clock* tab. The GUI display shall now look as shown in Figure 19. In this window, the user can change the Clock Settings and Clock Adjustments.
5. Click on the *PLL* tab. The GUI display shall now look as shown in Figure 16. In this window, the user can change the PLL mode, view the PLL status, change the PLL Ratios and PLL Gain settings. After the DAC5688 and CDCM7005 have been configured, make sure that the PLL Lock indicator on the GUI turns from **Red** to **Green**. If this does not work, click on the *Auto-Sync* button on the top right side of the GUI. If PLL Lock indicator still does not turn **Green**, press the DAC Reset button SW5 on the TSW4100 and reload the DAC and CDC settings. The PLL Lock Indicator must be **Green** for the DAC5688 to be working properly.

6. Click on the *Output* tab. The GUI display shall now look as shown in Figure 20. In this window, the user can change the DAC gains, turn on or off the two DAC channels, and modify the DAC output delays and enable or disable the LPF option for each DAC.
7. Click on the *Sync* tab. The GUI display shall now look as shown in Figure 21. In this window, the user can change the SIF control, the FIFO sync source, the Clock Divider, the QMC, and the NCO.
8. The *Advanced* tab is for factory test only. This window should not be used.
9. More information regarding the operation of theses registers can be found in the DAC5688 Data Sheet.
10. After completion of all changes, click the *Send All* button on the top right side of the GUI. The register values will now be loaded into the DAC5688.
11. Click on the *Read All* button, located on the top right side of the GUI, to view the current register settings of the DAC5688. If an error message is not received, the program is working properly.

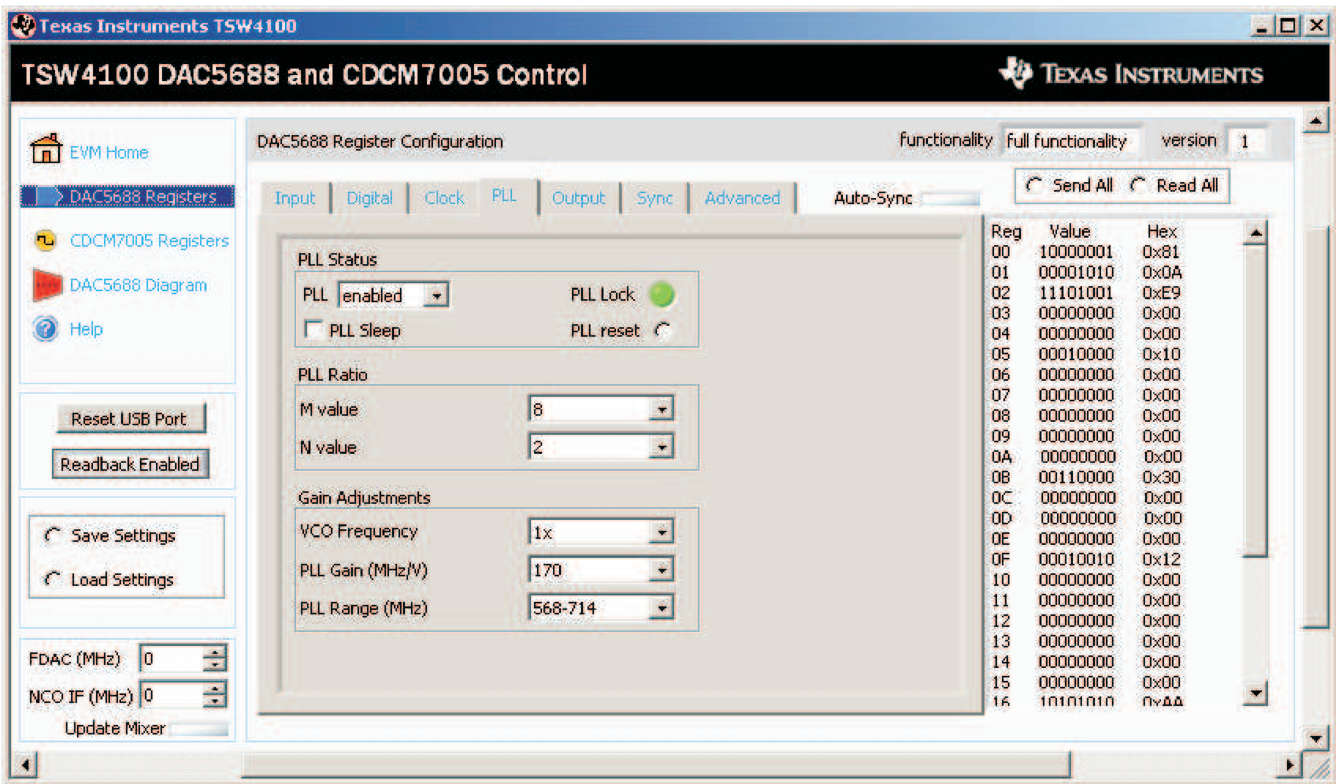


Figure 16. DAC5688 Interface

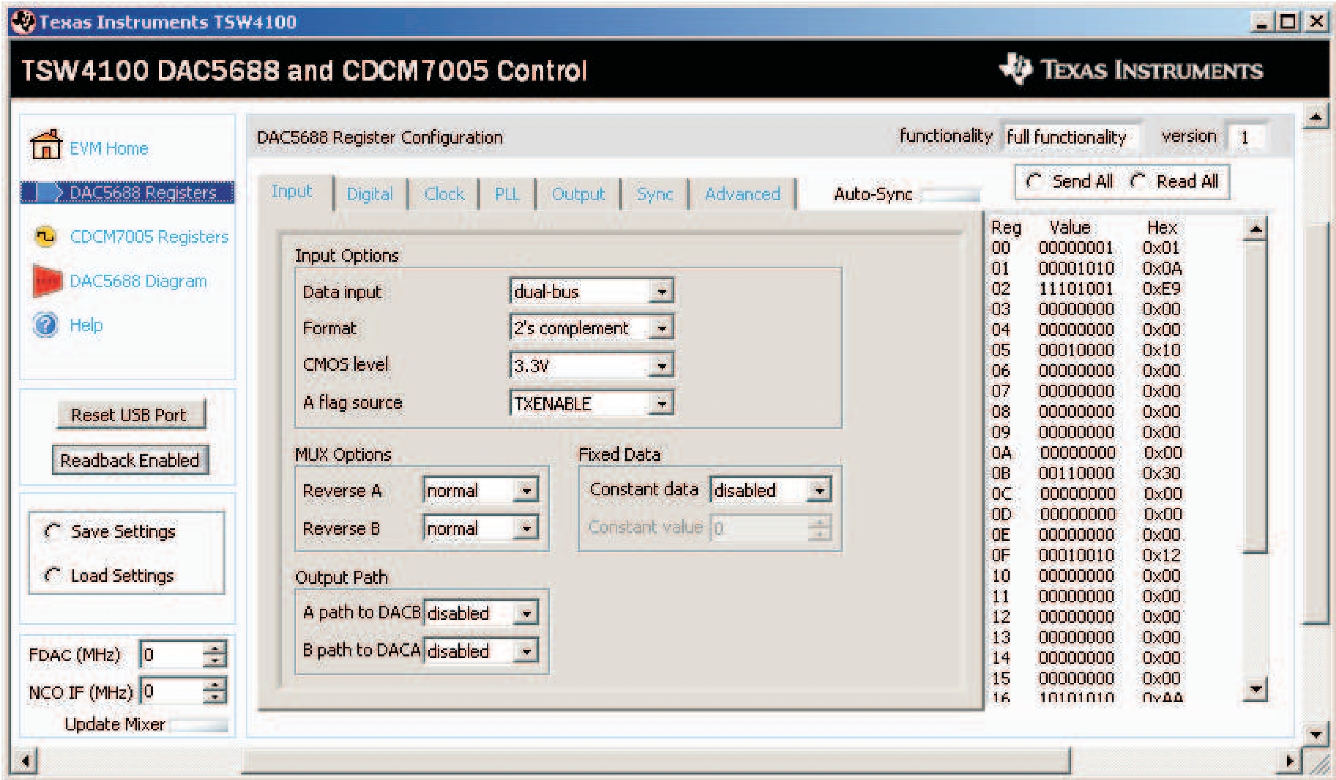


Figure 17. DAC5688 Options

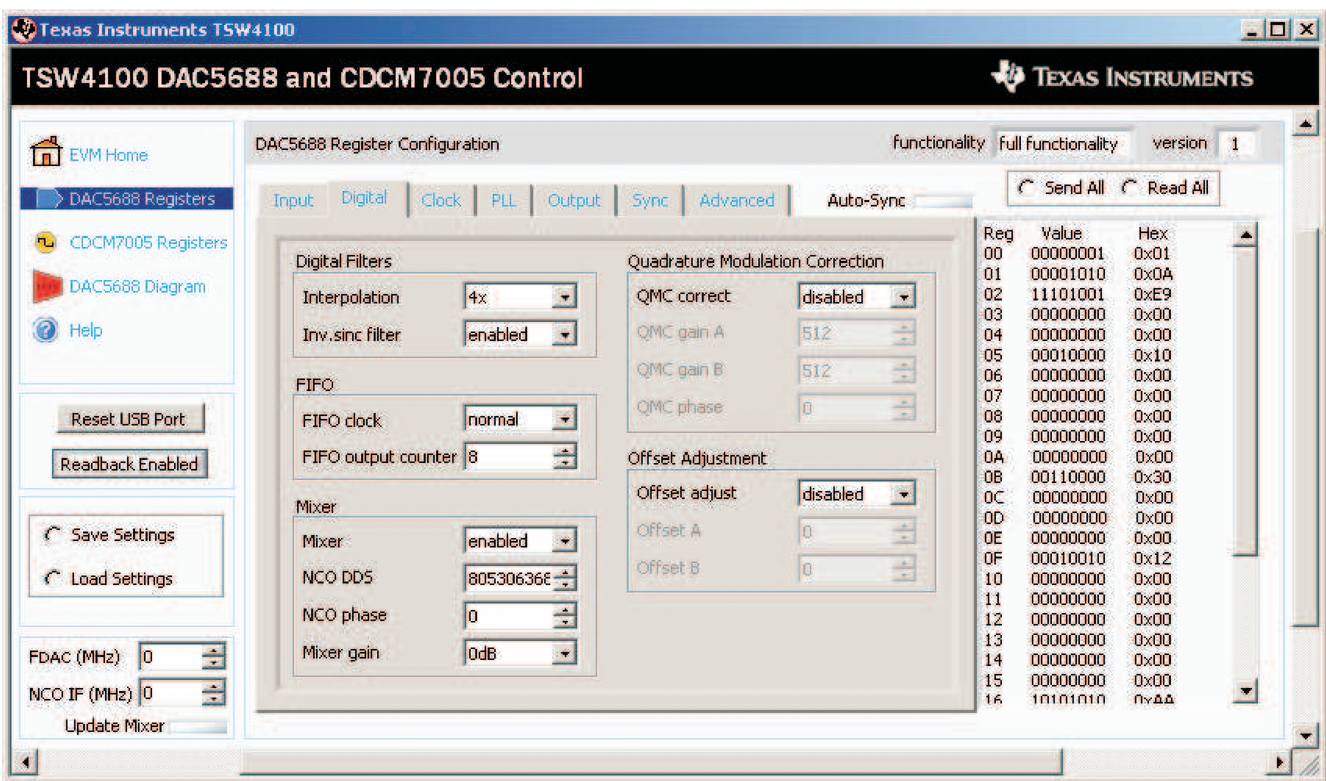


Figure 18. DAC5688 Filters

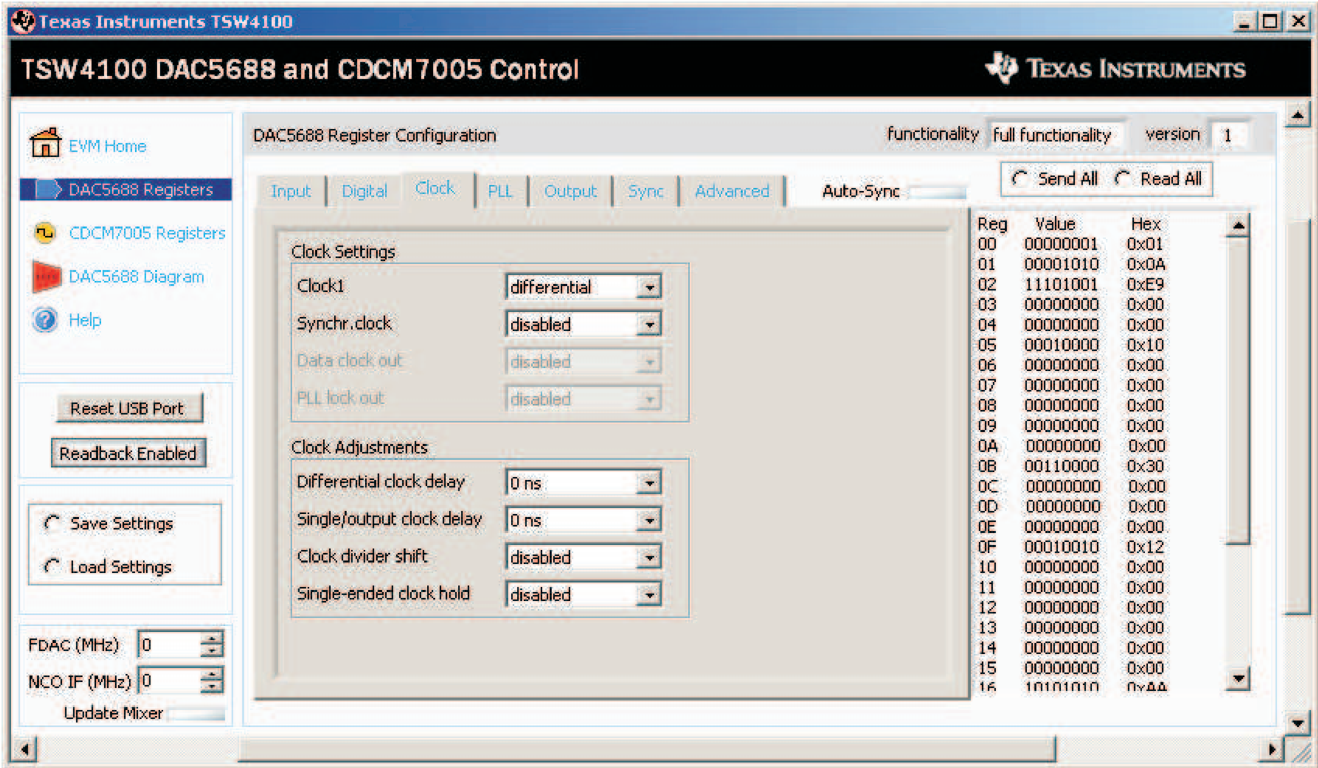


Figure 19. Clock Settings

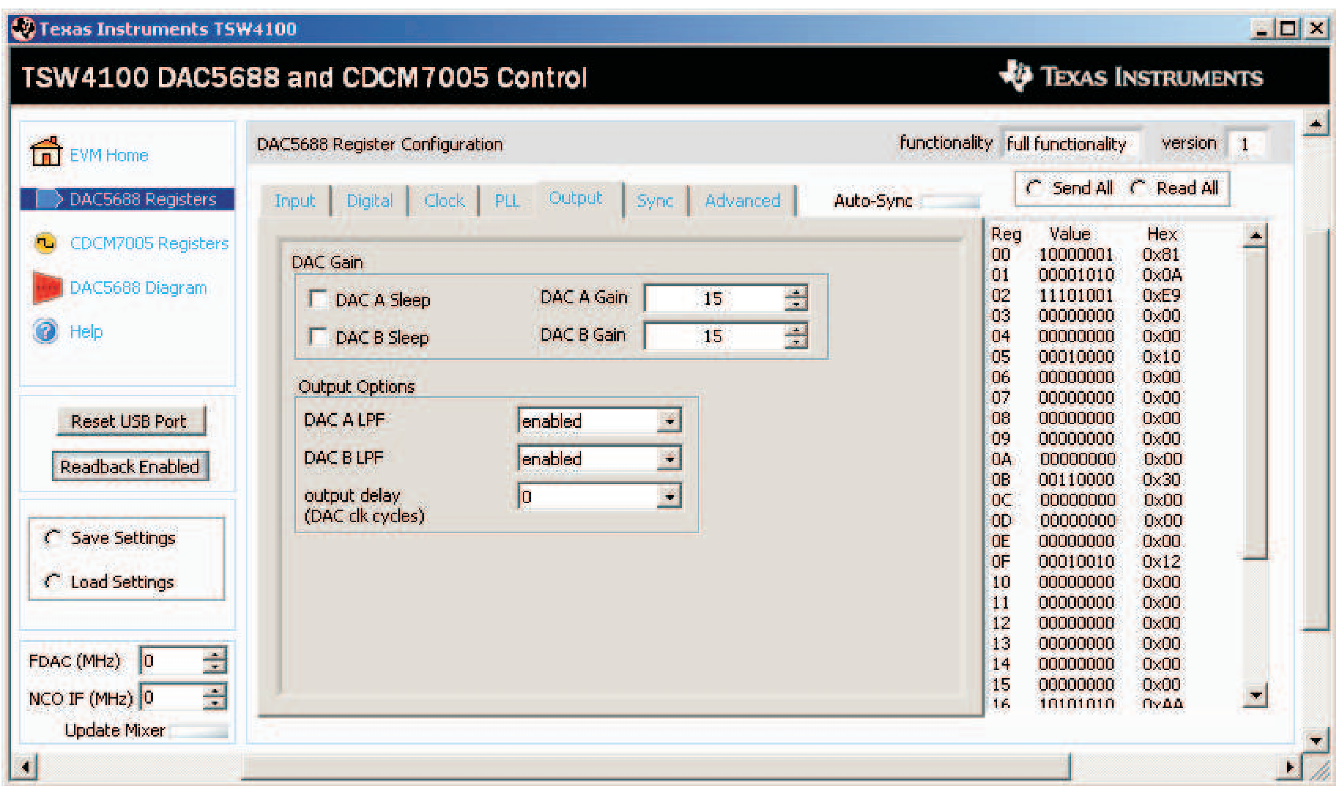


Figure 20. DAC Gain

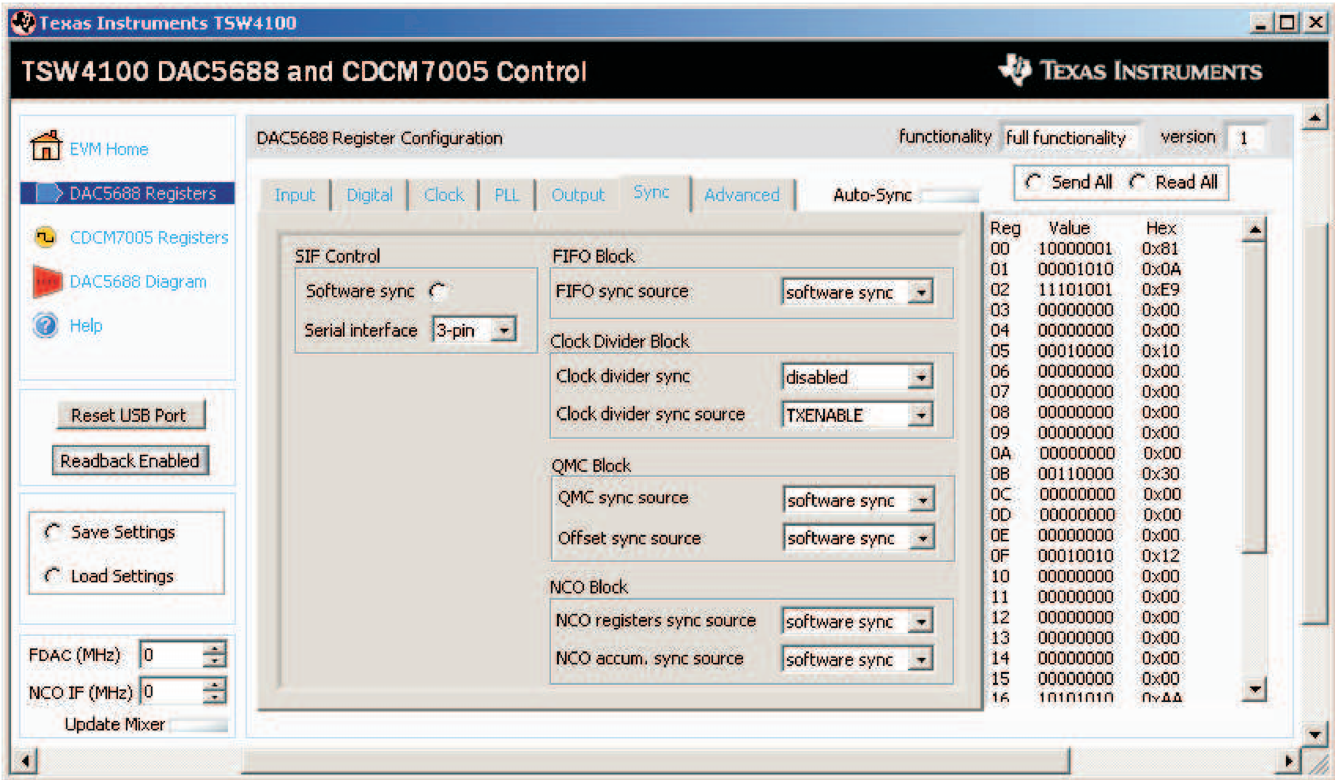


Figure 21. SIF Control

6 TSW4100 Graphical User Interface (GUI) Software

Using the provided software, the user can download control register and coefficient information data to the GC5016 and read back status register information.

Note: The TSW4100 ships with firmware installed to operate this interface with a PC. This interface must be added to any new firmware that is installed or generate an alternative method of writing and reading to the GC5016.

The next two sections describe how to start the TSW4100GUI user interface (Section 6.1) and the graphical user interface controls (Section 6.2).

6.1 Starting the TSW4100GUI

Note: To interface with the TSW4100, the CDCM7005 must be operating and locked.

To start the TSW4100GUI interface:

1. Click the Windows menu sequence **start** → **All Programs** → **Texas Instruments** → **TSW4100GUI** → **TSW4100GUI_vXpXX.exe,** (Figure 14) where **vXpxx** represents the version of software. The application first displays a DOS Test Window. The text **Extracting CTF**… …**CTF archive extraction complete.** only displays the first time the **TSW4100GUI** application runs.

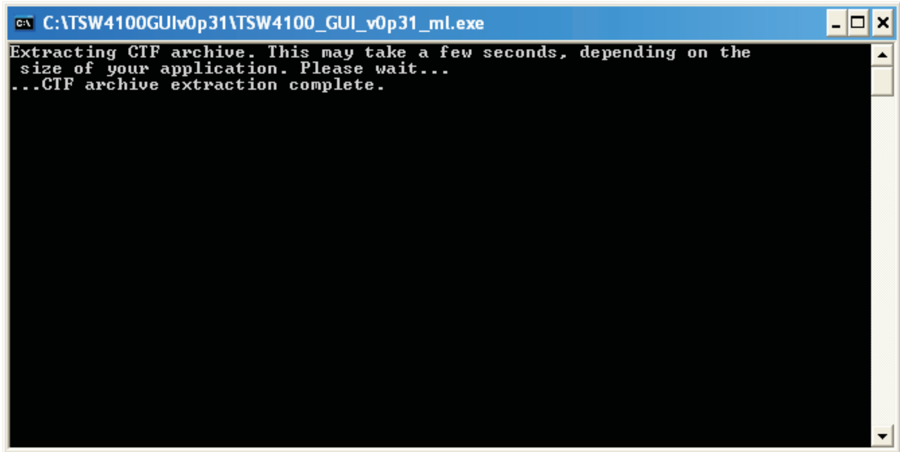


Figure 22. TSW4100GUI DOS Test Window

2. The TSW4100 graphical user interface displays.

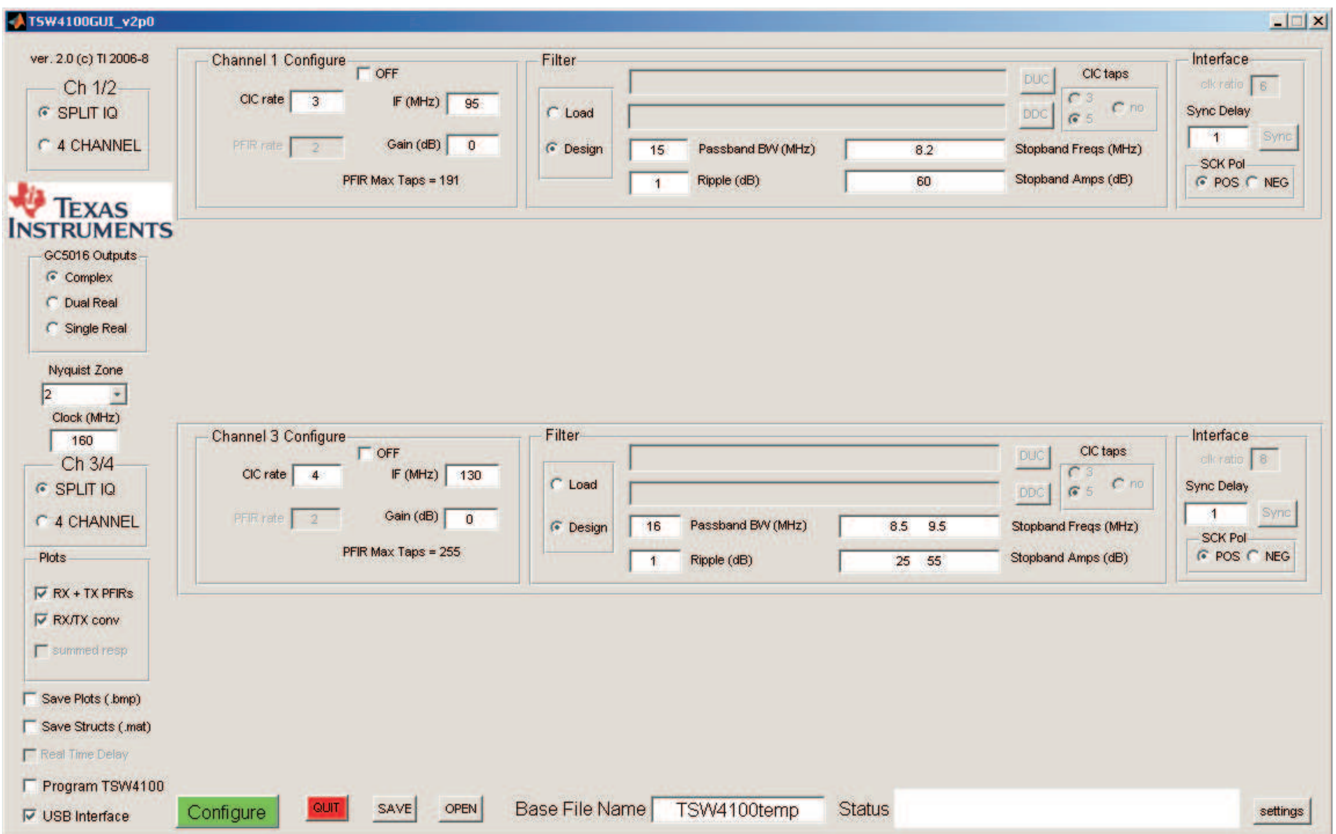


Figure 23. TSW4100GUI Interface

Tip: The DOS Test window displays the same information as the MATLAB command window would display. Use it to monitor the application for internal MATLAB errors.

Note: If the TSW4100 GUI display does not fit on the user's monitor, a second version of the GUI can be loaded which reduces the size of the GUI. This executable is called *TSW4100GUI_vXpXX_resize.exe* and can be found at **C:\Program Files\Texas Instruments\TSW4100GUI.**

6.2 Graphical User Interface Controls

General Settings area

This area helps the user load and save the necessary configurations and results (filter response figures):

- **Save Plots (.bmp)**—saves the filter response figures (Section 6.3) as bitmap (***.bmp** filename extension) graphic files.
- **Save Structs (.mat)**—saves the Matlab structures used to setup the channels in files (***.mat** filename extension) .
- **Real Time Delay**—adjusts the delay between DDC and DUC sync to occur when Sync delay setting is adjusted without reprogramming the DDC and DUC. (Enabled after the TSW4100 is programmed.)
- **Program TSW4100**—loads configurations into the TSW4100 and starts the sync sequences when selected.
- **Configure**—generates the DDC and DUC configurations and loads them to TSW4100 when the **Program TSW4100** check box is selected.
- **USB Interface**—use the USB connector to interface to the TSW4100, when selected. This is the default hardware configuration. The parallel port interface is *not* typically supported by hardware.
- **Base File Name**—name of the folders and files containing the programming and sync information.

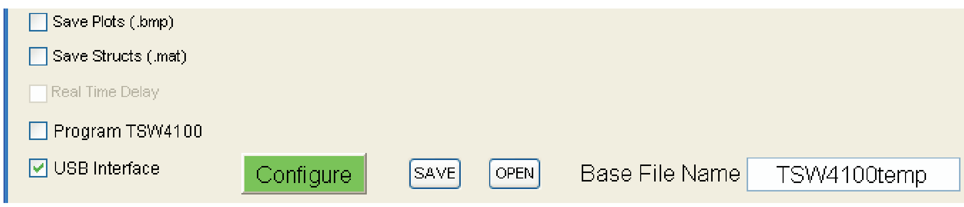


Figure 24. General Settings Controls

Status area

This area displays context-sensitive information and error messages. Also check the DOS Test window for MatLab and other diagnostic information.

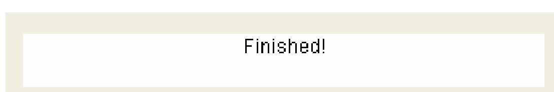


Figure 25. Status area

Left Column area

The user interface controls (Figure 26) on the left side of the screen control major functionality settings and the content of the output filter response displays.

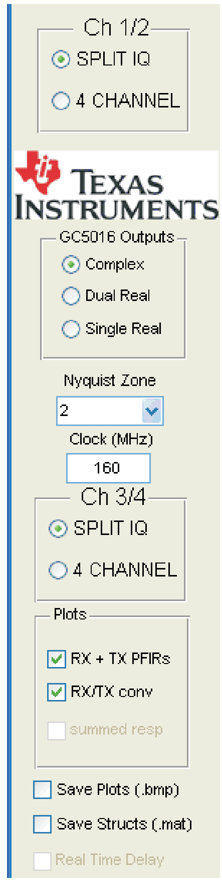


Figure 26. Left Column Interface Controls

- **Channel Mode selections**—Choose between SPLIT IQ and 4 CHANNEL modes.

> **CAUTION**
>
> The mixed mode **Ch** = = *SPLIT IQ* and **Ch 3/4** = *4 CHANNEL* is invalid. In this case, swap Ch = and Ch 3/4 option selections.

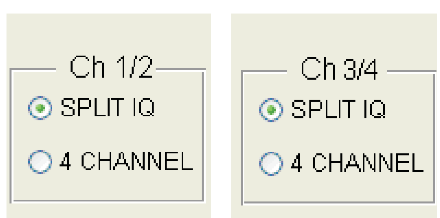


Figure 27. Channel Selection Controls

Table 4. Channel Selection Options

Ch = Option Selected	Ch 3/4 Option Selected	Description
SPLIT IQ	SPLIT IQ	Valid selection
SPLIT IQ	4 CHANNEL	**Invalid selection**
4 CHANNEL	SPLIT IQ	Valid selection
4 CHANNEL	4 CHANNEL	Valid selection

- **GC5016 Output options**:
  – *Complex* output sent to DAC.
  – *Dual Real* sends CH1 and CH2 outputs combined as a real signal to DAC channel A. Output frequency is in first Nyquist zone. Set DAC mixer to $F_S/2$ for second Nyquist zone output.
  – *Single Real* sends CH1–CH4 outputs combined as a real signal to DAC channel A. Output frequency is in first Nyquist zone. Set DAC mixer to $F_S/2$ for second Nyquist zone output.

- **Nyquist Zone**—ADC Nyquist Zone for the input signal. The frequency band and DAC settings are listed in Table 5.

Table 5. Nyquist Zone Frequencies and DAC Settings

Nyquist Zone	Minimum Frequency	Maximum Frequency	DAC NCO (Complex Output) / Real Output	DAC NCO Dual Real IF
1	0	Clock÷2	Clock÷4	0
2	Clock÷2	Clock	Clock*3÷4	F_S÷2
3	Clock	Clock*3÷2	Clock*5÷4	NA

- **Clock (MHz)**—clock rate for the GC5016. The default TSW4100 uses a 320 MHz VCXO, which is divided by 2 to produce a 160 MHz clock for the GC5016.
- **Plots - RX + TX PFIRs**—plots RX and TX PFIR filter spectra before CIC compensation and scaling. Displays the number of taps used for each filter. (See Figure 30 for an example.)
- **Plots - RX/TX CONV**—plots the convolved RX + TX filter response, including CIC compensation and design limits. (See Figure 31 for an example.)

Channel Configuration area

This area configures the channel signal, prior to filtering.

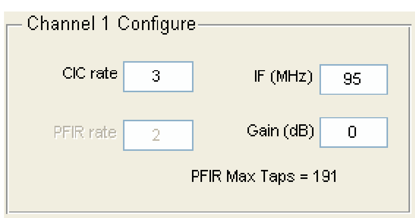


Figure 28. Channel Configuration Controls

- **CIC rate**—CIC decimation or interpolation.
- **PFIR rate**—PFIR decimation or interpolation. Only a value of *2* can be selected.
- **IF (MHz)**—frequency in ADC second Nyquist Zone of channel.
- **PFIR Max Taps**—maximum number of PFIR taps available for this mode. Includes CIC compensation taps, so the number of $Taps_{raw\ filter} = PFIR_{Max\ Taps}$–number of CIC compensation taps +1. (See Section 7.8 for more information and examples of CIC compensation taps design.)

- **Gain (dB)**—Nominally digital gain of channel from ADC input to DAC output. Does not include inherent analog gain loss (ADC input full scale is 11.2 dBm and DAC output full scale is 4 dBm). To disable a channel, set Gain (dB) to a large negative gain (approximately –80 dB).

Filter Settings area

Use this portion of the GUI to load a filter (Section 6.2.1) without CIC compensation or design a filter (Section 6.2.2 and Section 6.2.1) based on spectral information. For the Load Filter option, the Passband BW (MHz) needs to be set for calculating the CIC compensation.

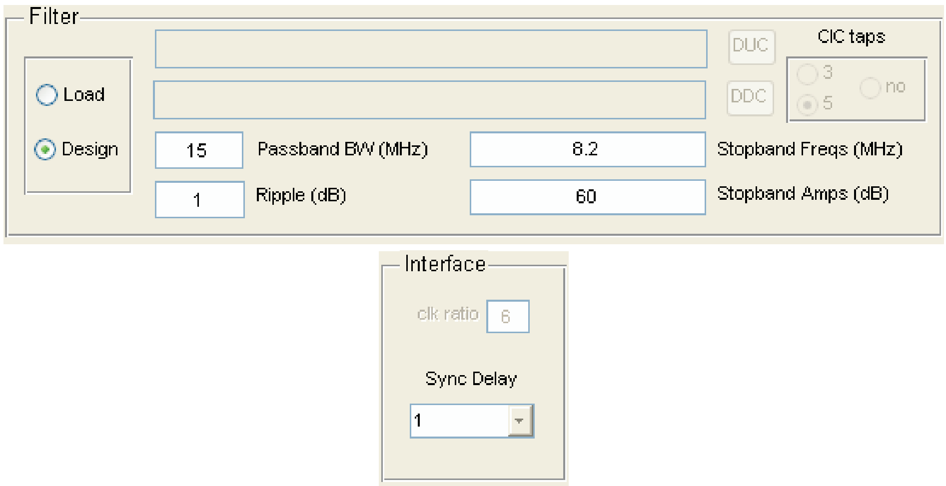


Figure 29. Filter Load and Design Settings

6.2.1 Load Filter controls

- **DDC**—loads the filter digital down converter (DDC) file (default filename extension is ***.taps**). This filter is used before adding cascaded integrator-comb (CIC) compensation and does not need to be quantized.
- **DUC**—loads the filter digital up converter (DUC) file (default filename extension is ***.taps**). This filter is used before adding CIC compensation and does not need to be quantized.
- **CIC taps**—sets 0, 3, or 5 CIC compensation taps to add for externally generated filters to be loaded. When no taps are added, the filter input is expected to be properly scaled.

6.2.2 Design Filter controls

- **Passband BW (MHz)**—full bandwidth across which the ripple is specified.
- **Ripple (dB)**—maximum ripple of passband.
- **Stopband Freqs (MHz)**—stopband frequencies ***offset from center of passband***. Separate multiple input frequencies with spaces (multiple spaces permitted).
- **Stopband Amps (dB)**—stopband amplitudes (dB) that correspond to each stopband frequency specified in the **Stopband Freqs (MHz)** text box. Stopband amplitude is held until stopband frequency (stair step). Separate multiple amplitudes with spaces (multiple spaces permitted).

6.2.3 Interface controls

- **Clk ratio**—clock divider ratio for DDC-DUC interface. Automatically set to **CIC rate**×**PFIR rate** for *SPLIT IQ* mode.
- **Sync Delay**—delay in DDC to DUC syncs. After TSW4100 is programmed, check real time sync for a new sync to be issued for the channel each time this is changed.

6.3 Filter Response Windows

After clicking the **Configure** button (if the filter is successfully designed) in the General Settings area the frequency response for each PFIR filter BEFORE CIC compensation and quantization is displayed in a window labeled Figure 2*N–1 (Figure 30) , where N is the channel number. The odd-numbered figures also display the number of PFIR taps used, plus if the filter is symmetric or asymmetric.

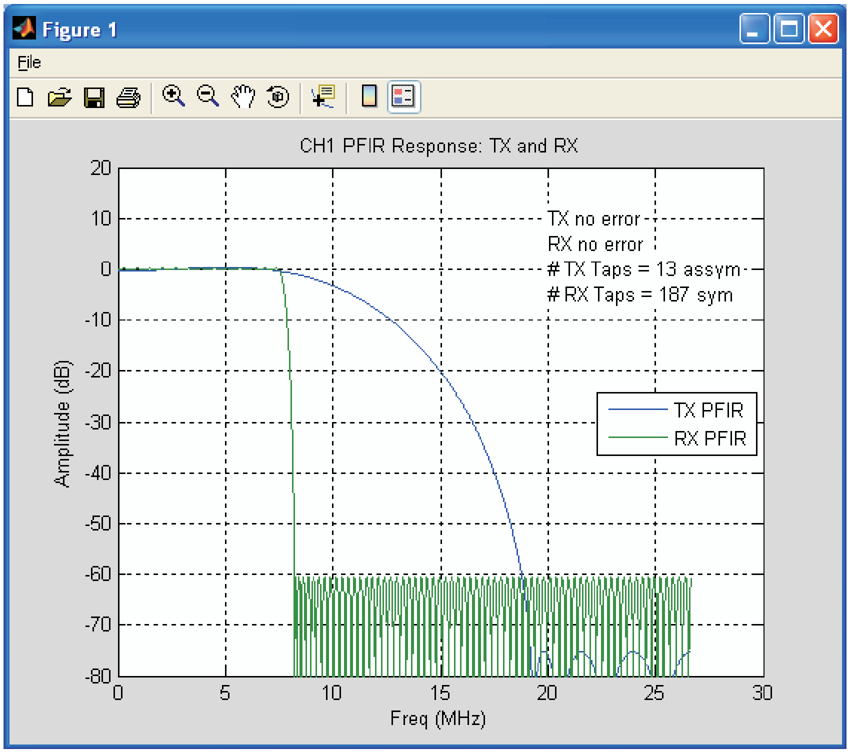


Figure 30. (Figure 2*N–1 Window) Frequency Response Before CIC Compensation and Quantitization

The frequency response for the convolved end-to-end response is displayed in a window labeled Figure 2*N (Figure 31), where N is the channel number. The even-numbered figures also display ripple and stopband limits in red, and actual ripple and stopband amplitudes.

Note: The stopband amplitudes are one half the input values, as the DDC and DUC filter operate in series, doubling the attenuation. The final band, which is the image band, is 1× the final stopband amplitude. These figures also include the image bands.

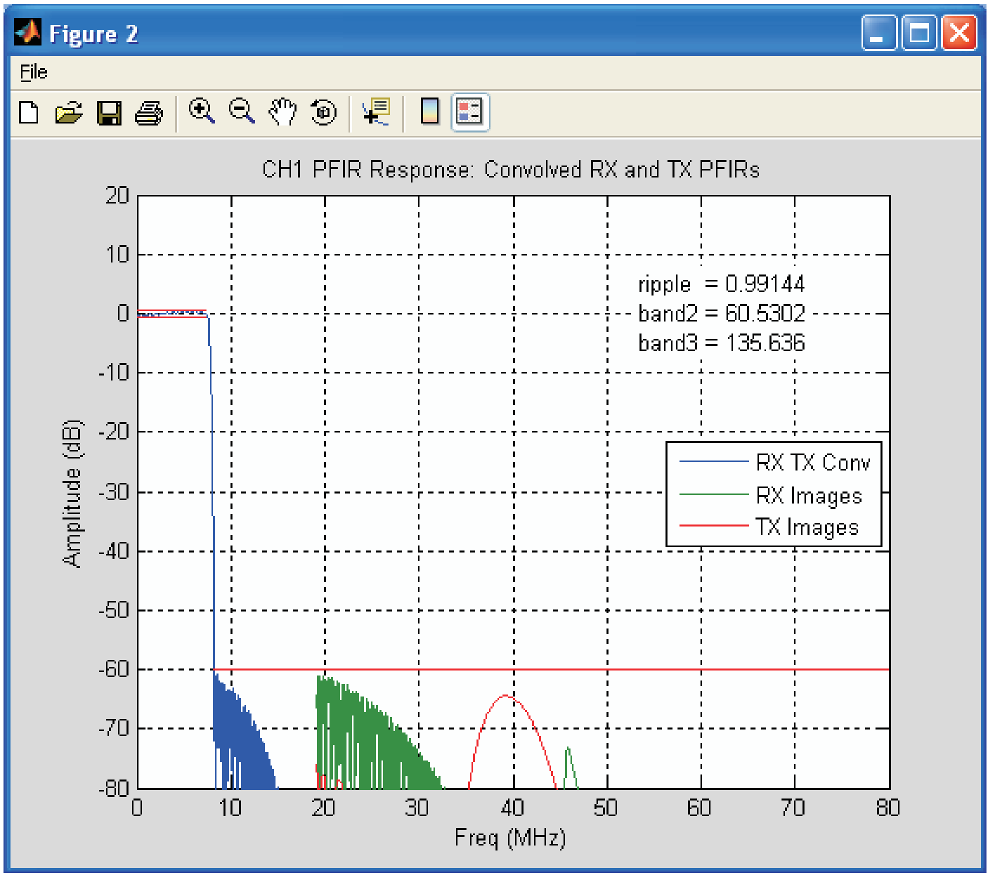


Figure 31. (Figure 2*N window) Frequency Response with Convolved End to End Response

7 Designing and Testing a Filter (Step-by-Step)

This example takes the user through the steps to design a new filter and configure the TSW4100.

Assume there are filter spectral requirements:

- Passband Bandwidth = 12 MHz
- Peak-to-Peak passband Ripple = 1 dB
- Stopband = 50 dB at 6.5 MHz (.05 MHz from band edge)
- 4 channels

Note: The TSW4100 GUI can be used stand alone (not connected to the TSW4100) to do filter design or generate the DUC and DDC configuration.

7.1 Step 1—Start TSW4100GUI

Click the Windows menu sequence **start** → **All Programs** → **Texas Instruments** → **TSW4100GUI** → **TSW4100GUI.exe** to start the TSW4100GUI.

7.2 Step 2—Channel Selection

Since 4 channels are needed, change the **Ch** = mode to the *4 CHANNEL* option.

Figure 32. Channel Selection Controls

Also, the user only wants to design a filter for channel 1. Turn off channels 2 and 3 by clicking on the "OFF" button on the GUI for Channel 2 and Channel 3. This prevents the software from doing the filter design for these channels, saving time.

7.3 Step 3—Selecting Filter Design Parameters

Begin by choosing the decimation rate for the CIC. For 12 MHz bandwidth, the total maximum decimation is calculated using Equation 1:

$$\text{Trunc (Clock M(Hz)} \div \text{filter BW)} = \text{Trunc } (160 \div 12) = 12 \tag{1}$$

(The final result in Equation 1 needs to be the next even value lower than the calculated value).

Because the PFIR has a fixed decimation of 2 (only value allowed), this results in a value of 6 for the maximum CIC decimation.

However, if the spectral requirements can be met with less decimation (more difficult as the number of PFIR taps is less and each tap covers less time), lower decimation typically results in a shorter latency. This is because other components (such as the interface circuits) are operating at a higher clock rate than the PFIR. Start with a decimation of 6, but then also try to decrease the decimation (Section 7.9) to find the minimum required to meet the spectral requirements (Section 7).

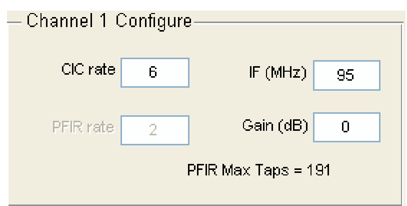


Figure 33. CIC Decimation Rate

Note: As the user changes the **CIC rate** value, the value for the **PFIR Max Taps** is recalculated (191 in the case of the CIC decimation rate of 6 for Figure 33).

To set up the **Filter Design** parameters, the user needs to translate the spectra requirements.

a. Set the **Passband BW (MHz)** to *12* for full bandwidth.
b. Set the **Ripple (dB)** to *1* for full bandwidth.
c. Set the **Stopband Freqs (MHz)** to *6.5* as shown in Equation 2.
d. Set the **Stopband Amps (dB)** to *50*.

$$\text{Stopband Frequency} = \text{Passband BW} \div 2 + \text{Bandedge Frequency} = 12 \div 2 + .5 = 6.5 \tag{2}$$

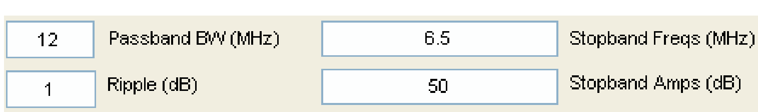


Figure 34. Filter Design Parameters

Note: In the TSW4100GUI, the target filter characteristics in the previous procedure are used to design the DUC and DDC PFIRs excluding the CIC compensation. When CIC compensation is added, there is an error between the frequency response of the filter taps and inverse CIC response in the passband. This is usually less than 0.2 dB, but adds to the ripple of the composite PFIR and CIC filter response. After designing the filter the user may need to go back and reduce the target ripple to adjust for the error in CIC compensation. See Section 7.10 for steps needed to manually reduce target ripple to adjust for error in CIC compensation.

7.4 Step 4—Saving Filter Design Information

Before running the design, go to the bottom left-hand corner and select the **Save Plots (.bmp)** and **Save Structs (.mat)** check boxes. This saves the filter response images (Section 6.3) and the MATLAB data structures containing channel configuration information.

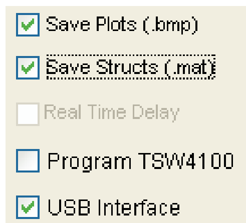


Figure 35. Save Filter Design and Responses

7.5 Step 5—Running the Filter Design

Now run the filter design program and calculate if the filter is achievable using the number of available PFIR taps. If there are other filters to design, use the other channels to design these filters simultaneously. However, for now keep the defaults in Ch 2 and Ch 3/4—these filters are designed but do not affect the design of our filter in Channel One.

Click the **Configure** button.

7.6 Step 6—Briefly Examining the Filter Response Windows

As the program calculates the spectra responses, the **Status** area (lower right-hand corner) displays the messages, *generating filter 1, generating filter 2,* and so forth. A total of six windows display when the filter design calculations are complete. Each Channel has two figures showing the:

- DDC and DUC separate PFIR spectral responses (Figure 36)
- Composite DDC filter input to DUC filter output (Figure 37)

First, look at Figure 36. This plot shows the PFIR spectral response of the DUC (TX) and DDC (RX) *before* convolution with CIC correction taps (using 3 or 5 taps).

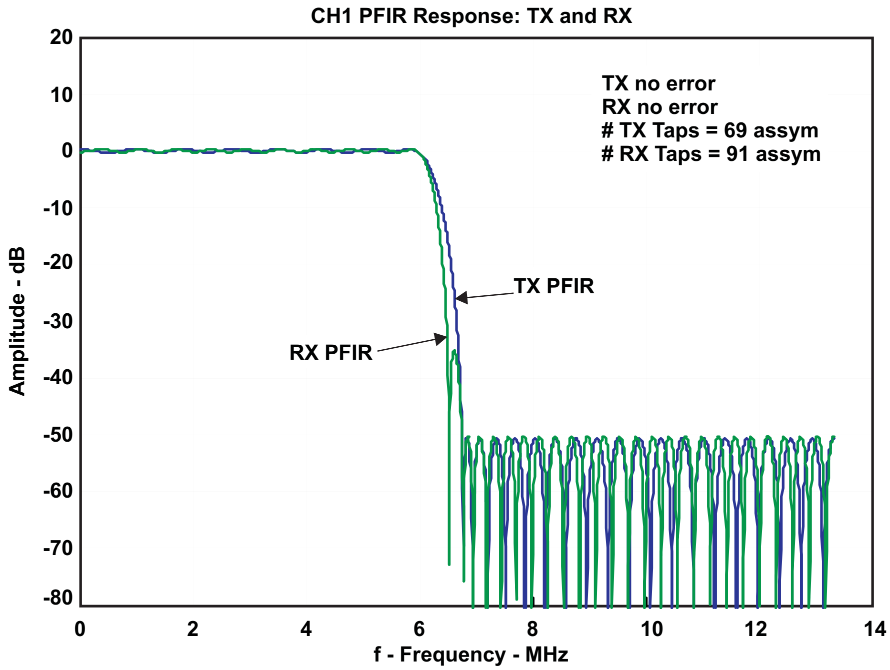


Figure 36. DDC (TX) and DUC (RX) PFIR Responses - Before CIC Correction Convolution

Now look at Figure 37, which shows the composite frequency response from DDC input to DUC output. There are three response curves; the composite response of the PFIRs and CIC filters, plus the images from the CIC decimation and interpolation filter.

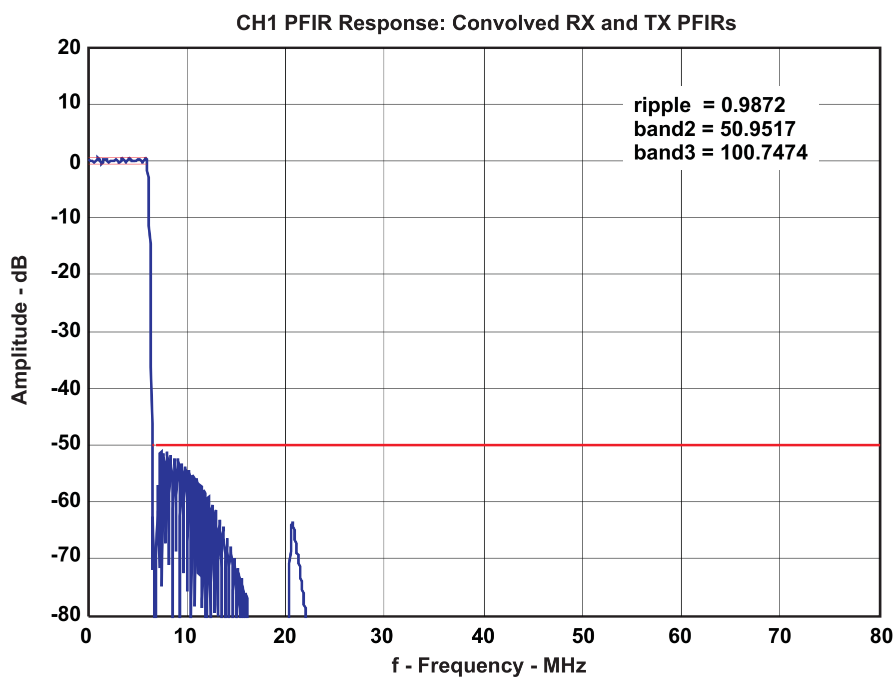


Figure 37. Composite Frequency Response

Also shown in red are the ripple and stopband targets, which are also reported in the text in the upper right-hand corner. As can be seen, the 50 dB stopband requirement is met by the composite response. However, focusing in on the passband ripple (Figure 38) shows the ripple is approximately 1 dB peak-to-peak, meeting our requirement. In some cases, the passband ripple can be slightly larger than the target ripple, due to the CIC compensation having a small error.

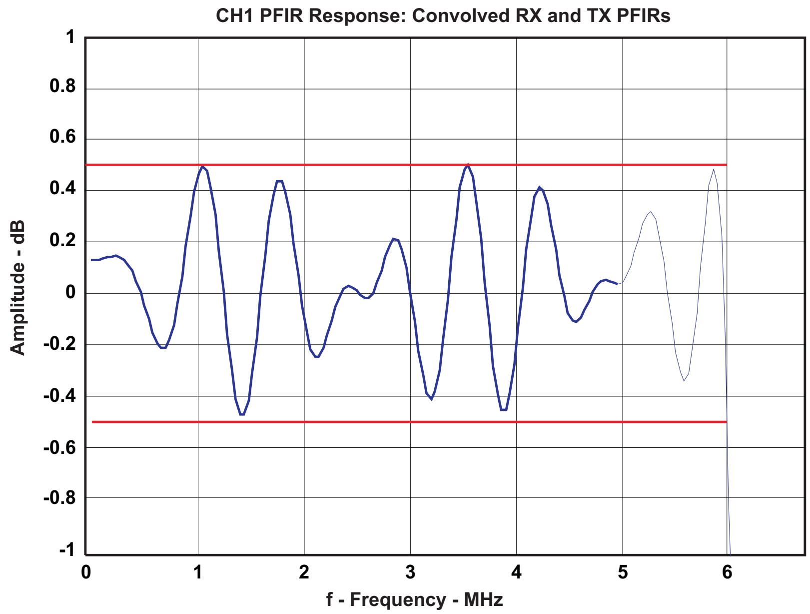


Figure 38. Passband for the Composite Frequency Response

7.7 Step 7—Examine the Filter Response Passband

The X-axis in Figure 36 has a frequency range from 0 Hz to F_{PFIR}÷2, where F_{PFIR} = Clock÷CIC rate or 160 MHz/6 (13.333 MHz). The Y-axis displays the filter response amplitude relative to the gain at 0 Hz. Image rejection for the DDC decimation and DUC interpolation of 2× requires that each filter response be 50 dB in the stopband F_{PFIR}÷2 – Passband BW (13.333–6 = 7.333 MHz) to F_{PFIR}÷2.

The passband in Figure 36, expands the display by choosing the hourglass (+) icon, click a location on the window, and drag the mouse to define the passband area to magnify.

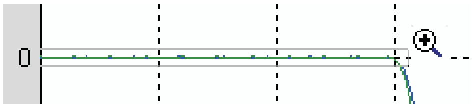


Figure 39. Define the Passband Area to Magnify

Releasing the mouse, yields the magnified filter response passband in Figure 40. The passband ripple for each filter is roughly equal at ±0.25 dB each, or 0.5 dB peak-to-peak. The filter design program divides the allowed ripple equally between the DUC and DDC PFIR design; *not including* the CIC compensation and CIC. This allows no margin for incomplete CIC compensation, which is discussed in section Section 7.8.

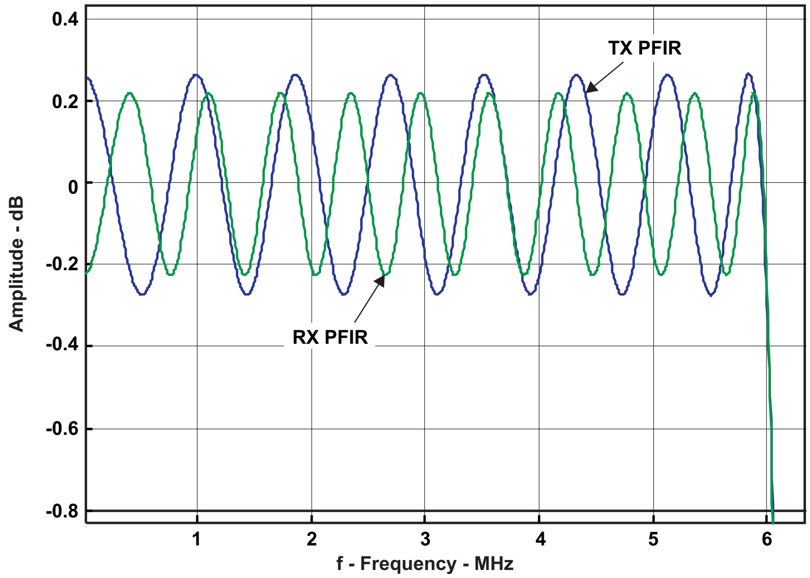
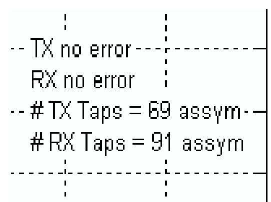


Figure 40. Magnified Filter Passband

Return Figure 40 to the normal scale by right-clicking and selecting the *Reset to Original View* shortcut command. Other shortcut commands provide additional Zoom options.

7.8 Step 8—Evaluate Effect of Taps on Filter Latency

In the original frequency response, the upper right-hand corner contains annotation regarding the number of filter taps and symmetry (or lack) of the DUC and DDC filters.



The number of TX taps used in the DUC PFIR without CIC compensation is 69. After convolving with the 5 CIC compensation taps, the total PFIR length is 74 taps. Since this is less than one-half of the maximum PFIR taps (191), the DUC is asymmetric in time around the center of the PFIR coefficient memory, which is 96 taps. This is done to minimize the latency of the filter. The PFIR coefficient memory locations for taps 60 to 96 (Figure 41) are set to zero.

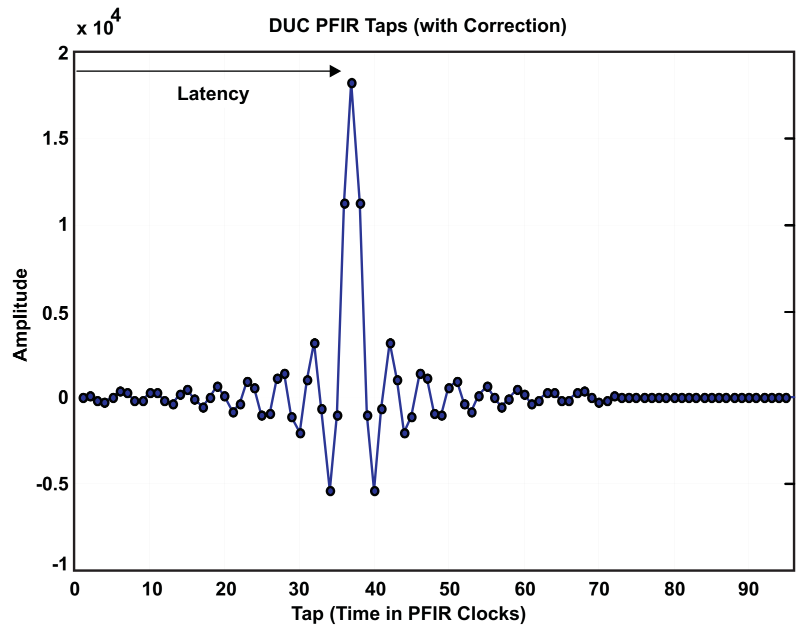


Figure 41. PFIR Tap and Filter Latency

The latency of the PFIR filter (excluding other latency in the GC5016–CIC filter, interface circuits, NCO, gain, and so forth) is the time from the beginning of the filter taps to half of (number of taps + 1). By placing the filter in the forward part of the memory space and appending with zeros, as opposed to the placing it symmetrically in the coefficient memory space, the latency is minimized. However, the number of available taps for an asymmetric coefficient memory space is only half of a symmetric coefficient memory, so it may not be possible to design a filter meeting the spectral requirements asymmetrically.

The number of RX taps is 91 without CIC compensation and is also asymmetric. After including the 5 tap CIC correction, the number of RX taps is 95.

7.9 Step 9—Redesign by Decreasing the CIC Decimation

Now modify the Channel 1 filter design to include less CIC decimation. Reset the **CIC rate** to *4* and click on the "Configure " button(Figure 42) The maximum number of PFIR taps is reduced to 127, when the CIC rate is reduced.

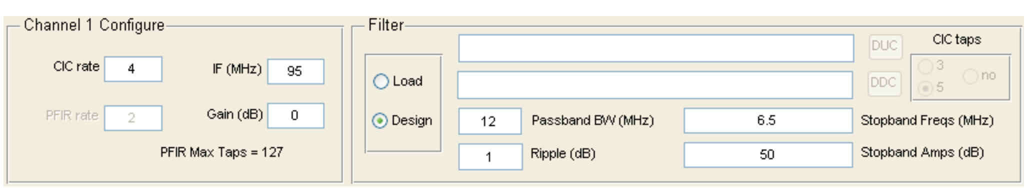


Figure 42. Redesigned Filter Settings

As shown in Figure 43, the redesign is successful and resulted in 71 uncompensated DUC PFIR taps and 123 uncompensated PFIR taps.

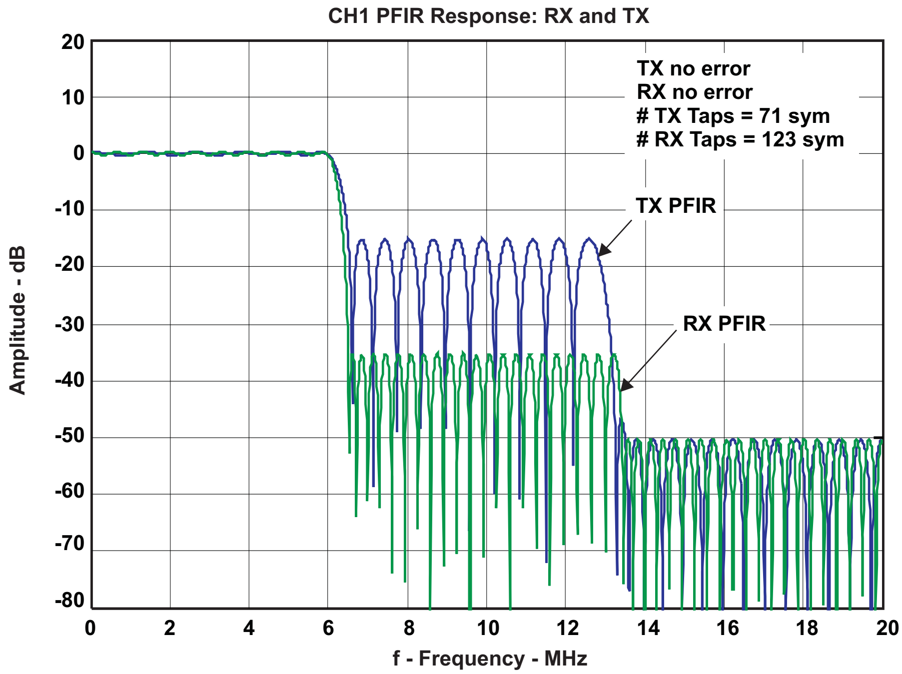


Figure 43. Redesigned Filter Response (without CIC Compensation)

Examining the Passband ripple for the complete response in Figure 31, measure it at 1.12 dB or 0.1 dB greater than the design requirement.

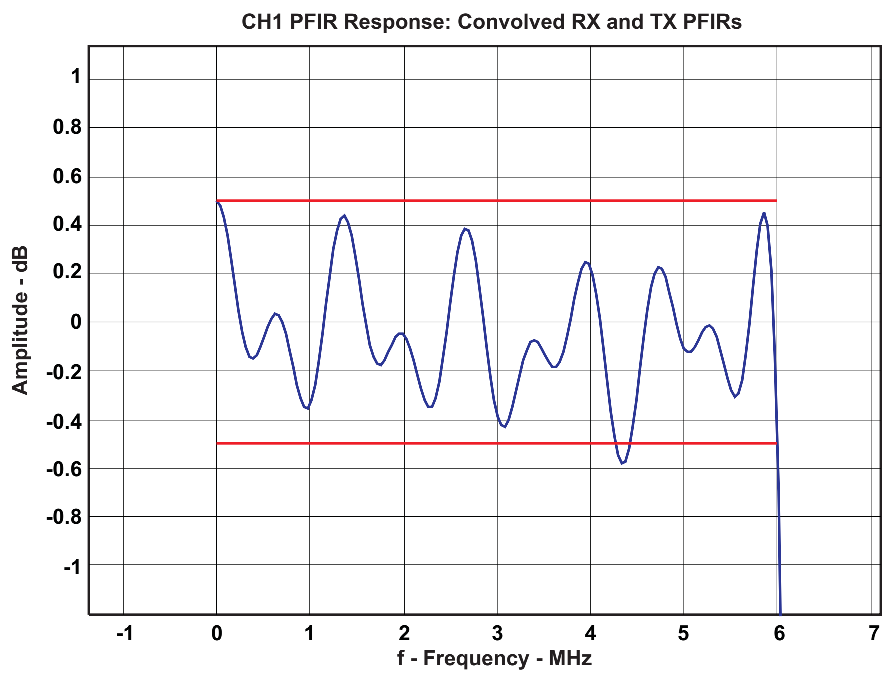


Figure 44. Redesigned Filter Passband

Also, looking at the stopband, the attenuation is only about 46 dB or 4 dB less than the 50 dB design requirement.

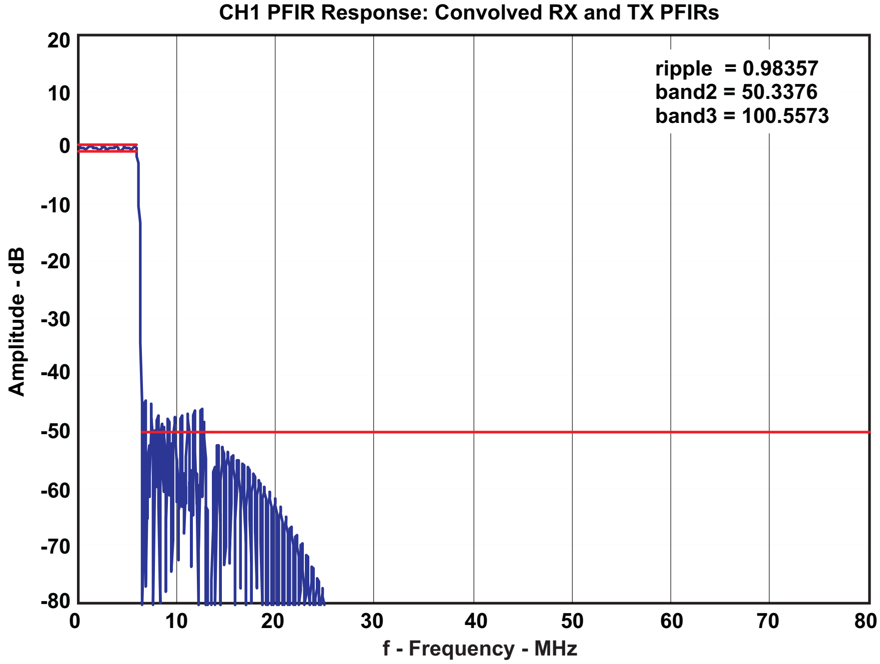


Figure 45. Redesigned Filter Stopband

7.10 Step 10—Redesign by Changing the Filter Parameters

By adjusting the Filter parameters for the passband (0.9 dB ripple) and stopband (60 dB) the user can meet the design requirements. Figure 46 displays the magnified passband for the successfully redesigned filter.

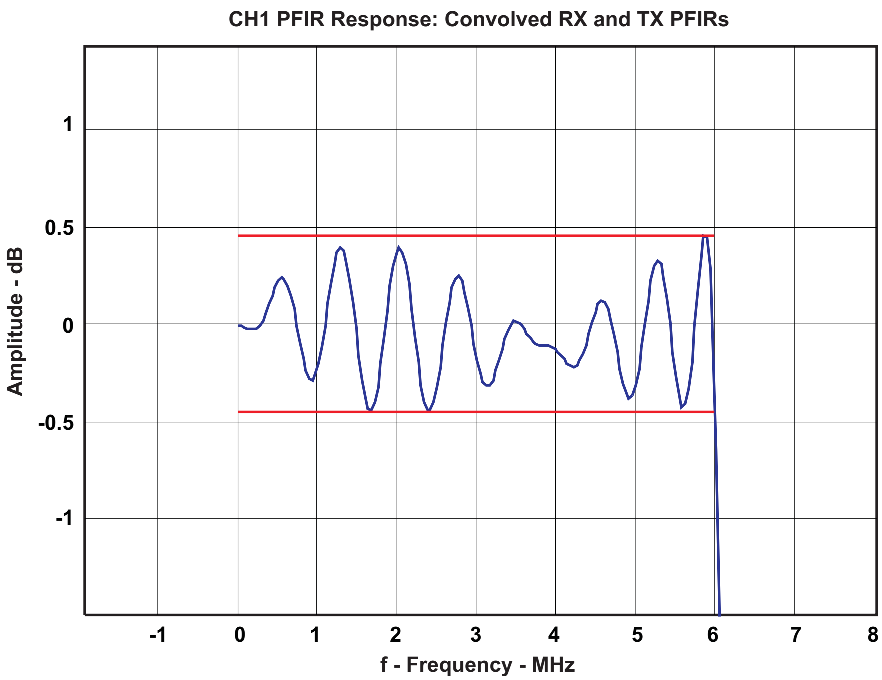


Figure 46. Passband of Successful Filter Design

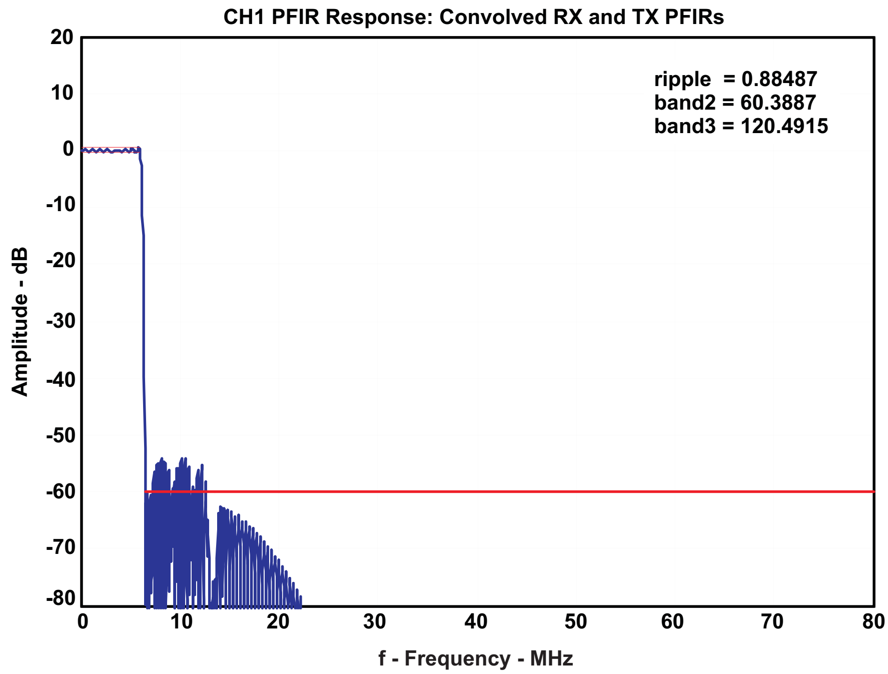


Figure 47. Complete Response of Successful Filter Design

Changing the target ripple to 0.9 dB increases the DUC uncompensated filter taps to 105, but reduces the ripple to 1 dB.

Since both the total PFIR taps for the DUC and DDC are greater than half the maximum PFIR taps, filters must be symmetric in the PFIR coefficient memory space. This implies the latency is fixed, regardless of the number of PFIR taps in the design (up to the maximum).

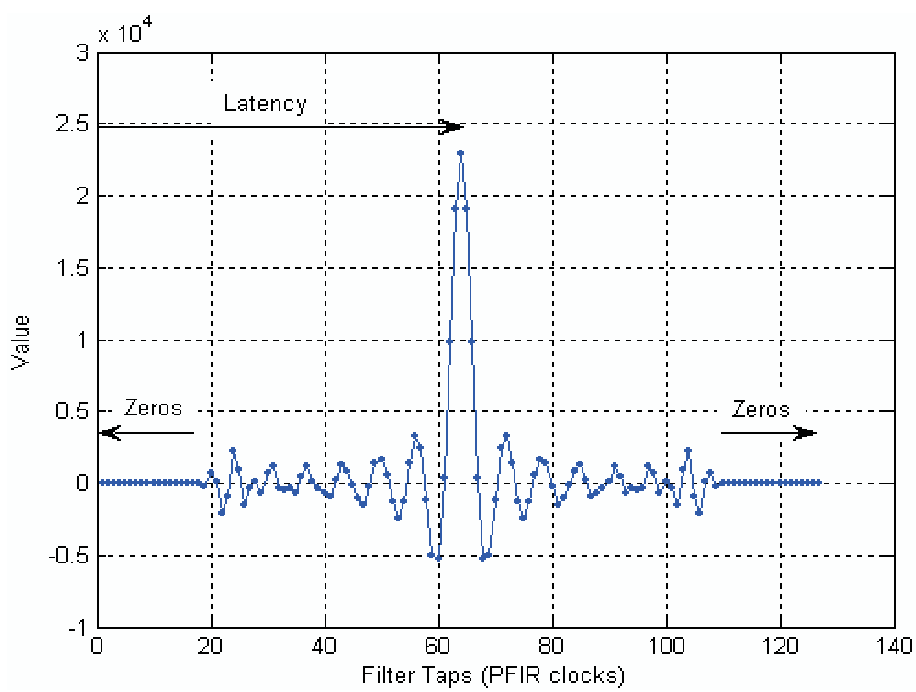


Figure 48. Filter Latency

So without any penalty, make the filter requirements more stringent, such as reduce the transition band. By trial and error, reduce the Stopband Frequency to 6.46 MHz and still design the filter.

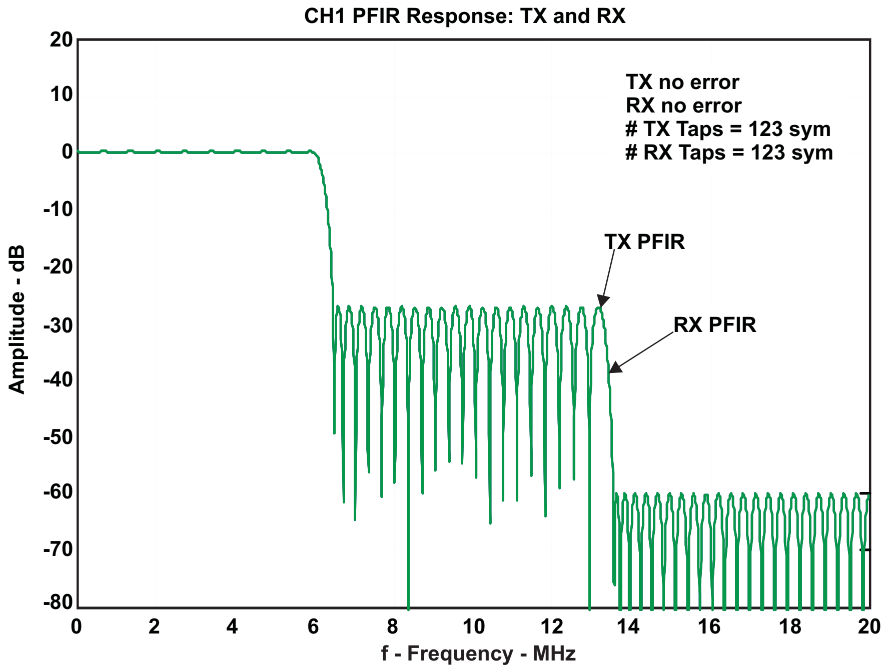
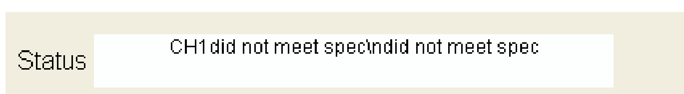


Figure 49. Filter with Reduced Stopband

With this target, the number of DDC and DUC PFIR taps are both 123 taps (before adding 4 taps for the CIC compensation), at the maximum for CIC decimation of 4. Reducing the Stopband Frequency further, to approximately 6.4 MHz, gives an error in the **Status** area, indicating the filter requirements are not achievable:



8 Programming the TSW4100

8.1 Connecting an input source and output analyzer

To match the test below, connect a 100 MHz, 0 dBm tone to the ADC input SMA. The IF of the channel is tested at 95 MHz with a 12 MHz bandwidth, so 100 MHz is within the channel passband. Ideally this tone should be filtered to reduce spurious products outside the 80 to 160 MHz Nyquist band of the ADC. Removing unwanted output harmonics is described later in Section 8.7.

Connect the DAC output SMA to a spectrum analyzer.

8.2 Program clock PLL and DAC

The first step in programming the TSW4100 is to program the clock PLL and DAC. This procedure assumes the installation of the TSW4100GUI in Section 4.4.

1. Apply power to the TSW4100. Connect the USB and parallel port cables.
2. Before programming the GC5016 DDC and DUC, perform the DAC5688 stand alone test.
3. Select the *Load Settings* button and load the file TSW4100_DAC_CDC_example_1.txt, as was done in section 5.2.
4. **Click on the DAC5688** Register button. The Input tab should now be displayed. In the Input Options window, change the Format from 2's compliment to offset binary. The DAC5688 will now be operating in stand alone mode.
5. Verify there is an output tone at SMA connectors J11 and J12 at 120 MHz with approximately 4 dBm power and 70 dBc SFDR between 80 and 160 MHz per Figure 50.

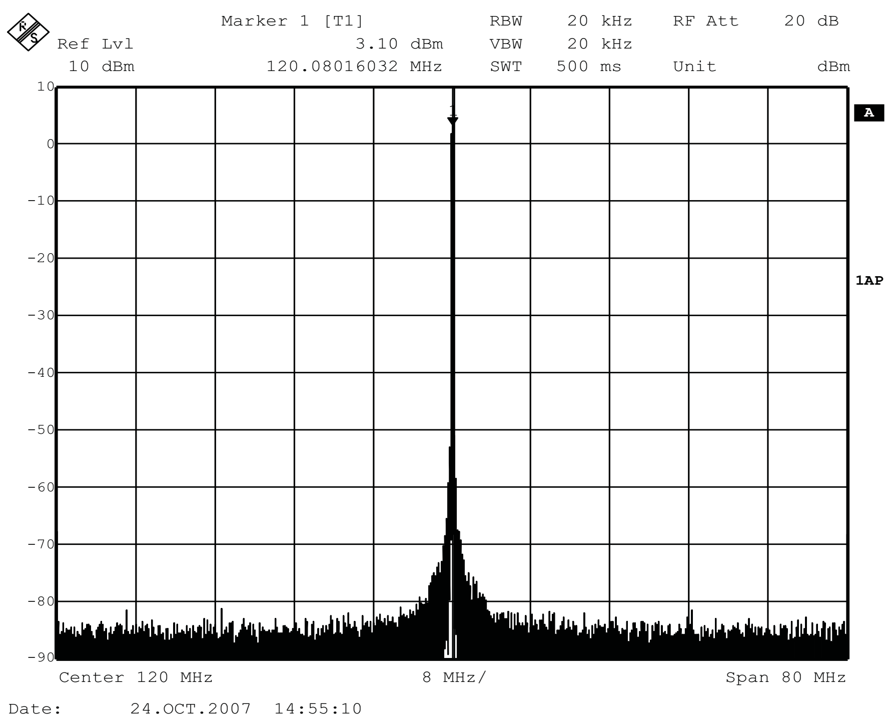


Figure 50. DAC Stand Alone Test Spectrum

6. Now program the DAC5688 normal operation as described in Section 5.3 by changing the output **format** back to *two's complement*. This should result in removing the tone.

8.3 Programming the DUC and DDCs

Following the filter design steps in Section 7 the TSW4100 GUI should look like Figure 51. If the settings are different, adjust the settings to match Figure 51.

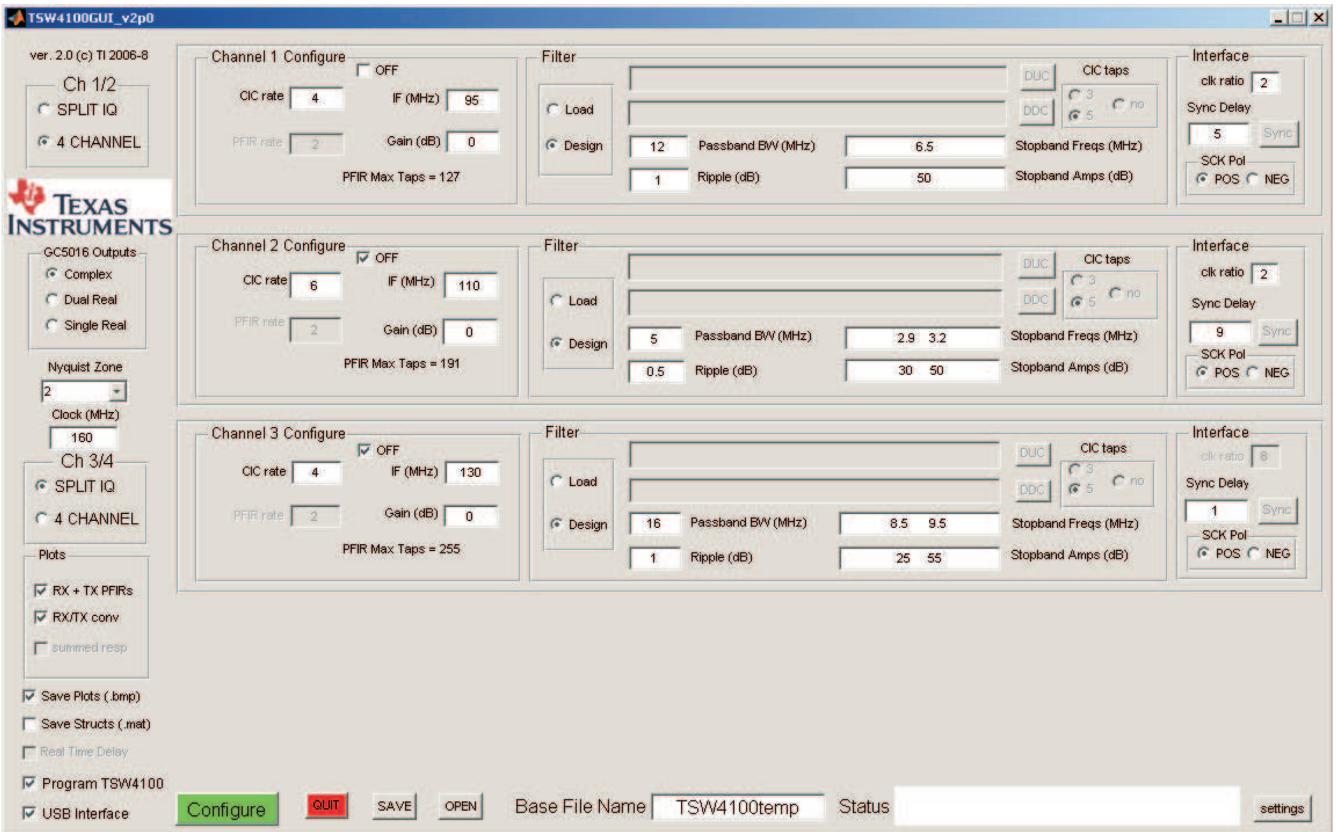


Figure 51. TSW4100 Interface with Filter Design Settings

The **Sync Delay** setting of 5 controls the delay between the start of channel 1 in the DDC and the start of channel 1 in the DUC, and is critical to align the timing of the (interleaved I and Q) data transfer between the DDC and DUC for each channel in the 4 CHANNEL modes.

1. Change the **Sync Delay** in the Channel 1 Interface to *5*.
2. Select the **Real Time Delay** and **Program TSW4100** check boxes in the interface lower left corner. These settings are also saved in the filename *C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example1_config.mat*.
3. Click *Configure*. The filter design starts. After the design is complete, the GUI programs the DDC, followed by the DUC. These actions display in the **Status** area. After *Finished* displays in the **Status** area, the user should see the output spectrum in Figure 52.

The spectra should have a single tone present at exactly the same frequency as the input. The output amplitude should be approximately –10 dBm, reflecting 7 dB loss between the ADC and DAC full scale and another 3 dB loss due to cables, transformers, and so forth.

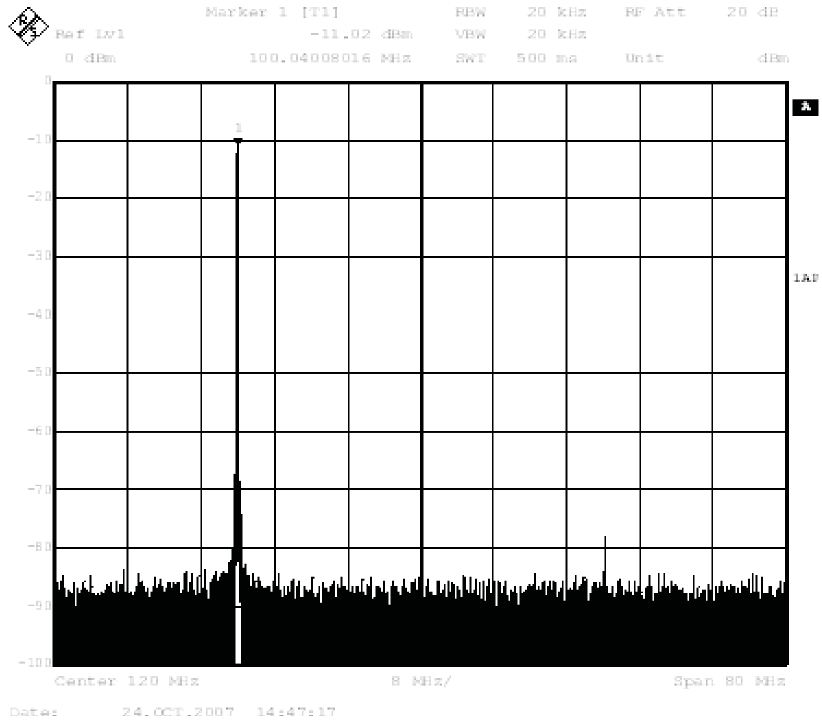


Figure 52. Filter Design Output Spectrum

8.4 Setting the Sync Delay for a Channel

In 4 channel mode, the DDC I and Q data is transferred interleaved to the DUC. The GC5016 is the master of the interleave timing in both DDC and DUC modes — the DDC sends an indication with the frame strobe signal of when the I and Q data are present, and likewise, the DUC sends an indication with the frame strobe signal of when I and Q data should be present, see Figure 53. Since neither chip can use the others frame strobe as an input, a synchronization delay is needed between the DDC and DUC to align the DDC output I and Q samples to the DUC input I and Q samples.

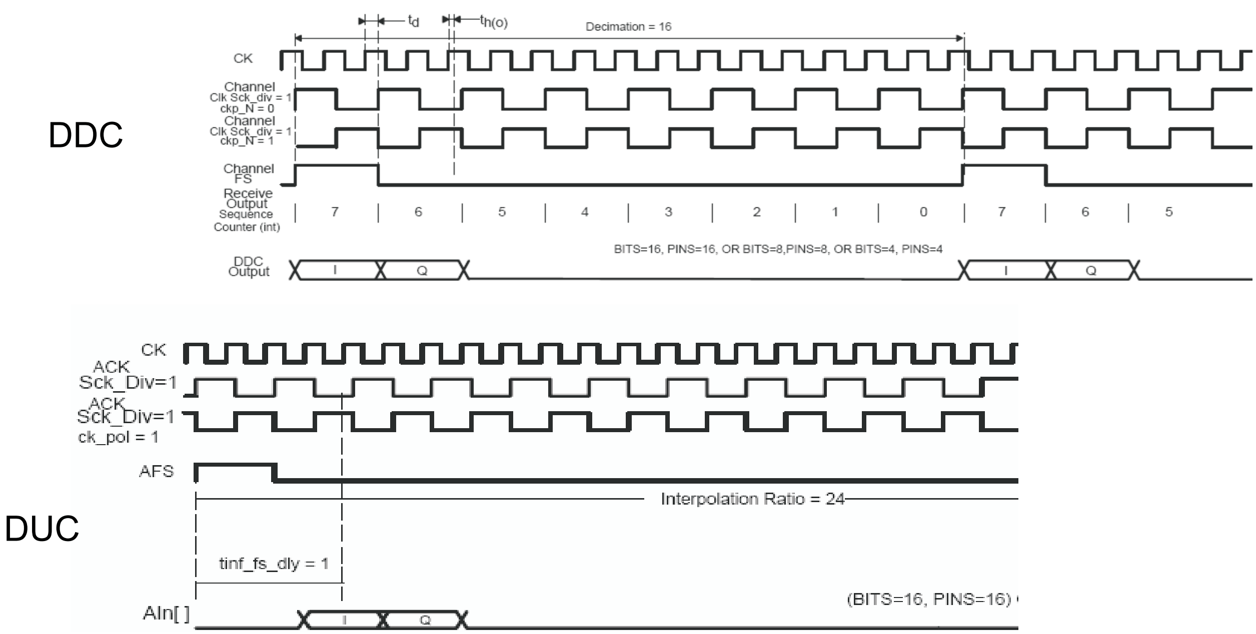


Figure 53. Proper DDC Output and DUC Input Timing Alignment

Similarly, in splitIQ mode, where I and Q are output in parallel, the DDC output data is held a maximum of 16 clock cycles. Therefore, if the decimation ratio exceeds 16, synchronization of the DDC output and DUC input is needed to make sure the DDC output data is present during the input time of the DUC. See Figure 54.

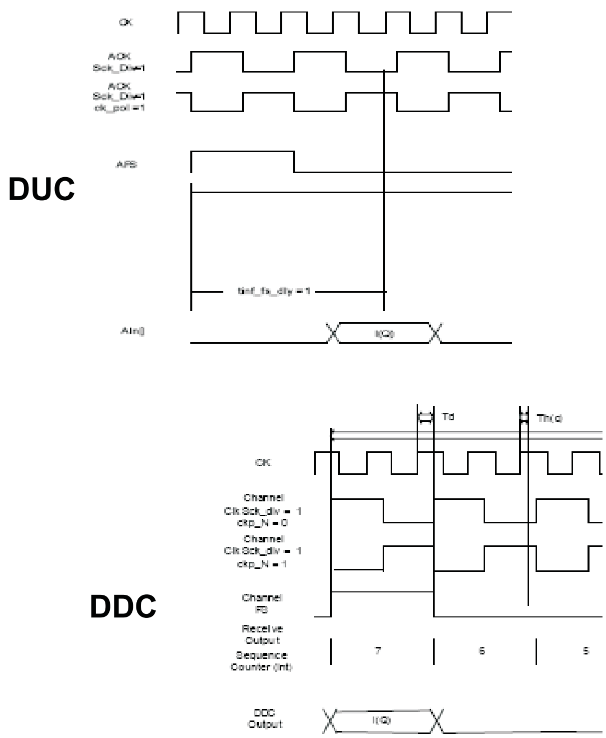


Figure 54. DUC Input Time

The TSW4100 can send an external sync signal to the SyncA input of both the DDC and DUC. The SyncA is used to individually synchronize each DDC or DUC channel, which for a given configuration will result in a deterministic and repeatable delay between the DDC SyncA signal and DDC output timing or DUC SyncA signal and DUC input timing. A time delay between the DUC SyncA signal and the DDC SyncA signal of up to 256 clock periods can be programmed using the TSW4100GUI. By adjusting the delay between the DUC and DDC SyncA signals, the output timing of the DDC can be adjusted to be properly aligned with the input timing of the DUC. Once the delay is found for a given configuration, it should be repeatable for a given channel configuration.

Output channels 1 and 2 of the DDC are routed through and latched by the FPGA using the DDC divided output clocks. As a result, when adjusting the DDC output data to DUC input timing using the SyncA delay, the timing of the DUC input data will only shift in steps of one divided clock cycle. To allow finer control for these channels, the polarity of the divided clock can be inverted from positive to negative, which results in a cycle shift in the DDC output data and DUC input timing. This is illustrated in the examples below.

There are two methods to find the proper DDC and DUC timing — either by observing the output signal with a spectrum analyzer or using an oscilloscope to directly monitor the DDC & DUC framestrobes, input clocks and data bits (LSB). The spectrum analyzer method is convenient as it does not require additional equipment, but can be tedious for larger decimation values. For a CIC decimation of > 8 (overall decimation of 16), it is recommended to use the oscilloscope method.

8.5 Calibrating the Sync Delay Using an Oscilloscope

For this example, the starting configuration example_200kHz_load_start_config.mat was loaded and the TSW4100 programmed using the instructions in Section 8.4. Make sure the setting for the Nyquist Zone is set to "2" before running this configuration. After configuring the TSW4100, verify that the “Real Time Delay” box is checked, which allows immediate update of the DDC to DUC delay without completely reprogramming the parts.

To calibrate each channel 1–4 corresponding to the DUC inputs A–D, oscilloscope probes should be connected to the appropriate frame strobe (AFS/BFS/CFS/DFS) , DUC input clock (ACK/BCK/CCK/DCK) and the DUC input LSB (A0/B0/C0/D0). All these signals are available on test points near the DUC device (see Figure 55). The DUC input LSB test points are small pads and the input clock and frame strobe are loops.

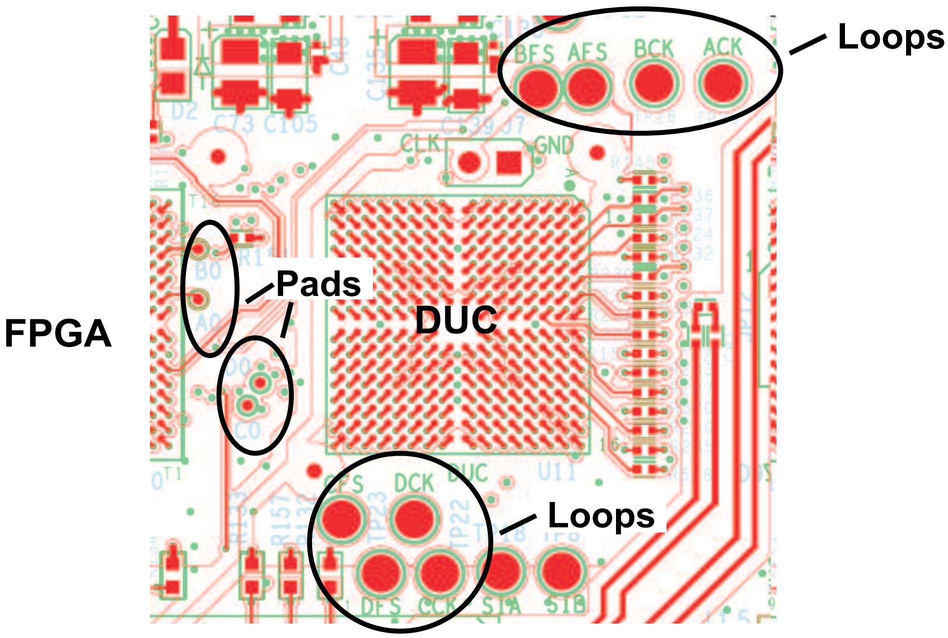


Figure 55. Test Points

Starting with Channel 1, connect 3 probes to AFS, ACK and A0. The oscilloscope display should look like this:

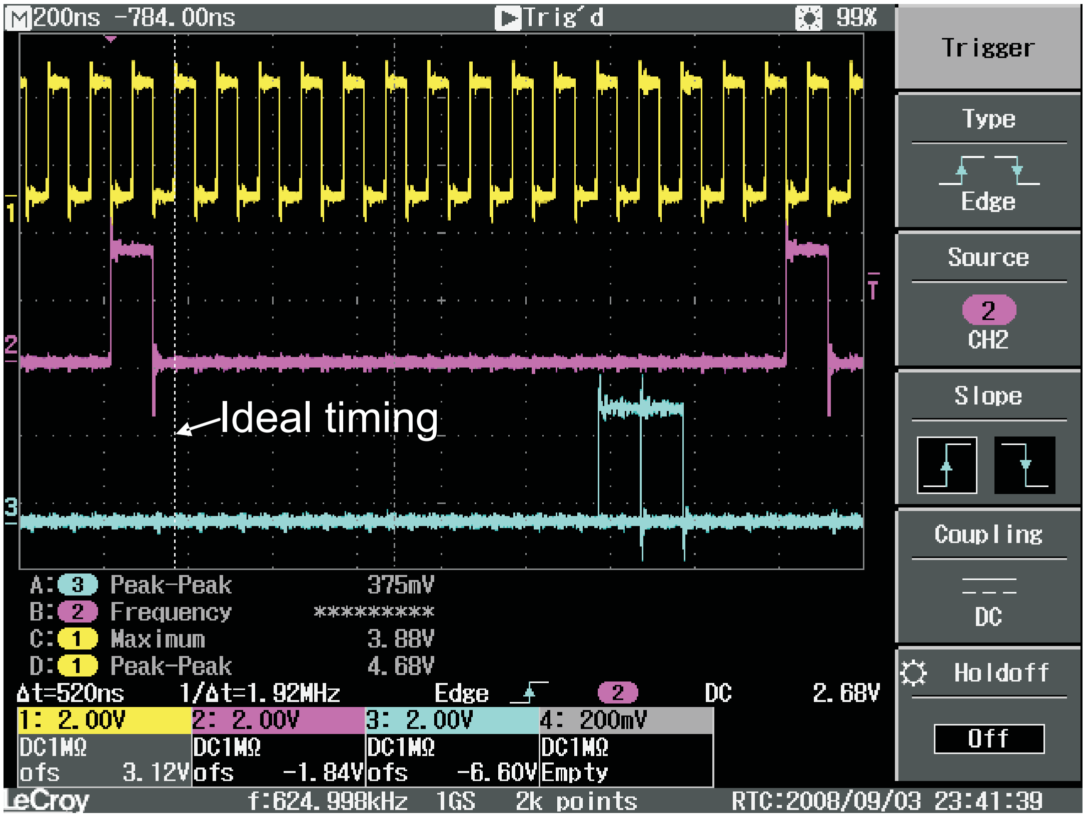


Figure 56. Starting Interface Timing for Channel 1

The traces are as follows: yellow = ACK, pink = AFS and blue = A0. In this case, with the default Channel 1 sync delay of 0, the data signal A0 comes 10.5 divided clock cycles too late, compared to the dashed cursor showing ideal timing. Since the data can only be delayed (not advanced) by the sync delay, and the total number of divided clocks for an AFS cycle is 16, delay the data 5.5 divided clock cycles. As discussed in Section 8.4, the sync delay will only result in delays that are integer multiples of the divided interface clock period. To align the timing, first delay the data by 6 divided clock cycles with an SCK ratio of 16, or 6×16 = 96 high speed clock cycles by setting the sync delay to 96 and pressing the sync button. This should result in a shifting of the data A0 to divided clock cycles after AFS, as shown in the oscilloscope display in Figure 57:

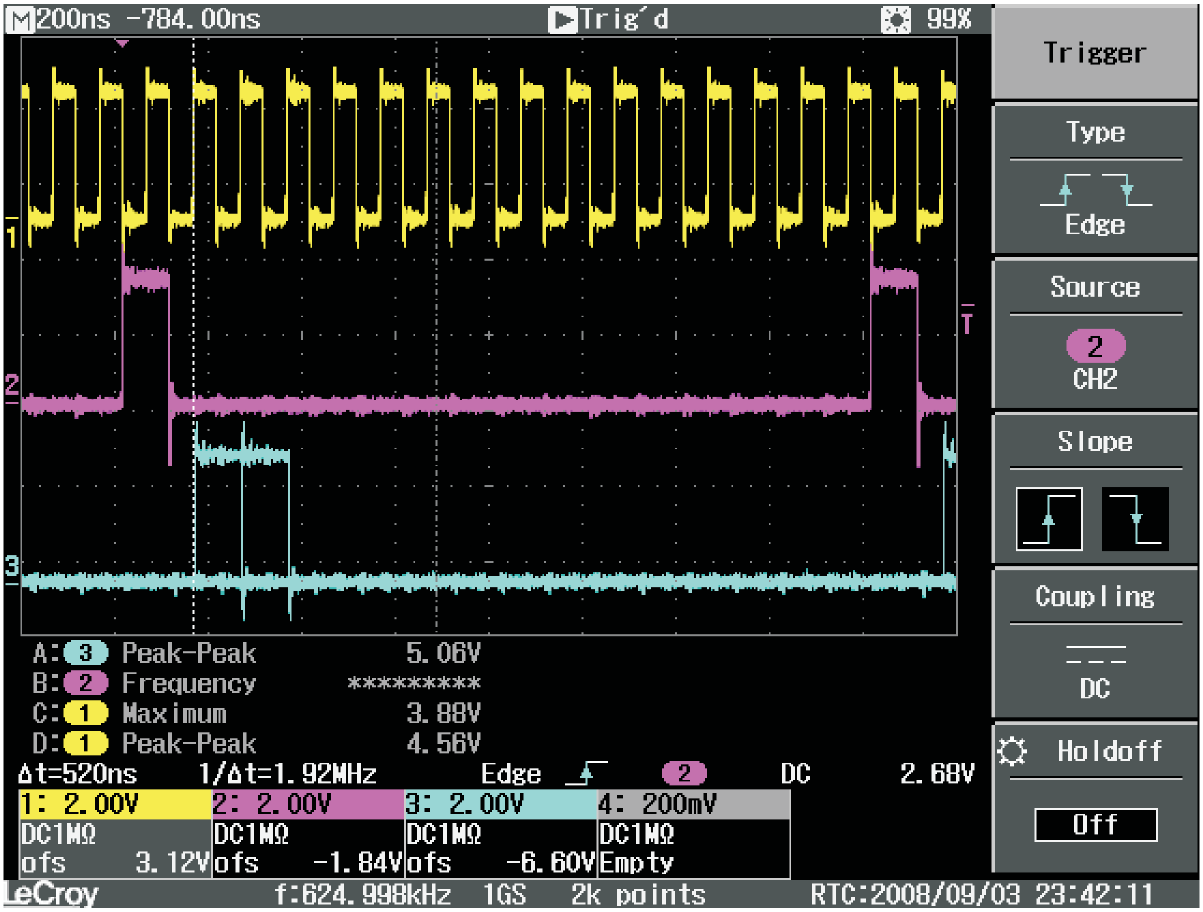


Figure 57. Channel 1 Interface Timing After a Sync Delay of 96

To backup the data clock cycles (again, this is only needed for channels 1 and 2, not 3 and 4, where the minimum delay step size is 1 divided clock cycle), change the SCK polarity for channel 1 to negative and resync. This should shift the data to the appropriate time as shown in the oscilloscope display in Figure 58.

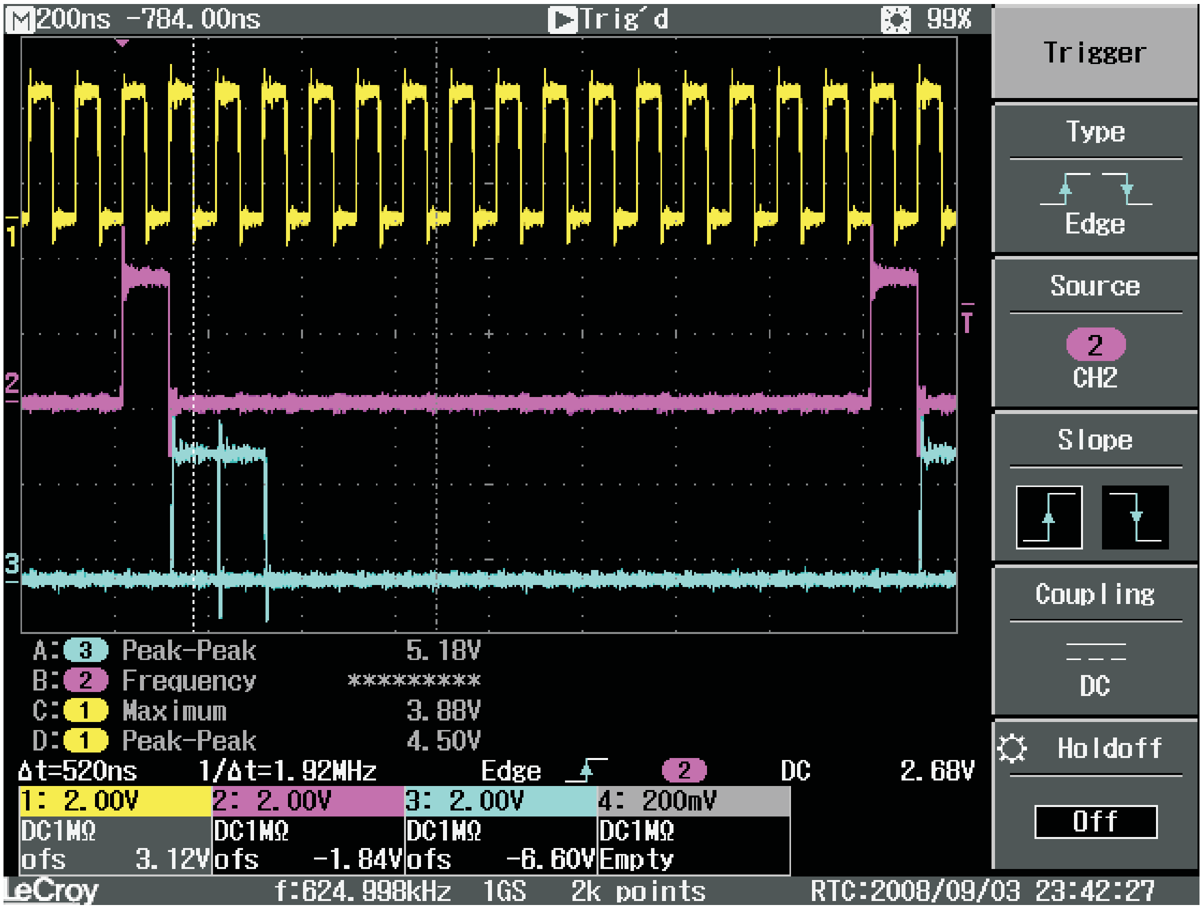


Figure 58. Channel 1 Interface Timing With a Sync Delay of 96 and Negative SCK Polarity

Finally, to verify that a sync delay of 96 is repeatable, find the middle point of the sync delay setting that has the correct delay. For this board, the delay settings for 83 to 96 have the correct delay, so the final delay setting should be the mid-point of 90.

The timing for Channels 1 and 2 are identical, so if the decimation and filters are identical, the same setting should work for channel 2.

Channels 3 and 4 are easier to align, as the DUC data to DUC framestrobe delay can be controlled to 1 fast clock cycle. Using the default settings from the configuration file loaded previously and connecting the oscilloscope to CFS, CCK and C0, the user finds that the data is again out of timing alignment with the framestrobe (Figure 59):

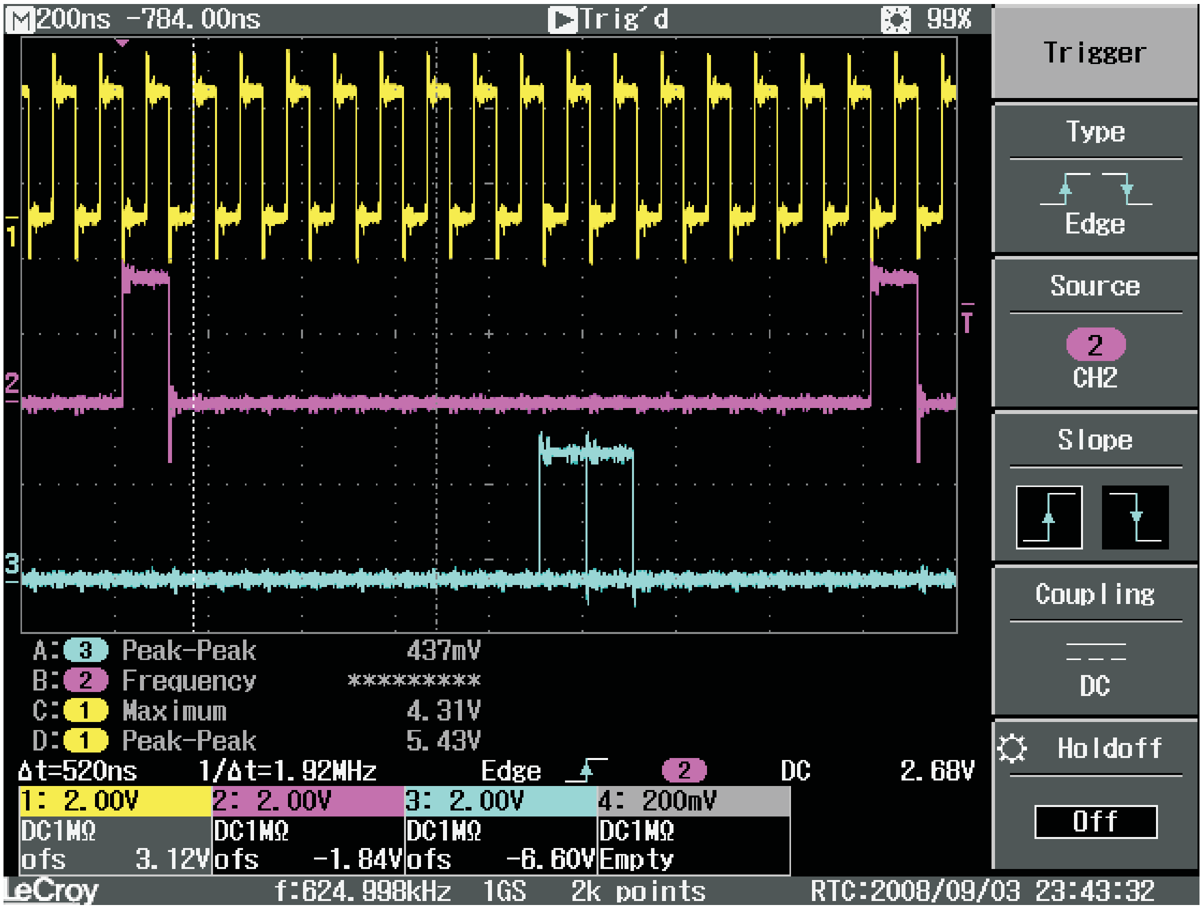


Figure 59. Starting Interface Timing for Channel 3

By trial and error, it is determined that the ideal sync delay is 129, which results in the following oscilloscope display shown in Figure 60.

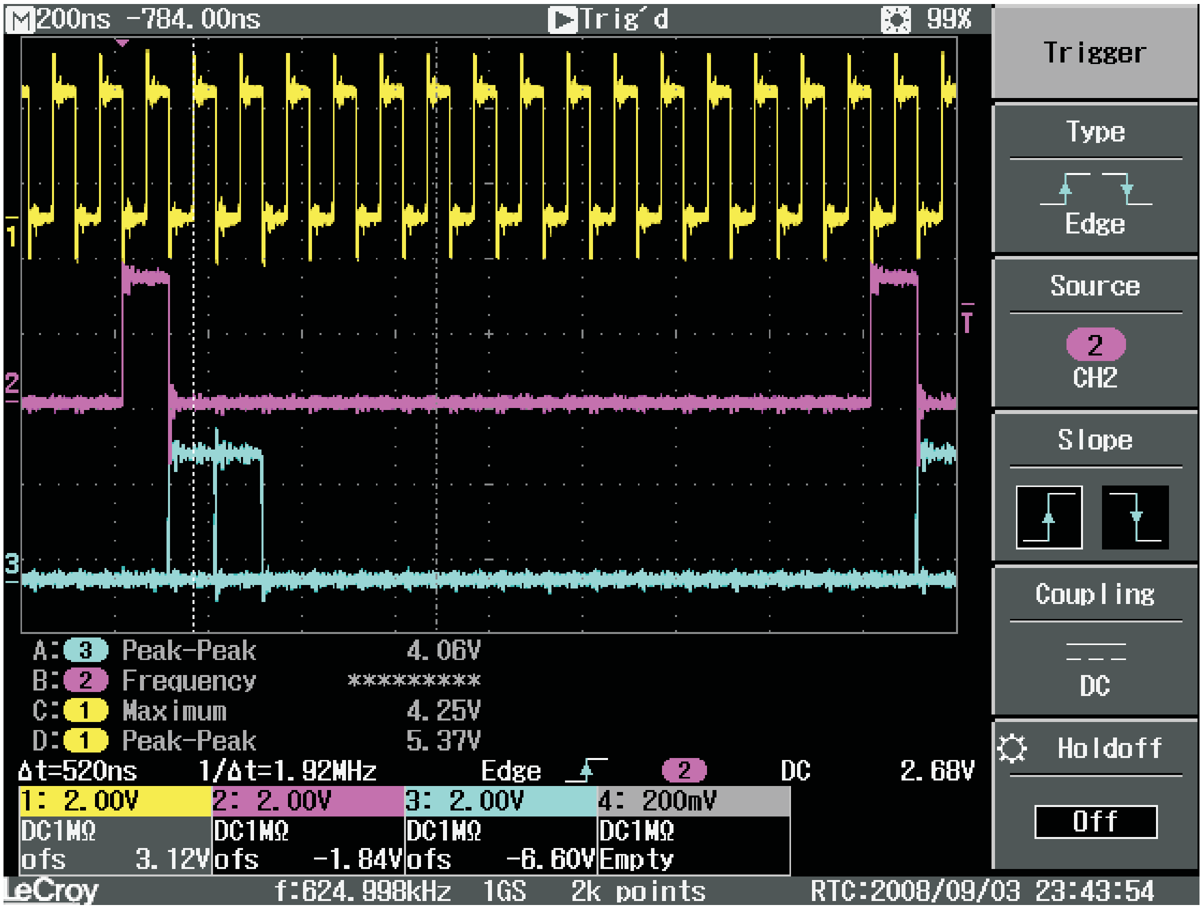


Figure 60. Channel 3 Interface Timing With a Sync Delay of 129

Note that the timing for channel 4 will be identical to channel 3 if the decimation and filter are the same. The user can now load the configuration file called configuration example_200kHz_load_final_config.mat, which will load the default sync delay values as mentioned above.

The oscilloscope method can also be used with much lower decimation rates. For example, with a total decimation of 6 and a SCK divider ratio of 2, Figure 61 and Figure 62 show examples of incorrect and correct interface timing:

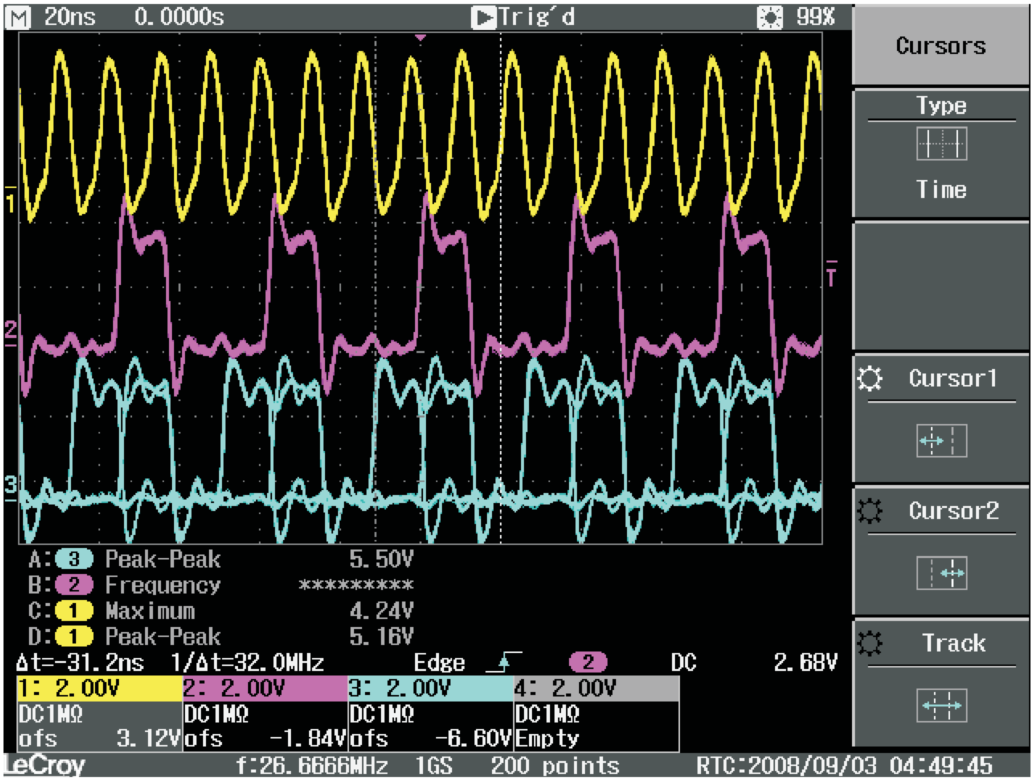


Figure 61. Incorrect Interface Timing for a Decimation of 6 and SCK Divider Ratio of 2

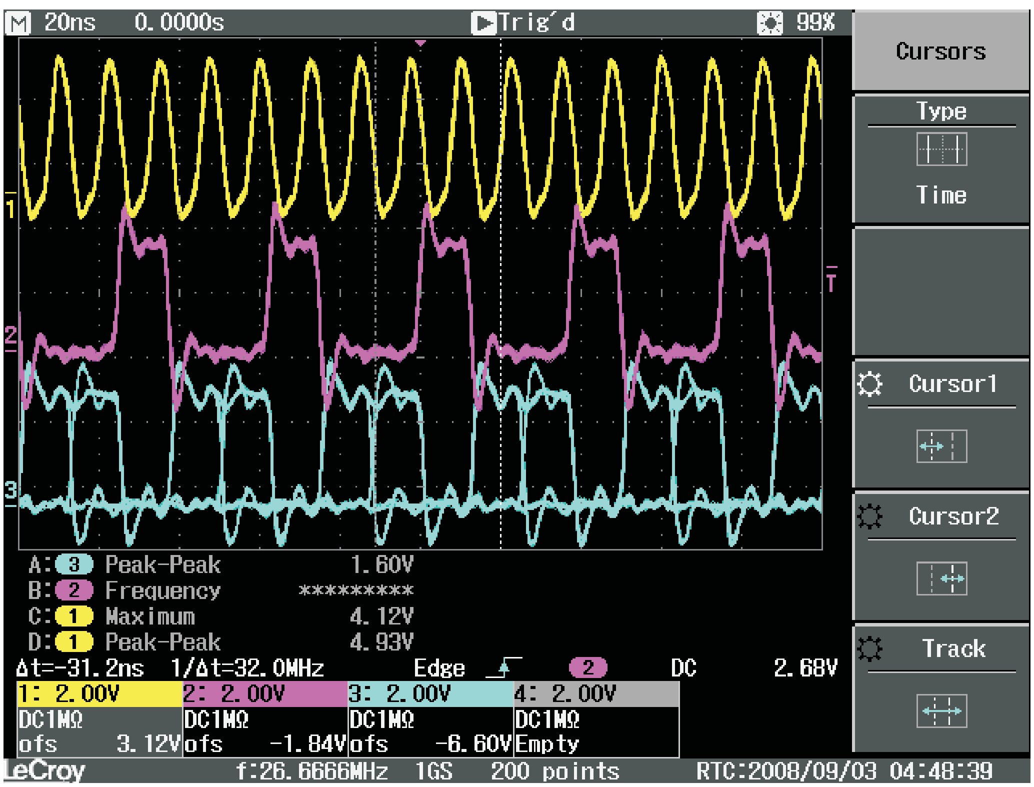
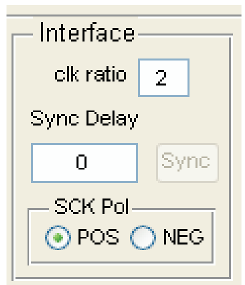


Figure 62. Correct Interface Timing for a Decimation of 6 and SCK Divider Ratio of 2

8.6 Calibrating the Sync Delay Using an Spectrum Analyzer

The correct sync delay can be determined by looking at the TSW4100 output with a single input tone that is set slightly off center of the band center.

Consider the example presented in Section 8.5. In the interface settings, the interface clock ratio is set to 2:



This means that two GC5016 input clock cycles (at 160 MHz) are used for 1 interface clock cycle (80 MHz). See the GC5016 Input Output Mode Application Note (SLWA037) for details on the interleave IQ interface.

For proper data transfer, align the DDC output and DUC input timing to look like Figure 62.

With a decimation/interpolation of 8, there are 8 possible phases between the DDC output data and DUC input timing. With the interface clock ratio of 2, I and Q are held for two input clock cycles. For the DUC input, the I latch and Q latch occur 2 input clock cycles apart. By adjusting the sync delay, find the appropriate timing for the channel. This is represented in Table 6, where each row is an input clock cycle and the 8 possible Sync phases of the DUC are shown.

Table 6.

Clock Cycle	DDC output	DUC Input							
		Phase 1	Phase 2	Phase 3	Phase 4	Phase 5	Phase 5	Phase 7	Phase 8
1	—	I latch	—	—	—	—	—	Q latch	—
2	—	—	I latch	—	—	—	—	—	Q latch
3	—	Q latch		I latch	—	—	—	—	—
4	—	—	Q latch		I latch	—	—	—	—
5	I	—	—	Qlatch	—	I latch	—	—	—
6	I	—	—	-	Qlatch	—	I latch	—	—
7	Q	—	—	-	—	Q latch	—	I latch	—
8	Q	—	—	-	—	—	Q latch	—	I latch
Result	Good/Bad	Bad	Bad	Bad	Bad	Good	Good	Bad	Bad
	Tones	0	0	2	2	1	1	2	2

The correct value of the sync delay is dependent on decimation, filter mode, filter length, etc. and is deterministic and repeatable. As is seen in Table 6, there are two phases that should be “good”. In this case, both I and Q are correctly transferred and a single tone in the spectram above is observed. However, it cannot be predicted ahead of time. For the TSW4100 example above, a value ‘5’ should be correct. However, a design flaw in the timing for the TSW4100 (there is board to board latency uncertainty in the crystal filter for the ADC) means some boards may have slightly different values – this will be corrected in a revised version.

As an example, consider the configuration described above with the decimation ratio is 8, with an input tone offset from the center of the channel. There are 4 phases where only I or Q are transferred (and swapped). Observing the output of these 4 phases, this results in two tones with 6 dB lower power:

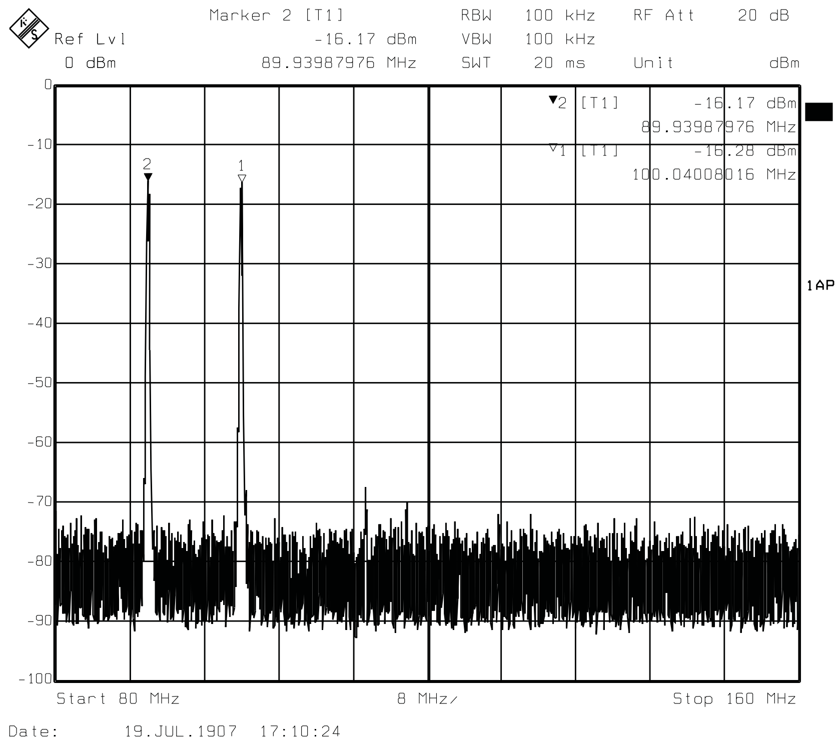


Figure 63. 4 Phases Where Only I or Q Are Transferred

And finally, there are 2 phases where neither I nor Q are transferred. In this case, there is no tone observed in Figure 64.

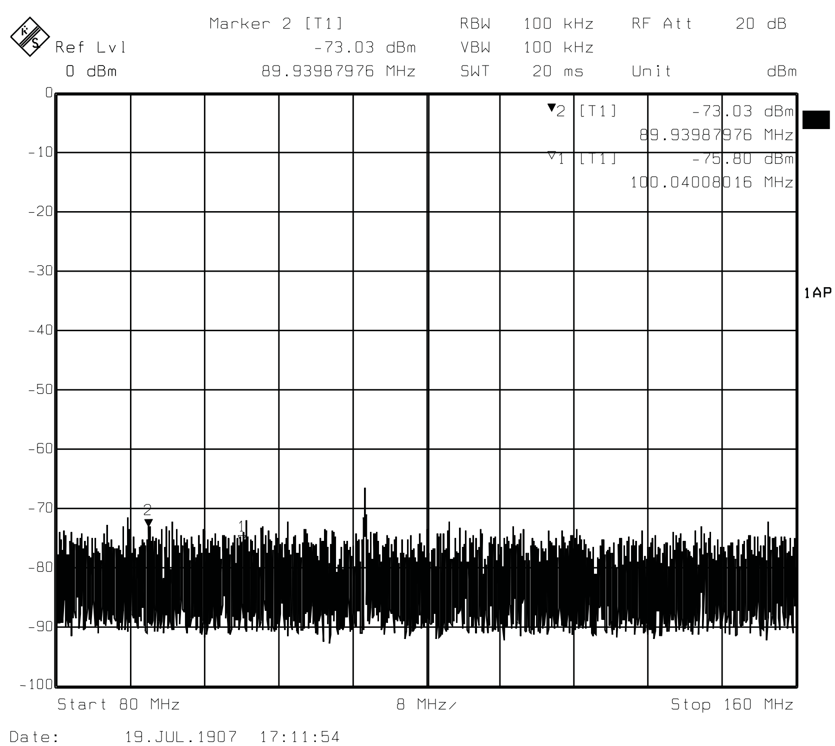
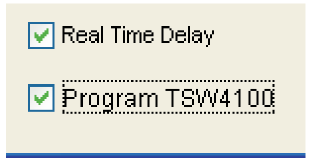


Figure 64. 2 Phases Where Only I or Q Are Transferred

This may appear complicated, but the TSW4100 GUI eases the adjustment and finds the right setting. Note that each channel will require separate adjustment, even if the configurations are the same (this is because 2 channels are routed through the FPGA, which adds a set delay to the data).

Note that for the test, the input tone must be offset from the center of the filter and with the “Real Time Delay” box checked.



Changing the Sync Delay value in the interface box will enable the sync for that channel, send sync pulses to the DDC and DUC with a delay determined by the pull down menu, and then disable the sync.

If either 2 or 0 tones are observed, make sure “Real Time Delay” is checked and adjust the Sync Delay value until 1 tone is observed. At most, only the range of 1 to the decimation ratio need to be tried.

The same steps can be done using a network analyzer. In the case where neither I nor Q are transferred, there will be no signal in the network analyzer. If there is I or Q but not both, the gain will be 6 dB too low, except for a spike at the center as the two tones merge. When set properly, the output power will increase 6 dB.

8.7 Requirement for Nyquist Filtering for the ADC

Even high performance signal generators have harmonics at multiples of the output frequency. Unless a filter is used between the signal generator and the ADC to limit the passband to one Nyquist zone of the ADC (in this case 80 to 160 MHz), these harmonics can alias back into a passband and result in increase spurious output. This is shown in the two spectral plots for Figure 65. On the left, a filter is used for the 100 MHz tone, resulting in the highest spur is at –70 dBm. Without the input filter, the highest spur is at –56 dBm, or 14 dB worse.

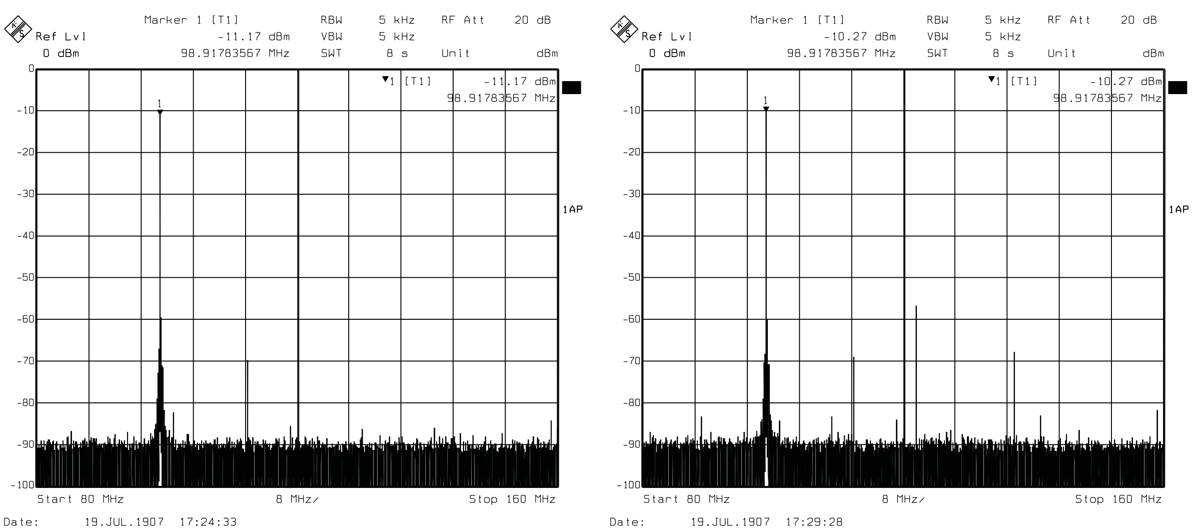


Figure 65. With and Without an ADC Filter to Remove Output Frequency Harmonics

8.8 Adding Other Channels

Although the filter design example was for a single channel, it is easy to test multiple channels simultaneously. To enable the other channels, deselect the **OFF** check box in the Channel N Configure area. This setting is also saved as in the *C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example2_config.mat* example MATLAB settings file.

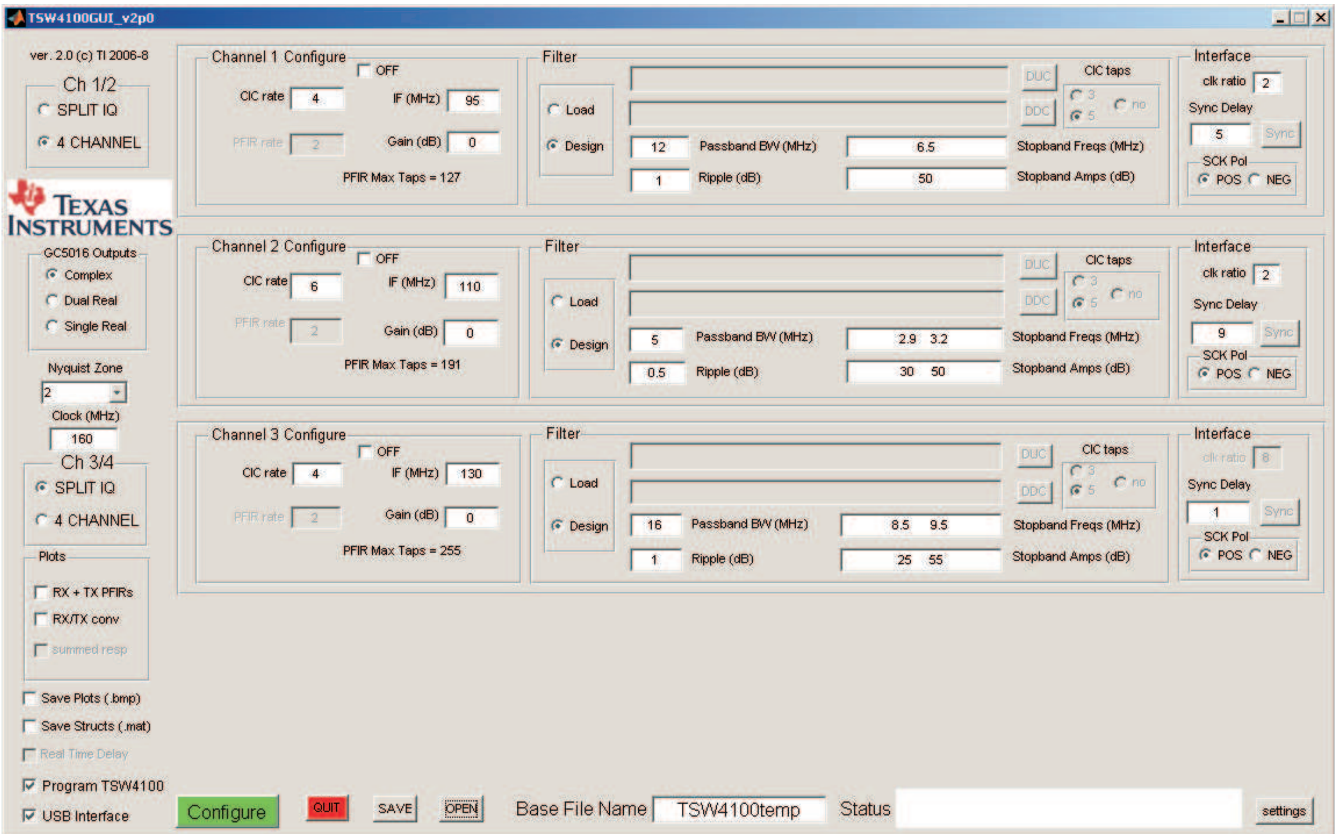


Figure 66. Multiple Channel Configuration

Note: The center spacing and bandwidth should be chosen so that there is no overlap between channels, or else the channels output adds together, resulting in possible signal saturation.

To test the TSW4100 response across the entire Nyquist band (80–160 MHz), the input signal is swept from 80 to 160 MHz while the spectrum analyzer has a trace set to MAX HOLD (blue in Figure 67) and a trace set to clear/write (yellow). Clicking the **Configure** button generates the output (observed after allowing the sweep to complete).

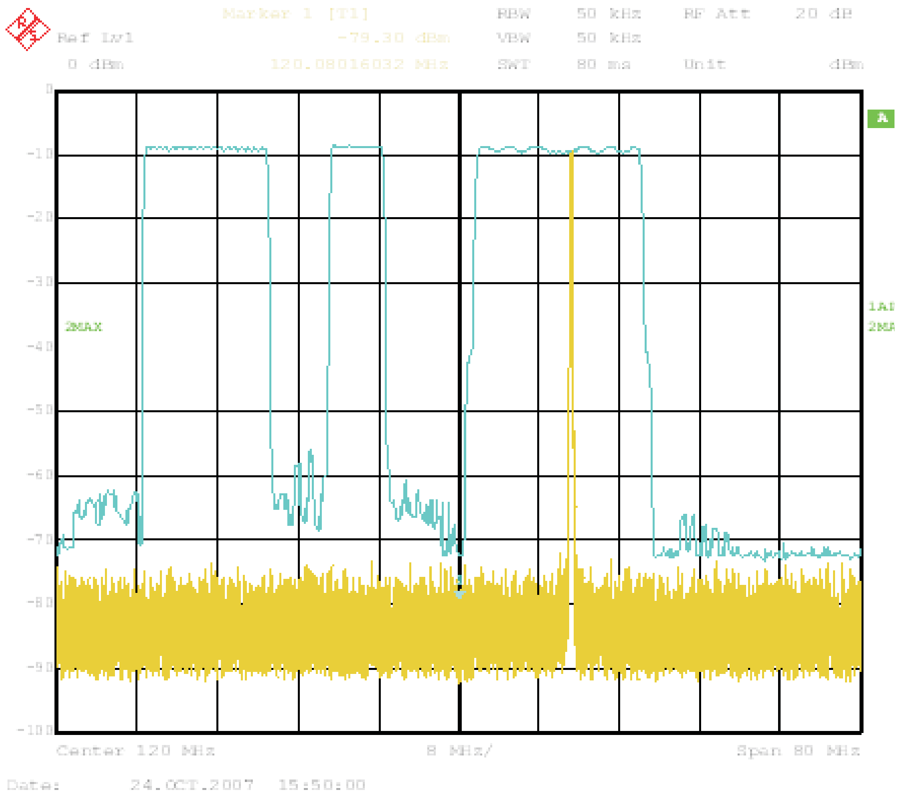


Figure 67. Multiple Channel Example on Spectrum Analyzer

8.9 *Using Other Nyquist Zones*

8.9.1 Third Nyquist Zone Example

The previous example used the 2nd ADC Nyquist Zone (80–160 MHz) for a 160 MSPS clock rate. Other Nyquist zones can be selected in the TSW4100GUI by using the Nyquist Zone drop-down list (Figure 68, under the TI Logo). Figure 68 and Figure 69 show the TSW4100GUI settings and TSW4100 output for a 3rd Nyquist Zone Example. This setting is saved as *C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example3_config.mat* and also on the provided CD. Make sure that the Nyquest Zone is set to "3" before running this example.

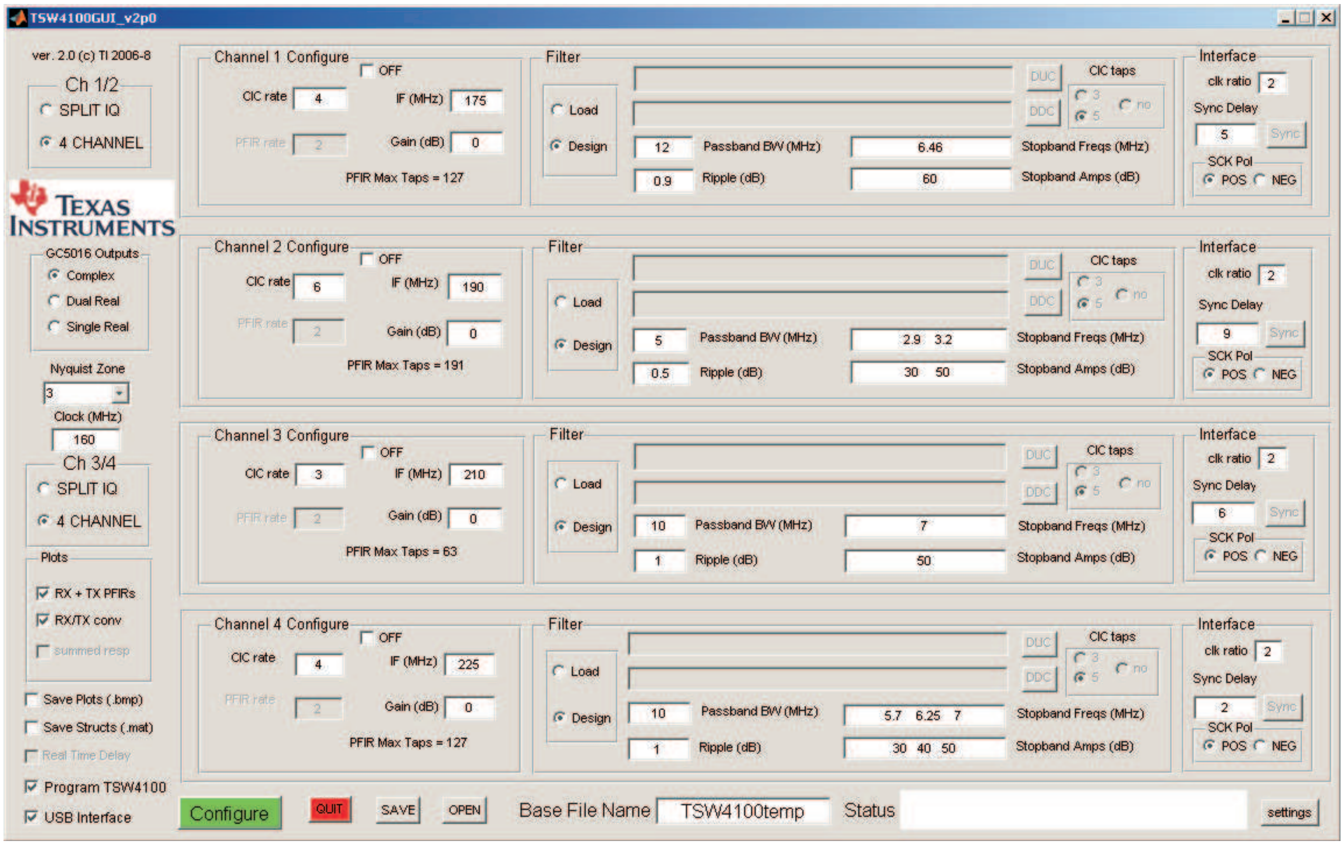


Figure 68. TSW4100GUI Settings to Generate Third Nyquist Zone

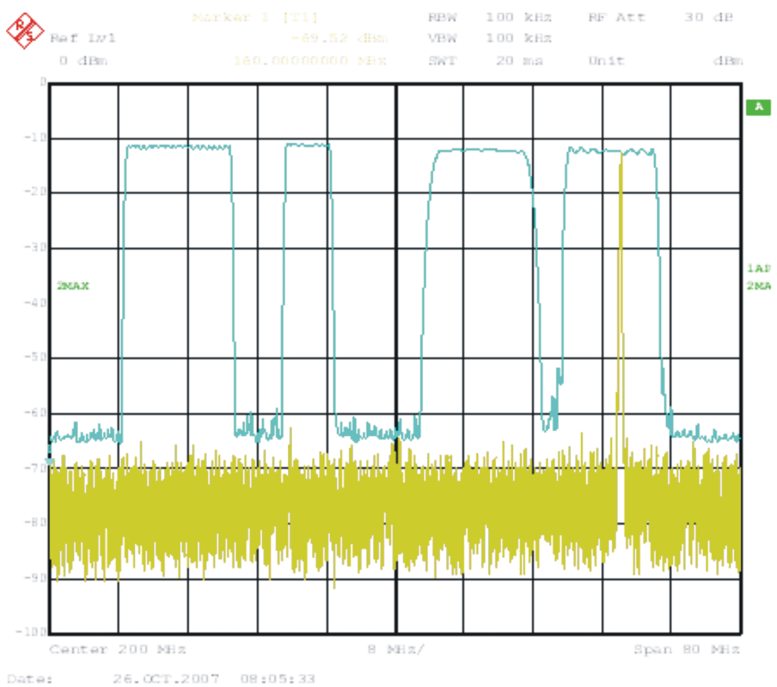


Figure 69. Third Nyquist Zone Example Output Spectrum

Appendix A Firmware Downloading (if updates are needed)

The TSW4100 contains an Altera EP2C8 Cyclone II™ FPGA device (U10) and an Altera EPCS4 reprogrammable serial configuration device (U13). Upon power application or reset (SW4), the EPCS4 programs the FPGA. If firmware (other than what is delivered with the EVM) is used, either the EPCS4 or the FPGA can be reprogrammed through JTAG connector J14.

Reprogram the EPCS4 with these steps:

1. Connect an Altera ByteBlaster II™ parallel port download cable to J14. Ensure pin 1 of cable lines up with pin 1 of J14. Connect the other end to the PC parallel port.
2. Start the Altera Quartus II™ Programming software. The Quartus II application window displays as in Figure A-1.

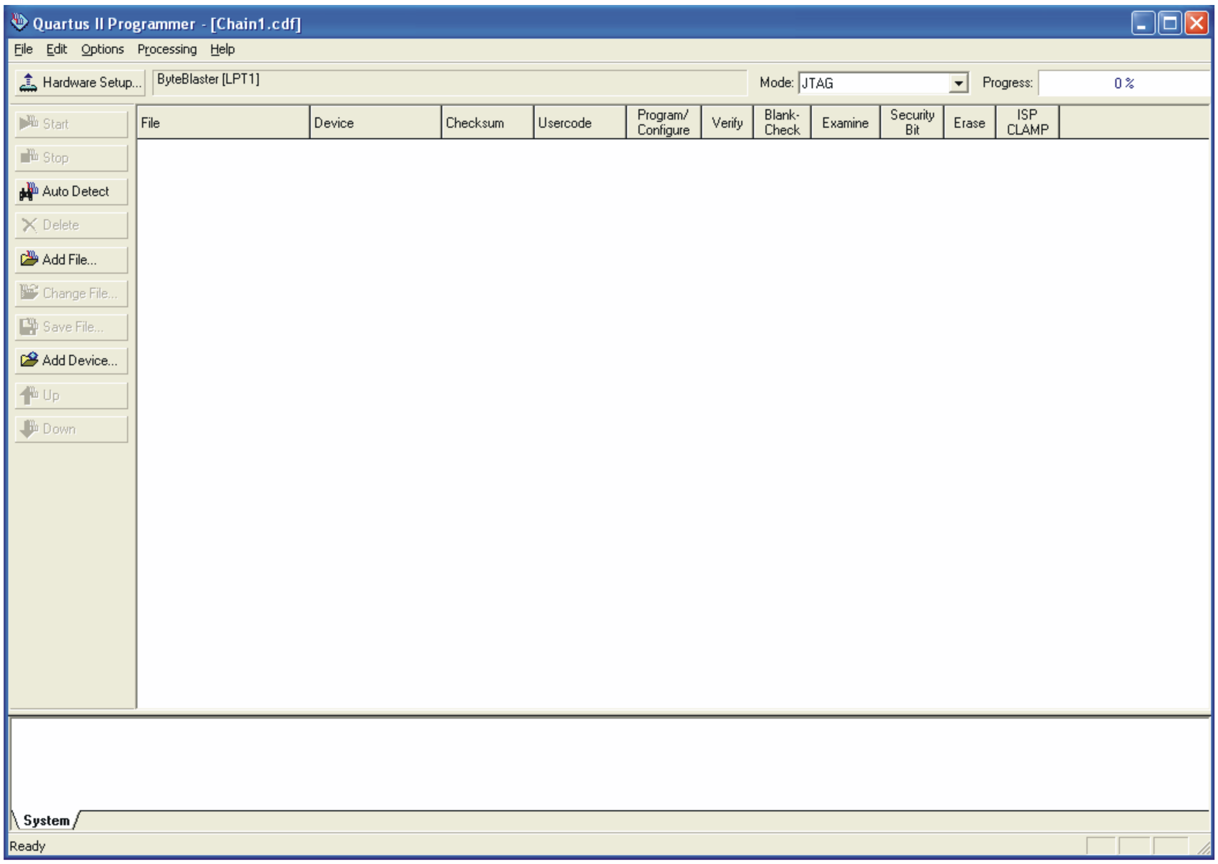


Figure A-1. Quartus II Programming Interface

3. Click **Tools** icon.
4. Select *Programmer* option.
5. Ensure the **Mode** text box uses the *JTAG* selection.
6. Make sure **Hardware Setup** text box has the *ByteBlaster [LPT1]* selection. If not:
   a. Click the **Hardware Setup** text box in the top left-hand corner of the Quartus II application (Figure A-1).
   b. Click the **Add Hardware** button.
   c. In the *Currently selected hardware widow*, select *ByteBlasterMV[LPT1]*. The **Hardware Setup** window should look similar to Figure A-2.
   d. Click **Close**.

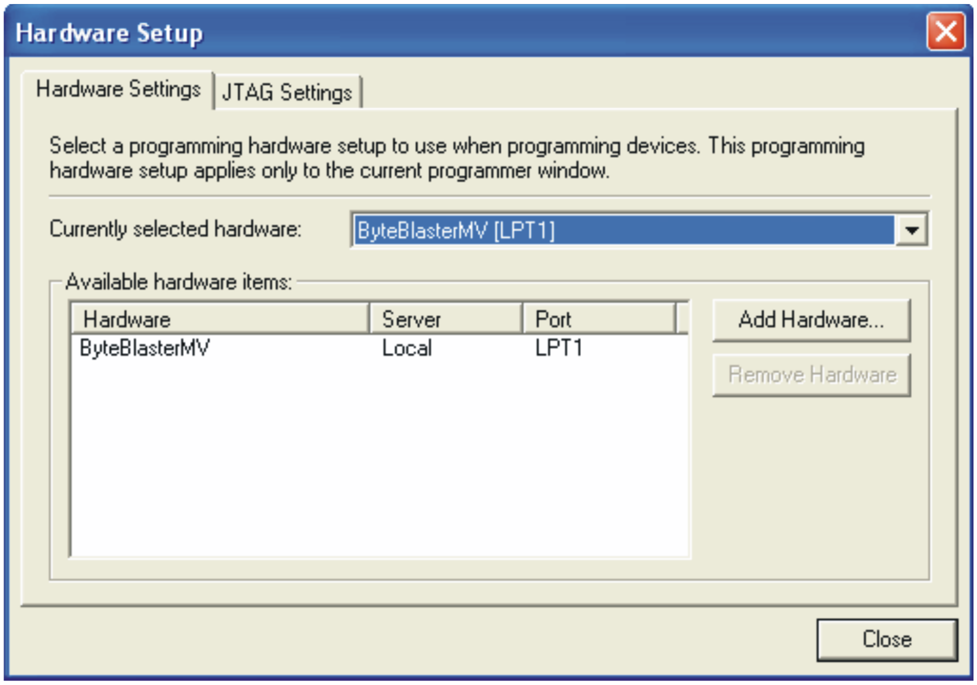


Figure A-2. Hardware Setup Window

7. Click **Auto Detect**. The software should recognize the EP2C8 device, as shown in Figure A-3.
8. Click on the line with the device name to select it. Click **Delete**.
9. To load a new configuration, click **Add File** button.
10. Search for desired *filename.jic* file and double-click to select it.
11. Select the **Program/Configure** check box for both files.
12. Click the **Start** button.

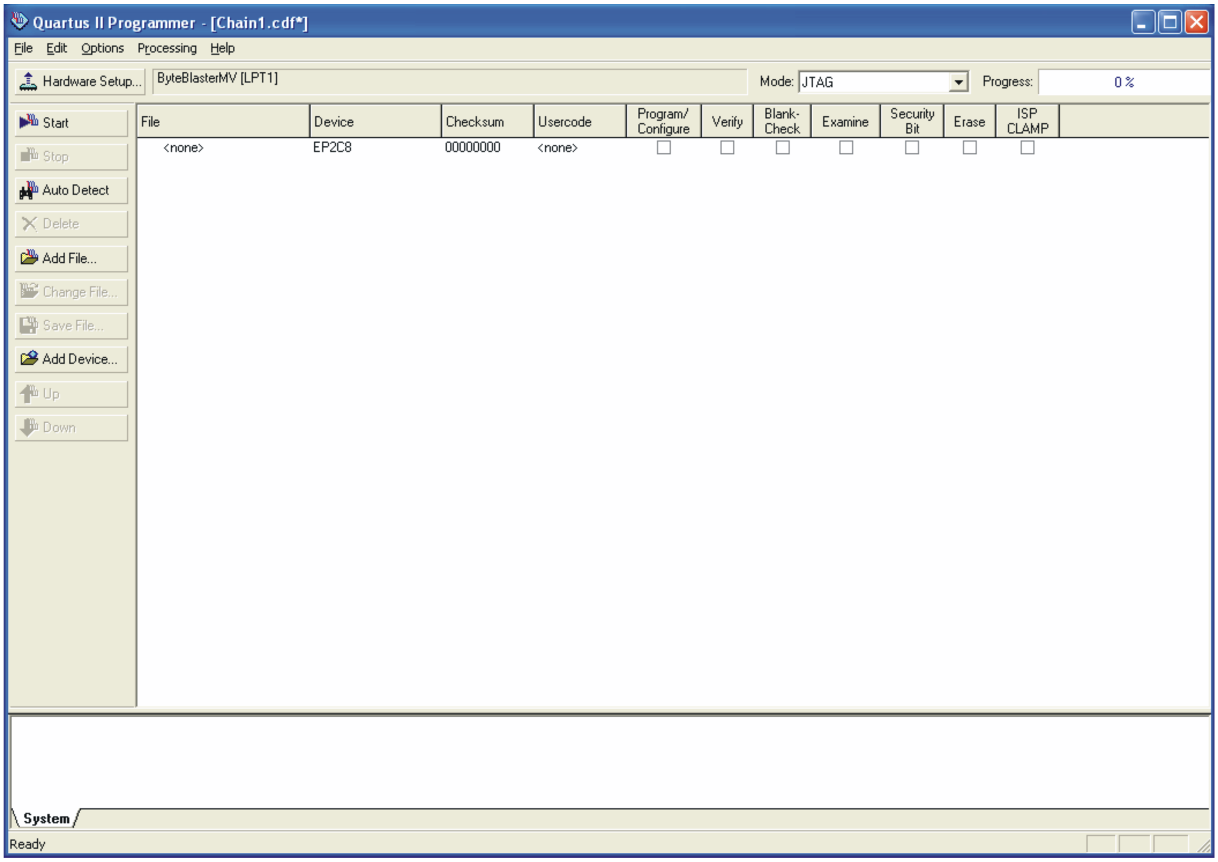


Figure A-3. EP2C8 Device Detected

The software first erases the serial configuration PROM, loads it, and configures the FPGA. The progress indicator increases from 0% to 100%, indicating the configuration progress. Upon completion, LED D2 lights, indicating the FPGA is properly configured.

To reprogram the FPGA directly, repeat steps nine through 12, but use a **.sof* file instead of a **.jic* file. If power is cycled or reset switch SW4 is pressed, the **.sof* file is over written by the **.jic* file loaded inside the serial PROM.

Table A-1. JTAG Connector J14 Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	TCK	I	Clock	2	GND	–	Digital Ground
3	TDO	O	Data from Device	4	VCC	I	System Power
5	TMS	I	JTAG State Machine Control	6	VCC	I	System Power
7	NC	-	No Connect	8	NC	–	No Connect
9	TDI	I	Data to Device	10	GND	–	Digital Ground

Appendix B Bill of Materials

Table B-1. TSW4100 Bill of Materials

Qty	Part Reference	Value	Manufacturer	Manufacturer's Part_Number	Note
0	A B C CCK D DCK	PROBE POINT	N/A	N/A	DNI
13	C1 C21 C29 C39 C45 C58 C72 C73 C135 C148 C151 C153 C501	47 µF	Kemet	T494B476M010AT	
145	C3 C31 C36 C38 C41 C44 C48 C49 C50 C51 C52 C53 C54 C56 C57 C61 C62 C63 C64 C66 C71 C78 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C97 C98 C99 C100 C103 C106 C111 C116 C120 C121 C128 C138 C147 C150 C154 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C171 C172 C173 C174 C175 C177 C178 C179 C228 C230 C232 C233 C234 C235 C236 C237 C240 C241 C242 C243 C244 C245 C246 C247 C248 C249 C250 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C261 C262 C263 C264 C265 C266 C267 C268 C269 C270 C271 C272 C273 C274 C275 C276 C277 C278 C279 C280 C281 C282 C283 C284 C285 C286 C287 C288 C289 C290 C291 C292 C293 C294 C295 C296 C297 C298 C299 C300 C301 C302 C303 C304 C305 C344 C345 C346 C347 C349 C350	0.1 µF	Panasonic	ECJ-0EB1C104K	
1	C4	1.0 µF	Panasonic	ECJ-1V41E105M	
6	C5 C77 C80 C81 C82 C96	0.01 µF	Panasonic	ECJ-0EB1E103K	
11	C6 C7 C8 C9 C10 C11 C12 C13 C209 C213 C306	0.1 µF	Murata	GRM188R71C104KA01	
25	C24 C25 C26 C28 C34 C37 C40 C43 C47 C60 C107 C130 C134 C140 C141 C145 C146 C156 C157 C168 C170 C189 C217 C227 C239	10 µF	Panasonic	ECS-T1AX106R	LOW ESR
34	C27 C30 C32 C123 C124 C188 C190 C191 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C211 C212 C214 C215 C218 C219 C220 C221 C222 C223 C224 C225 C229 C231 C307 C500	0.1 µF	Panasonic	ECJ-0EB1A104K	
14	C33 C35 C42 C46 C59 C65 C105 C129 C139 C149 C152 C155 C348 C351	10 µF	Panasonic	ECJ-3YB1C106K	
10	C55 C67 C68 C69 C70 C79 C83 C84 C101 C122	10 µF	Kemet	T494A106M016AS	
4	C95 C104 C127 C202	.001 µF	Panasonic	ECJ-0EB1E102K	
1	C102	560 pF	Panasonic	ECJ-0EB1H561K	
2	C108 C109	0.1 µF	Murata	GRM188R71C104KA01D	

Table B-1. TSW4100 Bill of Materials (continued)

Qty	Part Reference	Value	Manufacturer	Manufacturer's Part_Number	Note
1	C110	22 µF	AVX	TAJA226K010R	
1	C119	100 pF	Panasonic	ECJ-0EB1E101K	
1	C136	0.033 µF	AVX	0402ZC333KAT2A	
1	C137	330 pF	Panasonic	ECJ-0EB1E331K	
2	C169 C183	4.7 µF	AVX	TAJA475K020R	
0	C176	0.1 µF	Panasonic	ECJ-0EB1C104K_DNI	DNI
1	C180	470 pF	Murata	GRM155R71H471KA01D	
0	C181 C205	1.0 pF	Murata	GRM1555C1H1R0CZ01D_DNI	DNI
1	C182	220 pF	Murata	GRM1555C1H221JA01D	
4	C187 C216 C226 C238	2.2 µF	AVX	TAJT225K035R	
1	C203	1.0 µF	Panasonic	ECJ-0EB1A105M	
2	C204 C206	22 pF	PANASONIC	ECJ-0EC1H220J	
4	C383 C384 C387 C388	47 pF	Panasonic	ECJ-1VC1H470J	
2	C385 C386	10 nF	Panasonic	ECJ-1VB1C103K	
8	D1 D2 D4 D5 D6 D7 D8 D9	LED GREEN	Panasonic	LNJ306G5UUX	
1	D3	LED RED	Panasonic	LNJ206R5RUX	
21	FB1 FB2 FB6 FB7 FB8 FB9 FB10 FB11 FB12 FB13 FB14 FB15 FB16 FB17 FB18 FB19 FB20 FB21 FB22 FB23 FB24	68	Panasonic	EXC-ML32A680U	
1	FL1	160 MHz	Epson Toyocom	TF2-G0EC2	
2	J1 J2	TSM-117-01-S-DV-LC	SAMTEC	TSM-117-01-S-DV-LC	
1	J3	CONN JACK PWR	Switchcraft	RAPC722	
1	J4	BANANA_JACK_RED	Alectron Connectors	ST-351A	
1	J5	BANANA_JACK_BLK	Alectron Connectors	ST-351B	
11	J6 J8 J9 J11 J12 J13 J16 J20 J21 J22 J23	SMA_END_RND	Johnson Components	142-0761-801	
0	J7 J10	Header_1x2_100	Samtec	TSW-102-07-L-S_DNI	DNI
1	J14	102153-1	AMP/Tyco	102153-1	
1	J15	HTSW-105-07-G-T	SAMTEC	HTSW-105-07-G-T	
6	J17 JP1 JP4 JP5 JP6 JP7	Header_1x3_100_230L	Samtec	TSW-103-07-L-S	
2	J18 J19	Header_1x2_100_230L	Samtec	TSW-102-07-L-S	
1	J24	CON_DB25_RT_F	AMP	745536	
2	J25 J26	USB_B_S_F_B_TH	SAMTEC	USB-B-S-F-B-TH	
2	JP12 JP13	Jumper_1x3_100_430L	SAMTEC	HMTSW-103-07-G-S-.230	
1	L1	240 nH	Toko	LLQ2012-ER24J	
0	L2 L3	56 nH	PANASONIC	ELJ-RE56NJF3_DNI	DNI
1	L9	39	PANASONIC	EXC-ML20A390U	
2	L10 L11	91 nH	Toko	LLQ2012-F91NJ	
1	R10	10 KΩ	Panasonic	ERJ-3EKF1002V	
8	R13 R14 R15 R18 R49 R60 R510 R515	100 KΩ	Panasonic	ERJ-3EKF1003V	

Table B-1. TSW4100 Bill of Materials (continued)

Qty	Part Reference	Value	Manufacturer	Manufacturer's Part_Number	Note
8	R23 R24 R30 R31 R38 R103 R105 R110	1.0 KΩ	Panasonic	ERJ-2RKF1001X	
0	R25 R37 R57 R70 R156 R178	130 Ω	Panasonic	ERJ-2RKF1300X_DNI	DNI
3	R27 R62 R502	15.8 KΩ	Panasonic	ERJ-3EKF1582V	
4	R28 R503 R504 R512	30.1 KΩ	Panasonic	ERJ-3EKF3012V	
9	R32 R33 R82 R86 R89 R92 R93 R96 R206	100 Ω	Panasonic	ERJ-2RKF1000X	
7	R34 R35 R36 R255 R508 R514 R522	750 Ω	Panasonic	ERJ-2RKF7500X	
8	R39 R40 R41 R42 R43 R44 R97 R98	130 Ω	Panasonic	ERJ-2RKF1300X	
96	R45 R46 R48 R63 R67 R68 R69 R71 R72 R75 R76 R87 R90 R91 R101 R106 R107 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R127 R128 R129 R130 R135 R136 R137 R138 R141 R142 R143 R144 R145 R146 R147 R150 R152 R153 R155 R158 R159 R161 R162 R163 R164 R165 R166 R167 R168 R170 R171 R179 R180 R181 R203 R227 R228 R229 R230 R231 R232 R233 R234 R235 R236 R237 R238 R239 R240 R241 R243 R245 R247 R249 R253 R259 R260 R509 R513 R516 R517 R518 R519 R520 R521	22.1 Ω	Panasonic	ERJ-2RKF22R1X	
0	R47	30.1 KΩ	Panasonic	ERJ-3EKF3012V_DNI	DNI
26	R50 R66 R83 R148 R149 R154 R186 R187 R188 R202 R250 R267 R268 R271-R283	0	Panasonic	ERJ-2GE0R00X	
3	R51 R169 R262	0	Panasonic	ERJ-3GEY0R00V	
0	R52 R242 R244 R246 R248	22.1 Ω	Panasonic	ERJ-2RKF22R1X_DNI	DNI
8	R53 R54 R55 R56 R58 R59 R100 R102	82.5 Ω	Panasonic	ERJ-2RKF82R5X	
10	R61 R65 R77 R79 R81 R84 R94 R95 R131 R151	10 KΩ	Panasonic	ERJ-2RKF1002X	
0	R64	1.0 KΩ	Panasonic	ERJ-2RKF1001X_DNI	DNI
1	R73	162	Panasonic	ERJ-2RKF1620X	
1	R74	4.75 KΩ	Panasonic	ERJ-2RKF4751X	
0	R78 R80	82.5 Ω	Panasonic	ERJ-2RKF82R5X_DNI	DNI
0	R85 R139 R140 R174 R175 R507	200 Ω	Panasonic	ERJ-2RKF2000X_DNI	DNI
0	R88 R125 R126 R172 R173 R176 R177 R204 R205 R218 R219 R252 R256 R270	100 Ω	Panasonic	ERJ-2RKF1000X_DNI	DNI
1	R99	100 Ω	Panasonic	ERJ-2RKF1000XI	
0	R108 R185 R189 R222 R223 R251 R263 R264 R269 R284-R296	0	Panasonic	ERJ-2GE0R00X_DNI	DNI
1	R109	300 Ω	Panasonic	ERJ-3EKF3000V	

Table B-1. TSW4100 Bill of Materials (continued)

Qty	Part Reference	Value	Manufacturer	Manufacturer's Part_Number	Note
8	R132 R133 R134 R157 R160 R184 R225 R226	1.0 KΩ	Panasonic	ERJ-3EKF1001V	
0	R182	1.0 KΩ	Panasonic	ERJ-3EKF1001V_DNI	DNI
0	R183 R190 R191 R195 R196 R197 R201	0	Panasonic	ERJ-3GEY0R00V_DNI	DNI
0	R192 R198 R265 R266	60.4 Ω	Yageo	RC0603FR-0760R4L_DNI	DNI
4	R193 R194 R199 R200	100 Ω	Panasonic	ERJ-3EKF1000V	
0	R207	10 KΩ	Panasonic	ERJ-2RKF1002X_DNI	DNI
1	R208	56.2 KΩ	Panasonic	ERJ-2RKF5622X	
0	R209 R217	49.9 Ω	Panasonic	ERJ-2RKF49R9X_DNI	DNI
5	R210 R211 R254 R257 R258	200 Ω	Panasonic	ERJ-2RKF2000X	
1	R511	100 Ω	Panasonic	ERJ-2RFK1000X	
2	R212 R213	49.9 Ω	Panasonic	ERJ-2RKF49R9X	
1	R214	24.9 Ω	Panasonic	ERJ-2RKF24R9X	
2	R215 R216	4.3 Ω	Panasonic	ERJ-2GEJ4R3X	
2	R220 R221	60.4 Ω	Panasonic	ERJ-3EKF60R4V	
1	R224	499 Ω	Panasonic	ERJ-3EKF4990V	
1	R261	93.1 Ω	Panasonic	ERJ-2RKF93R1X	
1	R506	53.6 KΩ	Panasonic	ERJ-3EKF5362V	
4	RN1 RN2 RN3 RN4	22 Ω	Bourns	4816P-001-220	
2	RP16 RP17	ZERO	CTS	742C163000X	
0	SJP1 SJP2 SJP3 SJP8 SJP9 SJP11	JUMPER_1X3_SMT	DNI	DNI	DNI
4	SW1 SW3 SW4 SW5	EVQPJX	Panasonic	EVQPJX04M	
1	SW2	SPST	Grayhill	76RSB04	
2	T1 T2	T4-1-KK81	MINI-CIRCUITS	T4-1-KK81	
3	T3 T4 T5	TC4-1W	MINI-CIRCUITS	TC4-1W	
25	TP1 TP5 TP6 TP8 TP12 TP13 TP14 TP15 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33	RED	KEYSTONE	5000	
6	TP2 TP3 TP4 TP7 TP9 TP16	BLK	KEYSTONE	5001	
5	U1 U2 U3 U4 U6	TPS76701QPWP	Texas Instruments	TPS76701QPWP	
1	U10	EP2C8	Altera	EP2C8F256C7N	
2	U11 U9	BGA_252_GC5016_0	Texas Instruments	GC5016	
3	U5 U7 U20	TPS76733QPWP	TI	TPS76733QPWP	
1	U8	ADS5545	Texas Instruments	ADS5545IRGZT	
1	U12	DAC5688	TI	DAC5688RGC	
1	U13	EPCS4	Altera	EPCS4SI8	
1	U14	SGA-4586	Sirenza	SGA-4586	
1	U15	CDCM7005	Texas Instruments	CDCM7005RGZT	
2	U16 U17	SN74LVC1G125DBVR	Texas Instruments	SN74LVC1G125DBVR	
1	U18	74LVC161284	TI	SN74LVC161284DGG	
1	U19	2111-320MHz	EPSON TOYOCOM	TCO-2111T	

Table B-1. TSW4100 Bill of Materials (continued)

Qty	Part Reference	Value	Manufacturer	Manufacturer's Part_Number	Note
1	U21	FT245RL	FTDI Chip	FT245RL	
1	U22	SN74HC241PW	Texas Instruments	SN74HC241PW	
1	U23	SN74AHC541PW	Texas Instruments	SN74AHC541PW	
0	U24	FT245RL	FTDI Chip	FT245RL	
1	Y1	VTD3-J0BC-10M	VECTRON	VTD3-J0BC-10M000	
0	Y2	VTC4	VECTRON	VTC4_B01C-10M00_DNI	DNI
6	4 - FOR THE STANDOFFS 2 - FOR J24	SCREW PANHEAD 4-40 x 3/8	Building Fasteners	PMS 440 0038 PH	
4		STANDOFF ALUM HEX 4-40 x .500	Keystone	2203	STANDOF F
2	FOR J24	NUT			

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5 V to 6 V and the output voltage range of 0.0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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