

## TPS61175 Data Sheet Errata

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### 1 Errata / Observed Device Behavior

The TPS61175PWP was designed to operate in the pulse-skipping mode at light load condition. However, in one special case, TI has observed that this pulse-skipping mode does not work in some devices. This special case is that the switching frequency setting resistance at the FREQ pin is less than 60kΩ. These affected devices always work in the fixed PWM mode with minimum on-time when the light load requires the pulse-skipping mode operation. This malfunction may lead to output unregulated voltage at light load.

The TPS61175PWP internal circuitry uses a short pulse to skip turning on the switcher in one switching cycle if the output voltage of the error amplifier at the COMP pin is below a threshold. The duration time of this short pulse is related to the switching frequency. The design simulation shows that this short pulse may not be generated due to the IC process variation and/or temperature change if the switching frequency setting resistance at the FREQ pin of the TPS61175PWP is less than 60kΩ, i.e. the nominal switching frequency is set to above 1.6MHz.

### 2 Workarounds

TI has identified two possible workarounds for testing and considerations by our customers in their systems or applications.

1. Lower the switching frequency by using higher than 60kΩ resistance at the FREQ pin. The design simulation shows that the pulse-skipping mode function works well at light load.
2. For those applications using less than 60kΩ resistance at the FREQ pin, apply a minimum load to make the TPS61175PWP always work in the fixed PWM mode. The minimum load is related to the input voltage, output voltage, switching frequency, external inductor value and the minimum on-pulse width. The minimum on-pulse width ( $T_{min\_ON}$  in the datasheet) is 60ns (typical value at 1.2MHz in the datasheet). The design simulation shows the maximum value is 80ns over the full temperature range and process variation. Use [Equation 1](#) or [Equation 2](#) to calculate the required minimum load at the worst case.

$$I_{min\_load} = \frac{1}{2} \times \frac{\left( V_{IN} \times T_{min\_ON} + (V_{OUT} - V_{IN}) \times \sqrt{L \times C_{SW}} \right)^2 \times f_{SW}}{L \times (V_{OUT} - V_{IN})} \quad \text{when } V_{OUT} - V_{IN} < V_{IN} \quad (1)$$

or

$$I_{min\_load} = \frac{1}{2} \times \frac{\left( V_{IN} \times T_{min\_ON} + V_{IN} \times \sqrt{L \times C_{SW}} \right)^2 \times f_{SW}}{L \times (V_{OUT} - V_{IN})} \quad \text{when } V_{OUT} - V_{IN} > V_{IN} \quad (2)$$

Where  $C_{SW}$  is the total parasite capacitance at the switching node SW pin. It could be estimated to 100pF.

### 3 Severity

Medium

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