EVM User's Guide: TCAN5102-Q1

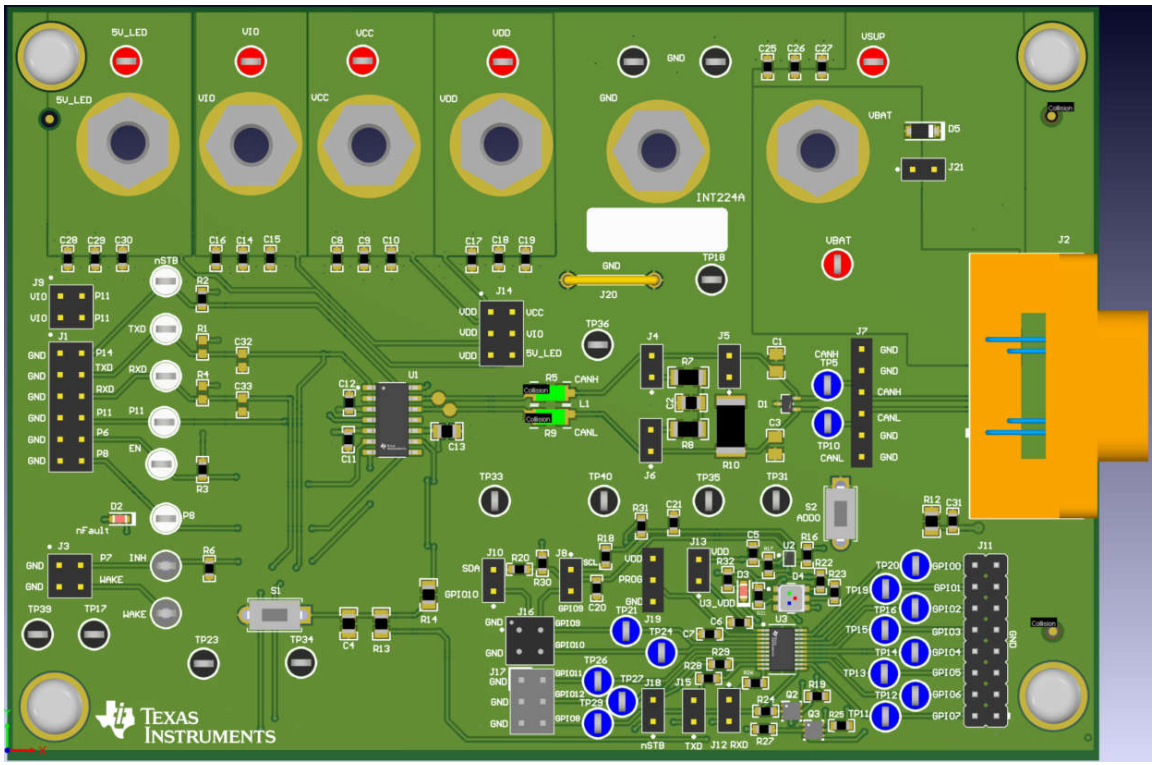
TCAN5102-Q1 Automotive Self-supplied CAN FD Light Responder to SPI, UART, or I2C Controller Evaluation Module

Description

The TCAN5102-Q1 EVM provides users with the ability to evaluate TCAN5102-Q1 CAN FD (Controller Area Network with Flexible Data Rate) Light Responder. The EVM is configurable for use with both 8-pin and 14-pin CAN transceiver families by populating the transceiver and setting the appropriate jumpers on the EVM.

Features

- Standard and split termination on the CAN bus
- Pads for CANH / CANL short to battery test
- Footprints for filter capacitors, common-mode choke, and TVS diode for CAN bus protection from RF noise and transient pulses
- Footprints for common 8-pin and 14-pin SOIC transceivers
- DSUB9 connector with the CAN bus signals and GND for typical automotive cable harness connections
- All digital signals for configuration and control brought out to a header for easy access
- Multifunctional jumpers for different functional use of generic pins



TCAN5102-Q1 EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide details the TCAN5102-Q1 CAN FD Light Responder EVM operation. All of the options and the overall operation of the EVM are explained in this user's guide. This user's guide explains the EVM configurations for basic CAN evaluation, various load and termination settings.

1.2 Kit Contents

1. TCAN5102-Q1 CAN FD Light (CAN FDL) Responder EVM.

1.3 Specification

TI offers the TCAN5102-Q1 CAN FDL Responder. The responder includes a single V_{DD} supply supporting 3V to 5.5V, with I/O level shifting CAN transceivers.

The device is designed to support CAN FDL Responder node applications in a commander - responder architecture which does not require a responder node processor. All control for the responder node is through the CAN bus, from the commander node processor which eliminates the need for responder node processor and software. The TCAN5102-Q1 receives data and/or commands from a CAN FDL commander node which controls SPI, UART, or an I^2C controller for communication to peripheral devices connected to the TCAN5102-Q1. The pins can be used as GPIOs if serial interfaces are not needed. Pulse width modulation (PWM) output channels also support trapezoidal ramp profiles in hardware for controlling stepper motors or PWM LEDs. Ramping of duty cycle or frequency is possible. No external crystal or clock is required.

The device controls the external 8-pin or 14-pin CAN FD transceivers (examples - TCAN844-Q1, TCAN1044A-Q1, TCAN1462-Q1, TCAN1162x-Q1, TCAN1043A-Q1 or TCAN1463A-Q1), for system level flexibility. The device relies upon the CAN FD transceiver / SBC to control the node power and communicate a wake up signal to the TCAN5102-Q1 by latching the CAN RXD (CRXD) pin low.

The EVM is setup to help system designers evaluate the operation and performance of the TCAN5102-Q1 device with various peripherals communicating through I^2C, PMW and GPIOs. Peripheral components are poupulated on the EVM. There are also populated headers that offer the flexibility to communicate with SPI, UART, or I^2C to other peripherals off-board. The peripherals populated includes a U2 temperature sensor (TMP117 - controlled via I^2C) and a RGB multi-color LED (LRTBVSR - controlled via GPIO and PWMs). The EVM also provides bus termination, bus filtering, and protection concepts. The EVM is easily configured by the users as needed by jumper settings, simple soldering tasks, and replacement of standard components.

1.4 Device Information

The EVM has simple connections to all necessary pins of the CAN transceiver device, the CAN FDL Responder and jumpers, where necessary, to provide flexibility for device pin and CAN bus configuration. There are test points (loops) for all main points where probing is necessary for evaluation such as GND, V_{DD}, V_{CC}, V_{IO}, V_{SUP}, $5V_{LED}$, TXD, RXD, CANH, CANL, and other logic pins. The EVM supports many options for CAN bus configuration. The EVM allows for two termination schemes through the use of jumpers to select between the split termination configuration or a single 120Ω resistor. If needed, there are footprints for a common-mode choke, TVS diode for ESD protection, and capacitors for further EMC protection or signal conditioning. A DSUB9 connector is included to allow the evaluation and use of the CAN bus in larger systems.

2 Hardware

Jumper Information

Table 2-1 lists the jumper connections for the EVM.

Table 2-1. Jumper Connections

Connection	Type	Description
J1	12-pin header	Access to all critical digital I/O and GND for connecting the CAN transceiver externally with test equipment or interfaced to a processor EVM. **For 8-pin CAN transceivers:** Pull J1.2 low to GND when using an 8-pin CAN transceiver with STB. This is typically required to be low for normal operation. Leave J18 floating if 8-pin CAN transceivers are used. J1.2 low is used in combination with J18 floating.
J2	DSUB9 connector	Provides an alternative way to connect CANH, CANL, and GND all through a standard DSUB9 CAN pinout rather than through a regular header.
J3	4-pin header	Access to pin 7 (INH), WAKE, and GND.
J4	2-pin jumper	Implements 120Ω split termination. Must be used in combination with J6.
J5	2-pin jumper	Implements 120Ω termination resistor. Along with the split termination (J4 and J6), this allows the simulation of the true CAN bus impedance of 60Ω (that is, two 120Ω terminations in parallel).
J6	2-pin jumper	Implements 120Ω split termination. Must be used in combination with J4.
J7	6-pin header	CAN bus connection (CANH, CANL) and GND. Can be used to send CAN frames (through Vectors CANoe for example)
J8	2-pin jumper	Shunt for the temperature sensor's SCL connection to CAN FDL GPIO9/CS4/SCL pin. Leave floating / disconnected if the temperature sensor (U2) is not needed and the GPIO8 is needed for other connections.
J9	4-pin header	Shunt for a shared V_{IO} connection to pin 11. Pin 11 is typically a NC pin or V_{IO}. **For 8-pin CAN transceivers:** Shunt V_{IO} to P11 to make sure the V_{IO} pin is supplied.
J10	2-pin jumper	Shunt for temperature sensor SDA connection to CAN FDL GPIO10/CS5/SDA pin Leave floating / disconnected if the temperature sensor (U2) is not needed and GPIO10 is needed for other connections.
J11	16-pin header	Access to all critical CAN FDL GPIO (GPIO0 - GPIO7) and GND for using the CAN FDL IOs externally with test equipment or interfaced to a processor EVM.
J12	2-pin jumper	Shunt for CAN FDL Responder CRXD to the CAN transceiver RXD.
J13	2-pin jumper	**Required, to power the CAN FDL Responder:** Shunt for CAN FDL Responder V_{DD} connection to P4 V_{DD} banana jack connection.
J14	6-pin header	Shunt for a sharing V_{DD}, V_{cc}, V_{IO} and $5V_{LED}$ connections. Share as needed.
J15	2-pin jumper	Shunt for CAN FDL Responder CTXD to the CAN transceiver TXD
J16	4-pin header	Access to CAN FDL GPIO9/CS4/SCL, GPIO10/CS5/SDA pins and GND for driving the CAN FDL Responder externally with test equipment or interfaced to a processor EVM. **When J16 is used for other connections other than U2:** Make sure J8 and J10 are disconnected / floating.
J17	6-pin header	Access to CAN FDL GPIO11/CS6/PMW0, GPIO12/CS7/PMW1, GPIO8/URXD pins and GND for driving the multi-color RGB LED D4 peripheral.
J18	2-pin jumper	Shunt for CAN FDL CSLP pin to the CAN transceiver nSTB pin **For 8-pin CAN transceivers with STB:** Disconnect / float J18.
J19	3-pin jumper	Shunt for CAN FDL PROG pin to V_{DD}, or GND
J20	Ground Clip	Provides extra connection to GND.
J21	2-pin jumper	Shunt to connect V_{BAT} and V_{VSUP}. This bypasses diode D5.

Table 2-1. Jumper Connections (continued)

Connection	Type	Description
Test point	Red	Voltage supplies
	Black	GND
	White	CAN transceiver's logic I/Os
	Grey	CAN tranceiver INH and WAKE logic I/Os
	Blue	CAN FDL GPIOs and CAN transceiver's CANH / CANL

3 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation.

3.1 Overview and Basic Operation Settings

3.1.1 Power Supply Inputs V_{BAT}, V_{CC}, V_{IO}, V_{DD} and $5V_{LED}$

Each supply pin can be connected with a banana jack, test point, or header. V_{DD}, V_{CC}, V_{IO} and $5V_{LED}$ can share a voltage supply by shunting the J14 header. This is optional for a quick evaluation, if the user prefers to supply all the power supplies by the same 5 V supply. Otherwise, users can supply their desired supply to each power supply, independently through their respective connectors. Diode D5 can be biased by shunting V_{BAT} and V_{SUP} on the J21 header.

The 14-pin CAN transceivers require V_{SUP}, V_{CC}, and V_{IO}. The nFault LED D2, CAN FDL's LED D3 and LED peripheral D4 uses $5V_{LED}$. The nFault LED D2 lights up when a fault is present or when the nFault pin of the 14-pin device is disconnected (nFault is floating).

The 8-pin CAN transceievers typically require V_{CC}, and V_{IO}. V_{IO} and P11 share a voltage supply by shunting the J9 header. **This is required for 8-pin CAN transceivers with V_{IO}** . P11 can either be a No Connect (NC) or V_{IO} pin for 8-pin CAN transceivers. This gives flexibility while evaluating with 8-pin CAN transceiver options.

The CAN FDL Responder requires V_{DD}. The CAN FDL's LED D3 lights up when V_{DD} is supplied. **It is required to shunt J13, connecting the supplied V_{DD} from the banana jack (or from J14) to the V_{DD} pin of the TCAN5102-Q1 CAN FDL Responder**.

3.1.2 Getting Started - An Example of A Quick EVM Setup

For a quick evaluation with either the 8-pin or 14-pin transceiver options, use the recommended jumper connections in Table 3-1 as a default EVM setup. In this example, PCAN-USB Pro FD adapter is used to enable the CAN connection to a computer via USBCAN frames, sent through J2 (DSUB9) of the EVM.

Figure 3-1. PCAN-TCAN EVM Hardware Setup

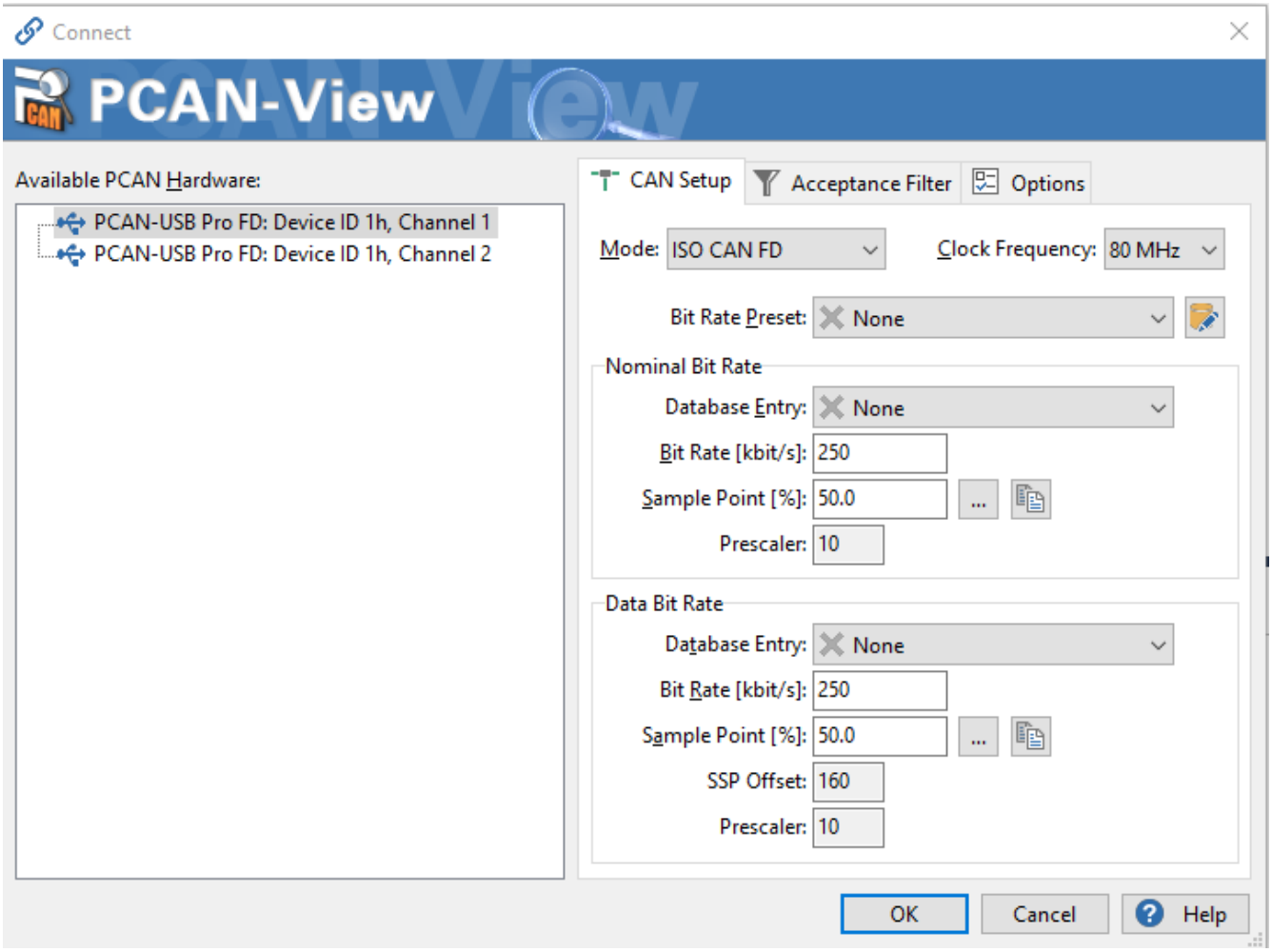


Figure 3-2. PCAN-USB Pro FD Setup

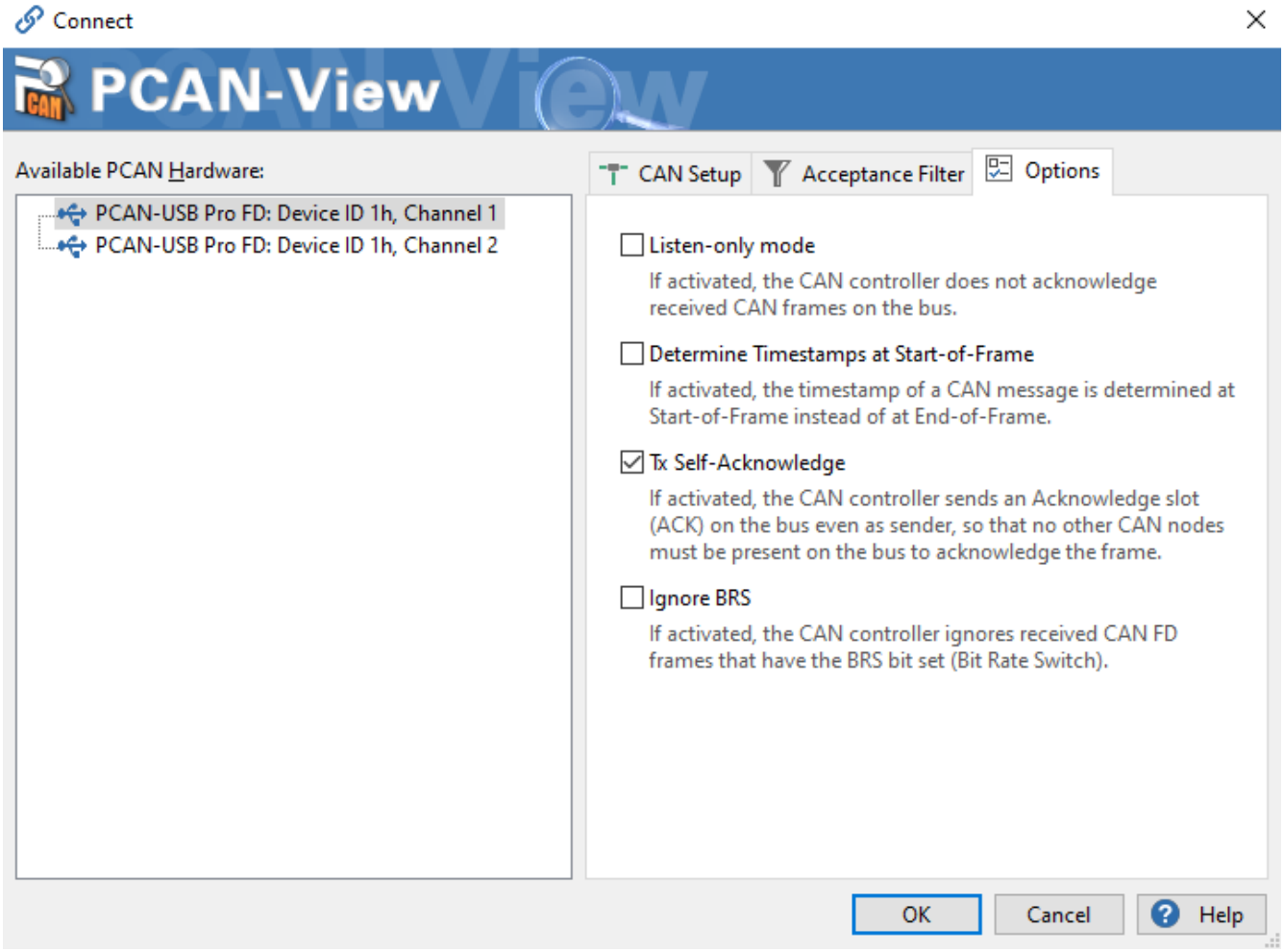


Figure 3-3. PCAN-USB Pro FD ACK Setup

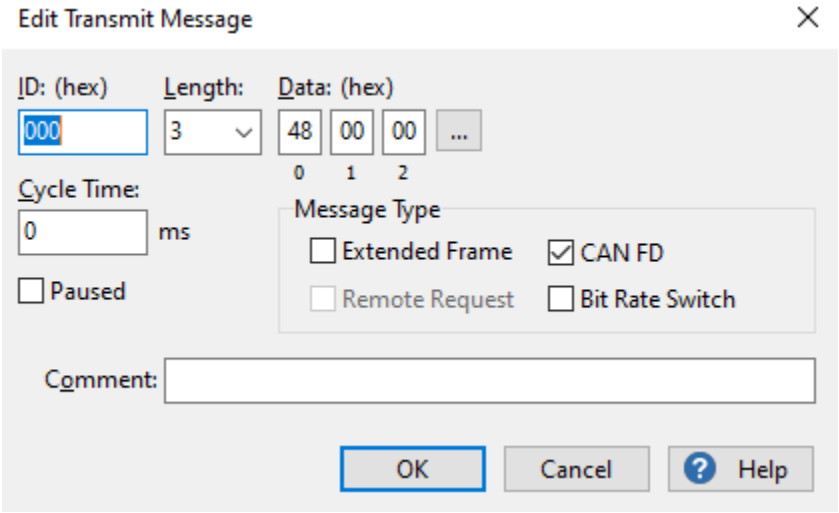


Figure 3-4. TX Frame

Figure 3-1 shows the CAN setup for TCAN5102-Q1's default speed of 250 kbps with 50 % sample point. Tx Self Acknoledged is ON, allowing for the ACK bit on the bus. The TCAN5102-Q1 default CAN identifier of 000h was selected and sent with the standard CAN frame format using 3 bytes of the CAN payload as a header -

containing 3 fields: operation code (op code), data length and an address. A valid response with ID 001h of 12 bytes of data was received as 48 81 54 43 35 31 30 32. This implies the PCAN Electronic Control Unit (ECU) and the TCAN5102-Q1 CAN FDL Responder are communicating. The ECU transmitted the CAN FD frame and the TCAN5102-Q1 device recognized it as query, responding with ID 001h received as "TCA5102" (encoded in ASCII).

CANH (yellow), CANL (blue), TXD / RXD Waveforms shows the TXD, RXD, CANH (yellow) and CANL (blue) traffic. The bottom traces show TXD / RXD toggling, and PCAN-View decodes it into frames. The CAN bursts of differential activity corresponds to the TX frame (ID 000h, 3B) and the RX responder's reply (ID 001h, 12B). TXD shows the transmitted activity only for the first burst while RXD shows activity for both (first, for self acknowledging and secondly, the responder's frame received from the bus).

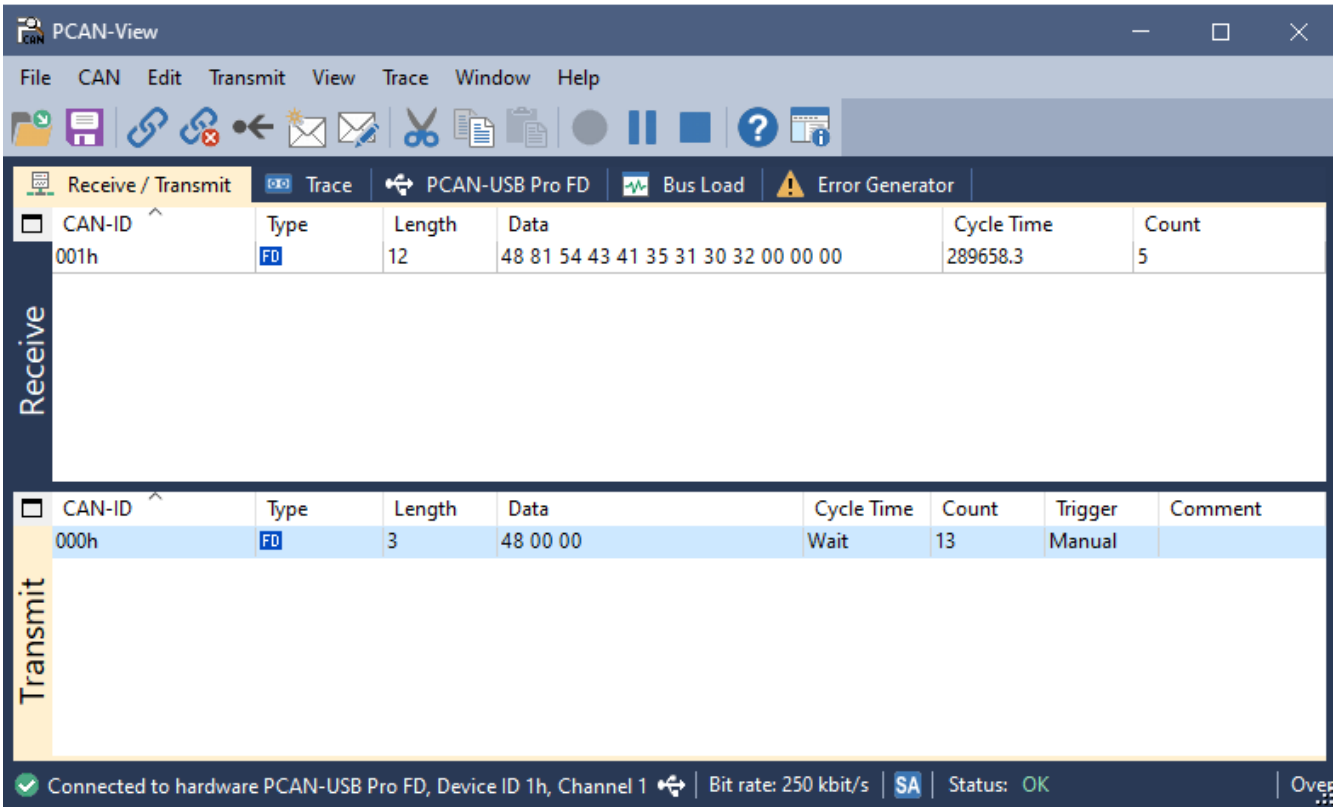
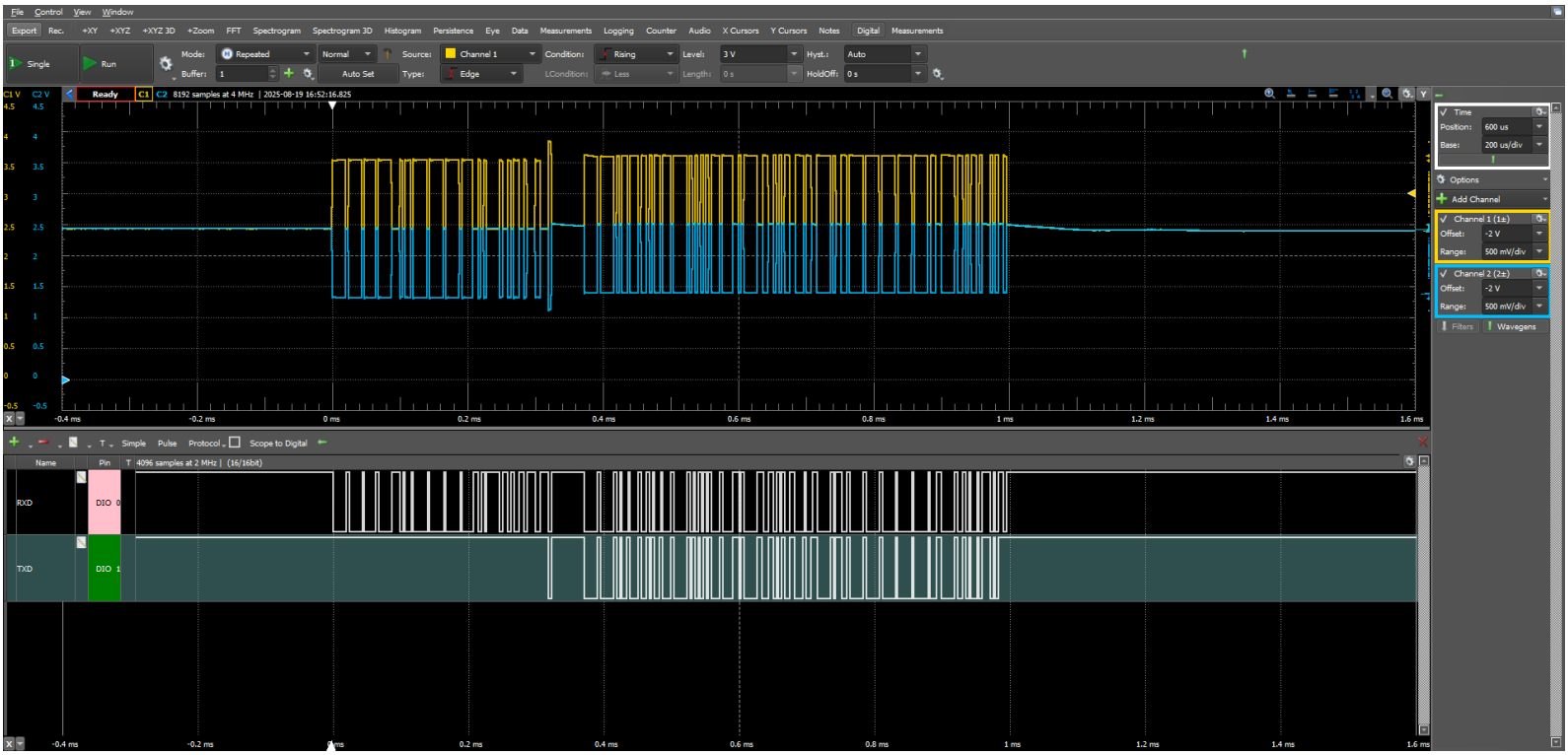


Figure 3-5. Transmitted / Received Messages



CANH (yellow), CANL (blue), TXD / RXD Waveforms

The EVM may be re-configured as intended, and used with the TCAN5102-Q1 data sheet for additional programming examples (CAN FDL protocol, SPI, UART, I2C and PWM) to communicate with peripherals.

Table 3-1. Recommended Connections

Connection	Transceiver Type	Recommendations
J1	8-Pin	Shunt J1.2 low to GND
	14-Pin	Leave J1.2 floating
J2	Any	Provides an alternative way to connect CANH, CANL, and GND all through a standard DSUB9 CAN pinout rather than through a regular header.
J3	14-Pin	Access to pin 7 (INH), WAKE, and GND as needed.
J4	Any	Shunt to implement a 120Ω split termination. Must be used in combination with J6.
J5	Any	Shunt to implement a 120Ω termination resistor. Along with the split termination (J4 and J6), this allows the simulation of the true CAN bus impedance of 60Ω (that is, two 120Ω terminations in parallel).
J6	Any	Shunt to implement a 120Ω split termination. Must be used in combination with J4.
J7	Any	CAN bus connection (CANH, CANL) and GND. Can be used to send CAN frames via Vector CANoe for example.
J8	Any	Shunt to make sure the populated temperature sensor's SCL is connected to CAN FDL Responder. Or leave floating / disconnected if the GPIO pin (may or may not be configured as SCL) is needed for other connections (also access through J16.1).
J9	8-Pin	Shunt V_{IO} to P11.
	14-Pin	Can leave floating / disconnected.

Table 3-1. Recommended Connections (continued)

Connection	Transceiver Type	Recommendations
J10	Both	Shunt to make sure the populated temperature sensor SDA is connected to CAN FDL Responder. Or leave floating / disconnected if the GPIO pin (may or may not be configured as SDA) is needed for other connections (also access through J16.2).
J11	Any	Access to all critical CAN FDL GPIO (GPIO0 - GPIO7) and GND for using the CAN FDL IOs externally with test equipment or interfaced to a processor EVM.
J12	Any	Shunt for CAN FDL Responder CRXD to the CAN transceiver RXD.
J13	Any	Shunt to supply V_{DD} to CAN FDL.
J14	Any	Shunt to share V_{DD}, V_{CC}, V_{IO} and $5V_{LED}$ connections, as needed. As an example, may use a single 5V supply to power all the power supplies needed for the EVM, by supplying V_{DD} with 5V and shunting V_{DD} to V_{CC}, V_{IO} and the $5V_{LED}$ supply).
J15	Any	Shunt for CAN FDL Responder CTXD to the CAN transceiver TXD
J16	Any	Access to CAN FDL GPIO9/CS4/SCL, GPIO10/CS5/SDA pins and GND. By default, the GPIO pins are used for driving the TMP117 temperature sensor peripheral. Can be used for driving the CAN FDL Responder externally with test equipment or interfaced to a processor EVM when the temperature sensor is disconnected via floating J8 and J10.
J17	Any	Access to CAN FDL GPIO11/CS6/PMW0, GPIO12/CS7/PMW1, GPIO8/URXD pins and GND. By default, the GPIO pins are used for driving the multi-color RGB LED D4 peripheral. If the GPIOs are needed for other peripherals, disconnect from D4 by depopulating R24, R25 and R27 0Ω resistors.
J18	8-Pin	Disconnect / float, to allow J1.2 pulled low
	14-Pin	Shunt to allow CnSLP of the CAN FDL responder to control nSTB of the transceiver.
J19	Both	Float / leave disconnected by default.
J20	Ground Clip	Provides extra connection to GND.
J21	14-Pin	Shunt to connect V_{BAT} and V_{VSUP}. This bypasses diode D5.
Test point	Red	Voltage supplies
	Black	GND
	White	CAN transceiver's logic I/Os
	Grey	CAN tranceiver INH and WAKE logic I/Os
	Blue	CAN FDL GPIOs and CAN transceiver CANH / CANL

3.1.3 I/O Headers (J1, J3, J11, J16, J17)

All key I/O and supply GND functions are brought to headers J1, J3, J11, J16 and J17. These headers can be used on either interface to test equipment or a short cable can be made to connect to an existing customer-application board with a CAN controller.

These headers are arranged to provide a separate ground for each signal pair (TXD/GND, RXD/GND, GPIOs/GND). If the EVM is being used with lab equipment, connect separate cables to these main points via simple 2-pin header connectors. If connecting the board to a processor-based system, connect cables to all necessary signals to these headers.

Table 3-2. J1 Pin Definitions

Row	Connection	Description
1	P14	Pin 14 of 14-Pin transceiver: nSTB or nCS. Pin 8 of 8-pin transceiver: STB.
2	TXD	CAN transmit data input

Table 3-2. J1 Pin Definitions (continued)

Row	Connection	Description
3	RXD	CAN receive data output
4	P11	Pin 11 of 14-Pin transceiver: No Connect (NC), nSTB or nCS. Pin 5 of 8-Pin transceiver: No Connect (NC) or V_{IO}. **Shunt J9 for V_{IO}** .
5	P6	Pin 6 of transceiver: EN or nINT/SDO
6	P8	Pin 8 of transceiver: nFAULT or SCLK

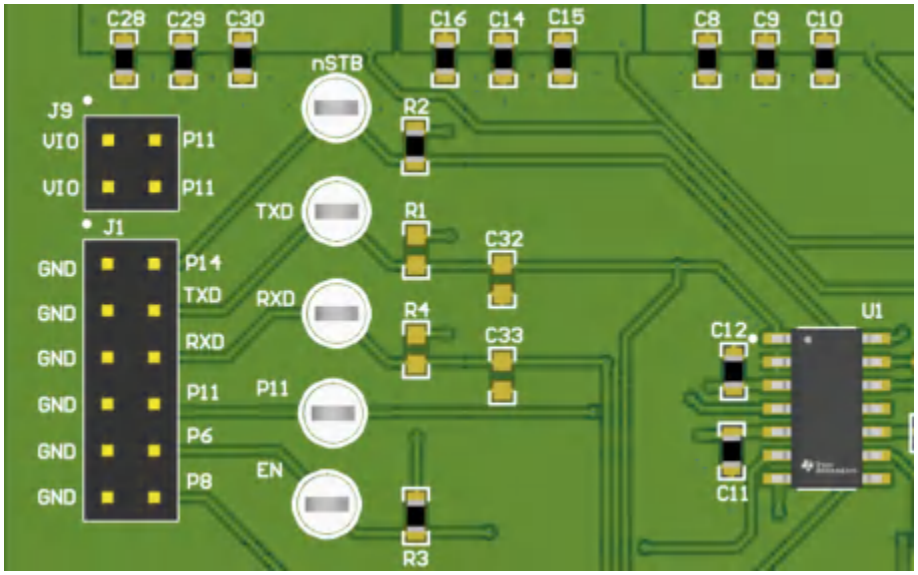


Figure 3-6. J1 Board Layout

Table 3-3. J3 Pin Definitions

Row	Connection	Description
1	P7	Pin 7 of transceiver: INH or INH/LIMP
2	WAKE	Wake input terminal. Switch S1 can be used to toggle pin high or low.

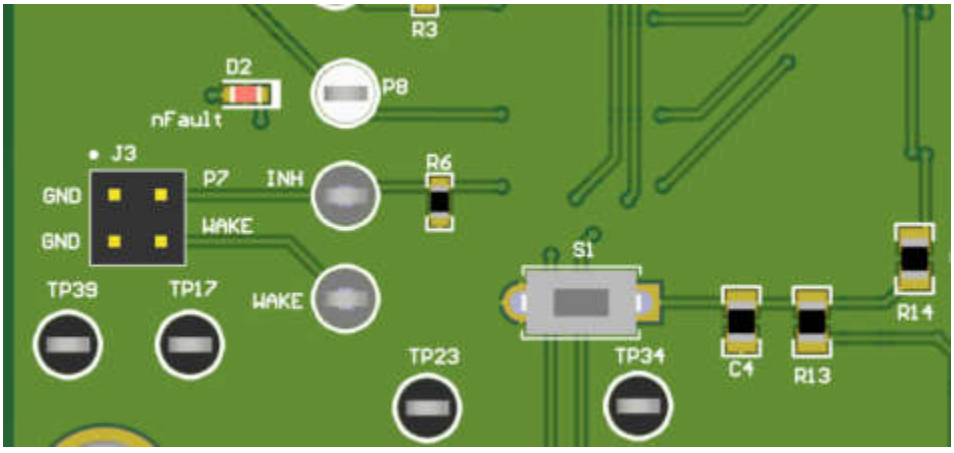


Figure 3-7. J3 Board Layout

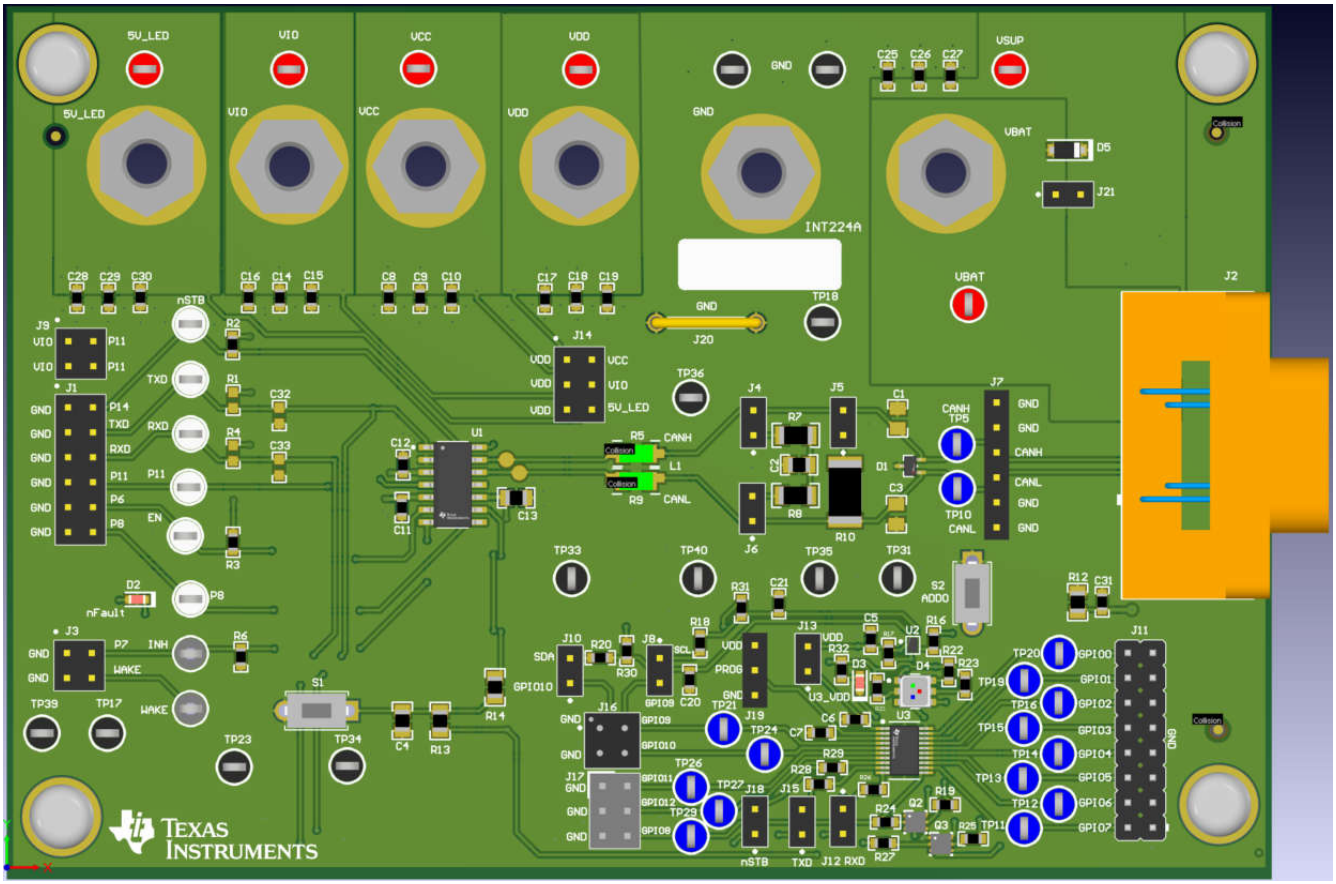


Figure 3-8. EVM layout (Top Layer)

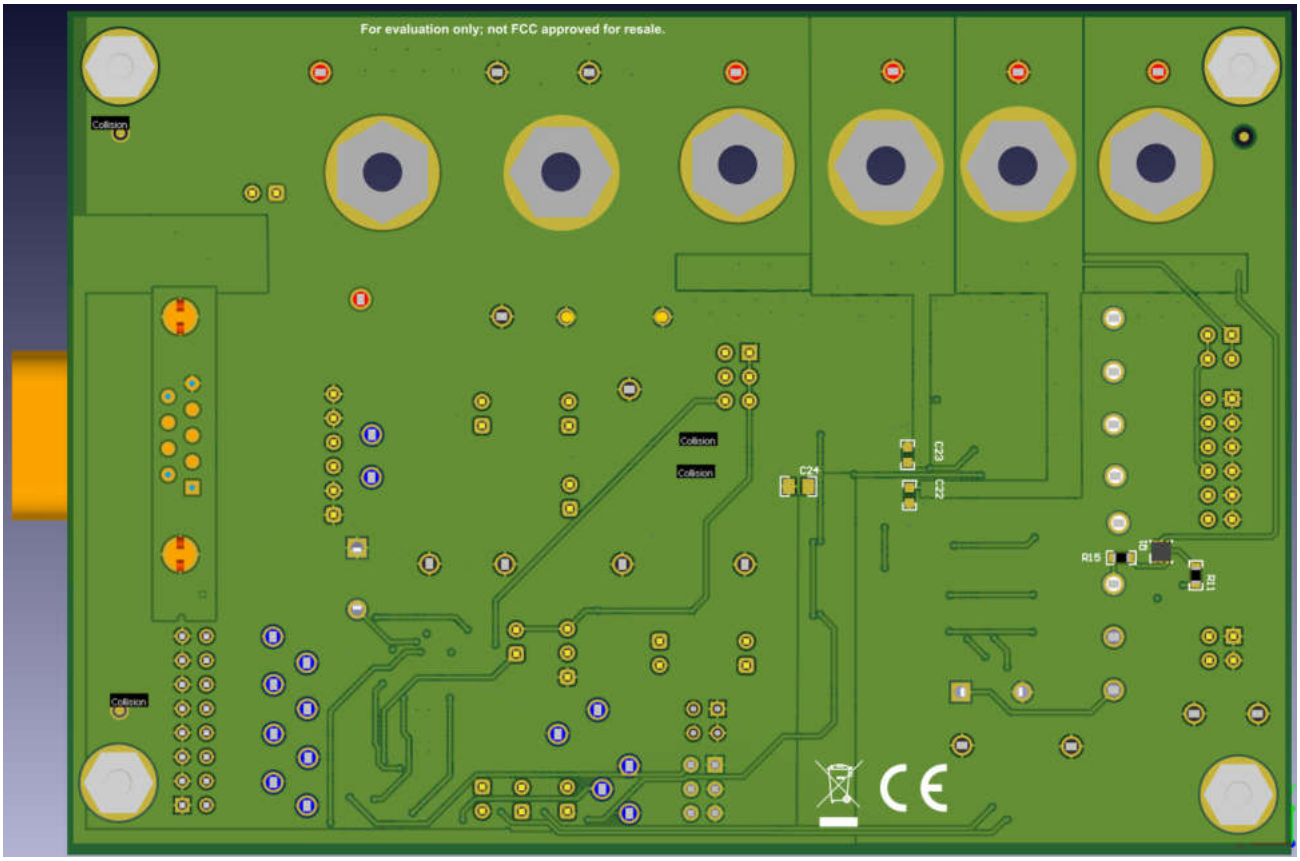


Figure 3-9. EVM layout (Bottom Layer)

3.1.4 Pin 14 of the 14-Pin Transceiver (Pin 8 of the 8-Pin Transceiver)

Pin 14 of the 14-pin transceiver is normally for mode selection (nSTB or STB for pin 8 of the 8-pin transceiver). The signal path to the J1 header is pre-installed with a pullup resistor to VIO installed, R2.

3.1.5 TXD Input

The TXD (pin 1) of the transceiver, transmit data, is routed to J1. The signal path to the J1 header includes the option for an optional filtering capacitor, C32 and an optional pullup resistor to VIO can be installed on R1.

3.1.6 RXD Output

The RXD (pin 4) of the transceiver, receive data, is routed to J1. The signal path to the J1 header includes the option for an optional filtering capacitor, C33 and an optional pullup resistor to VIO can be installed on R4.

3.1.7 Pin 11 of the 14-Pin Transceiver (Pin 5 of the 8-Pin Transceiver)

Pin 11 of the 14-pin transceiver is normally a No Connection pin (NC), an enable pin for Inhibit function (INH_MASK) or the SPI serial data input pin (SDI). For the 8-pin transceievers, the pin is used as pin $5V_{IO}$. The signal path to the J1 header can be **shunted to V_{IO} via J9**.

3.1.8 Pin 6

Pin 6 of the 14-pin transceiver is normally for mode selection (EN). The signal path to the J1 header is pre-installed with a pullup resistor to VIO installed, R3.

3.1.9 Pin 8 of the 14-Pin Transceiver

Pin 8 of the 14-Pin transceiver is normally a status indicator flag (nFAULT) or a SPI clock pin (SCLK). The signal path to the J1 header connects to diode D2, signifying whether pin 8 is high or low. Note that the diode is inverted and the nFault LED D2 lights up when a fault is present or when the 14-pin device is disconnected (nFault is floating).

3.1.10 Pin 7

Pin 7 of the 14-pin transceiver is normally a high voltage output to control external regulators (INH) or a split output for external regulators combined with LIMP home mode (INH/LIMP). The signal path to the J3 header is pre-installed with a 111kΩ pulldown resistor, R5.

3.1.11 WAKE Pin

The WAKE pin of the transceiver (pin 9) is routed to J3. The signal path to the J3 header is pre-installed the with a 100nF filtering capacitor, C4, a 20kΩ pullup resistor to VSUP, R13, and a 33.2kΩ series resistor, R14. The switch S1 can be used to generate a rising or falling edge to wake up the device in addition to the J3 header.

3.1.12 Using CAN Bus Load, Termination, and Protection Configurations

The TCAN5102-Q1 CAN FDL EVM is populated with one 120Ω resistor selectable via jumper, between CANH and CANL, and the 120Ω split termination (two 60Ω resistors in series) including the split capacitor. When using only split termination, the EVM is used as a terminated end of a bus. For electrical measurements to represent the total loading of the bus, use both the split termination and the 120Ω resistor in parallel to give the standard 60Ω load for parametric measurement. Table 3-4 summarizes how to use these termination options.

Table 3-4. Bus Termination Configuration

Termination Configuration	Termination Jumpers			Split Termination Resistors		Split Termination Capacitor
Jumper	**J4**	**J5**	**J6**	**R7**	**R8**	**C2**
No termination	Open	Open	Open	Not available	Not available	Not available
120Ω standard termination	Open	Shorted	Open			
60Ω load	Shorted	Shorted	Shorted			
Split termination (common mode stabilization)	Shorted	Open	Shorted	60Ω	60Ω	4.7nF

The EVM also has footprints for various protection schemes to enhance robustness for extreme system-level EMC requirements. Table 3-5 summarizes these options.

Table 3-5. Protection and Filtering Configuration

Configuration	Footprint Reference	Use Case	Population and Description
Series resistors or common mode choke (CMC)	R5/R9	Connects the CAN transceiver to the CAN bus	R5 and R9 populated with 0Ω (default population)
		Series resistance protection	R5 and R9 populated with MELF resistor as necessary for harsh EMC environment.
	L1 (common footprint)	CMC (bus filter)	L1 can be populated with CMC to filter noise (necessary for harsh EMC environment). Remove R5 and R9 to populate L1.
Bus filtering caps transient protection	C1/C3	Bus filter	Filter noise as necessary (for harsh EMC environment). Use filter caps in combination with L1 CMC.
	D1	Transient and ESD protection	D1 populated with ESD2CAN24-Q1 (adding extra protection for system level transients and ESD)

3.1.12.1 CAN FDL Responder Configurations

The CAN FDL EVM has footprints on the PCB for the installation of various filtering and protection options to evaluate the TCAN1052-Q1 CAN network topology requirements if the EVM is being used as a CAN node.

Each digital CRXD, CTXD and CnSLP input or output pin has footprints allowing for series current-limiting resistors (default populated with 0Ω) and shunts to connect to the CAN transceiver RXD, TXD and nSTB (or STB) pins respectively. CRXD of the CAN FDL Responder is an input incoming from the CAN transceiver RXD output, CTXD of the CAN FDL Responder is an output feeding into the CAN transceiver TXD input and CnSLP of the CAN FDL Responder is an output feeding into the CAN transceiver nSTB input. CnSLP is high by default (in normal mode), placing the CAN transceiver nSTB to normal mode. Note that, this is true for 14-pin transceivers with nSTB and the polarity is flipped for 8-pin transceivers with STB. When using an 8-pin transceiver, leave J18 open / floating / disconnected and use J1.2 header to pull STB pin low for normal operation.

Table 3-6. CAN FDL Responder Connections

Device Pin			Shunts / Pull-ups	C to GND	Description
Pin No.	Description	Type			
1	V_{DD}	Power	J13	C6	Device input, 3.3V or 5V
2	PROG	Input	J19		Input for device configuration and debug. Pull to V_{DD} at power up for ECU development phase and the CAN bus programming data rate is set to 1Mbps.
3	DIGFLTR	Power		C7	Output for an internal LDO used for the digital core.
4-5	GPIO9/CS4/SCL	Input / Output	J8 and J10. J16. R30 and R31	C20 and C21	Used to control TMP117 temperature sensor peripheral. Connect shunts to communicate with FDL responder and use switch, S2 to pull the address to GND.
	GPIO10/CS5/SDA	Input / Output			
6-7, 11	GPIO11/CS6/PWM0	Input / Output	J17		Used to control the D4 LED peripheral. The brightness for green and blue can be controlled with PWM while red retains constant brightness (or changed by controlling the current via R23 sizing).
	GPIO12/CS7/ PWM1	Input / Output			
	GPIO8/URXD	Input / Output			
8-10	CnSLP	Output	J12, J15, J18		Connects to transceiver nSTB (STB), TXD input and RXD output pins respectively.
	CTXD	Output			
	CRXD	Input			
12-19	GPIOs	Input / Output	J11		All other GPIOs.

4 Hardware Design Files

4.1 Schematics

Figure 4-1 shows the EVM schematic.

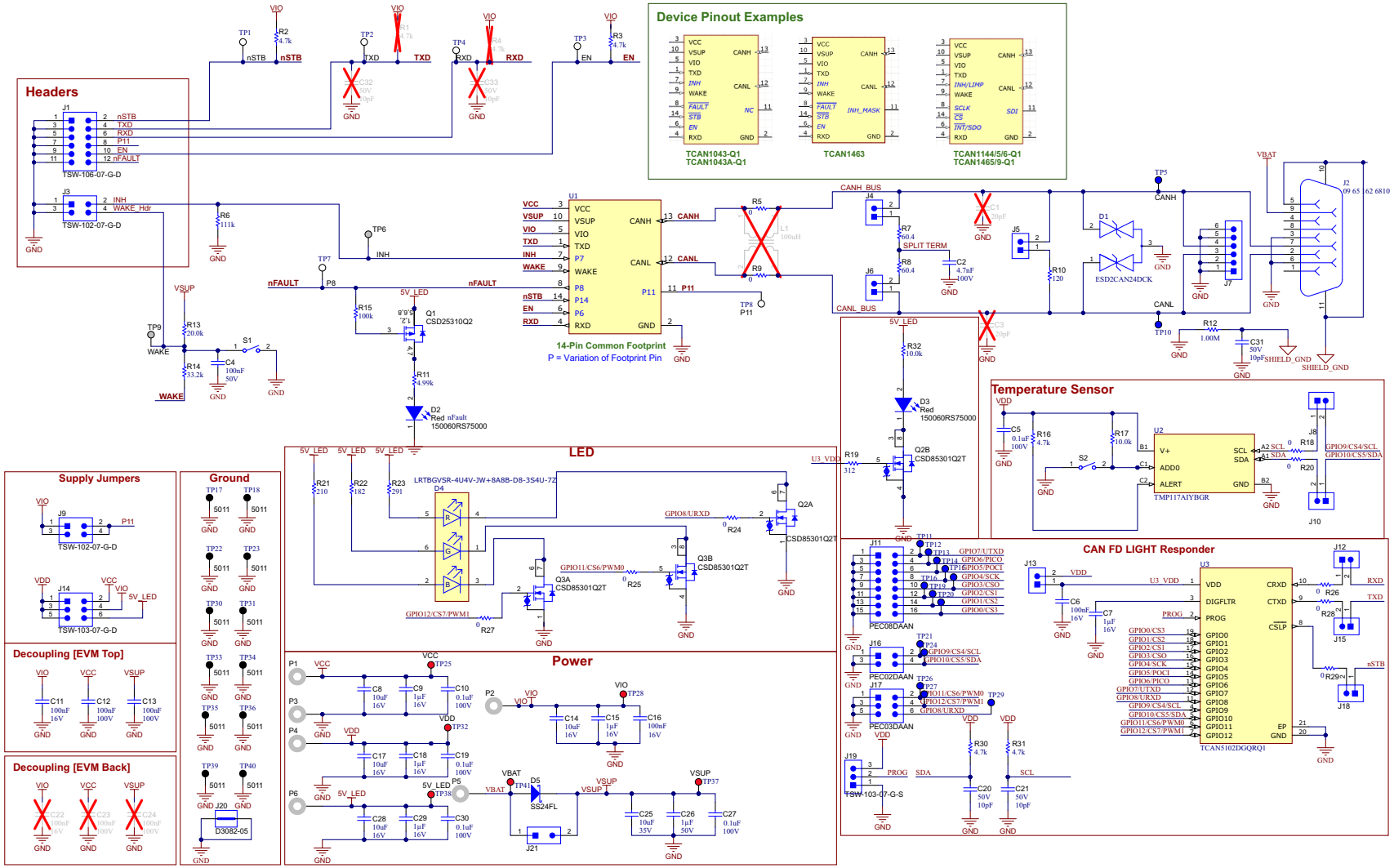


Figure 4-1. EVM Schematic

4.2 PCB Layouts

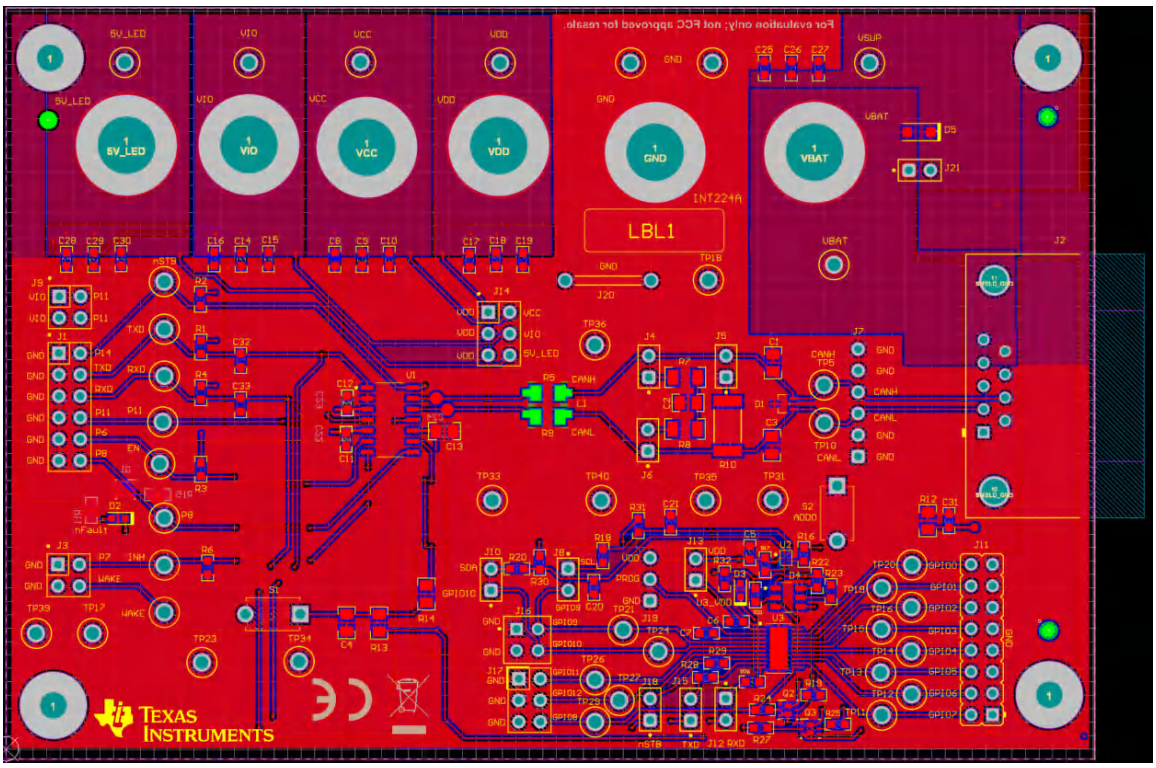


Figure 4-2. EVM Layout (Top Layer)

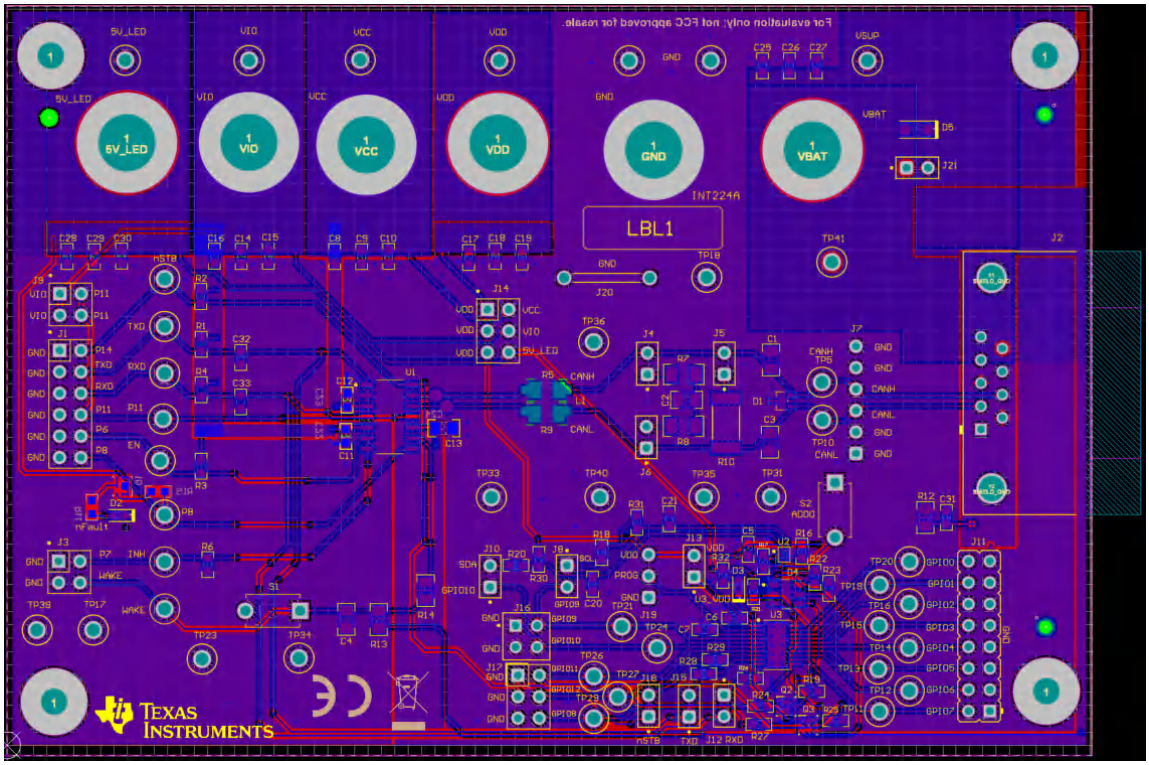


Figure 4-3. EVM Layout (Bottom Layer)

4.3 Bill of Materials (BOM)

Table 4-1. Bill of materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		INT224	Any
C2	1	4700pF	CAP, CERM, 4700 pF, 100 V, +/- 10%, X7R, 0805	0805	GRM219R72A472KA01D	MuRata
C4	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	0805	C0805C104J5RACTU	Kemet
C5, C10, C19, C27, C30	5	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7S2A104K080AB	TDK
C6, C11, C16	3	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGJ3E2X7R1C104K080AA	TDK
C7, C9, C15, C18, C29	5	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	C1608X7R1C105K080AC	TDK
C8, C14, C17, C28	4	10uF	CAP, CERM, 10 uF, 16 V, +/- 20%, X5R, 0603	0603	GRM188R61C106MAALD	MuRata
C12	1	0.1uF	CAP, CERM, 0.1 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	HMK107B7104KAHT	Taiyo Yuden
C13	1	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0805	0805	C2012X7R2A104K125AA	TDK
C20, C21, C31	3	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	CGA3E2C0G1H100D080AA	TDK
C25	1	10uF	CAP, CERM, 10 uF, 35 V, +/- 20%, X5R, 0603	0603	GRM188R6YA106MA73D	Murata
C26	1	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
D1	1		24-V, 2-Channel ESD Protection Diode for In-Vehicle Networks, SC70-3	SC70-3	ESD2CAN24DCK	Texas Instruments
D2, D3	2	Red	LED, Red, SMD	LED_0603	150060RS75000	Wurth Elektronik
D4	1		LED Multi-Color Chip Blue/Green/Red 465nm/528nm/626nm 50mA/50mA/40mA 6-Pin PLCC T/R	PLCC6	LRTBGVSR-4U4V-JW+8A8B-D8-3S4U-7Z	ams-OSRAM
D5	1	40V	Diode, Schottky, 40 V, 2 A, AEC-Q101, SOD-123F	SOD-123F	SS24FL	Fairchild Semiconductor
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
J2	1		D-Sub-9, 11Pos, Male, TH	D-Sub-9, 2rows, Male, TH	09 65 162 6810	Harting
J3, J9	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec
J4, J5, J6, J8, J10, J12, J13, J15, J18, J21	10		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J7	1		Header, 100mil, 6x1, Gold, TH	6x1 Header	TSW-106-07-G-S	Samtec

Table 4-1. Bill of materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
J11	1		Header, 2.54 mm, 8x2, Tin, Vertical, TH	Header, 2.54 mm, 8x2, TH	PEC08DAAN	Sullins Connector Solutions
J14	1		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J16	1		Header, 100mil, 2x2, Tin, TH	Header, 2x2, 2.54mm, TH	PEC02DAAN	Sullins Connector Solutions
J17	1		Header, 100mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions
J19	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J20	1		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
P1, P2, P3, P4, P5, P6	6		Standard Banana Jack, Uninsulated, 15A	Banana Jack	108-0740-001	Cinch Connectivity
Q1	1	-20V	MOSFET, P-CH, -20 V, -20 A, DQK0006C (WSON-6)	DQK0006C	CSD25310Q2	Texas Instruments
Q2, Q3	2	20V	MOSFET, 2-CH, N-CH, 20 V, 6.7 A, DQK0006B (WSON-6)	DQK0006B	CSD85301Q2T	Texas Instruments
R2, R3, R16, R30, R31	5	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K70JNEA	Vishay-Dale
R5, R9	2	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12060000Z0EA	Vishay-Dale
R6	1	111k	RES, 111 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD07111KL	Yageo America
R7, R8	2	60.4	RES, 60.4, 1%, 0.25 W, 1206	1206	RC1206FR-0760R4L	Yageo America
R10	1	120	RES, 120, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW2512120RFKEG	Vishay-Dale
R11	1	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD074K99L	Yageo America
R12	1	1.00Meg	RES, 1.00 M, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1004V	Panasonic
R13	1	20.0k	RES, 20.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF2002V	Panasonic
R14	1	33.2k	RES, 33.2 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080533K2FKEA	Vishay-Dale
R15	1	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
R17	1	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R18, R20, R24, R25, R26, R27, R28, R29	8	0	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	PMR03EZPJ000	Rohm
R19	1	312	RES, 312, 0.5%, 0.1 W, 0603	0603	RT0603DRE07312RL	Yageo America
R21	1	210	RES, 210, 0.5%, 0.1 W, 0603	0603	RT0603DRE07210RL	Yageo America
R22	1	182	RES, 182, 0.5%, 0.1 W, 0603	0603	RT0603DRE07182RL	Yageo America
R23	1	291	RES, 291, 0.1%, 0.1 W, 0603	0603	RT0603BRD07291RL	Yageo America
R32	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic
S1, S2	2		Switch, Tactile, SPST-NO, 0.05A, 12V, TH	SW, SPST 3.5x5 mm	PTS635SL50LFS	C&K Components

Table 4-1. Bill of materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
TP1, TP2, TP3, TP4, TP7, TP8	6		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone Electronics
TP5, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP19, TP20, TP21, TP24, TP26, TP27, TP29	15		Test Point, Multipurpose, Blue, TH	Blue Multipurpose Testpoint	5127	Keystone Electronics
TP6, TP9	2		Test Point, Multipurpose, Grey, TH	Grey Multipurpose Testpoint	5128	Keystone Electronics
TP17, TP18, TP22, TP23, TP30, TP31, TP33, TP34, TP35, TP36, TP39, TP40	12		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics
TP25, TP28, TP32, TP37, TP38	5		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone Electronics
U1	1		Modified footprint from Low-Power Signal Improvement CAN FD Transceiver with INH and WAKE	SOIC14	14-Pin Common Footprint	Texas Instruments
U2	1		±0.1°C accurate digital temperature sensor with integrated NV memory 6-DSBGA -55 to 150	DSBGA6	TMP117AIYBGR	Texas Instruments
U3	1		Automotive Self-supplied CAN FD Light Responder to SPI, UART, or I2C Controller	HVSSOP20	TCAN5102DGQRQ1	Texas Instruments
C1, C3	0	20pF	CAP, CERM, 20 pF, 100 V, +/- 5%, C0G/NP0, 0805	0805	08051A200JAT2A	AVX
C22	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGJ3E2X7R1C104K080AA	TDK
C23	0	0.1uF	CAP, CERM, 0.1 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	HMK107B7104KAHT	Taiyo Yuden
C24	0	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0805	0805	C2012X7R2A104K125AA	TDK
C32, C33	0	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	CGA3E2C0G1H100D080AA	TDK
L1	0	100uH	Inductor, Ferrite, 100 uH, 0.15 A, 2 ohm, SMD	SMD, 4-Leads, Body 4.7 x 3.7 mm	ACT45B-101-2P-TL003	TDK
R1, R4	0	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K70JNEA	Vishay-Dale

5 Additional Information

All TI's SOIC 14-pin CAN transceivers supported by this EVM are listed on ti.com: CAN transceivers.

5.1 Trademarks

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