# TPSI2240-Q1 Evaluation Module



## **Description**

The TPSI2240Q1EVM is a hardware evaluation module (EVM) containing multiple test points and jumpers to fully evaluate the performance and functionality of TPSI2240-Q1. The evaluation module contains the materials needed to test and assess the TPSI2240-Q1 device to seamlessly design the device into a larger applications, such as Battery Management Systems. Use the TPSI2240Q1EVM standalone or paired with an external microcontroller to drive the enable signal of the device. Evaluate application requirements, such as dielectric withstand testing (also known as High Potential [HiPot] Testing) and DC fast charger surge currents, using the EVM without requiring any external protection components. The EVM is populated with TPSI2240-Q1 in a SOIC package.

### **Features**

This EVM has the following features:

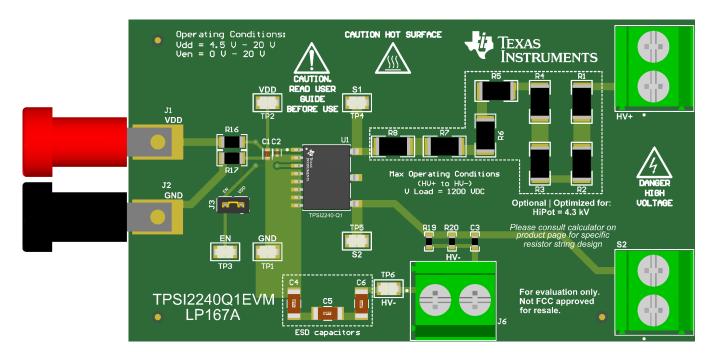
- Primary side operating voltage: 4.5V 20V
- High potential (HiPot) withstand testing capability: up to 4.3kV
- Terminal blocks connectors for easily wired connections
- Test points available for every pin and voltage supply to provide correct functionality

# **Applications**

- · HEV/EV insulation resistance monitoring
- · Hybrid, electric, and power train systems
- Battery management systems (BMS)
- Solar energy
- · Onboard charger
- EV charging infrastructure

#### Note

Disclaimer: Refer to the data sheet and design resources on the TPSI2240-Q1 product page to optimize component selections for the HiPot voltage and avalanche current requirements of the desired application.





### 1 Evaluation Module Overview

#### 1.1 Introduction

The TPSI2240-Q1 is an isolated solid-state relay, designed for high-voltage automotive and industrial applications. The TPSI2240-Q1 seamlessly replaces mechanical and photo relays by integrating TI's capacitive isolation technology. The capacitive isolation technology does not suffer from common failure modes such as mechanical wear out or photo degradation. The entire primary side of the device requires only 5mA of input current, incorporating a fail-safe EN pin preventing any possibility of back powering the VDD supply. The secondary side consists of back-to-back MOSFETs with a standoff voltage of 1200V from S1 to S2. The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2240-Q1 to withstand High Potential (HiPot) screening and DC fast charger surge currents, assuming appropriate component selection for the application. The TPSI2240Q1EVM helps users evaluate the operation and performance of the TPSI2240-Q1 isolated switch with reinforced isolation rating up to 5kVrms. The inputs and output connections to the board are terminal blocks, which allow for easily wired connections. This EVM user's guide provides the connectors, test point descriptions, operational modes, schematic, bill of materials, and board layout of the EVM.

### 1.2 Kit Contents

Table 1-1. Kit Contents

| Item          | Quantity |
|---------------|----------|
| TPSI2240Q1EVM | 1        |

### 1.3 Specification

This section summarizes the performance specifications of the TPSI2240Q1EVM in the default configuration. Refer to Section 3.1.1 for recommended typical voltages during testing.

Table 1-2. TPSI2240Q1EVM Input Voltage Limits

|                    | PARAMETER   | MIN | Тур | MAX  | UNIT |  |  |  |
|--------------------|---|-----|-----|------|------|--|--|--|
| $V_{VDD}$          | Primary side supply voltage                                 | 4.5 | -   | 20   | V    |  |  |  |
| V <sub>EN</sub>    | Enable Voltage  | 0   | -   | 20   | V    |  |  |  |
| V <sub>HV</sub> +  | Secondary side nominal high voltage input                   | 0   | -   | 800  | V    |  |  |  |
| V <sub>HiPot</sub> | Secondary side High Potential withstand voltage (60s pulse) | 0   | -   | 4300 | ٧    |  |  |  |

### 1.4 Device Information

Table 1-3. TPSI2240-Q1 Device Specifications

| Device Specifications                                  | Values                                 |
|--|--|
| Primary side supply current                            | 9mA ON state, 1uA OFF state            |
| Standoff voltage of integrated avalanche rated MOSFETs | 1200V                                  |
| Isolation barrier rating                               | 5000V <sub>RMS</sub>                   |
| Automotive qualification                               | AEC-Q100                               |
| Package  | DWQ (SOIC, 11)<br>10.3mm × 7.5mm (nom) |





### 1.5 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines



Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help maintain the safety of you and those working around you. Contact TI's Product Information Center <a href="http://ti.com/customersupport">http://ti.com/customersupport</a> for further information.

Save all warnings and instructions for future reference.

### **WARNING**

Failure to follow warnings and instructions can result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

### 1. Work Area Safety:

- a. Keep work area clean and orderly.
- b. Verify that qualified observers are present anytime circuits are energized.
- c. Verify that effective barriers and signage are present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
- d. Electrically load all interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC within a protected Emergency Power Off EPO protected power strip.
- e. Use stable and non-conductive work surface.
- f. Use adequately insulated clamps and wires to attach measurement probes and instruments. Whenever possible, do not freehand test.

#### 2. Electrical Safety:

- a. As a precautionary measure, a good engineering practice is to assume that the entire EVM can have fully accessible and active high voltages.
- b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Re-validate that TI HV EVM power has been safely deenergized.
- c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- d. Once EVM readiness is complete, energize the EVM as intended.

#### **WARNING**

While the EVM is energized, never touch the EVM or the electrical circuits, as the EVM or the electrical circuits can be at high voltages capable of causing electrical shock hazard.

### 3. Personal Safety

a. Wear personal protective equipment, for example, latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.



Limitation for safe use: Do not use EVMs as all or part of a production unit.

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### 2 Hardware

# 2.1 Recommended Test Equipment

The following list includes the recommended equipment to test the TPSI2240Q1EVM:

- Adjustable power supplies for the input
- Oscilloscope
- · Digital multimeter
- Optional: function generator or microcontroller to toggle the enable (EN) pin of the TPSI2240-Q1

### 2.2 Jumper Information

**Table 2-1. Input and Output Connector Descriptions** 

| Connector | Label | Description                                 |  |  |  |
|-----------|-------|---|--|--|--|
| J1        | VDD   | Primary side supply                         |  |  |  |
| J2        | GND   | Primary side GND                            |  |  |  |
| J3        | SH-1  | Jumper connecting EN pin to VDD when closed |  |  |  |
| J4        | HV+   | Secondary side positive input               |  |  |  |
| J5        | S2    | Voltage sense output                        |  |  |  |
| J6        | HV-   | Secondary side negative input               |  |  |  |

### 2.3 Test Points

**Table 2-2. Test Point and Jumper Descriptions** 

|  | Table 2 21 Took I dille dille Campor Decemptione |   |             |  |  |  |  |
|--|--|---|-------------|--|--|--|--|
| Test Point, Jumper Label                               |  |   | Description |  |  |  |  |
| TP1 GND Primary side GND test point                    |  | Primary side GND test point                     |             |  |  |  |  |
| TP2 VDD Primary side supply test point                 |  | Primary side supply test point                  |             |  |  |  |  |
| TP3 EN Enable pin test point                           |  | Enable pin test point                           |             |  |  |  |  |
| TP4 S1 Secondary side HV+ voltage after resistor chain |  | Secondary side HV+ voltage after resistor chain |             |  |  |  |  |
| TP5 S2 Voltage sense output test point                 |  | Voltage sense output test point                 |             |  |  |  |  |
| TP6 HV- secondary side test point                      |  | HV– secondary side test point                   |             |  |  |  |  |



# 3 Implementation Results

### 3.1 Evaluation Setup

### 3.1.1 Recommended Test Setup

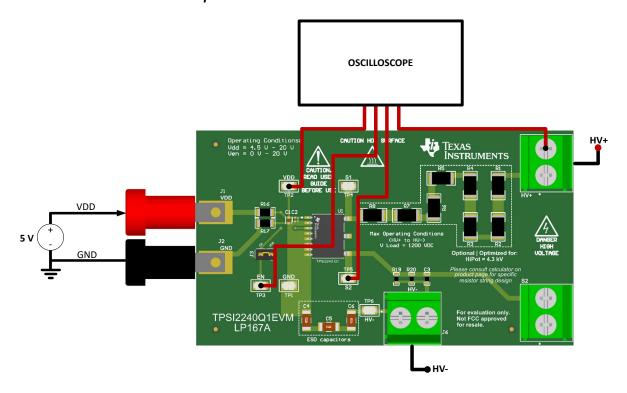


Figure 3-1. TPSI2240Q1EVM Test Setup

#### Note

**Important Note:** The setup shown in Figure 3-1 assumes that high and low voltage grounds (GND & HV-) are shorted to allow for safe oscilloscope capture. In this configuration, the isolation barrier in the TPSI2240-Q1 device is bypassed. To evaluate the device with the isolation barrier, use differential oscilloscope probes and keep high and low voltage grounds separated.

Verify that the TPSI2240Q1EVM has the following setting on the jumpers:

1. J3 – Connecting EN pin to VDD Rail

To test the normal operation of TPSI2240-Q1, follow the steps outlined below:

- Connect a 5V power supply to the banana jacks of J1 with the negative lead connected to J2 to power TPSI2240-Q1.
- 2. Before placing in the enclosure or connecting the High-Voltage (HV) power supply, verify all voltages on the primary side of TPSI2240-Q1 are as expected using **TP2** (VDD) and **TP3** (EN) referenced to **TP1** (GND).
- 3. Place the board in the enclosure. Attach the high-voltage power supply (800V) positive lead to **J4** and the negative to **J6**.
- 4. With oscilloscope probes connected to voltages of interest (VDD/EN, HV+, S2), turn on the high-voltage supply then subsequently toggle the 5V supply connected to EN. Observe that **TP3** (EN), **J4** (HV+), and **TP6** (S2) show the expected voltages.

To test the High Potential (HiPot) operation of TPSI2240-Q1, follow the steps below:

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1. Verify that no power supply connects to the TPSI2240-Q1 **J1** and **J2** primary side connectors during HiPot testing.

- 2. Place the board in the enclosure and attach the high-voltage power supply (4300V) positive lead to **J4** and the negative lead to **J6**.
- 3. With oscilloscope probes connected to voltages of interest (HV+, S1-S2), turn on the high-voltage supply with a 60s pulse then observe that **J4** (HV+), **TP4-TP6** (S1-S2) show the expected voltages.

### 3.2 Performance Data and Results

### 3.2.1 Waveforms

After completing the recommended test setup, verify that the following channels are displayed in the waveforms in Figure 3-2

- CH 1 = HV+
- **CH 2 =** S2
- CH 3 = VDD/EN

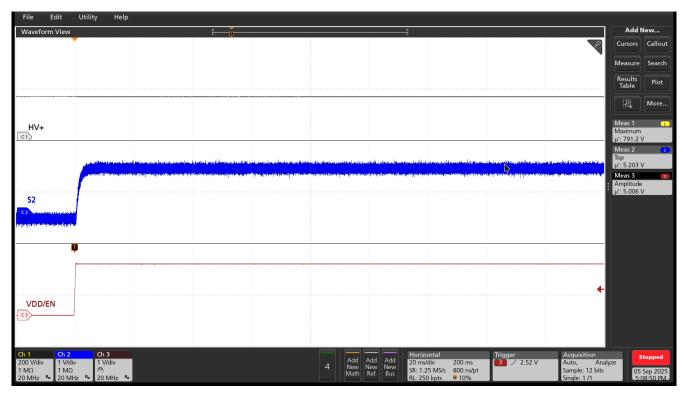


Figure 3-2. Voltage Sense Output (S2) Test Point at HV = 800V (EN = 5V)

Figure 3-3 shows two test points using the following channels settings.

- CH 1 = VHipot (HV+)
- CH 2 = S1-S2



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Figure 3-3. Secondary Sense (S1) and Voltage Sense (S2) Test Points at HV = 4300V

### 3.2.2 S2 Voltage Divider

The voltage sense output test point, S2 (TP6), is the voltage divider measurement. The voltage measured is dependent on parallel resistors R19 and R20, and the resistor network R1-R8. Calculate the voltage measurement using the following equation:

$$V_{S2} = \frac{R19 \mid R20}{(R1 + R2 + ... + R8) + (R19 \mid R20)} \times V_{HV}^{+}$$
(1)



## 4 Hardware Design Files

### 4.1 Schematics

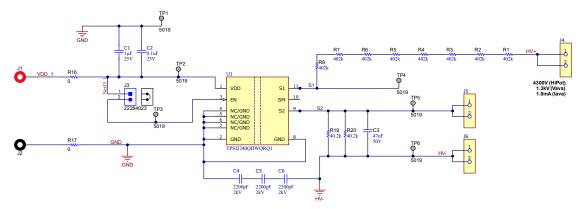


Figure 4-1. TPSI2240Q1EVM Schematic

## 4.2 PCB Layouts

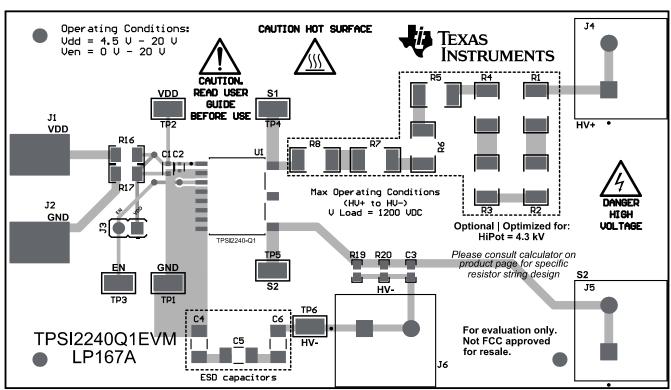


Figure 4-2. TPSI2240-Q1 EVM - Composite View



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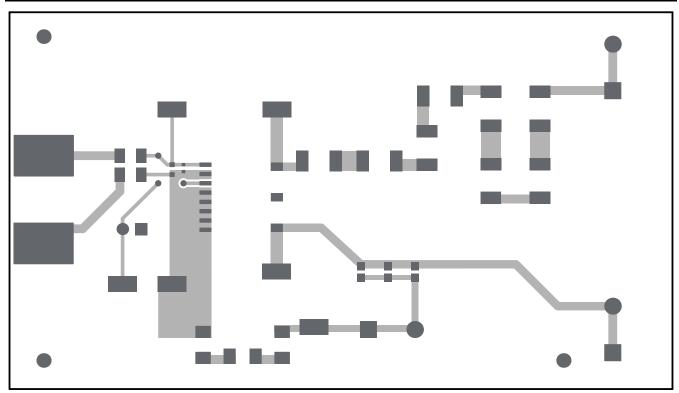


Figure 4-3. TPSI2240-Q1 EVM - Layer 1

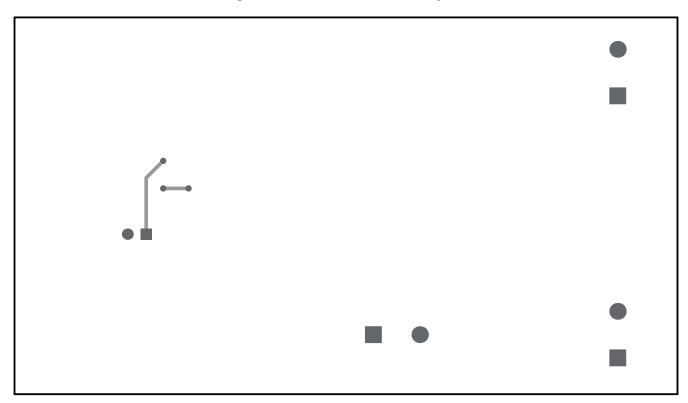


Figure 4-4. TPSI2240-Q1 EVM - Layer 2

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# 4.3 Bill of Materials (BOM)

| Designator                        | Quantity | Value   | Description   | PackageReference                     | PartNumber          | Manufacturer       |
|-----------------------------------|----------|---------|---|--------------------------------------|---------------------|--------------------|
| !PCB                              | 1        |         | Printed Circuit Board   |                                      | LP167               | Any                |
| C1                                | 1        | 1µF     | Ceramic Capacitor for<br>Automotive 1uF ±10%<br>25VDC X7R 0603 Paper<br>T/R | 0603                                 | GCM188R71E105KA64J  | Murata             |
| C2                                | 1        | 100nF   | Ceramic Capacitor<br>Automotive 0.1uF ±10%<br>25V X7R 0402                  | 0402                                 | TMK105B7104KVHF     | Taiyo Yuden        |
| C3                                | 1        | 0.047uF | CAP, CERM, 0.047 uF, 50<br>V, +/- 10%, X7R, 0603                            | 0603                                 | C1608X7R1H473K080AA | TDK                |
| C4, C5, C6                        | 3        | 2.2nF   | 2200 pF ±10% 2000V<br>(2kV) Ceramic Capacitor<br>X7R 1808 (4520 Metric)     | 1808                                 | C1808X222K202T      | Holy Stone         |
| FID1, FID2, FID3                  | 3        |         | Fiducial mark. There is nothing to buy or mount.                            | N/A                                  | N/A                 | N/A                |
| H1, H2, H3, H4                    | 4        |         | Bumpon, Hemisphere,<br>0.44 X 0.20, Clear                                   | Transparent Bumpon                   | SJ-5303 (CLEAR)     | 3M                 |
| J1                                | 1        |         | Banana Jack Insul Nylon<br>Red, TH  | Banana Jack Insul Nylon<br>Red, TH   | 108-0902-001        | Cinch Connectivity |
| J2                                | 1        |         | Banana Jack Insul Nylon<br>Black, TH  | Banana Jack Insul Nylon<br>Black, TH | 108-0903-001        | Cinch Connectivity |
| J3                                | 1        |         | Header, 2.54mm, 2x1,<br>Tin, TH   | Header, 2.54mm, 2x1, TH              | 22284023            | Molex              |
| J4, J5, J6                        | 3        |         |   | CONN_TERM_BLOCK2                     | 6.91251E+11         | Wurth Electronics  |
| R1, R2, R3, R4, R5, R6,<br>R7, R8 | 8        | 402k    | RES, 402 k, 1%, 0.75 W,<br>AEC-Q200 Grade 0, 2010                           | 2010                                 | CRCW2010402KFKEF    | Vishay-Dale        |
| R16, R17                          | 2        | 0       | RES, 0, 5%, 0.25 W, 1206  | 1206                                 | RC1206JR-070RL      | Yageo America      |
| R19, R20                          | 2        | 40.2k   | RES, 40.2 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603                            | 0603                                 | ERA-3AEB4022V       | Panasonic          |
| SH-1                              | 1        | 1x2     | Shunt, 100mil, Gold plated, Black   | Shunt                                | SNT-100-BK-G        | Samtec             |

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| TP1, TP2, TP3, TP4,<br>TP5, TP6 | 6 | Test Point, Miniature,<br>SMT  | Test Point, Miniature,<br>SMT | 5019            | Keystone          |
|---------------------------------|---|--|-------------------------------|-----------------|-------------------|
| U1                              | 1 | 1200-V, 50-mA,<br>Automotive Solid State<br>Relay With Avalanche<br>Protection | SOIC11                        | TPSI2240QDWQRQ1 | Texas Instruments |

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