TPS65916 User's Guide to Power AM570x

This user's guide can be used as a guide for integrating the TPS65916 power-management integrated circuit (PMIC) into a system powering the AM570x device.

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1 Introduction

This user's guide can be used as a guide for connectivity between the TPS65916 PMIC and the AM570x processor. This guide describes the platform connections as well as the power-up, power-down, and warm reset sequences, along with the OTP configurations. This document does not provide details about the power resources, external components, or the functionality of the device. For such information, refer to the *TPS65916 3.1-V to 5.2-V, 5 Buck Converter and 5 LDO Power Management IC (PMIC)* data sheet. When using TPS65916 device to power the other processors, the user should make sure that the power requirements of the processor do not exceed the current capabilities of the TPS65916 device.

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

2 Device Versions

One version of the TPS65916 device is available to power the AM570x processor device, and the OTP settings are described in this document. The OTP version can be read from the SW_REVISION register. In this guide, the device version is distinguished either by the part number or the SW_REVISION value which are both listed in Table 1.

In addition, a power solution is available using both the LP87332D and LP873220 devices as described in the *LP87332D and LP873220 User's Guide to Power AM570x*. See Table 1 to determine the recommended part number based on the V_{DD} current requirement and other features of the processor.

Texas Instruments recommends having 15% margin in the load current. Therefore, the current requirements listed in Table 1 are 15% lower than the maximum capability of the regulator. For example, the LP87332D device supports 3 A maximum, so the recommended load current is 15% less, or 2.55 A. If the V_{DD} current of the processor in the application is unknown, select the TPS65916 configuration because it supports the maximum performance of the processor.

Table 1. OTP Settings Differentiation

DDR Memory Type	V_{DD} Current Requirement	Special Features	Orderable Part Number	Content of SW_REVISION Register
DDR3L	V_{DD} < 2.55 A	N/A	LP87332DRHDR + LP873220RHDR	See User's Guide
DDR3L	V_{DD} < 3 A	VBUS detection, Integrated dual-voltage LDO for SD card	TPS659163RGZR	0x4C

3 TPS65916 to Processor Platform Connection

Figure 1 shows the detailed connections between TPS659163RGZR and the AM570x processor.

If VIO_IN of the PMIC should be 1.8 V, it could be supplied by SMPS4. If VIO_IN of the PMIC should be 3.3 V, it could be supplied by the switched 3.3-V output of the TPS22965-Q1 device. The VIO_IN voltage determines the voltage level of I/O pins on the VIO domain, including GPIO_2, GPIO_4, RESET_OUT, INT, and I²C pins. The I/O level should be chosen based on the voltage level of the processor connection or other external connection to these pins.

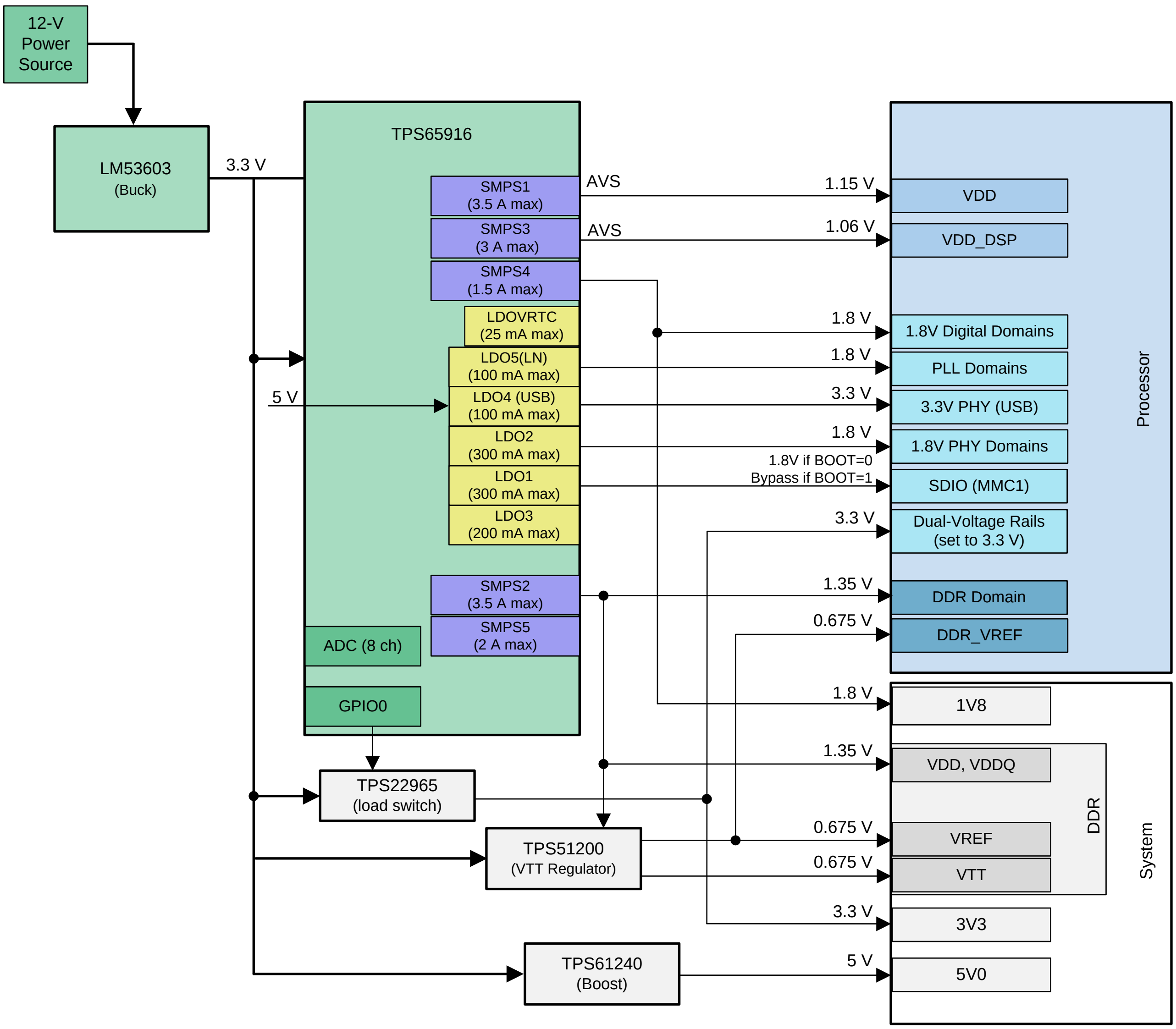

Figure 1. Processor Connection With TPS659163RGZR

Figure 2 and Figure 3 show the reset connections required between the TPS65916 and the processor. All of the OTP configurations have the same reset connections to the processor, along with one of the two options for enabling the power supply; either POWERHOLD or PWRON. Enabling either of these signals turns on the TPS65916 device and starts the startup sequence for the processor. Figure 2 shows the POWERHOLD configuration for the TPS65916 and the processor. GPIO_5 is configured as POWERHOLD in the OTP memory. To turn on the TPS65916, GPIO_5 must be set to a high logic level. When using POWERHOLD, the PWRON signal can be left floating.

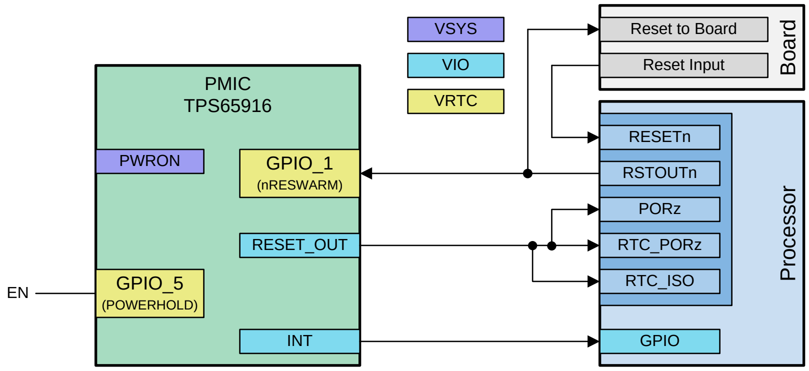

Figure 2. Reset Connections With POWERHOLD Configuration

Figure 3 shows the PWRON configuration for the TPS65916 and the processor. This configuration is used when a push button enables the system. As shown, PWRON is connected to a switch that pulls PWRON to a low logic level when the switch is pressed on.

In some applications, a warm reset is required. This allows for the TPS65916 to reset to its default settings without turning off first. To complete a warm reset correctly, POWERHOLD must be kept at a high logic level so the TPS65916 does not turn off. One solution for this scenario is that GPIO_5 is tied to GPIO_2 and pulled up to VIO. Pulling GPIO_5 to VIO ensures that POWERHOLD is kept high during a warm reset. Tying GPIO_2 to POWERHOLD provides a method to set POWERHOLD low, which is necessary to turn off the device.

For this solution to work, a few software writes must occur:

1. First, enable the TPS65916 by the push button.
2. Second, set GPIO_2 to a high logic level.
3. Third, set GPIO_2 as an output.

When ready to disable the TPS65916, set GPIO_2 to a low logic level.

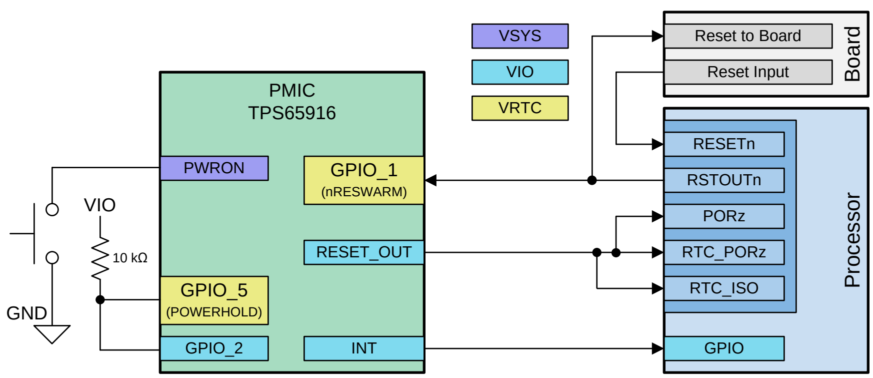

Figure 3. Reset Connections With PWRON Configuration

4 BOOT OTP Configuration

All TPS65916 resource settings are stored in the form of registers. Therefore, all platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from software or from a power sequence).

Resources and platform settings are stored in nonvolatile OTP memory. These settings are defined as follows:

Static platform settings — These settings define, for example, SMPS or LDO default voltages at power-up, and GPIO functionality. Most static platform settings can be overwritten by a power sequence or by the user.

Sequence platform settings — These settings define the TPS65916 power sequences between state transitions, such as the OFF2ACT sequence when transitioning from OFF mode to ACTIVE mode. The power sequence is composed of several register accesses that define which resources (and the corresponding registers) must be updated during the respective state transition. The state of these resources can be overwritten by the user after the power sequence completes execution.

5 Static Platform Settings

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device, distinguished by the SW_REVISION.

5.1 System Voltage Monitoring

Table 2. System Voltage Monitoring OTP Settings

Register	Bit	Description	0x4C Value	Unit
VSYS_MON	VSYS_HI	System voltage rising-edge threshold	3.1	V
VSYS_LO	VSYS_LO	System voltage falling-edge threshold	2.75	V

Comparators that monitor the voltage on the VCC_SENSE, and VCCA pins control the power state machine of the TPS65916 devices. For electrical parameters, refer to the data sheet.

POR — When the supply at the VCCA pin is below the POR threshold, the device is in the NO SUPPLY state. All functionality is off. The device moves from the NO SUPPLY state to the BACKUP state when the voltage in VCCA rises above the POR threshold.

VSYS_LO — When the voltage on the VCCA pin rises above VSYS_LO, the device enters from the BACKUP state to the OFF state. When the device is in an ACTIVE, SLEEP, or OFF state and the voltage on VCCA decreases below the VSYS_LO level, the device enters backup mode. The level of VSYS_LO is OTP programmable.

VSYS_MON — During power up, the value of VSYS_HI OTP is used as a threshold for the VSYS_MON comparator which is gating PMIC start-up (that is, as a threshold for transition from the OFF state to the ACTIVE state). The VSYS_MON comparator monitors the VCC_SENSE pin. After power up, software can configure the comparator threshold in the VSYS_MON register.

VBUS_DET — The VBUS_DET comparator is monitoring the VBUS_SENSE (secondary function of GPIO1) pin. This comparator is active when VCCA is greater than the POR threshold. Triggering the threshold level generates an interrupt. It can wake up the device from the SLEEP state, but can also switch on the device from the OFF state.

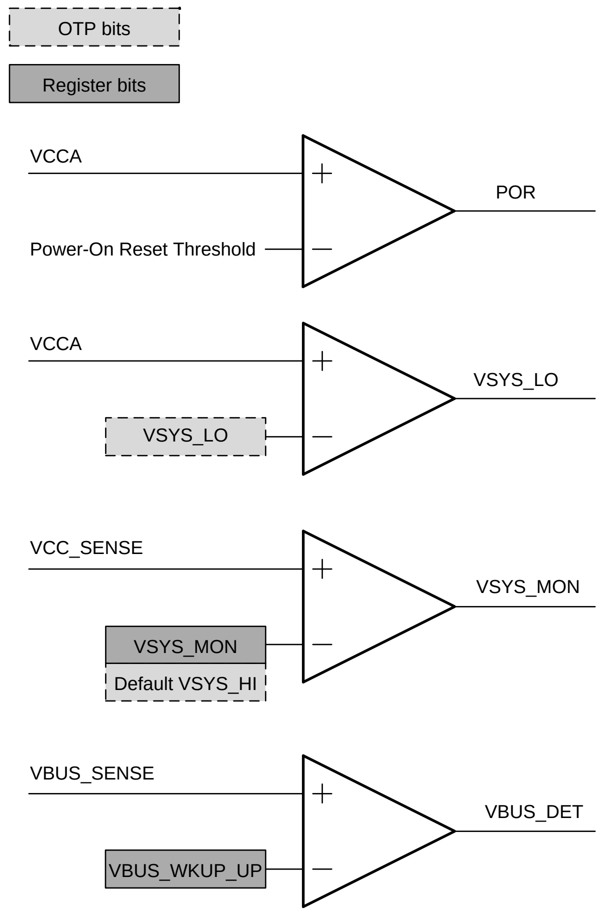

Figure 4. PMIC Comparators

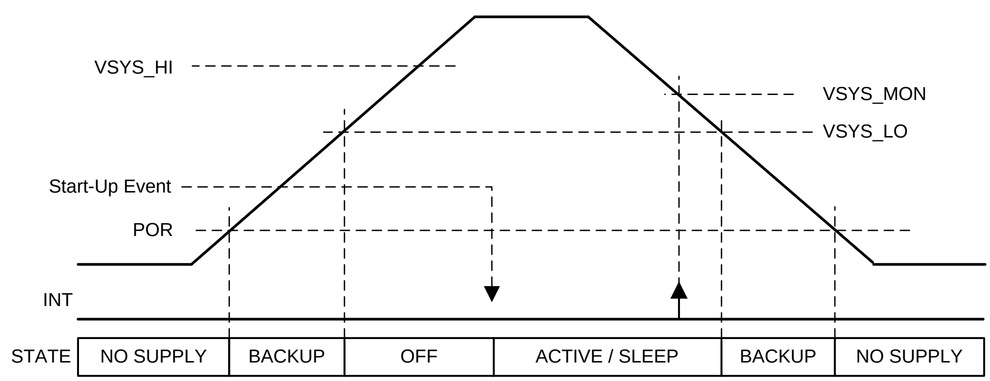

Figure 5. State Transitions

NOTE: The maximum input voltage of the VCC_SENSE pin depend on the OTP setting of PMU_CONFIG [HIGH_VCC_SENSE] as listed in the *Recommended Operating Conditions* table of the TPS65916 data sheet. This configuration is set as HIGH_VCC_SENSE = 0 with the VCC_SENSE and pins are connected to VCCA.

For the recommended operating conditions of the electrical parameters, see the TPS65916 data sheet.

5.2 SMPS

This section describes the default voltage for each SMPS.

Table 3. SMPS OTP Settings

Bit	Description [(1)]	0x4C Value	Unit
SMPS1_VOLTAGE	Default output voltage for the regulator	1.15	V
SMPS2_VOLTAGE	Default output voltage for the regulator	1.35	V
SMPS3_VOLTAGE	Default output voltage for the regulator	1.06	V
SMPS4_VOLTAGE	Default output voltage for the regulator	1.8	V
SMPS5_VOLTAGE	Default output voltage for the regulator	0	V
SMPS1_SMPS12_EN	SMPS12 single-phase or dual-phase configuration. 0: SMPS1 and SMPS2 single-phase 1: SMPS12 dual-phase	0	NA

(1) The regulator output voltage cannot be modified while active from one (0.7 to 1.65 V) voltage range to the other (1 to 3.3 V) voltage range or the other way around. The regulator must be turned off to do so.

5.3 LDO

This section describes the default output voltage for each LDO.

Table 4. LDO OTP Settings

Bit	Description	0x4C Value		Unit
		BOOT = 0	BOOT = 1	
LDO1_VOLTAGE	Default output voltage for the regulator	1.8	BYPASS	V
LDO2_VOLTAGE	Default output voltage for the regulator	1.8		V
LDO3_VOLTAGE	Default output voltage for the regulator	0		V
LDO4_VOLTAGE	Default output voltage for the regulator	3.3		V
LDO5_VOLTAGE	Default output voltage for the regulator	1.8		V

NOTE: LDO1 and LDO2 share a single input LDO12_IN and must by supplied by the same voltage. Refer to the input voltage parameter in the data sheet.

When LDO1 is in bypass mode, the input voltage on LDO12_IN should not exceed 3.6 V.

5.4 Interrupts

The interrupts are split into four register groups (INT1, INT2, INT3, and INT4). All interrupts are logically combined on a single output line, INT (default active-low). This line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the device. The OTP settings in this section show whether each interrupt is enabled or disabled by default.

Table 5. INT1 OTP Settings

Register	Bit	Description	0x4C Value
INT1_MASK	VSYS_MON	Enable and disable interrupt from the VSYS_MON comparator	1: Interrupt generation disabled
	PWRDOWN	Enable and disable interrupt from the PWRDOWN pin	0: Interrupt generated
	PWRON	Enable and disable interrupt from PWRON pin. A PWRON event is always an ON request.	1: Interrupt generation disabled
	LONG_PRESS_KEY	Enable and disable interrupt from long key press on the PWRON pin	1: Interrupt generation disabled
	HOTDIE	Enable and disable interrupt from device hot-die detection. The interrupt can be used as a pre-warning for processor to limit the PMIC load, before increasing die temperature forces shutdown.	0: Interrupt generated

Table 6. INT2 OTP Settings

Register	Bit	Description	0x4C Value
INT2_MASK	SHORT	Triggered from internal event of SMPS or LDO outputs failing. If an interrupt is enabled, it is an ON request.	0: Interrupt generated
	WDT	Enable and disable interrupt from watchdog expiration	0: Interrupt generated
	FSD	Enable and disable First Supply Detection (FSD) interrupt	1: Interrupt generation disabled
	RESET_IN	Enable and disable interrupt from the RESET_IN pin	1: Interrupt generated disabled

Table 7. INT3 OTP Settings

Register	Bit	Description	0x4C Value
INT3_MASK	VBUS	Interrupt to detect rising or falling VBUS line	1: Interrupt generation disabled
	GPADC_EOC_SW	GPADC result ready from software-initiated conversion	1: Interrupt generation disabled
	GPADC_AUTO_1	GPADC automatic conversion result 1 above or below the reference threshold	0: Interrupt generated
	GPADC_AUTO_0	GPADC automatic conversion result 0 above or below the reference threshold	0: Interrupt generated

Table 8. INT4 OTP Settings

Register	Bit	Description	0x4C Value
INT4_MASK	GPIO_6	Enable and disable interrupt from the GPIO6 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_5	Enable and disable interrupt from the GPIO5 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_4	Enable and disable interrupt from the GPIO4 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_3	Enable and disable interrupt from the GPIO3 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_2	Enable and disable interrupt from the GPIO2 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_1	Enable and disable interrupt from the GPIO1 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_0	Enable and disable interrupt from the GPIO0 pin rising or falling edge	1: Interrupt generation disabled

5.5 GPIO

TPS65916 integrate seven configurable general-purpose I/Os (GPIOs) that are multiplexed with alternative features. This section describes the default configuration of each GPIO, as well as the configuration of internal pullup or pulldown resistors on the GPIOs.

Table 9. GPIO Function OTP Settings

Register	Bit	Description	0x4C Value
PRIMARY_SECONDARY_PAD2	GPIO_6	Select pin function	POWERGOOD
	GPIO_5	Select pin function	POWERHOLD
	GPIO_4	Select pin function	REGEN2
PRIMARY_SECONDARY_PAD1	GPIO_3	Select pin function	SYNCDCDC
	GPIO_2	Select pin function	GPIO_2
	GPIO_1	Select pin function	NRESWARM
	GPIO_0	Select pin function	REGEN1

NOTE: The GPIO_0 pin is an open drain pin and therefore must be pulled up externally. TI does not recommend pulling the GPIO_0 pin up to any always-on signal such as VCCA or LDOVRTC_OUT. The GPIO_0 pin is configured as an input before the OTP memory is loaded at power up, and pulling the pin up to an always-on rail can cause a glitch on the GPIO_0 pin. Therefore, TI recommends pulling this signal up to a sequenced output, such as SMPS3 (1.8 V) or LDO4 (3.3 V).

Table 10 describes the pullup, pulldown, and open-drain settings for the corresponding GPIOs. These settings only apply in GPIO mode (for example: GPIO_0), and do not apply to any of the secondary functions (for example: REGENx, ENABLEx, POWERGOOD, and others). A full list of GPIO secondary functions, their associated input pullup and pulldown resistors, and output type is located in the *Signal Descriptions* table in the device data sheet.

Table 10. GPIO Pullup, Pulldown, and Open Drain Settings

Register	Bit	Description	0x4C Value
PU_PD_GPIO_CTRL2	GPIO_6_PD	Configure pulldown for GPIO_6	0: Pulldown disabled
	GPIO_5_PD	Configure pulldown for GPIO_5	0: Pulldown disabled
	GPIO_4_PU	Configure pullup for GPIO_4	0: Pullup disabled
	GPIO_4_PD	Configure pulldown for GPIO_4	0: Pulldown disabled
PU_PD_GPIO_CTRL1	GPIO_3_PD	Configure pulldown for GPIO_3	1: Pulldown enabled
	GPIO_2_PU	Configure pullup for GPIO_2	1: Pullup enabled
	GPIO_2_PD	Configure pulldown for GPIO_2	0: Pulldown disabled
	GPIO_1_PD	Configure pulldown for GPIO_1	0: Pulldown disabled
	GPIO_0_PD	Configure pulldown for GPIO_0	0: Pulldown disabled
OD_OUTPUT_GPIO	GPIO_4_OD	Configure GPIO_4 to be open-drain or push-pull	0: Push-pull
	GPIO_2_OD	Configure GPIO_2 to be open-drain or push-pull	0: Push-pull

Table 11 describes the polarity settings for each GPIO. These settings apply to both GPIO mode and secondary functions.

Table 11. GPIO Polarity Settings

Register	Bit	Description	0x4C Value
POLARITY_CTRL	GPIO_6_POLARITY	Enable or disable polarity inversion for GPIO_6	0: Inversion disabled
	GPIO_5_POLARITY	Enable or disable polarity inversion for GPIO_5	0: Inversion disabled
	GPIO_4_POLARITY	Enable or disable polarity inversion for GPIO_4	0: Inversion disabled
	GPIO_3_POLARITY	Enable or disable polarity inversion for GPIO_3	0: Inversion disabled
	GPIO_2_POLARITY	Enable or disable polarity inversion for GPIO_2	0: Inversion disabled
	GPIO_1_POLARITY	Enable or disable polarity inversion for GPIO_1	0: Inversion disabled
	GPIO_0_POLARITY	Enable or disable polarity inversion for GPIO_0	0: Inversion disabled

5.6 MISC

This section describes miscellaneous device configuration settings including pulldowns, polarity of signals, communication settings, and other functionality.

Table 12. MISC1 OTP Settings

Register	Bit	Description	0x4C Value
PU_PD_INPUT_CTRL1	RESET_IN_PD	Enable and disable internal pulldown for the RESET_IN pin	1: Pulldown enabled
	PWRDOWN_PD	Enable and disable internal pulldown for the PWRDOWN pin	1: Pulldown enabled

Table 13. MISC2 OTP Settings

Register	Bit	Description	0x4C Value
I2C_SPI	I2C_SPI	Selection of control interface, I^2C, or SPI	0: I^2C
	ID_I2C2	I2C_2 address for page access versus initial address (0H12)	0: Address is 0x12
	ID_I2C1	I2C_1 address for I^2C register access	I2C_1[0] = 1: 0x58 I2C_1[1] = 1: 0x59 I2C_1[2] = 1: 0x5A I2C_1[3] = 1: 0x5B
PMU_CONFIG	HIGH_VCC_SENSE	Enable internal buffers on VCC_SENSE to allow voltage sensing above 5.25 V	0: High VCC sense not enabled
	AUTODEVON	Automatically set DEV_ON bit after startup sequence completes	0: AUTODEVON disabled
	SWOFF_DLY	Delay before switch-off to allow host processor to save context. Device is maintained as ACTIVE until delay expiration then switches off.	00: No delay
PMU_CTRL2	INT_LINE_DIS	Configure INT output to be standard buffer or high-impedance buffer with pullup to VIO	0: Standard buffer: open-drain or push-pull
	WDT_HOLD_IN_SLEEP	Configure watchdog timer operation during device sleep state	1: Watchdog timer is suspended in sleep state
	PWRDOWN_FASTOFF	Configure shut-down sequence from PWRDOWN pin event	0: PWRDOWN pin event triggers sequenced shut down
	TSHUT_FASTOFF	Configure shut-down sequence from thermal shutdown event	0: Thermal shutdown triggers sequenced shut down
OD_OUTPUT_CTRL2	RESET_OUT_OD	Configure RESET_OUT to be push-pull or open-drain	0: RESET_OUT is push-pull
	REGEN2_OD	Configure REGEN2 to be push-pull or open-drain	0: REGEN2 is push-pull
PMU_SECONDARY_INT	FSD_MASK	Secondary level of mask for FSD interrupt line	1: FSD_INT_SRC is masked
POLARITY_CTRL	INT_POLARITY	Configure polarity of INT line	0: INT line is low when interrupt is pending
PRIMARY_SECONDARY_PAD2	SYNCCLKOUT	Configure SYNCCLKOUT to output SYNCDCDCCLK or CLK32KGO	0: SYNCDCDCCLK

5.7 SWOFF_HWRST

This section describes whether each reset type is configured to generate a HWRST or SWORST.

Hardware reset (HWRST) — A hardware reset occurs when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence). A HWRST will reset all registers in the HWRST and the SWORST domain, but leave the registers in the POR domain unchanged.

Switch-off reset (SWORST) — A switch-off reset occurs when any OFF request is configured to not generate a hardware reset. Like a HWRST, the device enters the OFF state from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence. A SWORST will only reset the SWO registers, and leave the registers in the POR and HWRST domains unchanged.

The power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally some registers control the SMPS and LDO voltages, REGENx signals, watchdog, and VSYS_MON comparator. This list is indicative only.

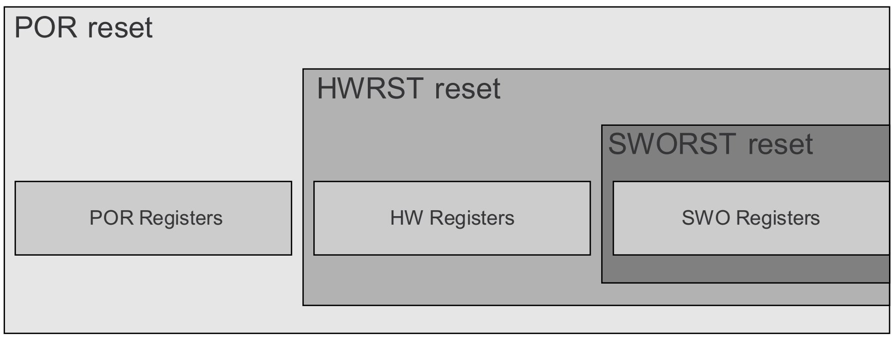

Figure 6. Reset Levels versus Registers

Table 14. SWOFF_HWRST OTP Settings

Register	Bit	Description	0x4C Value
SWOFF_HWRST	PWRON_LPK	Define if PWRON long key press is causing HWRST or SWORST	1: HWRST
	PWRDOWN	Define if PWRDOWN pin is causing HWRST or SWORST	0: SWORST
	WTD	Define if watchdog expiration is causing HWRST or SWORST	1: HWRST
	TSHUT	Define if thermal shutdown is causing HWRST or SWORST	1: HWRST
	RESET_IN	Define if RESET_IN pin is causing HWRST or SWORST	1: HWRST
	SW_RST	Define if register bit is causing HWRST or SWORST	1: HWRST
	VSYS_LO	Define if VSYS_LO is causing HWRST or SWORST	1: HWRST
	GPADC_SHUTDOWN	Define if GPADC event is causing HWRST or SWORST	0: SWORST

5.8 Shutdown_ColdReset

These OTP settings show whether each OFF request is configured to generate a shutdown request or cold reset request.

- When configured to generate a shutdown request, the embedded power controller (EPC) executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
- When configured to generate a cold reset request, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.

Table 15. Shutdown_ColdReset OTP Settings

Register	Bit	Description	0x4C Value
SWOFF_COLDRST	PWRON_LPK	Define if PWRON long key press causes shutdown or cold reset	0: Shutdown
	PWRDOWN	Define if PWRDOWN pin causes shutdown or cold reset	0: Shutdown
	WTD	Define if watchdog timer expiration causes shutdown or cold reset	1: Cold reset
	TSHUT	Define if thermal shutdown causes shutdown or cold reset	0: Shutdown
	RESET_IN	Define if RESET_IN pin causes shutdown or cold reset	0: Shutdown
	SW_RST	Define if SW_RST register bit causes shutdown or cold reset	1: Cold reset
	VSYS_LO	Define if VSYS_LO causes shutdown or cold reset	0: Shutdown
	GPADC_SHUTDOWN	Define if GPADC shutdown causes shutdown or cold reset	0: Shutdown

6 Sequence Platform Settings

A power sequence is an automatic preprogrammed sequence handled by the TPS65916 device to configure the device resources: SMPSs, LDOs, and REGEN functions (multiplexed with GPIO pins) into ON, OFF, or SLEEP state.

6.1 OFF2ACT Sequences

When an ON request occurs in the OFF state, the device is switched on and each resource is enabled based on the programmed OFF2ACT sequence.

Figure 7 shows the OFF2ACT sequence of the TPS659163RGZR.

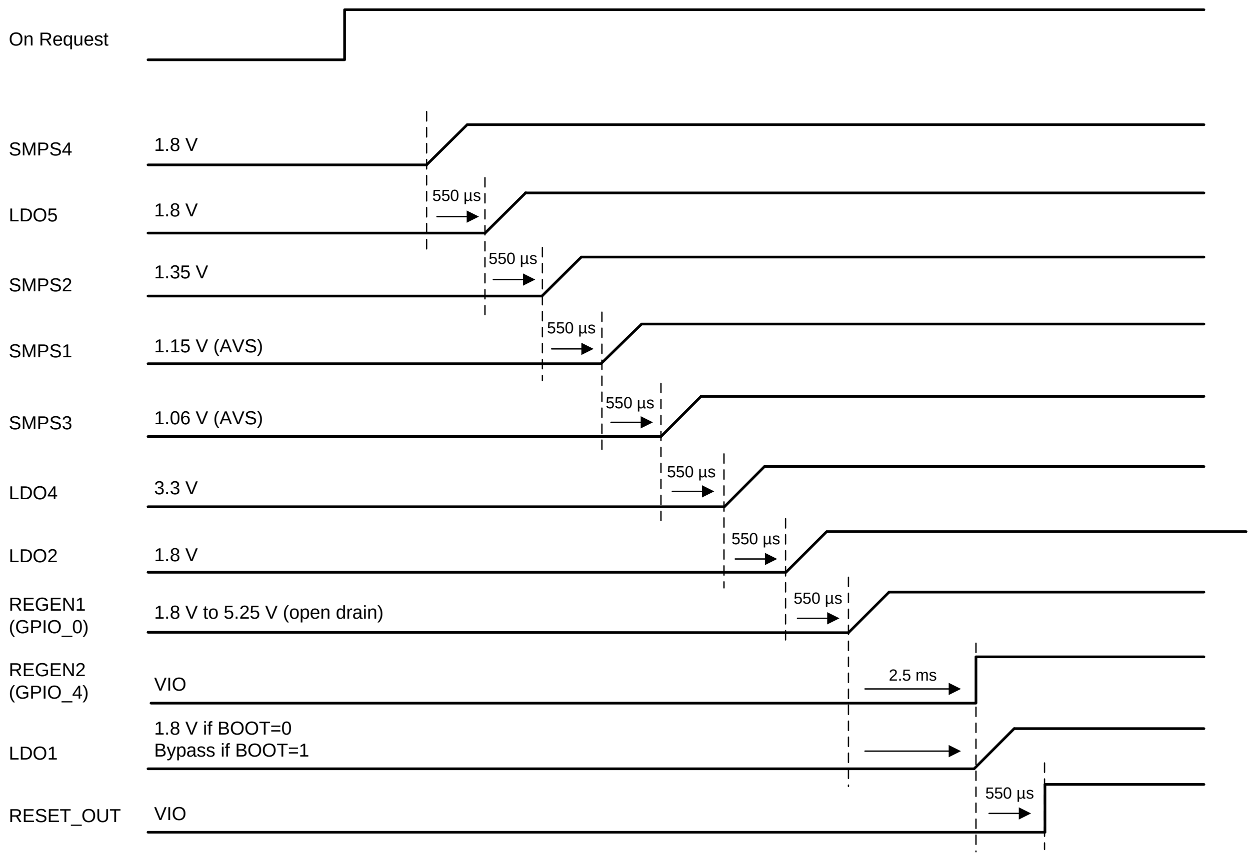

Figure 7. OFF2ACT Sequence of TPS659163RGZR

6.2 ACT2OFF Sequences

When an OFF request occurs during active mode, each resource is disabled based on the programmed ACT2OFF sequence.

Figure 8 shows the ACT2OFF sequence of TPS659163RGZR.

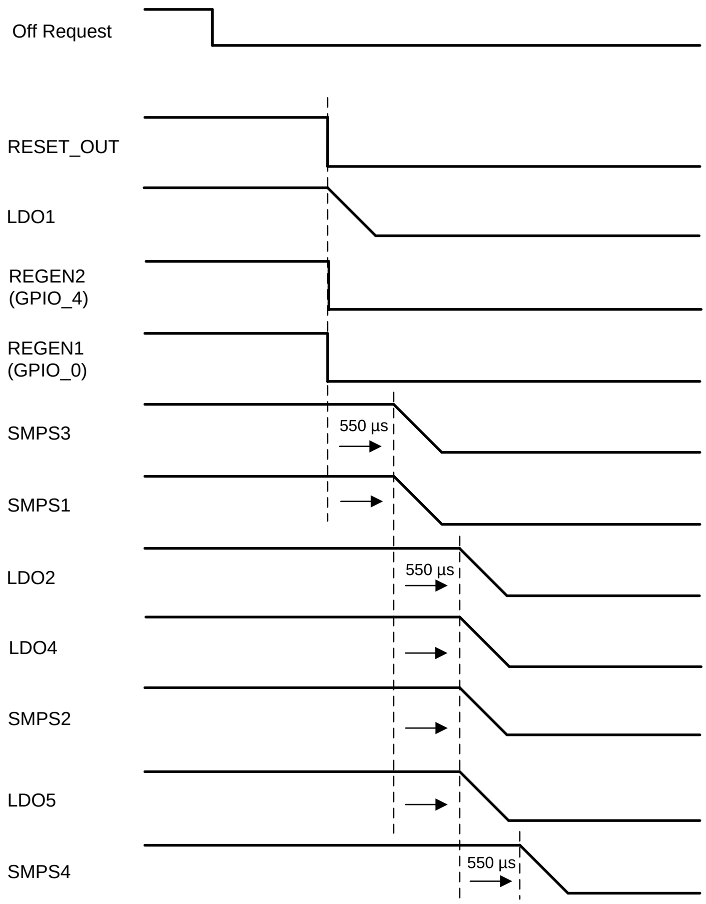

Figure 8. Power Down Sequence of TPS659163RGZR

6.3 Warm Reset Sequences

A warm reset is triggered by setting NRESWARM (GPIO_1) low, which causes the OFF2ACT sequence to be executed regardless of the actual state (ACTIVE, SLEEP), and the device returns to or remains in the ACTIVE state. Resources that are part of power-up sequence go to ACTIVE mode and the output voltage level is reloaded from OTP or kept in the previous value depending on the WR_S bit in the SMPSx_CTRL register or the LDOx_CTRL register. Resources that are not part of the OFF2ACT sequence are not impacted by a warm reset and maintain the previous state.

Additionally, if BOOT=1, then RESET_OUT is asserted low during the worm reset sequence. If BOOT=0, RESET_OUT is not asserted low. If BOOT=1 is used, then the PMIC must be enabled by the POWERHOLD (GPIO_5) pin. If the PMIC is enabled by the PWRON pin and kept on using the DEV_ON bit, then BOOT=0 must be used. If POWERHOLD is set to GND while BOOT=1, the PMIC will shut off during the warm reset sequence.

Figure 9 shows the warm reset sequence of TPS659163RGZR. If any resource is on when NRESWARM is asserted, the resource remains on as shown by the solid **black** lines. The dashed **red** lines show the timing in case any resource is off before the warm reset. If VIO_IN is switched off before the warm reset sequence, then RESET_OUT and GPIO_4 will be off because they are in the VIO domain. In this example, VIO_IN is supplied by SMPS4, so RESET_OUT follows the SMPS4 timing.

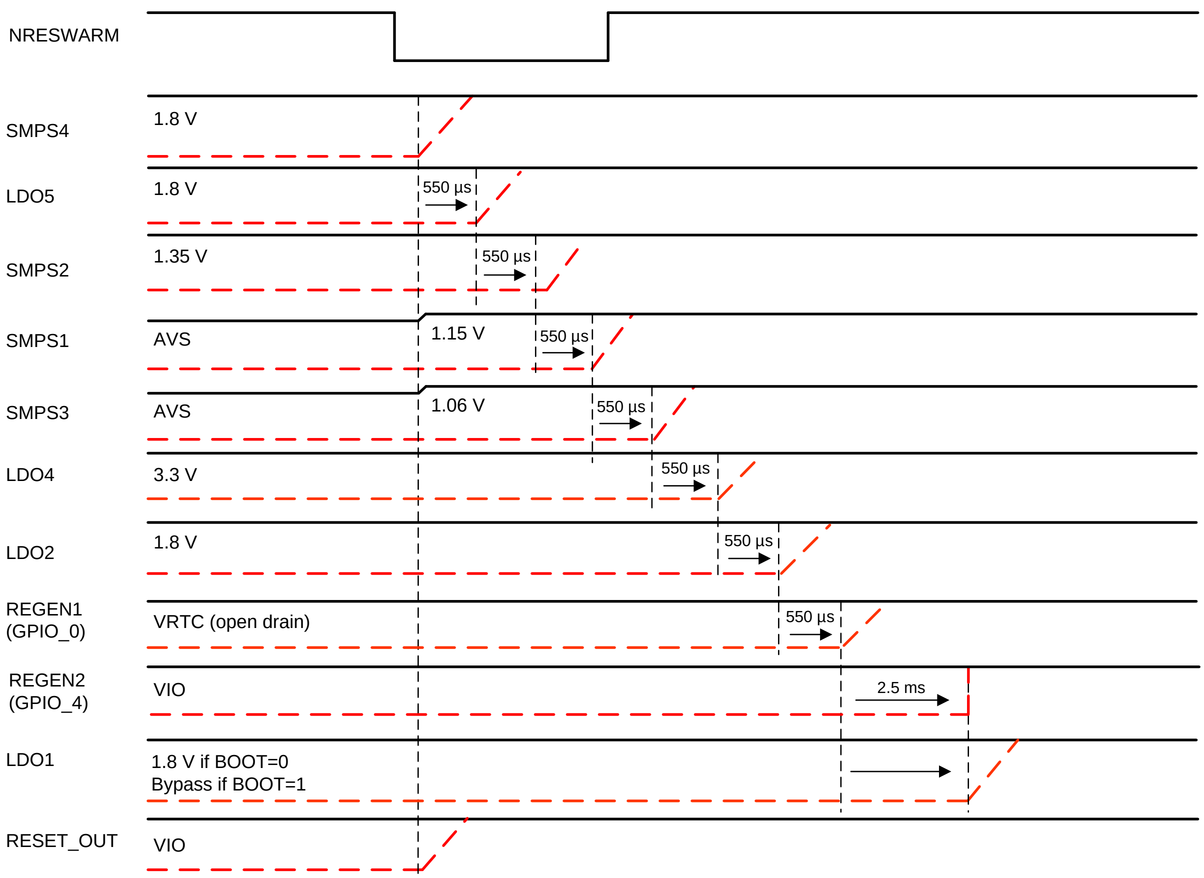

Figure 9. Warm Reset Sequence of TPS659163RGZR

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to A Revision	Page
• Added LP8733 and LP8732 solution information, and link to user's guide	2
• Added information and diagrams on the two power up options for the TPS65916.	3

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265