User's Guide

TPS54424 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54424EVM-779 evaluation module (PWR779) as well as for the TPS54424 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS54424EVM-779.

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Trademarks

1 Introduction

1.1 Background

The TPS54424 dc/dc converter is a synchronous buck converter designed to provide up to an 4-A output. The input (VIN) is rated for 4.5 V to 17 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54424 regulator. The RT/CLK pin is configured for 700-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS54424 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54424 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS54424 provides adjustable soft start and undervoltage lockout inputs and a power good output.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54424EVM-779	V_{IN} = 4.5 V to 17 V	0 A to 4 A

1.2 Performance Specification Summary

A summary of the TPS54424EVM-779 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54424EVM-779 is designed and tested for V_{IN} = 4.5 V to 17 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54424EVM-779 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
V_{IN} voltage range		4.5	12	17	V
V_{IN} start voltage			4.5		V
V_{IN} stop voltage			4		V
Output voltage setpoint			1.8		V
Output current range	V_{IN} = 4.5 V to 17 V	0		4	A
Load regulation	V_{IN} = 4.5 V to 17 V, I_O = 4 A		–0.05%		
Load transient response	I_O = 1 A to 3 A		–70		mV
	I_O = 3 A to 1 A		70		mV
Loop bandwidth	V_{IN} = 12 V, I_O = 4 A		80		kHz
Phase margin	V_{IN} = 12 V , I_O = 4 A		50		degree
Input ripple voltage	I_O = 4 A		200		mVPP
Output ripple voltage	I_O = 4 A		10		mVPP
Output rise time			1.1		ms
Operating frequency			700		kHz

Table 1-2. TPS54424EVM-779 Performance Specification Summary (continued)

Specification	Test Conditions		MIN	TYP	MAX	Unit
Peak efficiency	TPS54424EVM-779, V_{IN} = 5 V, I_O = 1.6 A to 1.8 A			94.0%		
		TPS54424EVM-779, V_{IN} = 12 V, I_O = 3 A		89.4%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54424. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R8 and R6. R6 is fixed at 6.04 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R6 can change the output voltage above the 0.6-V reference voltage V_{REF}. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = R6 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (1)$$

1.3.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R2 and R9. See the TPS54424 datasheet () for detailed instructions for setting the external UVLO.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54424EVM-779 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes.

2.1 Input/Output Connections

The TPS54424EVM-779 is provided with input/output connectors and test points as shown in Table 2-1. To support the full current capability of an unmodified TPS54424EVM-779, a power supply capable of supplying greater than 2 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability before hitting current limit is typically 6 A to 7 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP7 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP9 as the ground reference.

Table 2-1. TPS54424EVM-779 EVM Connectors and Test Points

Reference Designator	Function
J1	VIN input voltage connector (see Table 1-1 for V_{IN} range)
J2	VOUT terminal to connect load
J3	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J4	2-pin header for power good resistor pullup connection. Add a shunt to pull up to VOUT only if VOUT < 6.0 V. If VOUT > 6.0 V keep open and use external supply with TP5 to pullup PGOOD.
TP1	VIN test point
TP2	EN test point
TP3	SW node test point
TP4	1.8-V test point
TP5	PGOOD pullup test point
TP6	PGOOD test point
TP7	PGND test point
TP8	SS/TRK test point
TP9	PGND test point
TP10	Test point between voltage divider network and output of TPS54424 converter. Used for loop response measurements.
TP11	PGND test point
TP12	AGND test point
TP13	AGND test point
TP14	PGND test point
TP15	Test point for supplying external CLK for synchronization. C20 and R10 should be populated to use.

2.2 Efficiency

Figure 2-1 shows the efficiency for the TPS54424EVM-779 at an ambient temperature of 25°C. The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases toward full load.

Figure 2-2 shows the efficiency for the TPS54424EVM-779 using a semi-log scale to more easily show efficiency at lower output currents. The TPS54424 operates in continuous conduction mode at light loads in order to keep a fixed frequency and this results in lower efficiency at lower output currents.

Figure 2-3 shows the efficiency for the TPS54424EVM-779 versus input voltage with a fixed load.

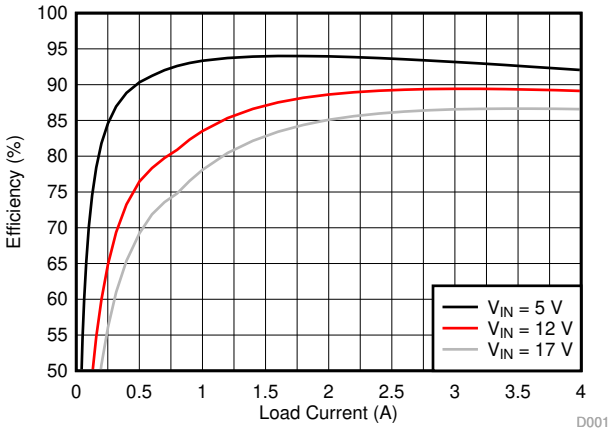

Figure 2-1. TPS54424EVM-779 Efficiency

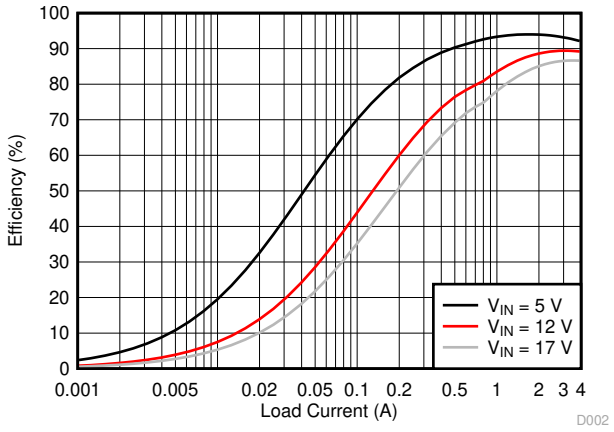

Figure 2-2. TPS54424EVM-779 Low Current Efficiency

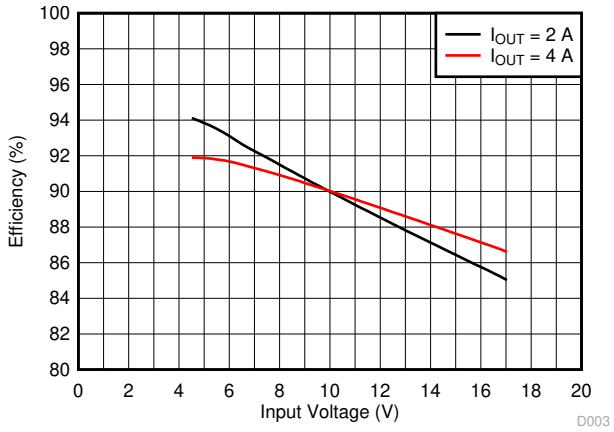

Figure 2-3. TPS54424EVM-779 Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFETs.

2.3 Output Voltage Regulation

Figure 2-4 shows the load regulation for the TPS54424EVM-779. Figure 2-5 shows the line regulation for the TPS54424EVM-779.

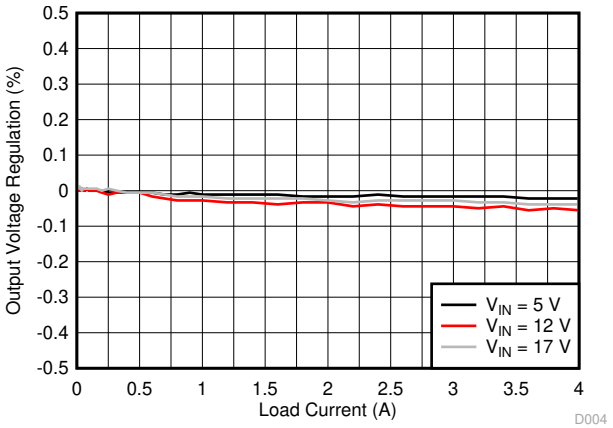

Figure 2-4. TPS54424EVM-779 Load Regulation

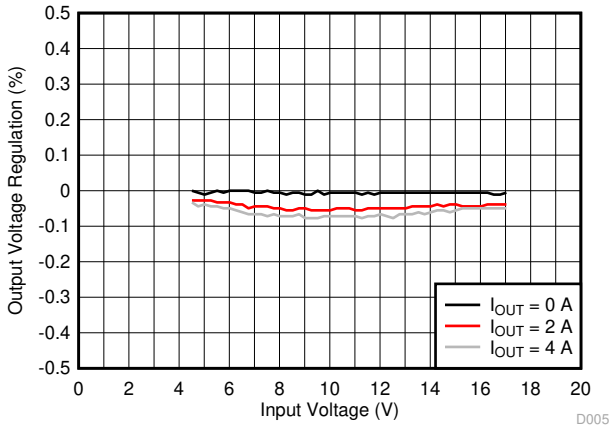

Figure 2-5. TPS54424EVM-779 Line Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Load Transient and Loop Response

Figure 2-6 shows the TPS54424EVM-779 response to load transients. The current step is from 1 A to 3 A. The current step slew rate is 1 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2-7 shows the TPS54424EVM-779 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 2 A.

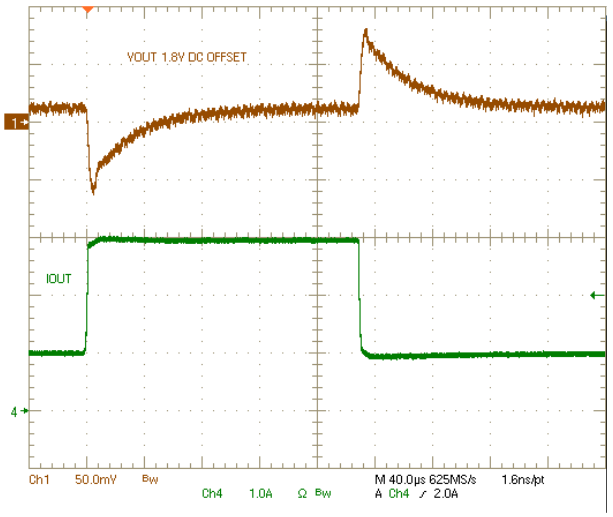

Figure 2-6. TPS54424EVM-779 Transient Response

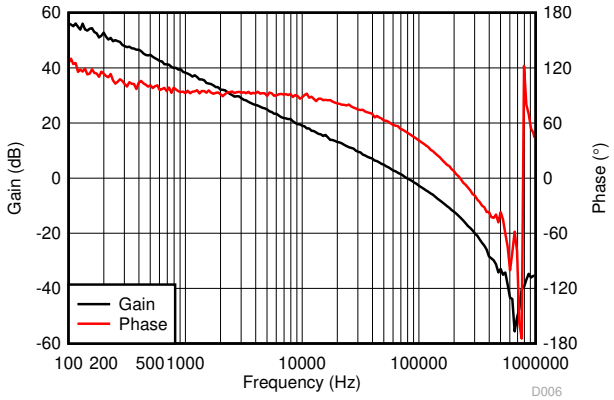

Figure 2-7. TPS54424EVM-779 Loop Response

2.5 Output Voltage Ripple

Figure 2-8 and Figure 2-9 show the TPS54424EVM-779 output voltage ripple. The load currents are no load and 4 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP9 and TP4.

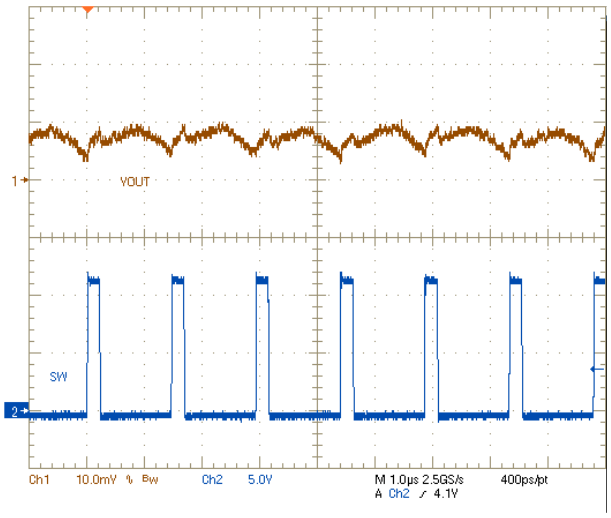

Figure 2-8. TPS54424EVM-779 Output Ripple, No Load

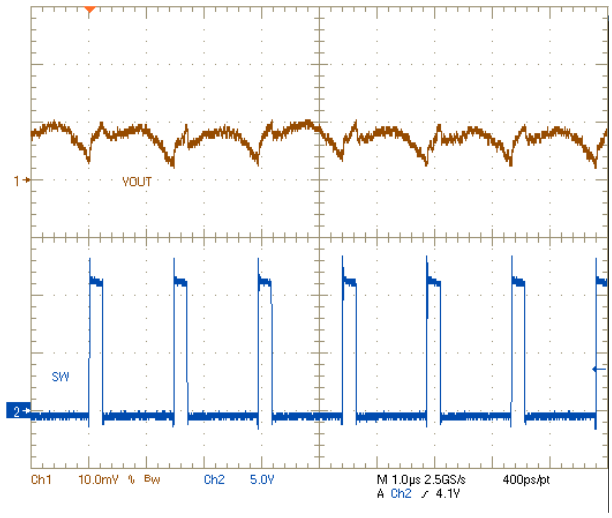

Figure 2-9. TPS54424EVM-779 Output Ripple, 4-A Load

2.6 Input Voltage Ripple

Figure 2-10 and Figure 2-11 show the TPS54424EVM-779 input voltage ripple. The load currents are no load and 4 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP1 and TP7.

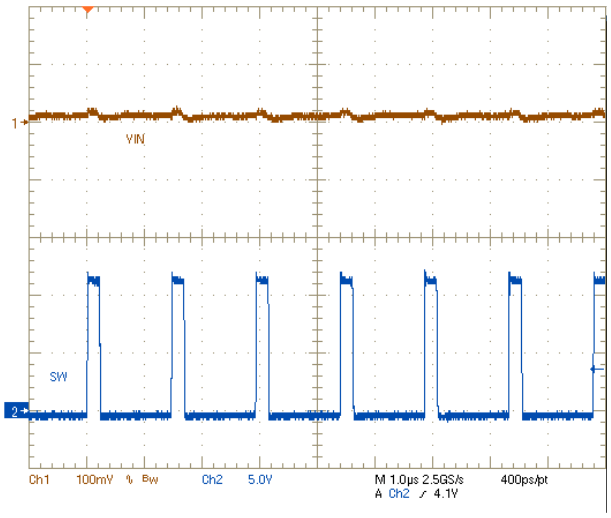

Figure 2-10. TPS54424EVM-779 Input Ripple, No Load

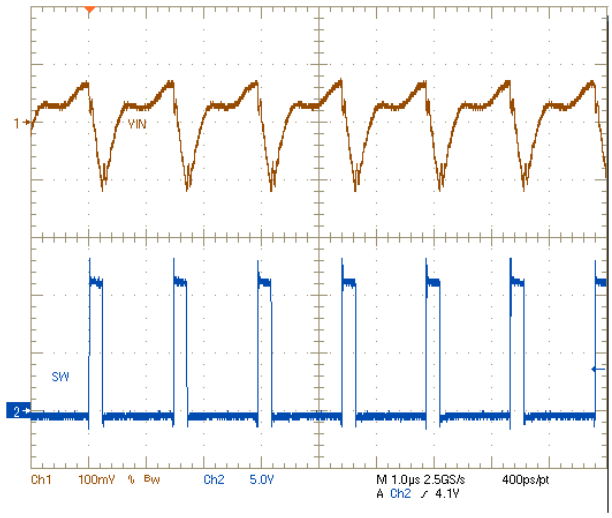

Figure 2-11. TPS54424EVM-779 Input Ripple, 4-A Load

2.7 Powering Up

Figure 2-12 and Figure 2-13 show the start-up waveforms for the TPS54424EVM-779. In Figure 2-12, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 2-13, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 12 V and the load is 1

Ω. Alternatively, a jumper at J3 to tie EN to GND can also be used. When the jumper is removed, EN is released and the start-up sequence will begin.

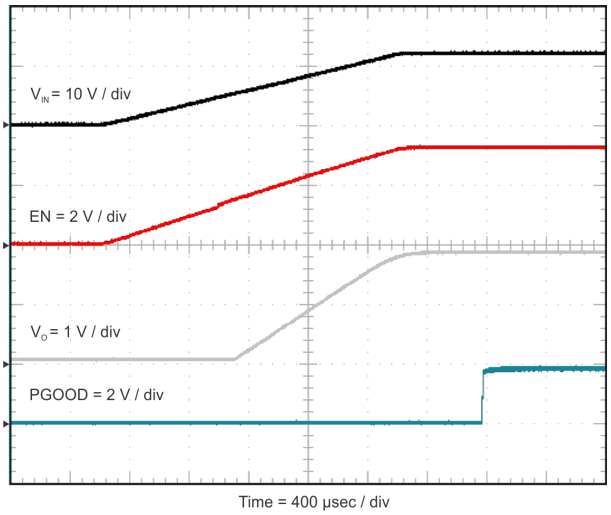

Figure 2-12. TPS54424EVM-779 Start-Up Relative to V_{IN}

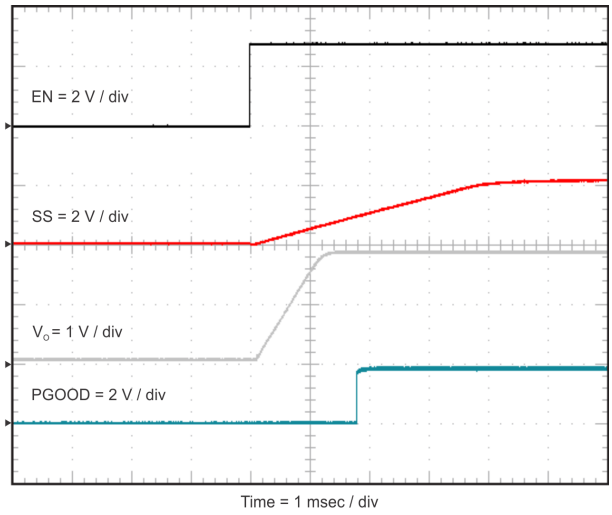

Figure 2-13. TPS54424EVM-779 Start-Up Relative to Enable

2.8 Powering Down

Figure 2-14 and Figure 2-15 show the TPS54424EVM-779 shutdown. The input voltage for these plots is 12 V and the load is 1 Ω.

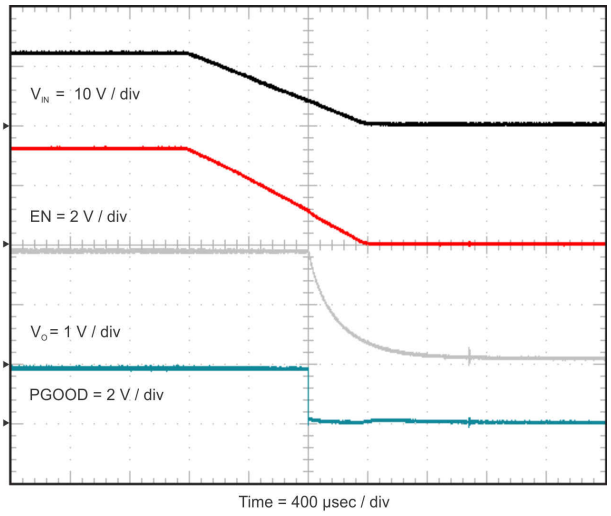

Figure 2-14. TPS54424EVM-779 Shutdown Relative to V_{IN}

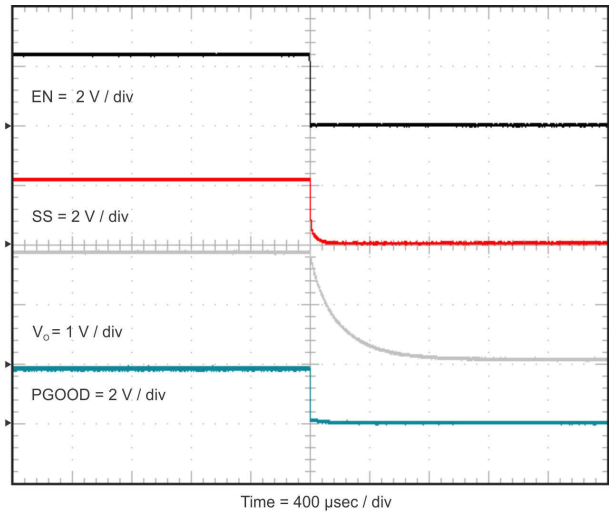

Figure 2-15. TPS54424EVM-779 Shutdown Relative to Enable

2.9 Start-Up Into Pre-Bias

Figure 2-16 shows the TPS54424EVM-779 start up into a pre-biased output. The output voltage is pre-biased to 1 V.

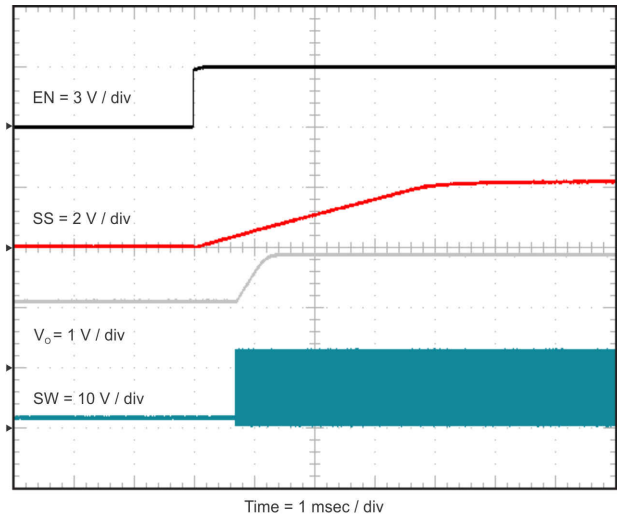

Figure 2-16. TPS54424EVM-779 Start-Up Into Pre-Bias

2.10 Hiccup Mode Current Limit

Figure 2-17, Figure 2-18, and Figure 2-19 show the TPS54424EVM-779 hiccup mode current limit feature. When an overcurrent event occurs, the TPS54424EVM-779 shuts down and restarts. Figure 2-17 shows the TPS54424EVM-779 entering hiccup mode in an overcurrent condition. Figure 2-18 shows TPS54424EVM-779 entering hiccup mode with a longer timescale to show the hiccup period. Figure 2-19 shows TPS54424EVM-779 exiting hiccup mode after the overcurrent condition is removed.

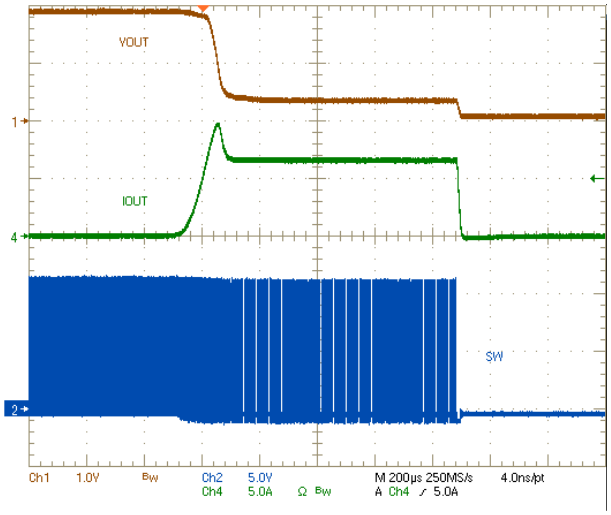

Figure 2-17. TPS54424EVM-779 Hiccup Mode Current Limit

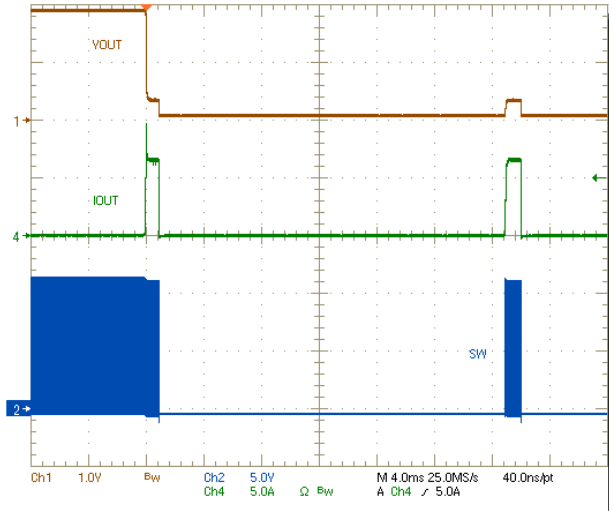

Figure 2-18. TPS54424EVM-779 Hiccup Mode Start

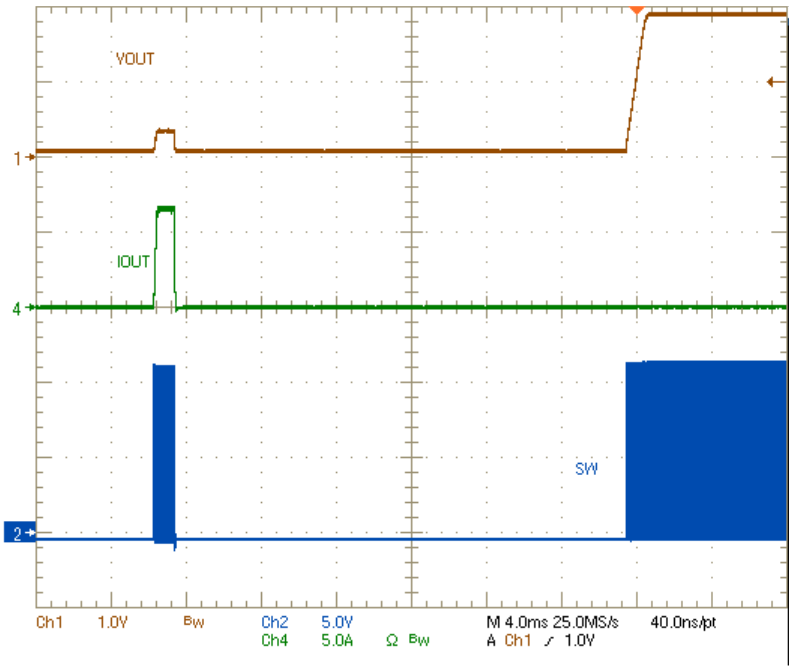

Figure 2-19. TPS54424EVM-779 Hiccup Mode Stop

3 Board Layout

This section provides a description of the TPS54424EVM-779 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54424EVM-779 is shown in Figure 3-2 through Figure 3-5. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for VIN, VOUT, and SW. Also on the top layer are connections for the remaining pins of the TPS54424 and the majority of the signal traces. The top layer has dedicated ground plane for quiet analog ground that is connected to the main power ground plane at a single point. The internal layer-1 is a large ground plane and also routes signals to test points. The internal layer-2 contains an additional large ground copper area as well as an additional VIN and VOUT copper fill. The bottom layer is another ground plane with two additional traces for the output voltage feedback. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP4 test point. An additional input bulk capacitor is used to limit the noise entering the converter from the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS/TRK capacitor, RT/CLK resistor, and COMP pin are terminated to the quiet analog ground island on the top layer.

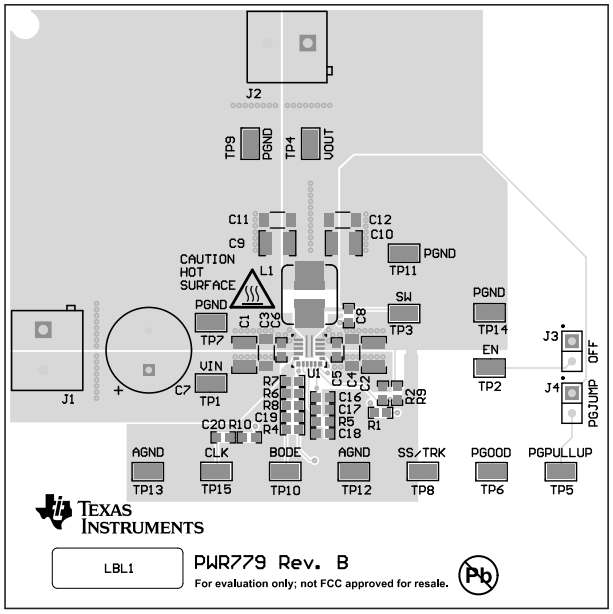

Figure 3-1. TPS54424EVM-779 Top-Side Composite View

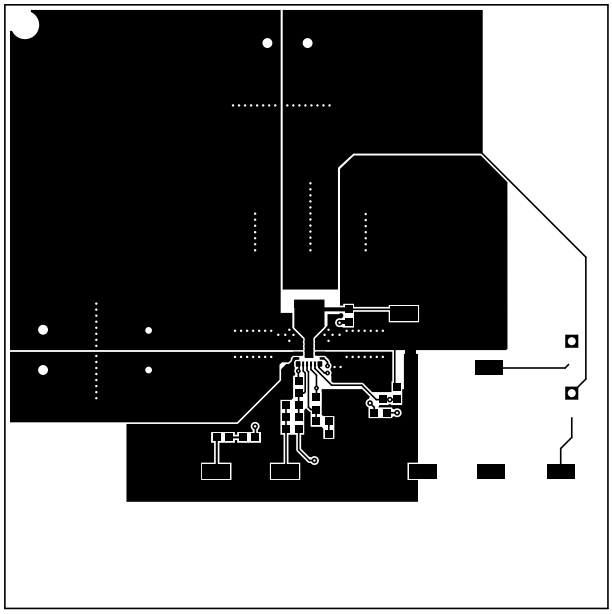

Figure 3-2. TPS54424EVM-779 Top-Side Layout

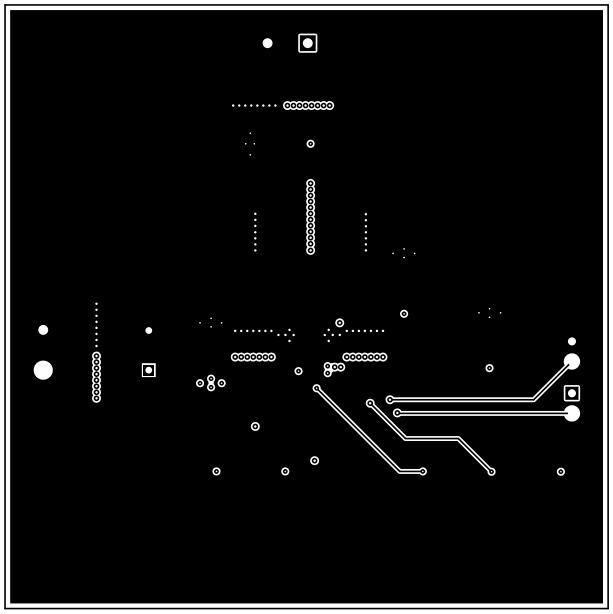

Figure 3-3. TPS54424EVM-779 Internal Layer-1 Layout

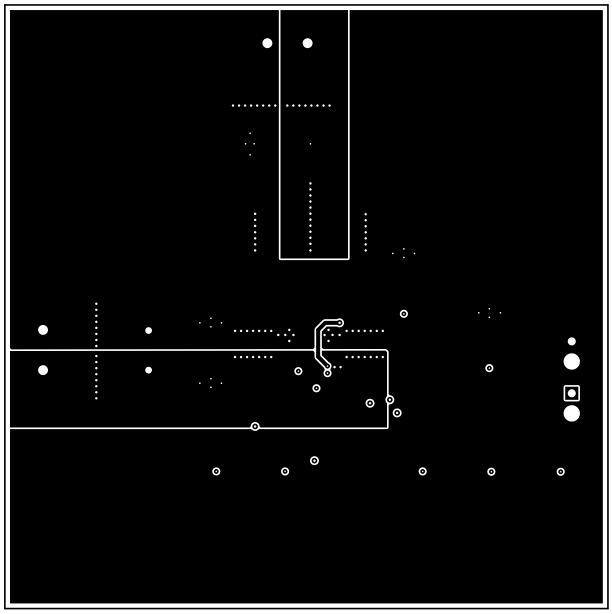

Figure 3-4. TPS54424EVM-779 Internal Layer-2 Layout

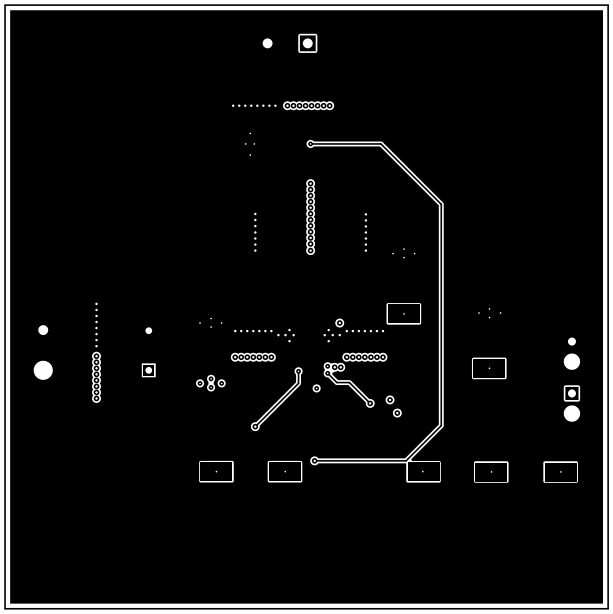

Figure 3-5. TPS54424EVM-779 Bottom-Side Layout

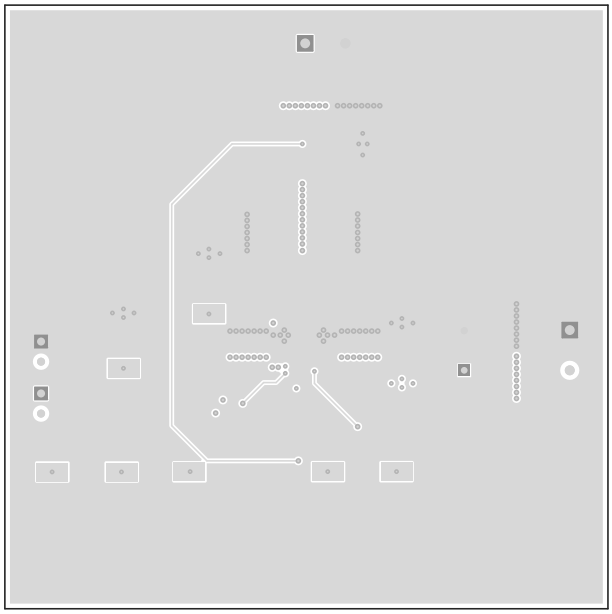

Figure 3-6. TPS54424EVM-779 Bottom-Side Composite View

4 Schematic and Bill of Materials

This section presents the TPS54424EVM-779 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54424EVM-779.

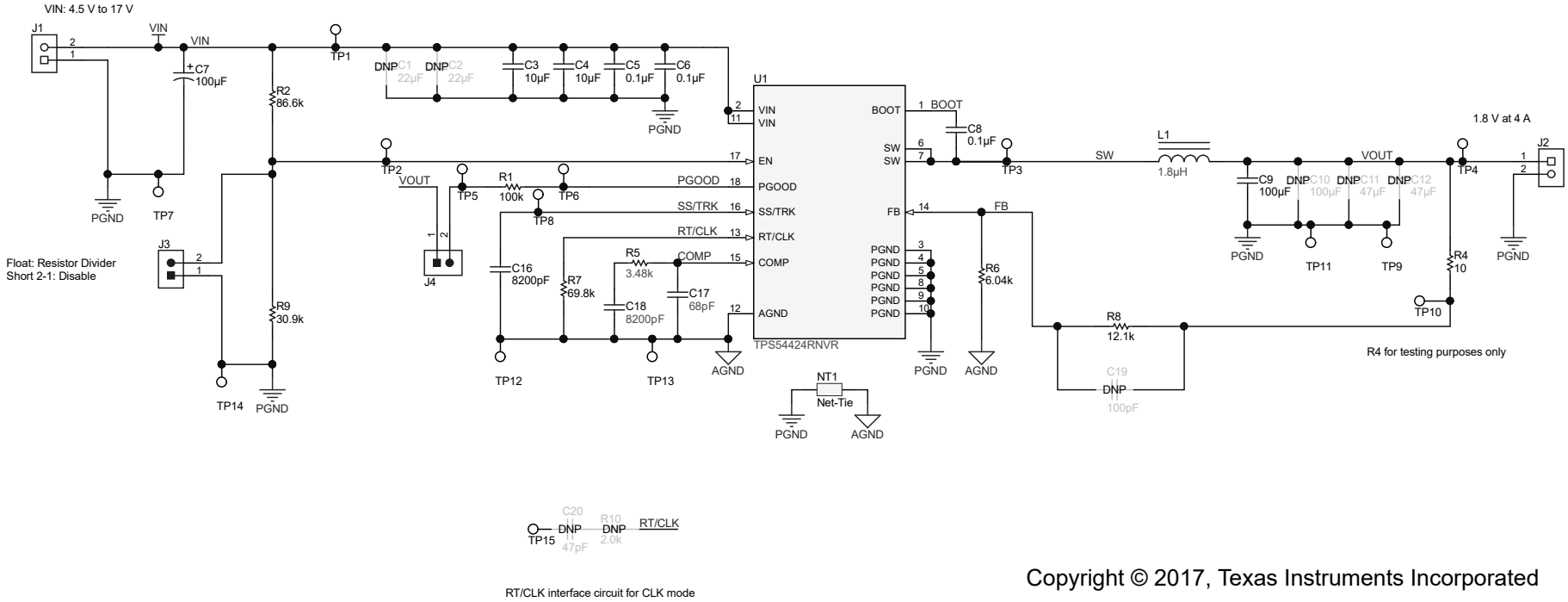

Figure 4-1. TPS54424EVM-779 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54424EVM-779.

Table 4-1. TPS54424EVM-779 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C3, C4	2	10 µF	CAP, CERM, 10 µF, 25 V, ± 10%, X5R, 1206	1206	GRM31CR61E106KA12L	Murata
C5, C6, C8	3	0.1 µF	CAP, CERM, 0.1 µF, 25V, ±10%, X7R, 0603	0603	06033C104KAT2A	AVX
C7	1	100 µF	CAP, AL, 100 µF, 50 V, ±20%, 0.18 Ω, TH	Cap, 10x12.5mm	UBT1H101MPD1TD	Nichicon
C9	1	100 µF	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1210	1210	GRM32ER60J107ME20L	Murata
C16, C18	2	8200 pF	CAP, CERM, 8200 pF, 25 V, ±10%, X7R, 0603	0603	GRM188R71E822KA01D	Murata
C17	1	68 pF	CAP, CERM, 68 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H680JA01D	Murata
J1, J2	2		Terminal Block, 5.08 mm, 2 × 1, Brass, TH	2 × 1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J3, J4	2		Header, 100 mil, 2 × 1, Gold, TH	Header, 100 mil, 2 × 1, TH	HTSW-102-07-G-S	Samtec
L1	1	1.8 µH	Inductor, Shielded, Powdered Iron, 1.8 µH, 5.8 A, 0.021 Ω, SMD	4.1 × 4.1 mm	74438357018	Wurth Elektronik

Table 4-1. TPS54424EVM-779 Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R1	1	100 k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R2	1	86.6 k	RES, 86.6 k, 1%, 0.1 W, 0603	0603	CRCW060386K6FKEA	Vishay-Dale
R4	1	10	RES, 10, 5%, 0.1 W, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R5	1	3.48 k	RES, 3.48 k, 1%, 0.1 W, 0603	0603	CRCW06033K48FKEA	Vishay-Dale
R6	1	6.04 k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	CRCW06036K04FKEA	Vishay-Dale
R7	1	69.8 k	RES, 69.8 k, 1%, 0.1 W, 0603	0603	CRCW060369K8FKEA	Vishay-Dale
R8	1	12.1 k	RES, 12.1 k, 1%, 0.1 W, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
R9	1	30.9 k	RES, 30.9 k, 1%, 0.1 W, 0603	0603	CRCW060330K9FKEA	Vishay-Dale
SH-J1, SH-J2	2	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	15		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		4.5-V to 17-V Input, 8-A Synchronous Step-Down Voltage Regulator, RNV0018B (VQFN-HR-18)	RNV0018B	TPS54424RNVR	Texas Instruments
C1, C2	0	22 µF	CAP, CERM, 22 µF, 35 V, ±20%, X5R, 1206	1206	C3216X5R1V226M160AC	TDK
C10	0	100 µF	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1210	1210	GRM32ER60J107ME20L	Murata
C11, C12	0	47 µF	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 1206	1206	GRM31CR60J476ME19L	Murata
C19	10	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	885012006057	Wurth Elektronik
C20	0	47 pF	CAP, CERM, 47 pF, 50 V, ±5%, C0G/NP0, 0603	0603	06035A470JAT2A	AVX
R10	0	2.00 k	RES, 2.00 k, 1%, 0.1 W, 0603	0603	CRCW06032K00FKEA	Vishay-Dale

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2017) to Revision A (September 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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