UCD90xxx Sequencer Schematics Guidelines

This document is a quick guideline to help the user perform a schematics review to achieve the best performance. This document does not apply to the UCD9080 and UCD9081 devices.

1 Introduction

The UCD90xxx family of digital power supply sequencers, also known as system health monitors are flexible and powerful enough to meet users sequencing, monitoring, margining and other needs. The entire family of devices are designed to have similar behaviors, with a different number of rails or some other minor features. Users only need to learn how to use the device once, and can then seamlessly switch to other devices within the family that best fit their future designs. This document is a quick guideline to help user to perform a schematics review to achieve the best performance. This document does not apply to the UCD9080 and UCD9081 device.

2 UCD Power Supply Review

If a brownout circuit is used, ensure that forward voltage of the selected Schottky diode does not trigger the brownout voltage threshold under operational temperature range. The pullup source for the $\overline{\text{RESET}}$ signal must be connected to the cathode side of the diode, if brownout circuitry is used.

2.1 UCD90240, UCD90320 and UCD90320U

The UCD90240, UCD90320 and UCD90320U devices have the following power supply parameters:

- Pin A2, G13, M12, and N10 leave floating or isolated
- Pin G12, K11, M10 and N13 ties to DVSS
- K12 ties to V33D
- Three 1-µF X7R ceramic capacitors in parallel with two 0.1-µF X7R ceramic capacitors for BPCAP decoupling
- Two 1-µF X7R ceramic capacitors in parallel with four 0.1-µF X7R ceramic capacitors and two 0.01-µF X7R ceramic capacitors for V33D decoupling
- One 1-µF X7R ceramic capacitor in parallel with one 0.1-µF X7R ceramic capacitor and one 0.01-µF X7R ceramic capacitor for V33A decoupling. A 1-Ω resistor can be placed between V33D and V33A to decouple the noise on V33D from V33A.
- One 1-µF X7R ceramic capacitor in parallel with one 0.01-µF X7R ceramic capacitor for VREFA+ decoupling (if used)
- Place decoupling capacitors as close to the device as possible
- If an application does not use the $\overline{\text{RESET}}$ signal, the $\overline{\text{RESET}}$ pin must be tied to V33D, either by direct connection to the nearest V33D pin, or by an R-C circuit as shown in Figure 1.

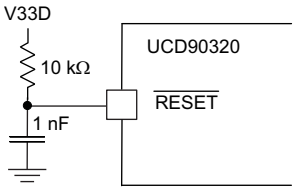

Figure 1. $\overline{\text{RESET}}$ With R-C Network

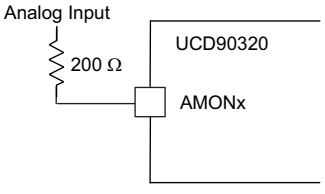

Figure 2. Example of Analog Inputs

2.2 Remaining UCD90xxx Devices

For supply-voltage decoupling, provide power-supply pin bypass to the device as follows:

- The $\overline{\text{TRST}}$ pin must have a 10-kΩ pulldown resistor to ground
- The $\overline{\text{RESET}}$ pin must have a 10-kΩ pullup resistor to V33D and 1-nF decoupling capacitor to ground as shown in Figure 1. The components should be placed as close to the $\overline{\text{RESET}}$ pin as possible
- 1-μF, X7R ceramic in parallel with 0.01-μF, X7R ceramic at the BPCAP pin
- 0.1-μF, X7R ceramic in parallel with 4.7-μF, X5R ceramic at the V33D pin
- 0.1-μF, X7R ceramic in parallel with 4.7-μF, X5R ceramic at the V33A pin
- 0.1-μF, X7R ceramic at pin 7 (V33DIO1 if applicable)
- Connect the V33D pin, V33DIO1 pin (if applicable), and V33DIO2 pin (if applicable), directly to the 3.3-V supply
- Connect V33A to V33D through a 4.99-Ω resistor. This resistor and V33A decoupling capacitors form a low-pass filter to reduce noise on V33A, which improves the ADC accuracy

3 I/O Signals Review

All pullup resistors must use the same 3.3-V source as the UCD90xxx devices.

It is recommended to ground all unused pins.

3.1 Analog Monitor (MONx/AMONx) Pin Review

The following list provides analog monitor (MONx/AMONx) pin information:

- Internal or external voltage reference is used by ADC to monitor the external signal. Be sure to have the proper voltage divider to limit the input signal.

Table 1. UCD90xxx Voltage References

	UCD90240, UCD90320 and UCD90320U	Remaining UCD90xxx Devices
Internal Voltage Reference	V33D	2.5 V
External Voltage Reference	2.4–3 V	N/A

- When a digital signal is connected to the analog monitor (MONx/AMONx) pin, please check the logic level of the input signal to see whether it is over the voltage reference
- TI recommends having a 10-nF to 100-nF decoupling capacitor close to the analog monitor (MONx/AMONx) pin to remove rail ripple voltage
- For UCD90240,UCD90320 and UCD90320U, TI recommends maintaining at least a 200-Ω resistance between a low-impedance analog input and an AMON pin. For example, when monitoring a rail voltage without a resistor divider, place a 200-Ω resistor in series between the rail output and AMON pin, as shown in Figure 2.
- Ground unused MONx/AMONx pins to save power consumption and decrease EMI.

3.2 PMBUS Signals Review

Pull up SCL and SDA (2.2 kΩ recommended) to the same power supplies as the UCD devices. The ALERT signal is pulled up to the same 3.3-V source as SCL or SDA. When the CONTROL pin is not used, either pull it down or up, the device does not care about the input state of the CONTROL pin. Do not leave it floating.

For the UCD90xxx (other than the UCD90240,UCD90320 and UCD90320U), make sure the resistors used for PMBUS_ADDRESS give a valid 7-bit I^2C address other than 126.

3.3 GPIO Pins Review

Consider the initial I/O states detailed in Table 2 when the device is under reset and initialization, and consider their impact to the application circuitry.

Table 2. Initial I/O States of UCD90xxx

DEVICE	RESET I/O STATE
UCD90240	Hi-Z
UCD90320	
UCD90320U	
UCD90xxx	FPWM pins are low, all other I/O pins are Hi-Z

3.4 Margin Pins Review

It is a good design practice to provide a series impedance of 20 Ω to 33 Ω at the signal source to slow fast digital edges and route FPWM signals away from sensitive analog signals when they are used for fan control or margining function. Consult *Design Voltage Margining Circuit for UCD90xxx Power Sequencer and System Manager* (SLVA845) for margining circuit design and *UCD90xxx Voltage Margining Circuit Design Tool* (SLVC676).

3.5 Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (September 2018) to C Revision **Page**

- Updated *Section 2.2* 2
- Updated *Section 3* 2

Changes from A Revision (June 2018) to B Revision **Page**

- Added reference to UCD90320U device in Section 2.1 1
- Added reference to UCD90320U device in Table 1 2
- Added reference to UCD90320U device in Section 3.2 2
- Added reference to UCD90320U device in Table 2 3

Changes from Original (June 2017) to A Revision **Page**

- Changed "K1 ties to V33D" to "K12 ties to V33D" in *Section 2.1* 1
- Added bullet item: 0.1- μF, X7R ceramic at pin 7 (V33DIO1 if applicable) in the *Section 2.2* 2
- Added bullet item: *Ground unused MONx/AMONx pins to save power consumption and decrease EMI. to Section 3.1* .. 2

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