TPD4E02B04EVM User's Guide

This user's guide describes the characteristics, operation, and use of the TPD4E02B04EVM evaluation module (EVM). This EVM includes 5 TPD4E02B04DQA's in various configurations for testing. Two TPD4E02B04DQA's are configured for IEC61000-4-2 compliance testing, with one those being setup to allow the capture of a clamping waveform during an ESD event. One TPD4E02B04DQA is configured for 4-port s-parameter analysis. One TPD4E02B04DQA is configured to pass-through USB 3.1 using one USB 3.1 Type A and one USB 3.1 Type B connector. This user's guide includes setup instructions, schematic diagrams, a bill of materials, and a printed-circuit board layout drawing of the EVM.

1 Introduction

Texas Instrument's TPD4E02B04DQA evaluation module helps designers evaluate the operation and performance of the TPD4E02B04DQA device. The TPD4E02B04DQA is a quad-channel ESD protection device in a small DQA package which offers IEC61000-4-2 Level 4 compliant ESD protection. The 0.2-pF line capacitance is suitable for high speed applications. The TPD4E02B04DQA is characterized for operation over an ambient air temperature range of –40°C to 125°C.

The EVM contains five TPD4E02B04DQA's. One TPD4E02B04DQA (U1) is configured with two end-launch SMA connectors (J9 & J10) for capturing Eye Diagrams through an HDMI Type A port (J11). The D2 data lines are connected to two of the TPD4E02B04DQA's IO protection pins. Another TPD4E02B04DQA (U2) is configured with 4 end-launch SMA (J1 – J4) connectors to use for 4-port analysis with a vector network analyzer. Two TPD4E02B04DQA's (U3 & U4) are configured with test points for striking ESD to the protection pins, U3 also has an SMB (J7) connector for capturing a clamping waveform with an oscilloscope during an ESD test. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope. A proper procedure is outlined below in the Section 3.4 section. One TPD4E02B04DQA (U5) is configured to protect the Super-Speed lines between a USB 3.1 Type A (J5) and a USB 3.1 Type B (J6) connector.

Table 1. EVM Configuration

Reference Designator	TI Part Number	Configuration
U1	TPD4E02B04DQA	HDMI 2.0 Eye Diagram
U2	TPD4E02B04DQA	S-parameters
U3 – U4	TPD4E02B04DQA	IEC61000-4-2 ESD Tests
U3	TPD4E02B04DQA	ESD Clamping waveforms
U5	TPD4E02B04DQA	USB 3.1 Eye Diagram

2 Definitions

Contact Discharge — a method of testing in which the electrode of the ESD simulator is held in contact with the device-under-test (DUT).

Air Discharge — a method of testing in which the charged electrode of the ESD simulator approaches the DUT, and a spark to the DUT actuates the discharge.

ESD simulator — a device that outputs IEC61000-4-2 compliance ESD waveforms shown in Figure 1 with adjustable ranges shown in Table 2 and Table 3.

IEC61000-4-2 has 4 classes of protection levels. Classes 1 – 4 are shown in Table 2. Stress tests should be incrementally tested to level 4 as shown in Table 3 until the point of failure. If the DUT does not fail at 8 kV, testing can continue in 2 kV increments until failure.

Table 2. IEC61000-4-2 Test Levels

Contact Discharge		Air Discharge	
Class	Test Voltage [± kV]	Class	Test Voltage [± kV]
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 3. Waveform Parameters in Contact Discharge Mode

Stress Level Step	Simulator Voltage [kV]	Ipeak ±15% [A]	Rise Time ±25% [nS]	Current at 30ns ±30% [A]	Current at 60ns ±30% [A]
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

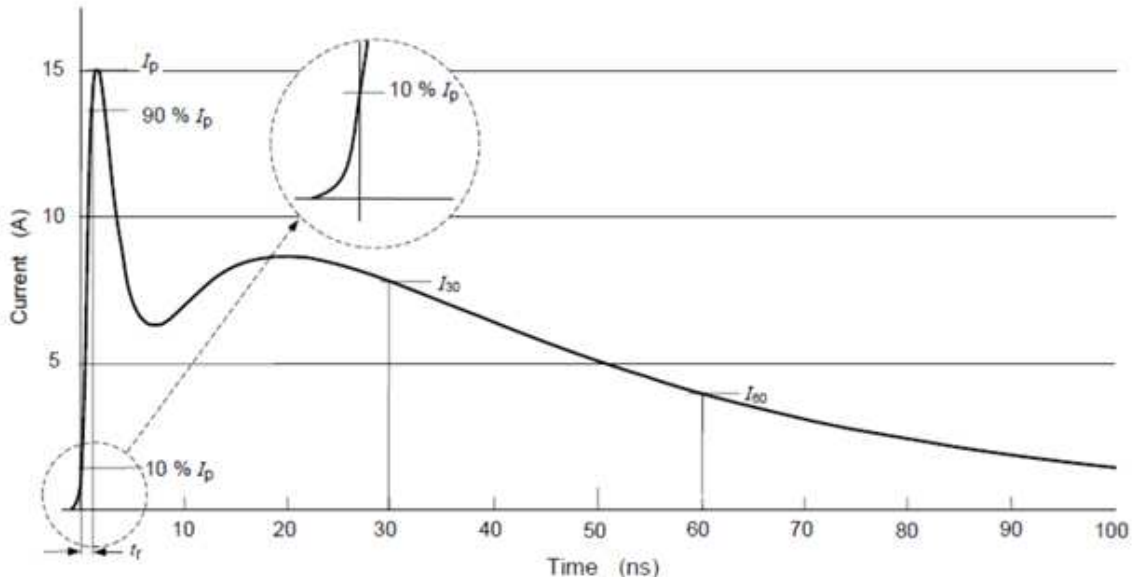

Figure 1. Ideal Contact Discharge Waveform of the Output Current of the ESD Simulator at 4 kV

3 Setup

This section describes the intended use of the EVM. A generalized outline of the procedure given in IEC-61000-4-2 is described here. IEC-61000-4-2 should be referred to for a more specific testing outline. Basic configurations for collecting S-parameters, Eye Diagrams, and ESD clamping waveforms are outlined as well.

3.1 U1 - HDMI

One TPD4E02B04DQA (U1) is configured with two end-launch SMA connectors (J9 & J10) for capturing Eye Diagrams through an HDMI Type A port (J11). The D2 data lines are connected to two of the TPD4E02B04DQA's IO protection pins. Using J9 as D2P and J10 as D2M, attach to an HDMI 2.0 compliant Eye Diagram tester setup for the intended application, using the HDMI Type A port (J11) as either the HDMI source or sink side connector.

3.2 U2 - 4-Port Analysis

TPD4E02B04DQA (U2) is configured with 4 SMA (J1 – J4) connectors to allow 4-port analysis with a vector network analyzer. Connect Port 1 to J1, Port 2 to J2, Port 3 to J3, and Port 4 to J4. This configuration allows for the following terminology in 4 port analysis:

- S_{11}: Return loss
- S_{21}: Insertion loss
- S_{31}: Near end cross talk
- S_{41}: Far end cross talk

3.3 U3 & U4 - ESD Tests

TPD4E02B04DQA (U3 & U4) can be used for destructive electrostatic discharge (ESD) pass/fail ESD strikes. Specifically, they can be used for both IEC-61000-4-2 air and contact discharge tests. The following procedure ensures proper testing setup and method for both discharge tests. Each IO has a Test Pad (TP1 – TP8) directly connected to it.

3.3.1 Test Method and Set-Up

An example test setup is shown in Figure 2. Details of the testing table and ground planes can be found in the IEC 61000-4-2 test procedure. Ground the EVM using the banana connector labeled GND (J8). Discharge the ESD simulator on any of the Test Points TP1 – TP8. Contact and air-gap discharge are tested using the same simulator with the same discharge waveform. While the simulator is in direct contact with the test point during contact, it is not during air-gap.

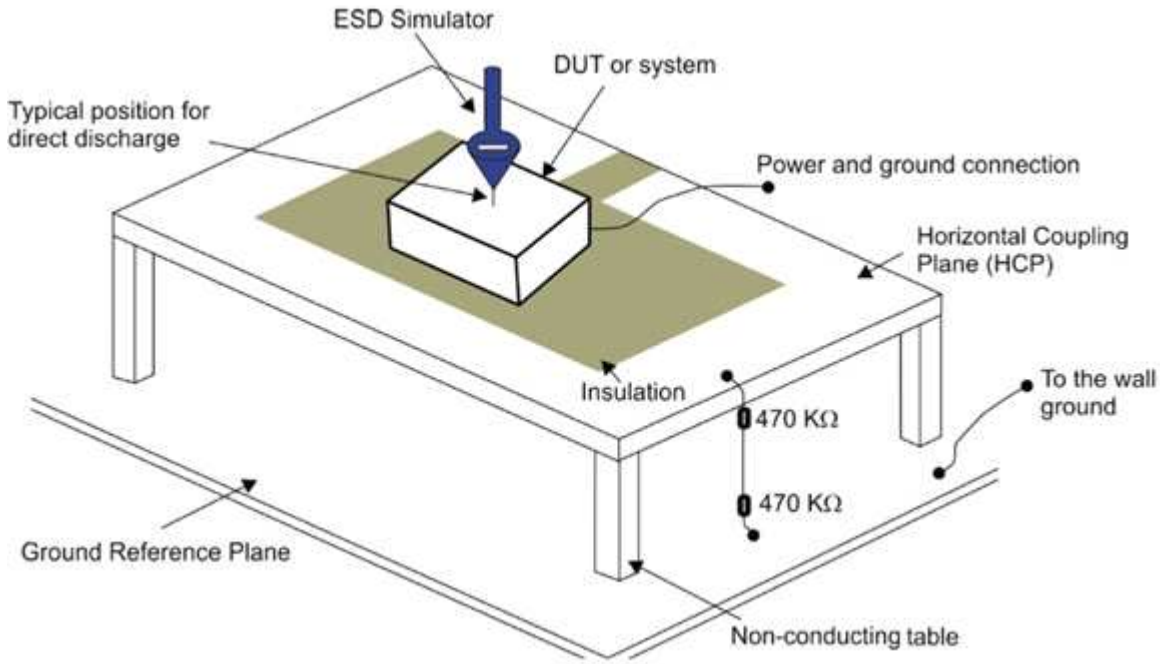

Figure 2. System Level ESD Test Setup

3.3.2 Evaluation of Test Results

Connect the tested device on the EVM to a curve tracer both before and after ESD testing. After each incremental level, if the IV curve of the ESD protection diode shifts ±0.1 V, or leakage current increases by a factor of ten, then the device is permanently damaged by ESD.

3.4 U3 - ESD Clamping Waveform

One TPD4E02B04DQA (U3) also has an SMB (J7) connector for capturing clamping waveforms with an oscilloscope during an ESD strike. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope.

3.4.1 Oscilloscope setup

Without a proper procedure, capturing ESD clamping waveforms exposes the oscilloscope to potential voltages higher than the rating of the equipment. Proper methodology can mitigate any risk in this operation.

Recommended equipment:

- Minimum of 1GHz bandwidth oscilloscope.
- Either of the following:
  - 2 10X 50Ω attenuators and one 0 Ω resistors (the resistor needs to be installed by the end user at R1).
  - 1 10X 50Ω attenuator and one 150 Ω resistor (the resistor is already factory installed at R1).
- 50 Ω shielded SMB cable.

Procedure

In order to protect the oscilloscope, attenuation of the measured signal is required. Here are two possible procedures for testing U3:

1. Using two 10X attenuators:
   - Install a 0 Ω resistor at R1.
   - Attach two 10X attenuators to the oscilloscope channel being used.
   - Attach the 50 Ω shielded SMB cable between J7 and the attenuator.
   - Set the scope attenuation factor to 100X.
   - Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The magnitude should be set to 20 V.
   - Following Section 3.3.1, strike contact ESD to TP1.
2. Using one 10X attenuator:
   - Attach one 10X attenuator to the oscilloscope.
   - Attach the 50 Ω shielded SMB cable between J7 and the attenuator.
   - Set the scope attenuation factor to 40X.
   - Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The magnitude should be set to 20 V.
   - Following Section 3.3.1, strike contact ESD to TP1.

Recommended settings for the time axis is 20 ns/div and for the voltage axis is 10 V division.

The voltage levels of the ESD applied to TP1 should not exceed +/– 8 kV when capturing clamping waveforms.

4 Board Layout

This section provides the TPD4E02B04EVM board layout. TPD4E02B04EVM is a 4-layer board of FR-408HR at 0.062” thickness. Layers 2, 3, and 4 are simple ground planes and not shown here.

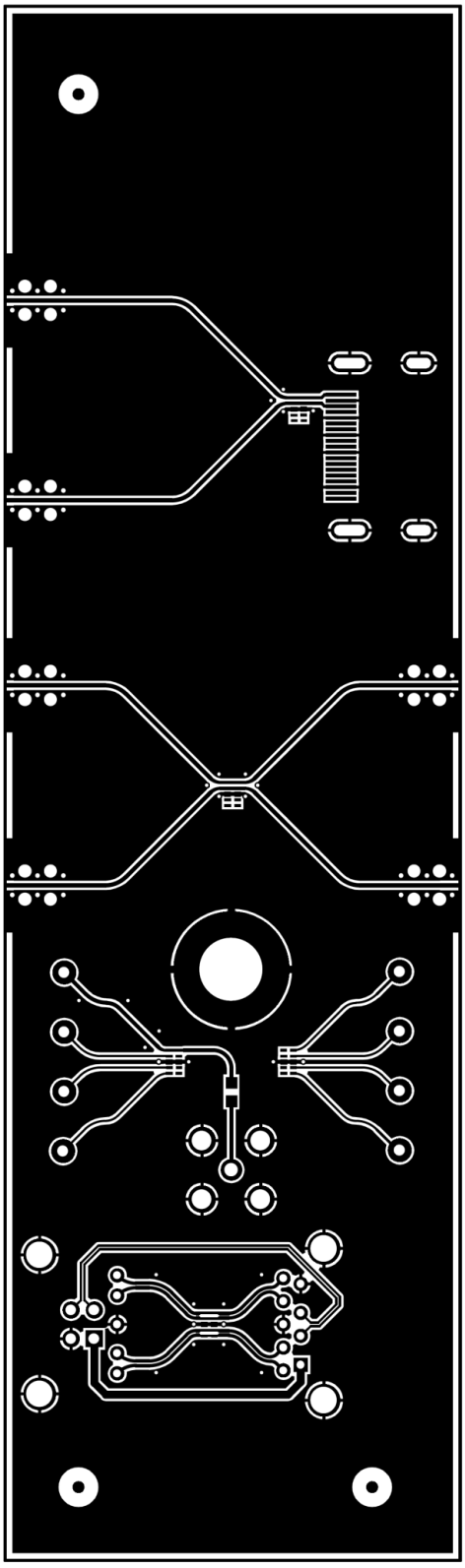

Figure 3. TPD4E02B04EVM Top Layer

5 Schematics and Bill of Materials

5.1 Schematics

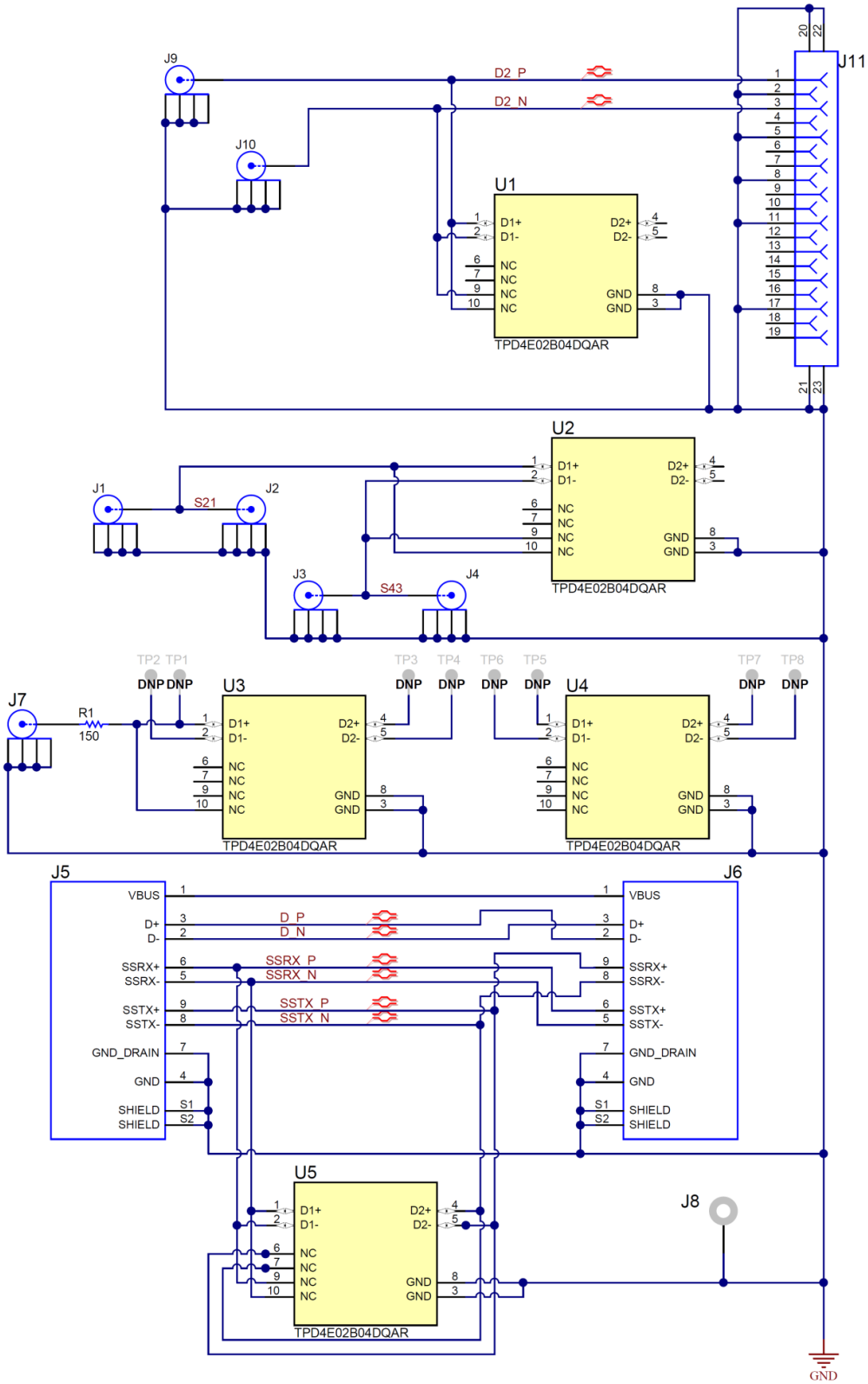

Figure 4. TPD4E02B04EVM Schematic

Table 4. Bill of Materials

Count	RefDes	Description	Size	Part Number	MFR
5	U1-U5	IC, 4-channel ESD solution	0.098 x 0.039 inch	TPD4E02B04	TI
4	J1-4, J9, J10	Connector, TH, End launch SMA 50 ohm	0.25 X 0.375 inch	142-0761-881	Johnson
1	J5	Connector, USB 3.1,TYPE A Female	0.650 X 0.492 inch	GSB4111312HR	Amphenol
1	J6	Conn SMB Jack Str 50 Ohm Pcb	0.722 X 0.496 inch	GSB4211311WEU	Amphenol
1	J9	Standard Banana Jack, Uninsulated, 5.5mm	0.312” diameter	575-4	Keystone
1	J11	Connector, HDMI, 19-Pos Recept, SMT	0.591 X 0.455 inch	1747981-1	TE Connectivity
1	R1	RES, 150 ohm, 1%, 0.1W, 0603	0603	STD	STD

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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