# TPS61046EVM-682 Evaluation Module

This user's guide describes the schematic, layout, and operation of the TPS61046EVM-682 evaluation module.

There are two TPS61046 power circuits in the EVM. U1 is for the adjustable output voltage version, where the FB pin is connected to the feedback network, so the VOUT can be set from 5 V to 28 V; U2 is for the fixed 12-V VOUT version as the FB pin is connected to the VIN pin directly. A 1.6 mm × 0.8 mm inductor is used in this circuit, limiting the input current no higher than 100 mA.

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# 1 Introduction

This section contains the electrical performance and components selection of TPS61046EVM-682.

## 1.1 Performance Specification

Table 1 provides a summary of the TPS61046EVM-682 performance specifications. All specifications are given at an ambient temperature of 25°C.

**Table 1. Performance Specification Summary**

| Specification | Test Condition | MIN | Typ | MAX | Unit |
|---|---|---|---|---|---|
| Input Voltage | | 1.8 | | 5.5 | V |
| Output Voltage | $V_{IN}$ = 3.6V, $I_{IN}$ < 600 mA (U1 circuit) | 5 | | 28 | V |
| | $V_{IN}$ = 3.6V, $I_{IN}$ < 100 mA (U2 circuit) | | 12.0 | | |
| Output Current | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V (U1 circuit) | 0 | 100 | | mA |
| | $V_{IN}$ = 3.6V, $V_{OUT}$ = 12 V (U2 circuit) | 0 | 20 | | mA |

## 1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. The external component can be changed according the real application.

### 1.2.1 Input Capacitor and Output Capacitor

A 150-µF tantalum capacitor is added as the input capacitor in the EVM. The ESR of the tantalum capacitor is 0.1 Ω which helps to damp the ringing in the input voltage when the EVM is powered by a power supply with long cable. The capacitor is not required for proper operation and can be removed in a real application.

C5, C6, C7, and C8 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response.

### 1.2.2 Feedforward Resistor and Capacitor

Feedforward capacitor C3 is used to speed up the device's respond when the output capacitor is much larger than the value in the EVM. When C3 is selected, a resistor with a value not lower than 100 Ω must be used to avoid switching noise coupling into the FB pin. This resistor, R2, also helps to stabilize the system because the frequency of the pole introduced by this feedforward capacitor decreases.

# 2 Input/output Connector Descriptions

This section describes how to properly use the TPS61046EVM-682.

## 2.1 Connection and Jumper for U1

| | |
|---|---|
| **J1 – VIN** | Positive input connection from the input supply for the EVM |
| **J2 – S+/S–** | Input voltage sense connections. Measure the input voltage at this point. |
| **J3 – GND** | Return connection from the input supply for the EVM |
| **J4 – GND** | GND |
| **J5 – VOUT** | Positive output connection |
| **J6 – S+/S–** | Output voltage sense connections |
| **J7 – GND** | GND for the output |
| **JP-1** | Enable/disable the device U1 |

## 2.2 Connection and Jumper for U2

| | |
|---|---|
| **J8 – VIN** | Positive input connection from the input supply for the EVM |
| **J9 – S+/S–** | Input voltage sense connections. Measure the input voltage at this point. |
| **J10 – GND** | Return connection from the input supply for the EVM |
| **J11 – VOUT** | Positive output connection |
| **J12 – S+/S–** | Output voltage sense connections |
| **J13 – GND** | GND for the output |
| **JP-2** | Enable/disable the device U2 |

# 3 Test Results

Refer to the datasheet (SLVSCQ7), *Application Performance Curves* section for the test result of the U1 circuit. The following measurements in this section are done on the U2 circuit.

## 3.1 Startup Waveform

The startup waveform is shown in Figure 1. The test condition: $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $R_{LOAD}$ = 1 kΩ, $T_a$ = 25°C. (CH2 $V_{OUT}$, CH3 EN)

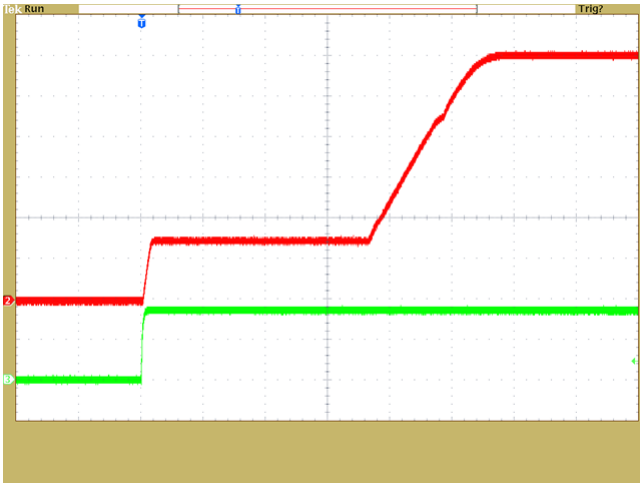


**Figure 1. Startup at $R_{LOAD}$ = 1 kΩ**

## 3.2 Output Ripple

The output ripple waveforms at different loads are shown Figure 2 and Figure 3, respectively. The test condition: $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 1 mA, 20 mA, $T_a$ = 25°C. (CH2 $V_{OUT}$, CH3 SW)

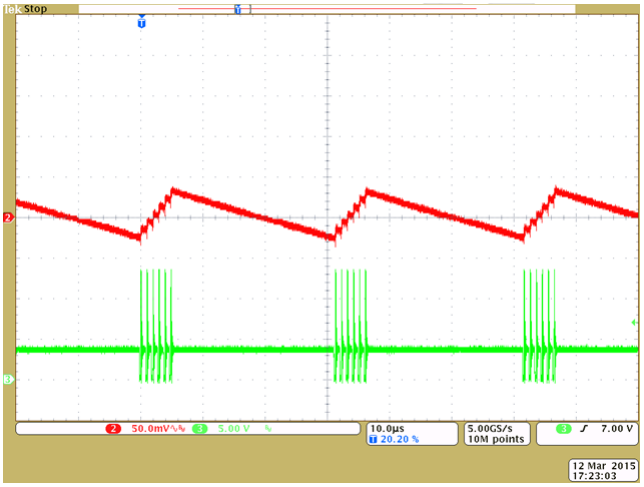


**Figure 2. Output Ripple at $I_{OUT}$ = 1 mA**

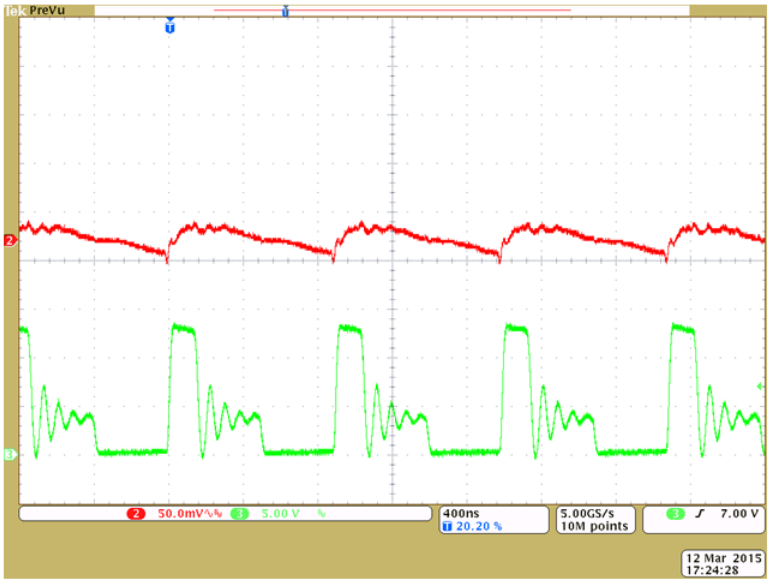


**Figure 3. Output Ripple at $I_{OUT}$ = 20 mA**

### 3.3 Load Transient

The load transient waveform is shown in Figure 4. The test condition: $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 5 mA–15 mA, $T_a$ = 25°C. (CH2 $V_{OUT}$(AC), CH4 $I_{LOAD}$). Please note that the effective output capacitance is only about 0.47 µF because of the ceramic capacitor characteristics, although a 2.2 µF is used in the EVM. Larger effective capacitance will help to improve the load transient performance.

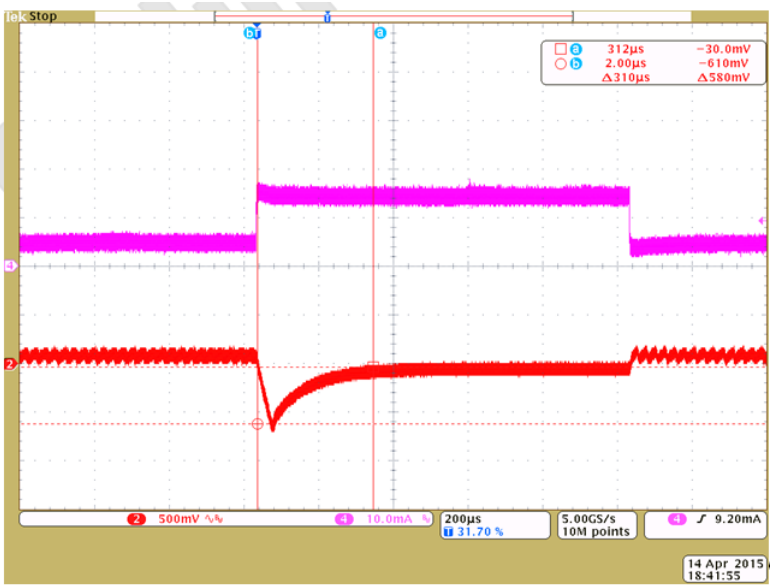


**Figure 4. Load Transient with $I_{OUT}$ from 5 mA to 15 mA**

# 4 Schematic and Bill of Materials

This section provides the TPS61046EVM-682 schematics and the bill of materials

## 4.1 Schematic

The schematics for U1, U2 circuit are shown in Figure 5 and Figure 6, respectively.

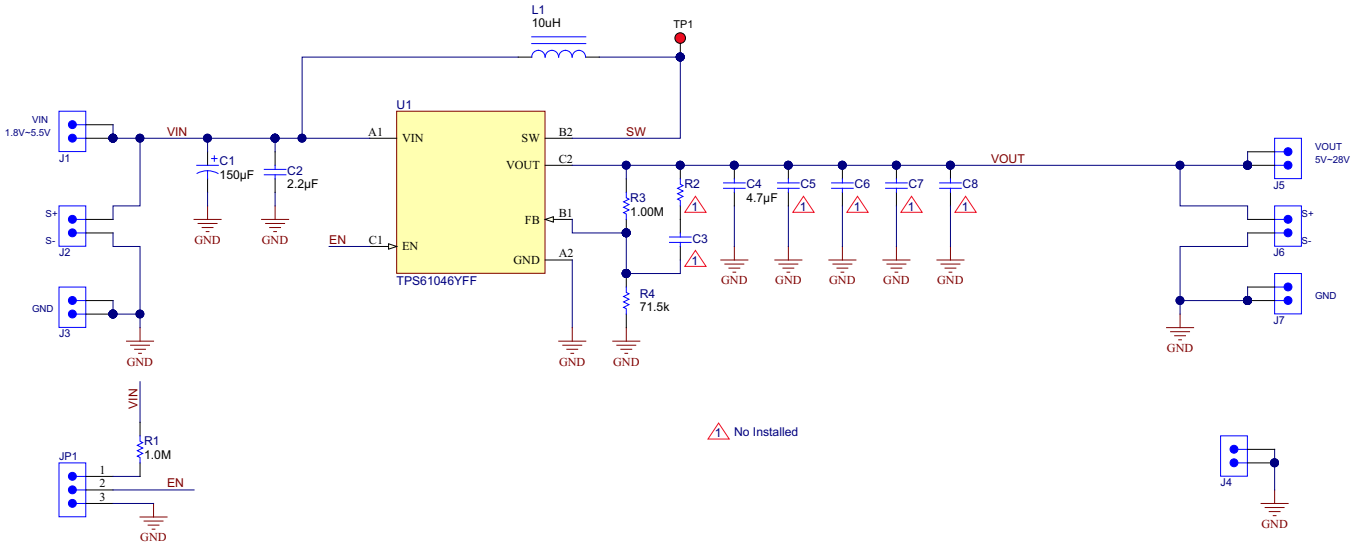


**Figure 5. TPS61046EVM-682 Schematic – U1 Circuit Configuration**

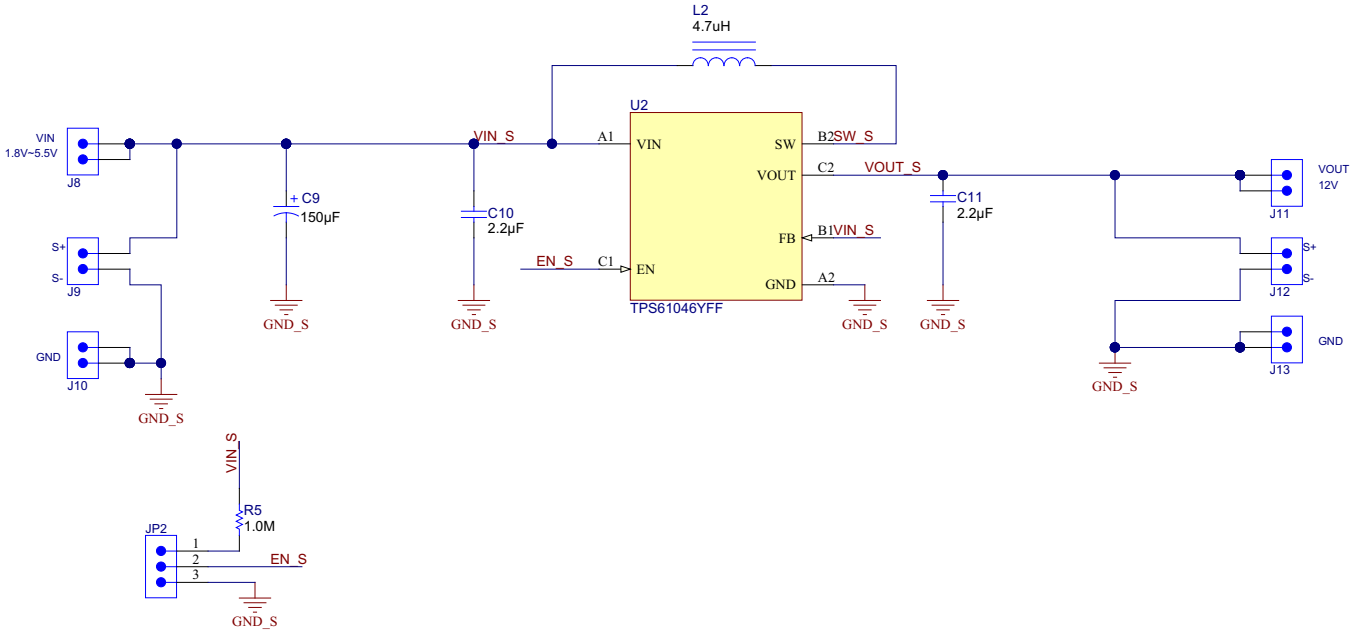


**Figure 6. TPS61046EVM-682 Schematic – U2 Circuit Configuration**

## 4.2 Bill of Materials

Table 2 provides the bill of the materials of the EVM board.

**Table 2. TPS61046 Bill of Materials**

| Designator | QTY | Value | Description | Package | Part Number | MFG |
|---|---|---|---|---|---|---|
| C1, C9 | 2 | 150uF | CAP, TA, 150uF, 10V, +/-10%, 0.1 ohm, SMD | 7343-31 | T495D157K010ATE100 | Kemet |
| C2 | 1 | 2.2uF | CAP, CERM, 2.2 µF, 10 V, +/- 10%, X5R, 0603 | 0603 | GRM188R61A225KE34D | Murata |
| C4 | 1 | 4.7uF | CAP, CERM, 4.7 µF, 35 V, +/- 10%, X5R, 0603 | 0603 | GRM188R6YA475KE15D | Murata |
| C10, C11 | 2 | 2.2uF | CAP, CERM, 2.2 µF, 25 V, +/- 10%, X5R, 0402 | 0402 | GRM155R61E225KE11D | Murata |
| L1 | 1 | 10uH | Inductor, Shielded, Powdered Iron, 10 µH, 2 A, 0.2 ohm, SMD | 4.2x4.2mm | FDSD0420-H-100M | Toko |
| L2 | 1 | 4.7uH | Inductor, Wirewound, Metal Composite, 4.7 µH, 0.37 A, 0.73 ohm, SMD | 0603 | MBKK1608T4R7M | Taiyo Yuden |
| R1, R5 | 2 | 1.0Meg | RES, 1.0 M, 5%, 0.1 W, 0603 | 0603 | CRCW06031M00JNEA | Vishay-Dale |
| R3 | 1 | 1.00Meg | RES, 1.00 M, 1%, 0.1 W, 0603 | 0603 | RC0603FR-071ML | Yageo America |
| R4 | 1 | 71.5k | RES, 71.5 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0771K5L | Yageo America |
| U1, U2 | 2 | | 28-V Output Voltage Boost Converter, YFF0006AAAA | YFF0006AAAA | TPS61046YFF | Texas Instruments |
| J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13 | 13 | | Header, 100mil, 2x1, Tin plated, TH | Header, 2 PIN, 100mil, Tin | PEC02SAAN | Sullins Connector Solutions |
| JP1, JP2 | 2 | | Header, 100mil, 3x1, Tin plated, TH | Header, 3 PIN, 100mil, Tin | PEC03SAAN | Sullins Connector Solutions |
| TP1 | 1 | Red | Test Point, TH, Multipurpose, Red | Keystone5010 | 5010 | Keystone |
| C3, C5, C6, C7, C8, R2 | open | | | | | |

## 5 Board Layout

This section provides the TPS61046EVM-682 board layout and illustrations, Figure 7 is the top layer and Figure 8 is the bottom layer.

The output capacitor should be as close to the IC as possible and be connected to VOUT and the GND pin with short, width track. If the bulk capacitor is too large to place close the IC, a small capacitor should be placed close to the IC.

Make sure the track and inductor node connected to the SW pin is far from the FB pin which is sensitive to noise.

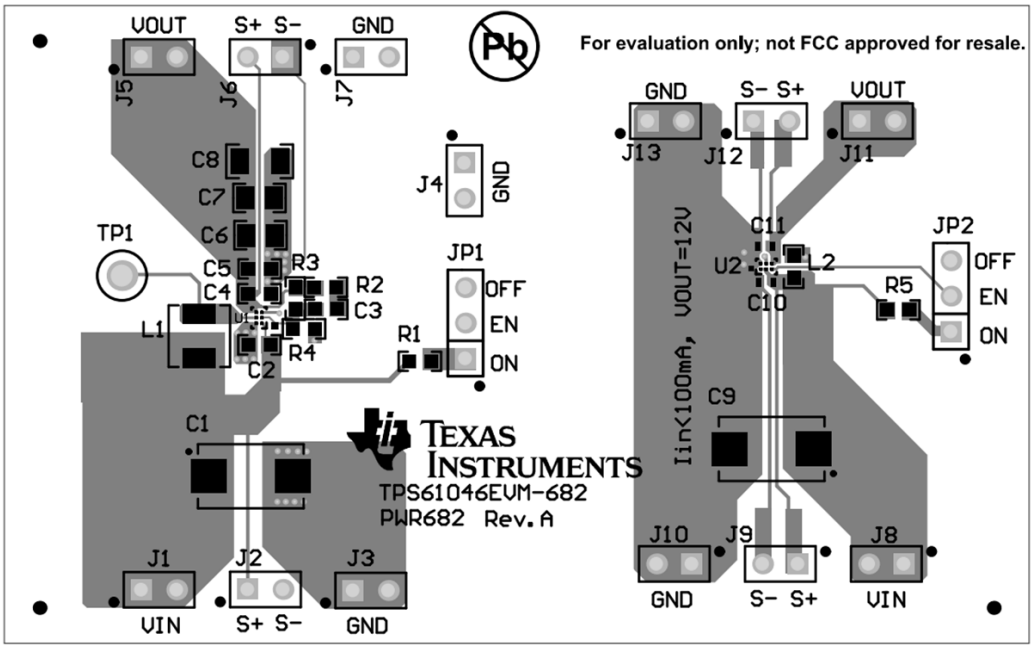


**Figure 7. Silkscreen and Top Layer**

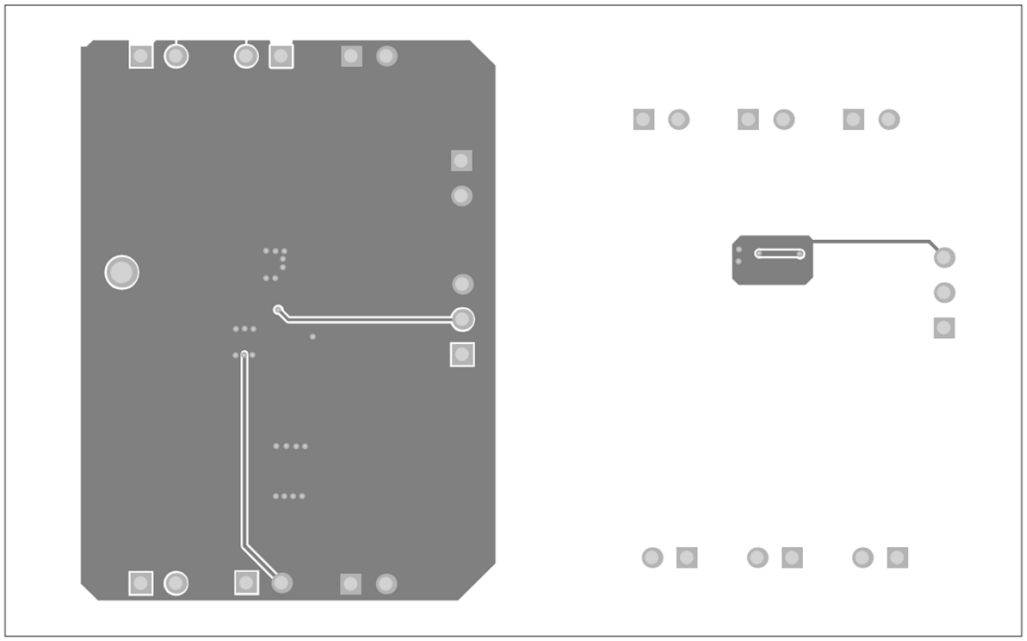

**Figure 8. Bottom Layer**

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