SMV512K32-CVAL SRAM Breakout Evaluation Board

This document outlines the basic steps and functions that are required to ensure proper operation of the SMV512K32-CVAL breakout evaluation board. It works in tandem with a customers' pattern generation and capture hardware to demonstrate the memory function features of the 16-Mbit asynchronous SRAM memory.

Contents

List of Figures

1 Overview

The SMV512K32-SP 16-Mbit asynchronous SRAM is a QML Class-V Radiation-Hardened memory co-developed with Silicon Space Technology corporation. The HARDSIL™ radiation hardening technology is an expansion optimization of the radiation performance window by tweaking the processing technology of the circuit design with the layout of the device. The HARDSIL™ technology provides superior radiation performance with no SWAP (size, weight and power) tradeoffs.

This ultra high performance asynchronous SRAM is functionally com patible with commercial SRAMs and is organized as 512K Words by 32 Bits and has 20ns Read, 13.8ns Write maximum access times. Since it is an Asynchronous Memory, it never needs a clock to refresh the memory and only Reads, Writes, ChipSelect Address, and Data need to be exercised at any given time.

The memory boasts the industries lowest Standby Current (I_{SB}) of 200µA which enables the lowest power consumption for Space-grade SRAMs enabling significant system-level power savings.

Figure 1 shows the SMV512K32-SP block diagram of key elements.

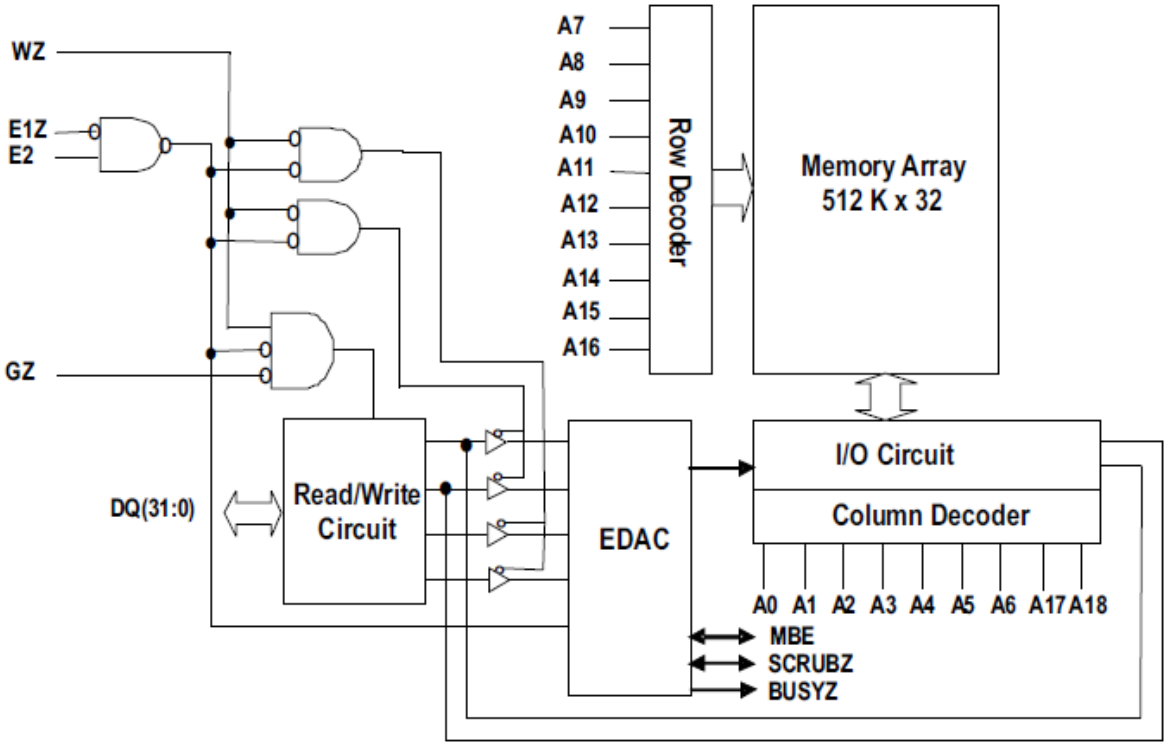

Figure 1. SMV512K32-SP Block Diagram

The device is pin selectable between Master and Slave modes, and Master-mode provides users with built-in a user defined autonomous Error-Detection-And-Control (or EDAC) for detecting a single bit error from a radiation strike in the device. The built-in “Scrub” engine is included for autonomous cleansing of Single-Event-Errors and avoids multiple errors and a permanent uncorrectable “Multiple-Bit-Error”. The combination of the EDAC and Scrub delivers Soft-Error-Rates (SER) < $5e^{-17}$ upsets per bit-day. This is the lowest architecture and power overhead for autonomous Soft-Error mitigation.

The SRAM is Latch up immunity > Linear Energy Transfer (LET) of 110 MeV-cm2/mg which ensures reliable memory data integrity under harshest conditions (T=125°C).

It has a three-state bidirectional data bus and has CMOS compatible Input and Output levels. The Core is powered with a 1.8V ±0.15V CORE and the I/O’s with a 3.3V ±0.3V supply.

The SMV512K32-SP device is offered in a 76-pin Ceramic QFP package, which is shown in Figure 2 below.

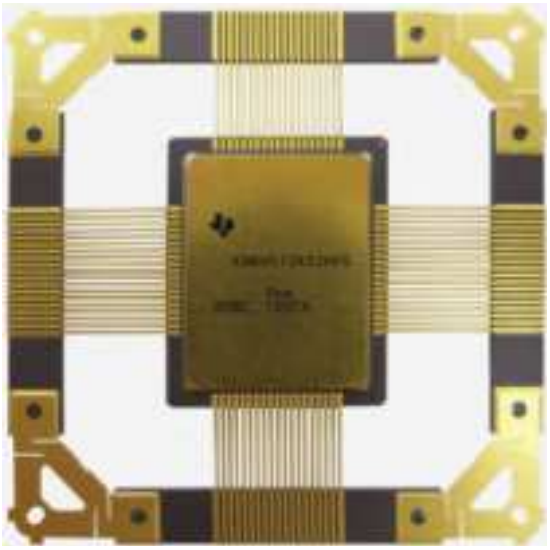

Figure 2. SMV512K32-SP 76-Pin QFP (HFG) Package

2 Hardware Description

The SMV512K32-CVAL breakout-board utilizes a board utilizes an ENPLAS OTQ-132-0.635-01 socket, which is shown in Figure 3 below.

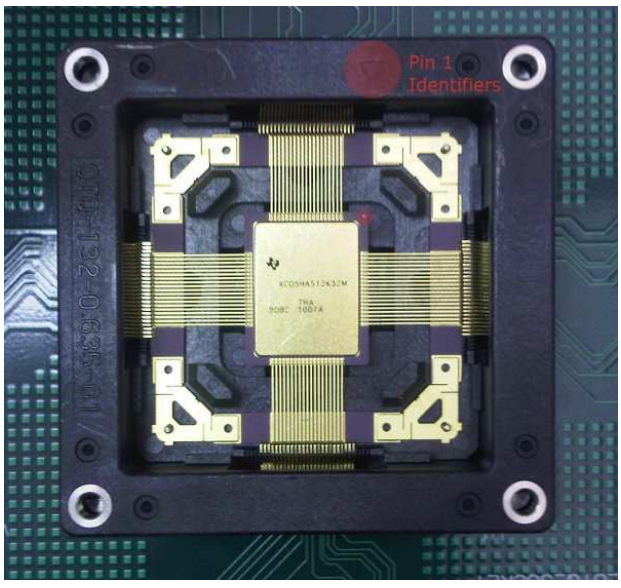

Figure 3. SMV512K32-CVAL ENPLAS Socket

Access to signals is provided in each quadrant with a three row 100mil standard header. This allows connection to static value, or to a signal generator or capture equipment. The traces are routed with matched length.

Please reference the SMV512K32-SP data sheet (SLVSA21) for proper device operation and power supply connections.

3 Device Insertion

For proper SMV512K32-CVAL breakout-board operation, the 76-pin HFG package must be inserted into the socket carefully with the correct orientation. See highlighted red dots in figure 3 for correct orientation. The device has small gold circle embedded into the ceramic in one corner. The socket has an embossed triangle.

To insert the device, place device with correct orientation in the socket. When properly aligned, press down on all four corners of the socket frame to allow cantilever pins to expand and allow device to seat and be captured properly.

4 Schematics

4.1 Element Schematics

The schematic for the SMV512K32-CVAL breakout-board is shown on the following page in Figure 4.

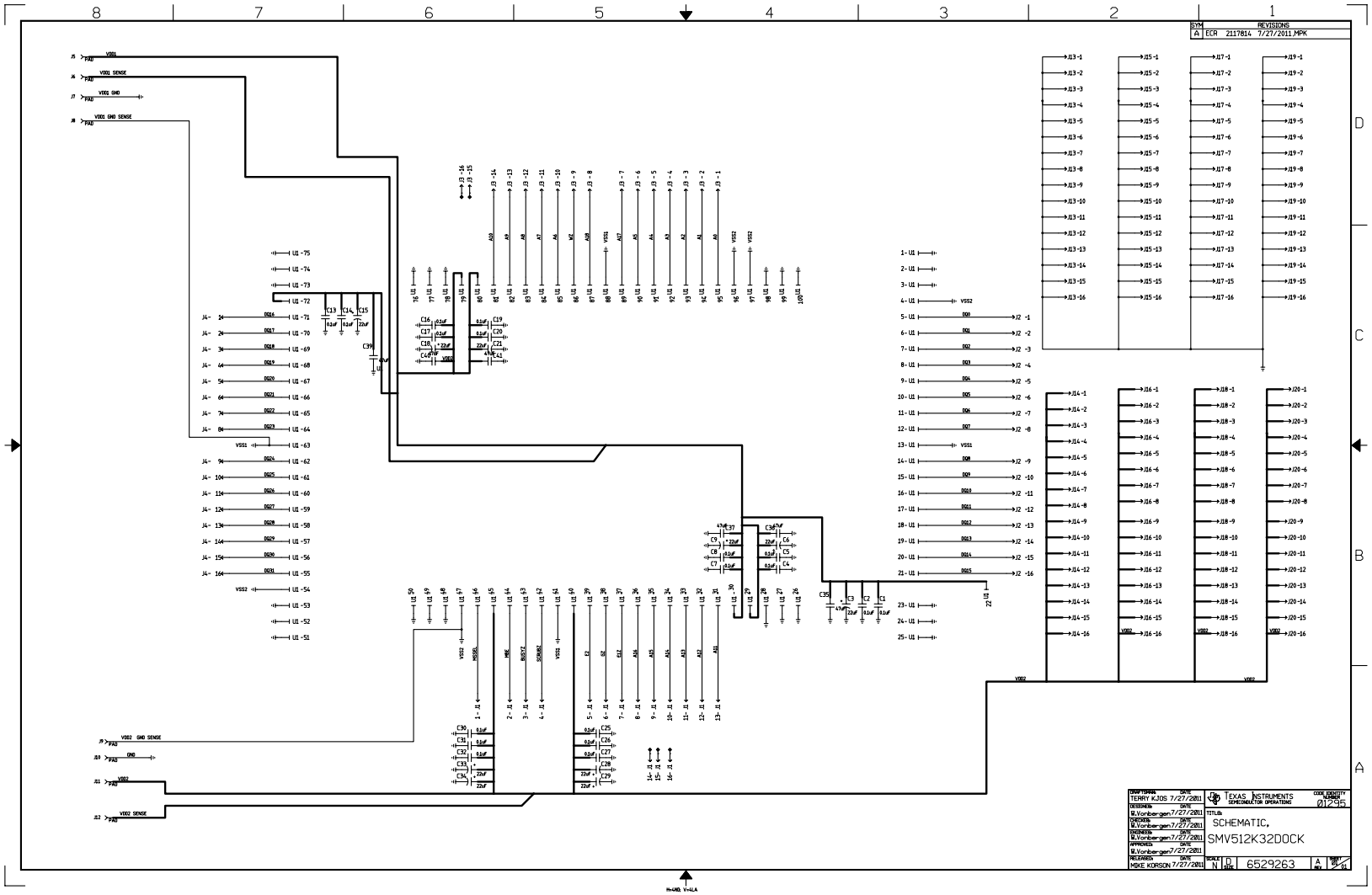

Figure 4. SMV512K32-CVAL Elemental Schematic

4.2 Printed-Circuit-Board Layout Schematics

The layout schematics for the SMV512K32-CVAL breakout-board are shown below for the six-layer PCB in Figure 5 through Figure 10.

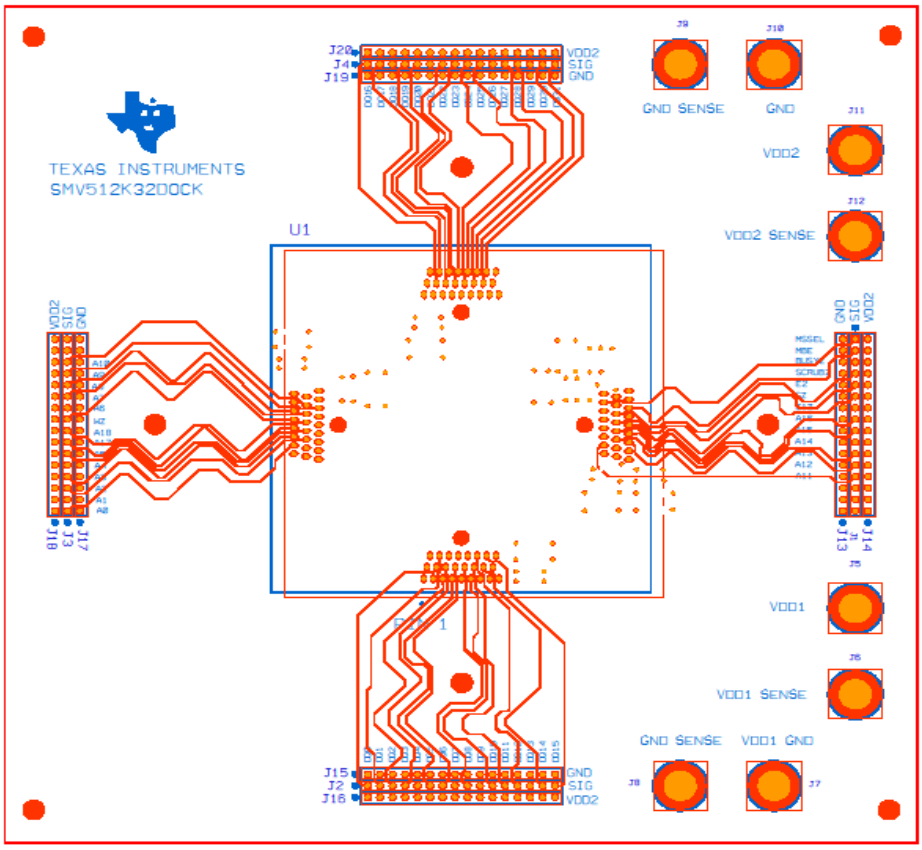

Figure 5. PCB Layout Layer 1

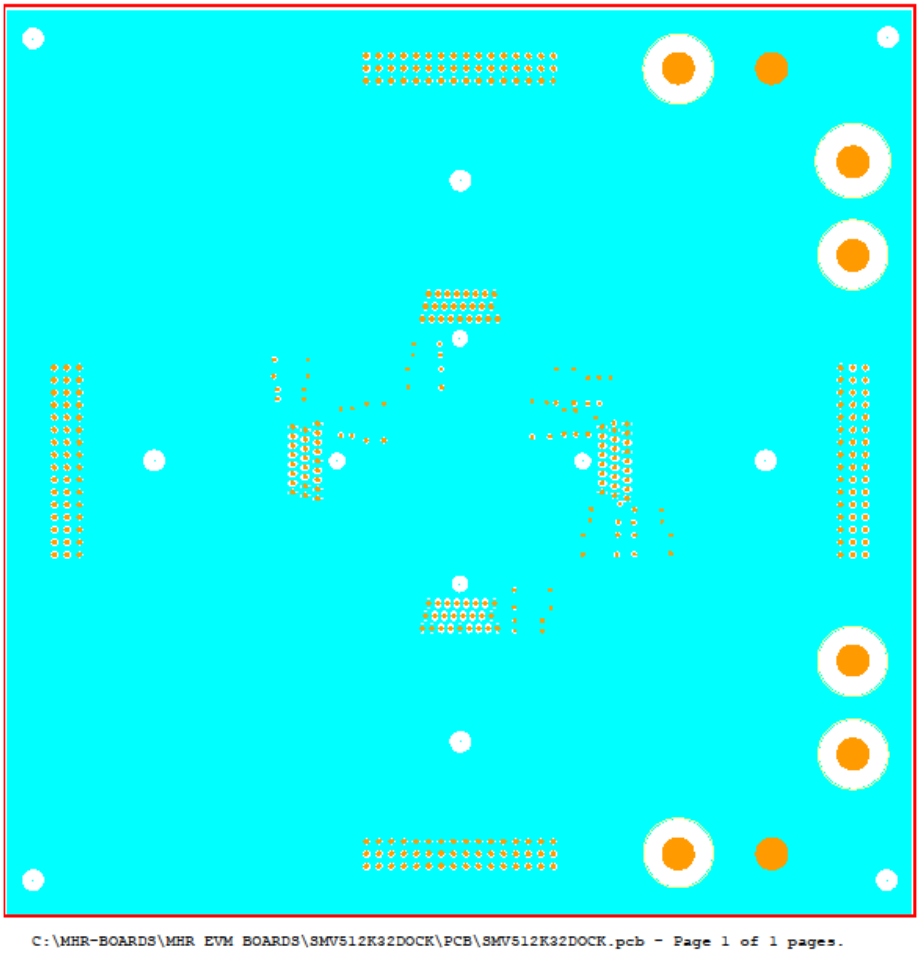

Figure 6. PCB Layout Layer 2

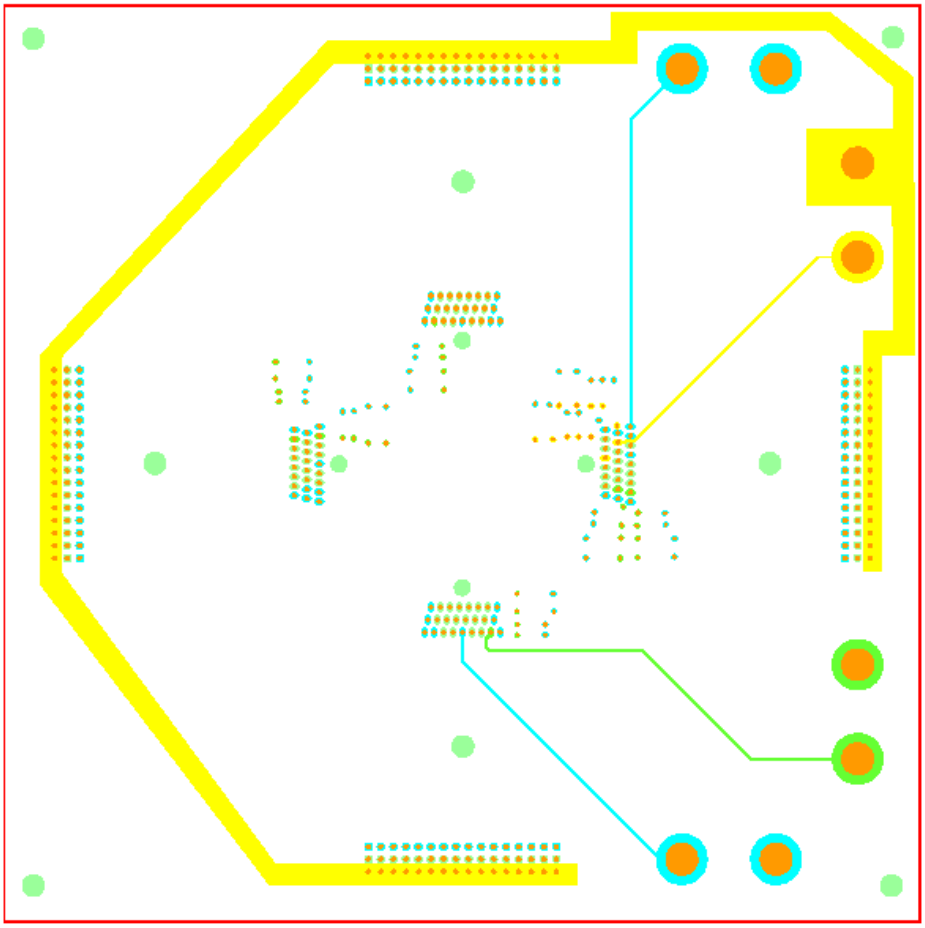

Figure 7. PCB Layout Layer 3

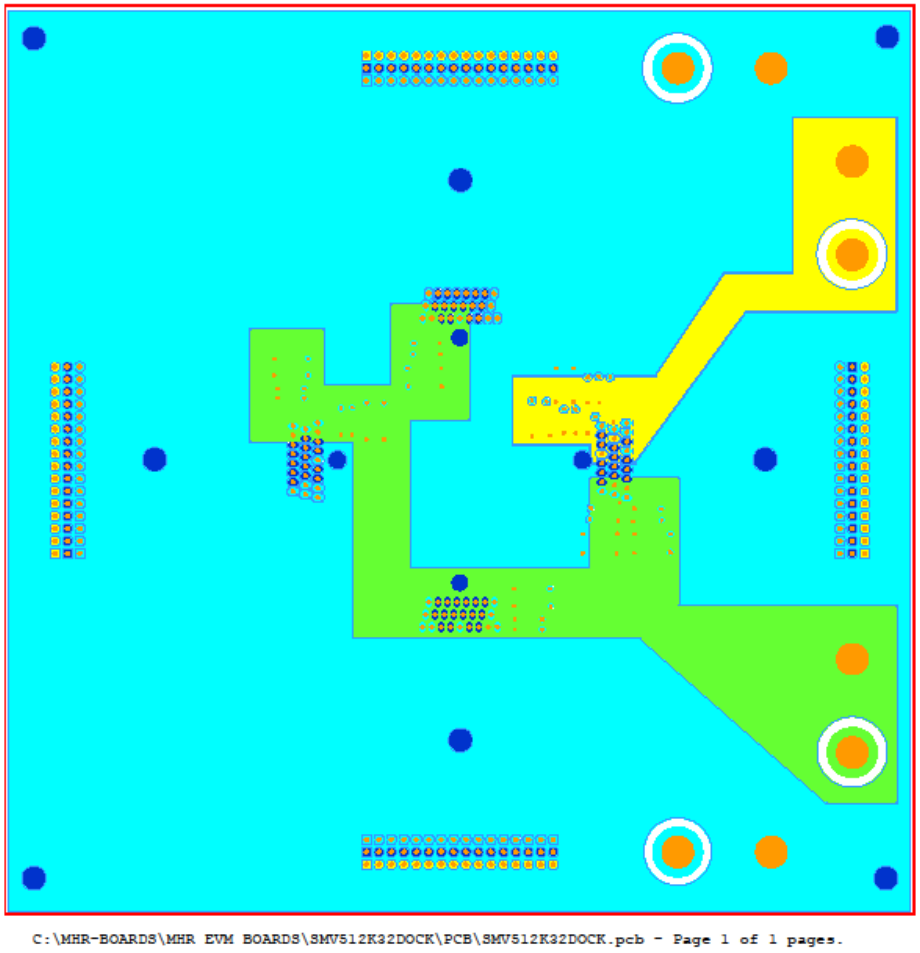

Figure 8. PCB Layout Layer 4

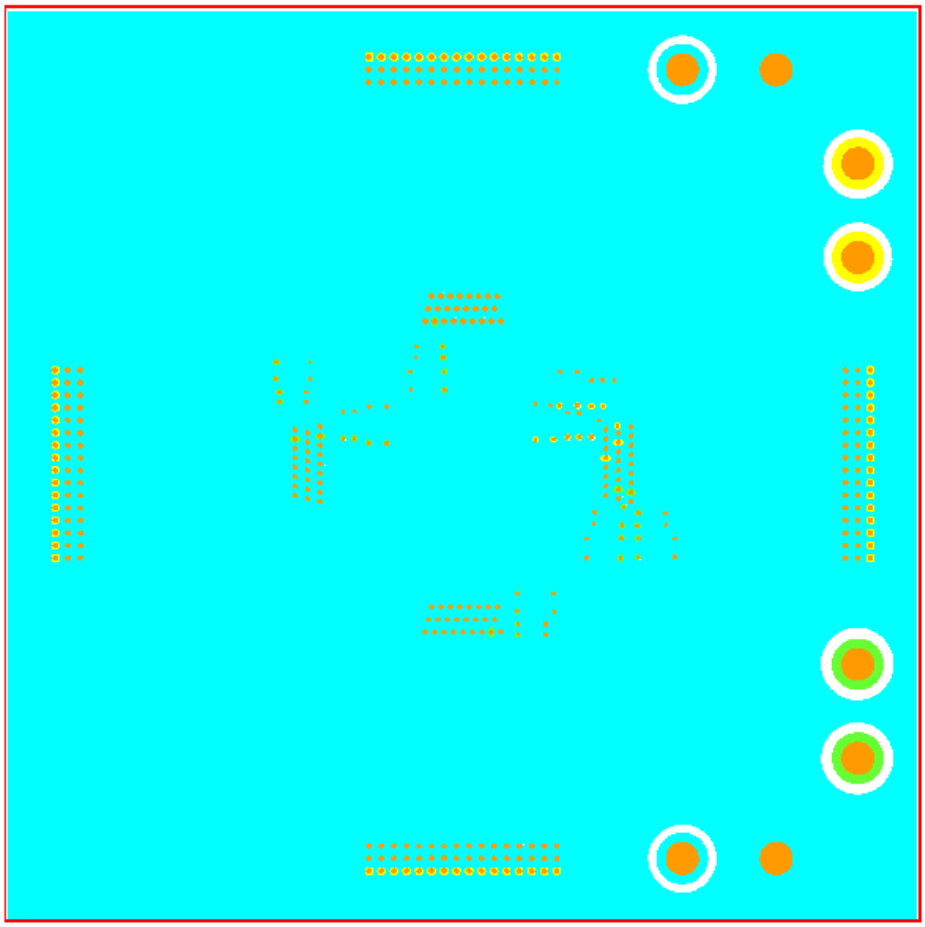

Figure 9. PCB Layout Layer 5

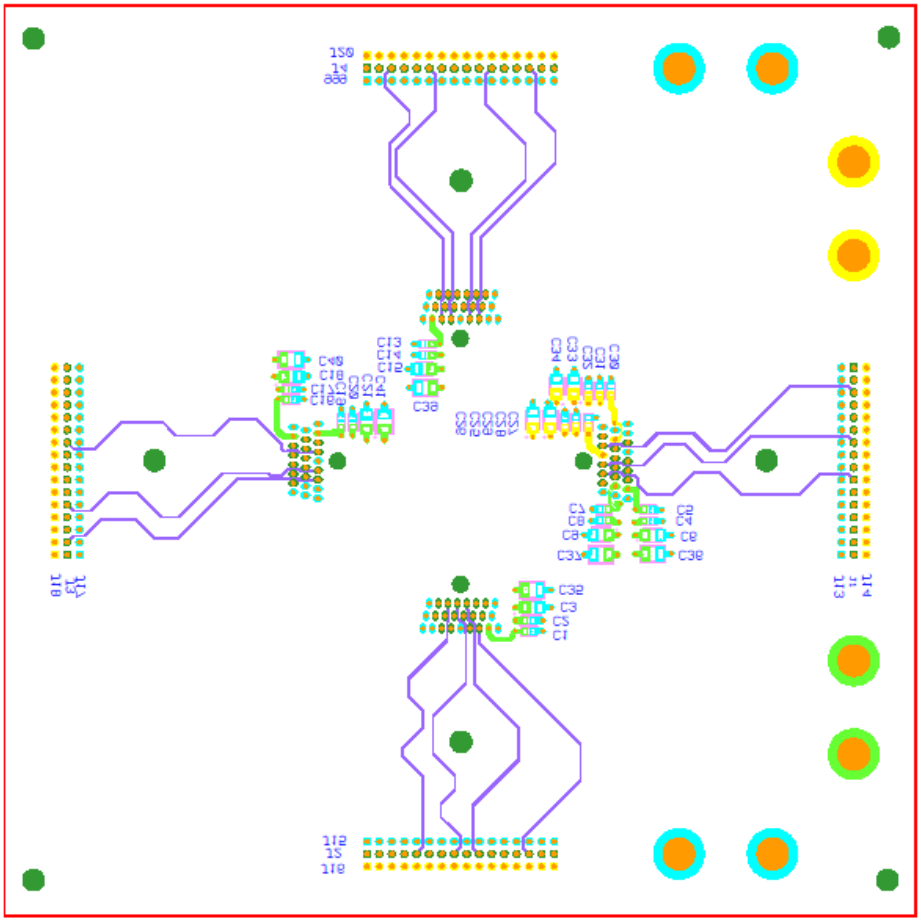

Figure 10. PCB Layout Layer 6

5 EVM Connectors

5.1 Description

The SMV512K3EVM is shown below in Figure 11 below.

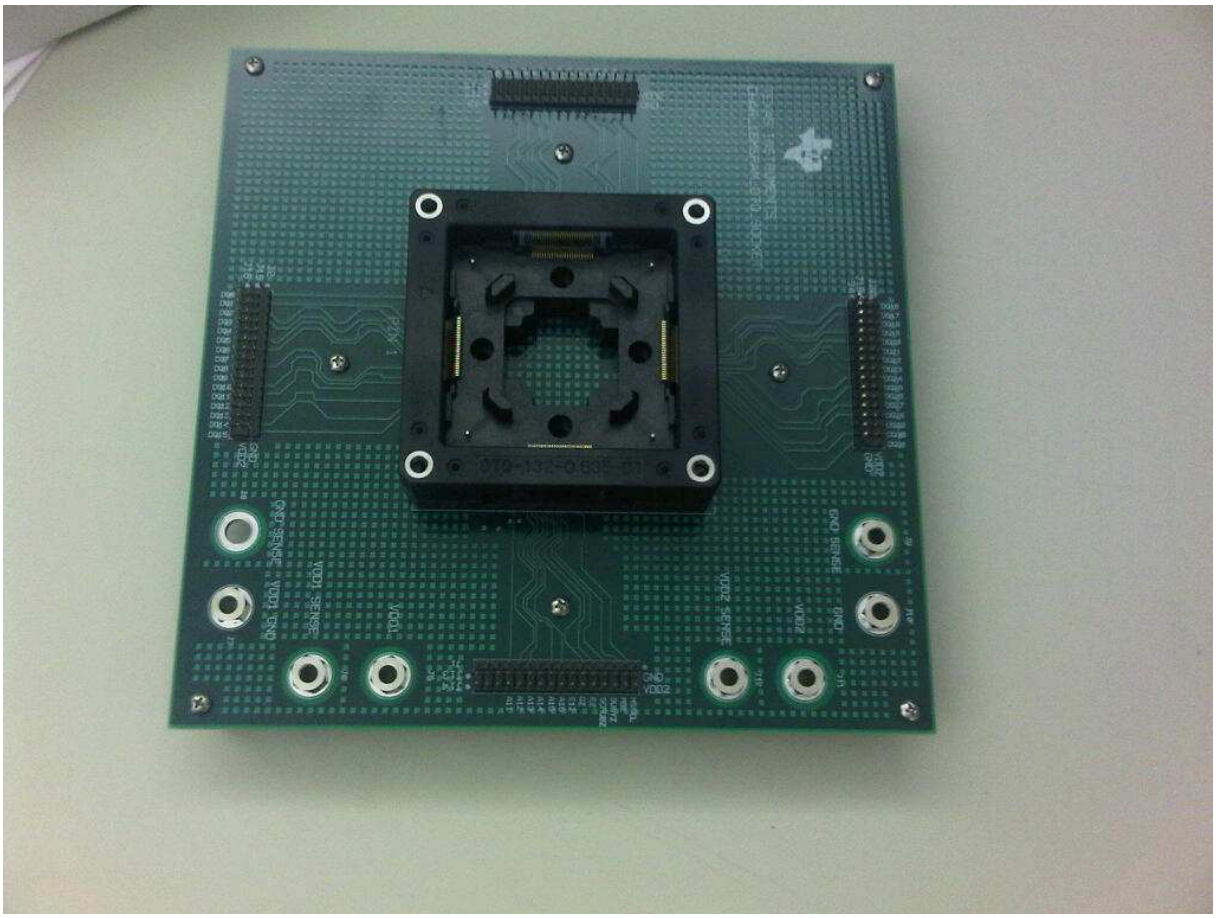

Figure 11. SMV512K32-CVAL

To provide the user with simple access and maximum flexibility, the SMV512K32-CVAL has four sets of 3-row 16-pin input/output connectors. These are labeled J1 through J4 and J13 through J20. They provide all of the Input and Output signals for the device.

There are also eight additional Power and Ground banana jack connectors designated as J5 through J12. The power supply is capable of 800 mA for VDD1, and 300 ma for VDD2. Current clamp levels can be greatly reduced with lower operating frequencies. See device datasheet electrical characteristics IDD1, and IDD2 parameters.

The SMV512K32-CVAL connector descriptions are listed in Table 1 below:

Table 1. SMV512K32-CVAL Connector Descriptions

REFERENCE DESIGNATOR	FUNCTION
J1	Address Inputs 11 through 16, E1Z, GZ, E2, SCRUBZ, BUSYZ, MBE, MSSEL
J2	DQ0 through DQ15 Data I/O's
J3	Address Inputs A0 through A10, A17, A18, WZ
J4	DQ16 through DQ31 Data I/O's
J5	VDD1 1.8V Power Supply
J6	VDD1 SENSE
J7	GND
J8	GND SENSE
J9	GND SENSE
J10	GND
J11	VDD2 3.3V Power Supply
J12	VDD2 SENSE
J13	GND
J14	VDD2
J15	GND
J16	VDD2
J17	GND
J18	VDD2
J19	GND
J20	VDD2

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It is important to operate this EVM within the input voltage range of -0.3 V to 2 V (VDD1), -0.3 V to 3.8 V (VDD2) and the output voltage range of -0.3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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