Test Report: PMP23611

48V_{IN}, 300W Automotive Two-Phase Buck Converter With GaN Half-Bridge Power Stage Reference Design

Description

This reference design offers power for automotive advanced driver assistance systems (ADAS), infotainment, and cluster applications. Operation is over the full automotive range up to 60V. The design exhibits a peak conversion efficiency of 92% to 96% in the $20V_{IN}$ to $60V_{IN}$ range with high power density at 2700mm^2. The results of this report demonstrate information to validate the design in terms of stability, thermal response, efficiency ranging across all input voltages and load requirements. It also shows overshoot and undershoot results of about 5% during a 25%–75% load transient event and a 50%–100% load transient event.

Resources

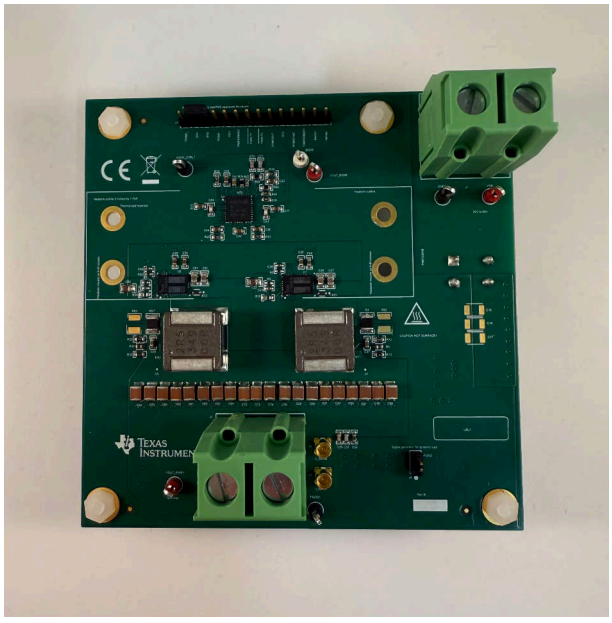
PMP23611	Design Folder
LM5137F-Q1	Product Folder
LMG2100R044	Product Folder

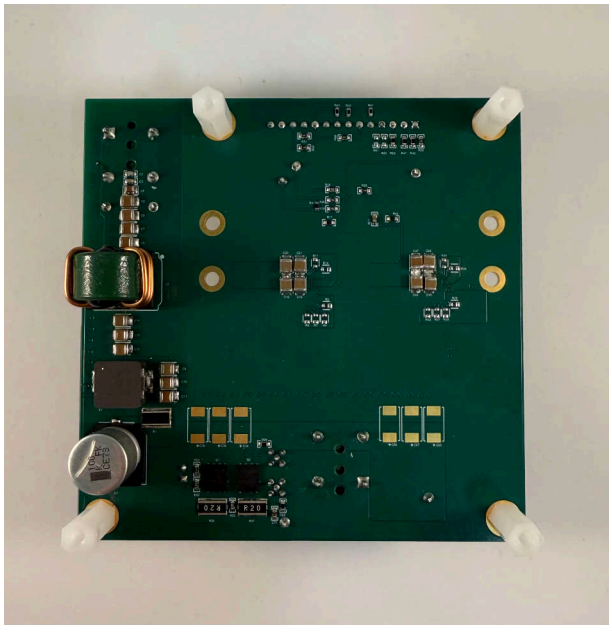
Features

- High current for advanced driver assistance systems (ADAS), infotainment, and cluster applications
- Peak conversion efficiency of 92% to 96% in the $20V_{IN}$ to $60V_{IN}$ range
- LM5137F-Q1 provides Automotive Safety Integrity Level D (ASILD) functional safety qualification
- LMG2100 provides an integrated Gallium Nitride (GaN) half-bridge power stage to allow for increased power density

Applications

- Driver and occupant monitoring ECU with local camera
- ADAS domain controller
- Surround view system ECU
- Radar ECU
- Vehicle instrument cluster
- Digital cockpit processing unit





1 Test Prerequisites

This section provides detailed testing of this reference design.

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	48VDC Nominal (20VDC minimum; 60VDC maximum)
Output Voltage	5VDC
Output Current	50A
Switching Frequency	440kHz

1.2 Required Equipment

- Power supply
- Electronic load
- Digital multimeter
- Oscilloscope

1.3 Considerations

Unless stated otherwise, the tests performed in this test report are taken at the nominal 48V input voltage, configured into FPWM mode, with a fan to aid in temperature control.

1.4 Dimensions

The dimensions of the board are 3.94in × 3.94in (100mm × 100mm). The true design size is 2.05in × 2.05in (52mm × 52mm).

2 Testing and Results

2.1 Efficiency Graphs

The efficiency of the system is demonstrated across an input voltage range of $20V_{in}$ to $60V_{in}$. According to Figure 2-1, when operating at full 50A load, the efficiency is within the range of 90% to 94%. The efficiency graph is derived from the conversion loss versus load current graph (Figure 2-2), which also spans over the same $20V_{in}$ to $60V_{in}$ input range. A peak efficiency can be seen at $20V_{in}$ input voltage under 10A to 20A of load. While at the nominal $48V_{in}$ input voltage, the peak can be seen at 93% between 20A and 30A.

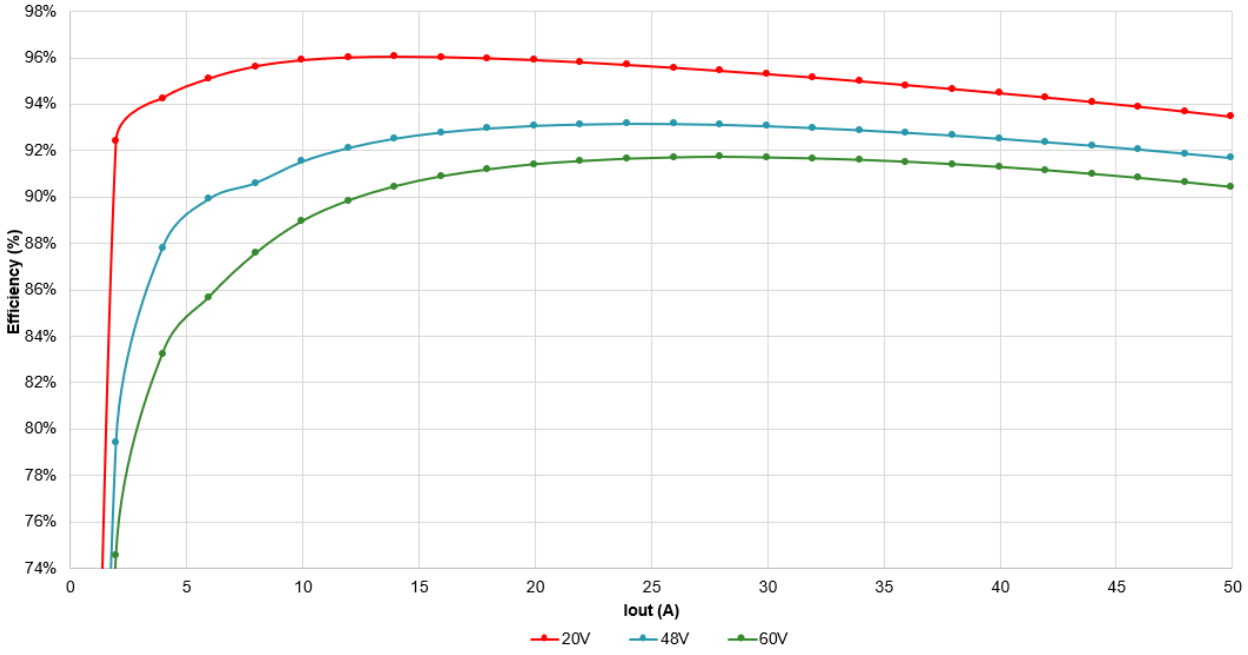


Figure 2-1. $5V_{out}$, System Efficiency Across Load

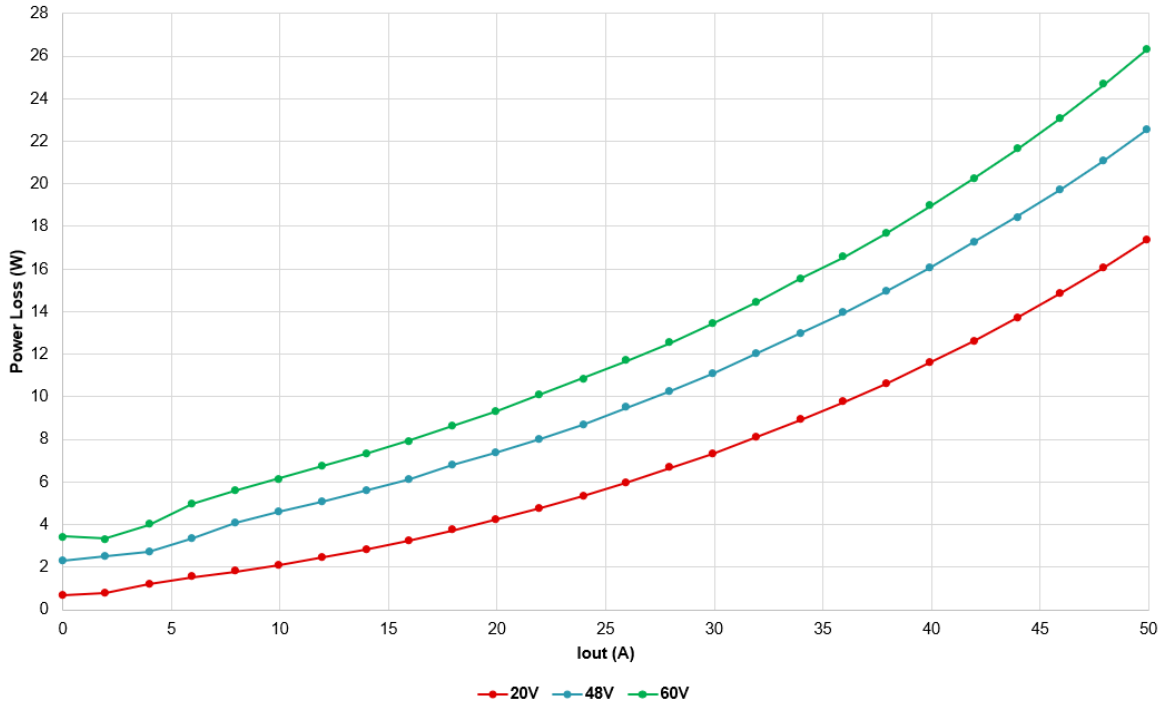


Figure 2-2. $5V_{out}$, Conversion Loss Across Load

2.2 Efficiency Data

This section details the efficiency data at various input voltages and load current demands.

Table 2-1. $20V_{IN}$ Efficiency and Power Loss Across Load

V_{in}	I_{in}	V_{out}	I_{out}	Eff	Ploss (W)
19.99	0.04	4.98	0.02	10.99%	0.67
19.99	0.53	4.98	1.97	92.43%	0.80
19.99	1.05	4.98	3.96	94.26%	1.21
19.99	1.56	4.98	5.96	95.12%	1.53
19.99	2.07	4.98	7.96	95.64%	1.80
19.99	2.59	4.98	9.96	95.91%	2.11
19.99	3.10	4.98	11.96	96.03%	2.46
19.99	3.62	4.98	13.95	96.06%	2.84
19.99	4.14	4.98	15.95	96.04%	3.27
19.99	4.66	4.98	17.95	95.99%	3.74
19.99	5.19	4.98	19.95	95.91%	4.24
19.99	5.71	4.98	21.95	95.82%	4.77
19.99	6.24	4.98	23.95	95.71%	5.37
19.99	6.77	4.98	25.95	95.58%	5.98
19.99	7.30	4.98	27.95	95.45%	6.65
19.99	7.83	4.98	29.95	95.31%	7.34
19.99	8.37	4.98	31.95	95.16%	8.10
19.99	8.91	4.98	33.95	95.00%	8.90
19.99	9.45	4.98	35.95	94.84%	9.75
19.99	9.99	4.98	37.95	94.67%	10.65
19.99	10.54	4.98	39.95	94.49%	11.62
19.99	11.09	4.98	41.95	94.30%	12.62
19.99	11.64	4.98	43.95	94.11%	13.71
19.99	12.19	4.98	45.95	93.91%	14.85
19.99	12.75	4.98	47.95	93.69%	16.09
19.99	13.32	4.98	49.95	93.47%	17.38

Table 2-2. $48V_{IN}$ Efficiency and Power Loss Across Load

V_{in}	I_{in}	V_{out}	I_{out}	Eff	Ploss (W)
47.99	0.05	4.99	0.02	4.15%	2.30
47.99	0.26	4.99	1.97	79.43%	2.52
47.99	0.47	4.99	3.96	87.82%	2.74
47.99	0.69	4.99	5.96	89.93%	3.34
47.99	0.91	4.99	7.96	90.62%	4.09
47.99	1.13	4.99	9.96	91.54%	4.59
47.99	1.35	4.99	11.96	92.13%	5.09
47.99	1.57	4.99	13.95	92.54%	5.59
47.99	1.79	4.98	15.95	92.80%	6.15

Table 2-2. 48V_{IN} Efficiency and Power Loss Across Load (continued)

V_{in}	I_{in}	V_{out}	I_{out}	Eff	Ploss (W)
47.99	2.01	4.98	17.95	92.97%	6.79
47.99	2.23	4.98	19.95	93.09%	7.38
47.99	2.45	4.98	21.95	93.15%	8.02
47.99	2.67	4.98	23.95	93.18%	8.71
47.99	2.89	4.98	25.95	93.17%	9.50
47.99	3.12	4.98	27.95	93.14%	10.24
47.99	3.34	4.98	29.95	93.08%	11.11
47.99	3.57	4.98	31.95	93.00%	12.03
47.99	3.80	4.98	33.95	92.90%	12.96
47.99	4.02	4.98	35.95	92.79%	13.92
47.99	4.25	4.98	37.95	92.67%	14.95
47.99	4.48	4.98	39.95	92.54%	16.07
47.99	4.72	4.98	41.95	92.39%	17.25
47.99	4.95	4.98	43.95	92.23%	18.46
47.99	5.18	4.98	45.95	92.07%	19.72
47.99	5.42	4.98	47.95	91.89%	21.09
47.99	5.66	4.98	49.95	91.70%	22.54

Table 2-3. 60V_{IN} Efficiency and Power Loss Across Load

V_{in}	I_{in}	V_{out}	I_{out}	Eff	Ploss (W)
59.99	0.06	4.99	0.02	2.88%	3.44
59.99	0.22	4.99	1.97	74.58%	3.33
59.99	0.40	4.99	3.96	83.26%	3.99
59.99	0.58	4.99	5.96	85.70%	4.95
59.99	0.76	4.99	7.96	87.58%	5.60
59.99	0.93	4.99	9.96	88.96%	6.15
59.99	1.11	4.99	11.96	89.85%	6.74
59.99	1.28	4.99	13.95	90.47%	7.35
59.99	1.46	4.99	15.95	90.90%	7.93
59.99	1.64	4.99	17.95	91.20%	8.64
59.99	1.81	4.98	19.95	91.43%	9.32
59.99	1.99	4.98	21.95	91.56%	10.09
59.99	2.17	4.98	23.95	91.66%	10.86
59.99	2.35	4.98	25.95	91.72%	11.69
59.99	2.53	4.98	27.95	91.75%	12.53
59.99	2.71	4.98	29.95	91.72%	13.47
59.99	2.90	4.98	31.95	91.68%	14.43
59.99	3.08	4.98	33.95	91.62%	15.53
59.99	3.26	4.98	35.95	91.53%	16.56
59.99	3.45	4.98	37.95	91.43%	17.69

Table 2-3. 60V_{IN} Efficiency and Power Loss Across Load (continued)

V_{in}	I_{in}	V_{out}	I_{out}	Eff	Ploss (W)
59.99	3.64	4.98	39.95	91.31%	18.95
59.99	3.82	4.98	41.95	91.17%	20.25
59.99	4.01	4.98	43.95	91.01%	21.63
59.99	4.20	4.98	45.95	90.84%	23.06
59.99	4.39	4.98	47.95	90.65%	24.66
59.99	4.59	4.98	49.95	90.45%	26.33

2.3 Thermal Images

The thermal images presented in Figure 2-3 and Figure 2-4 are taken with a load of 37.5A at steady-state and with a fan blowing on the hardware. Figure 2-4 has an input voltage of 20V_{in}, where the LMG2100s experienced a rise of about 21.5°C above the ambient room temperature of 22°C. Figure 2-3 has an input voltage of 48V_{in}, where the LMG2100s experienced a rise of about 57°C, again measured relative to the ambient room temperature of 22°C.

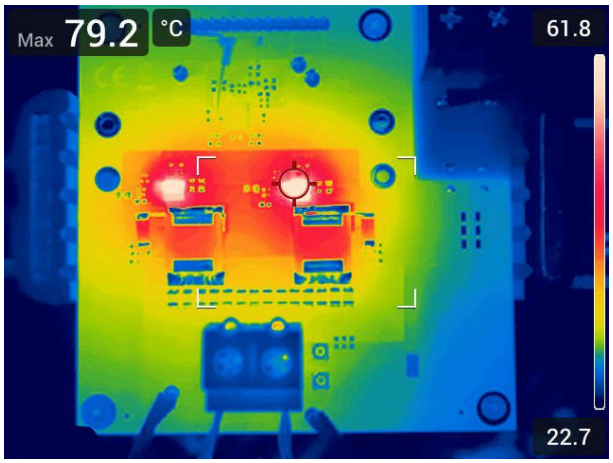


Figure 2-3. 48V_{IN}, 37.5A Thermal Image With Fan

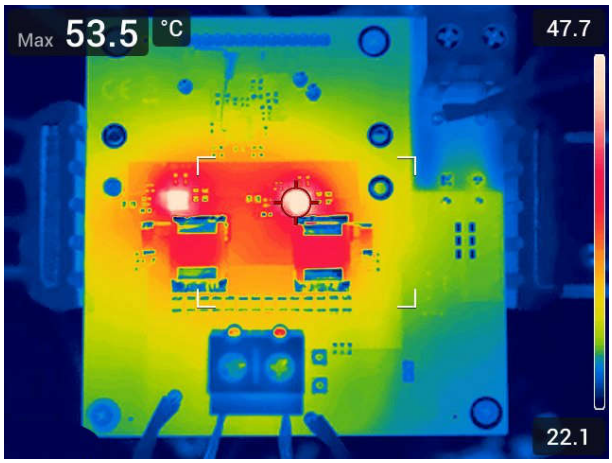


Figure 2-4. 20V_{IN}, 37.5A Thermal Image With Fan

The thermal images presented in Figure 2-6 and Figure 2-5 are taken with a load of 25A at steady-state and without a fan blowing on the hardware. Figure 2-6 has an input voltage of 20V_{in}, where the LMG2100s experienced a rise of about 39°C above the ambient room temperature of 22°C. Figure 2-5 has an input voltage of 48V_{in}, where the LMG2100s experienced a rise of about 71°C, again measured relative to the ambient room temperature of 22°C.

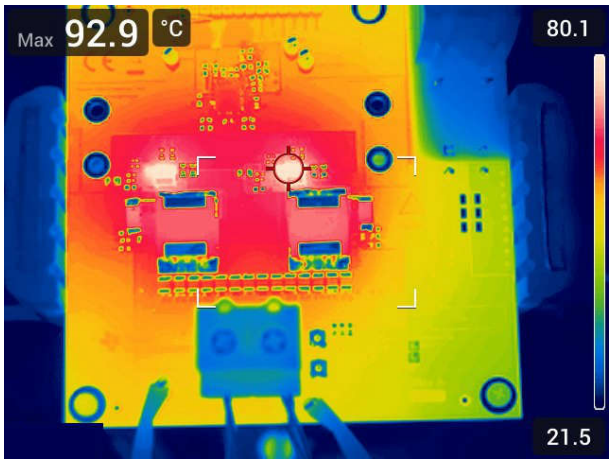


Figure 2-5. 48V_{IN}, 25A Thermal Image Without Fan

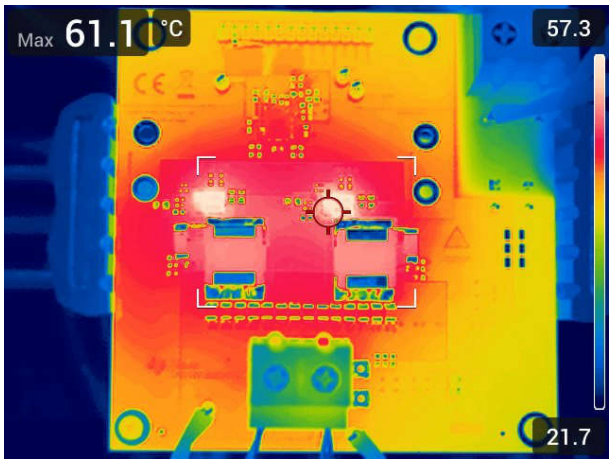


Figure 2-6. 20V_{IN}, 25A Thermal Image Without Fan

The thermal images presented in Figure 2-7 and Figure 2-8 are taken with a load of 50A at steady-state and with a fan blowing on the hardware. Figure 2-7 has an input voltage of 20V_{in}, where the LMG2100s experienced a rise of about 50°C above the ambient room temperature of 22°C. Figure 2-8 has an input voltage of 48V_{in}, where the LMG2100s experienced a rise of about 79°C, again measured relative to the ambient room temperature of 22°C.

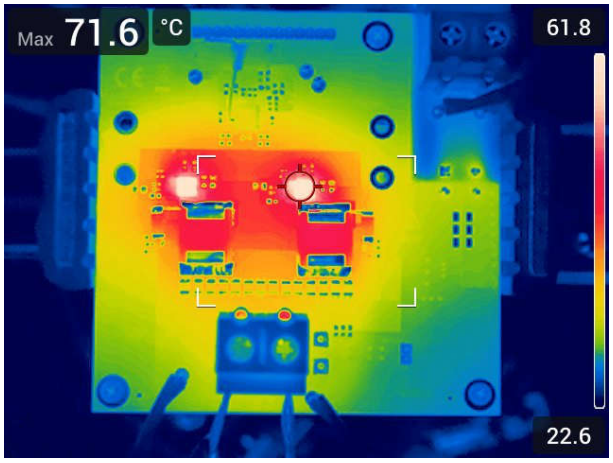


Figure 2-7. 20V_{IN}, 50A Thermal Image With Fan

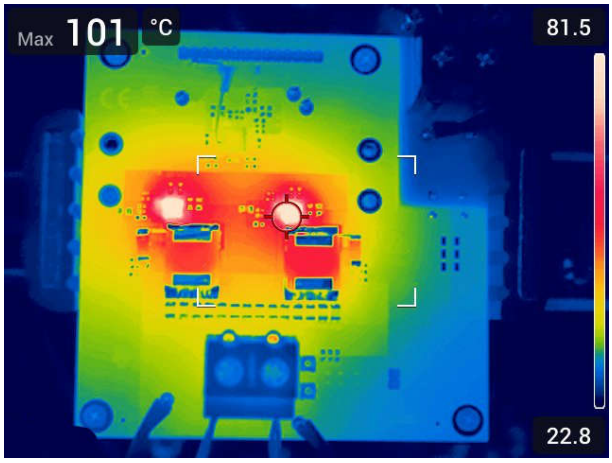


Figure 2-8. 48V_{IN}, 50A Thermal Image With Fan

2.4 Bode Plots

Each bode plot is shown at a $5V_{OUT}$ output. One bode plot is shown for both input voltages of $20V_{IN}$ and $48V_{IN}$. The phase margin is always at least 67.2° and gain margin is greater than 10dB. The bode plots in Figure 2-9 and Figure 2-10 were created at a full 50A load with Figure 2-10 having a $20V_{IN}$ input and Figure 2-9 having a $48V_{IN}$ input.

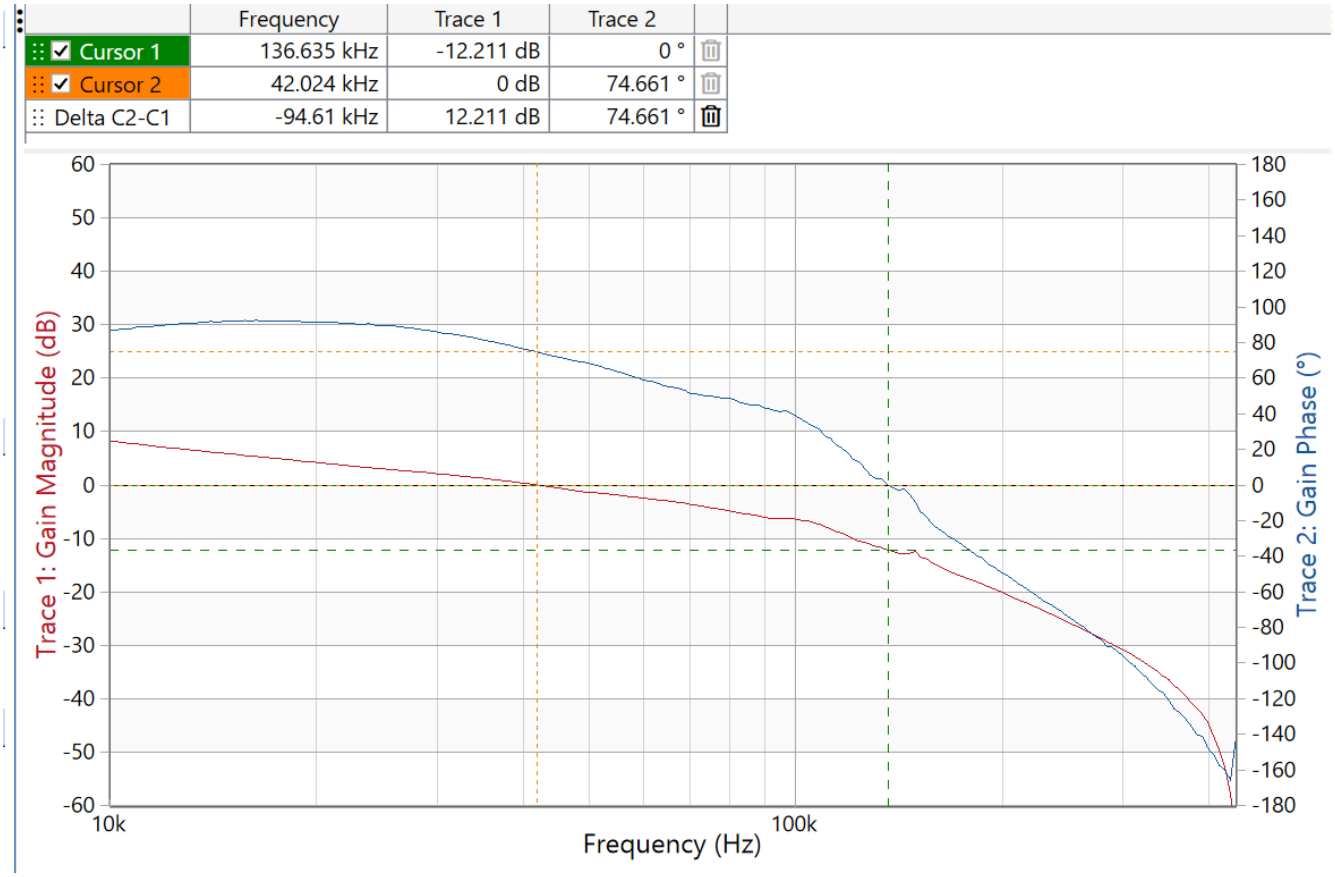


Figure 2-9. Bode Plot: $48V_{IN}$ at 50A

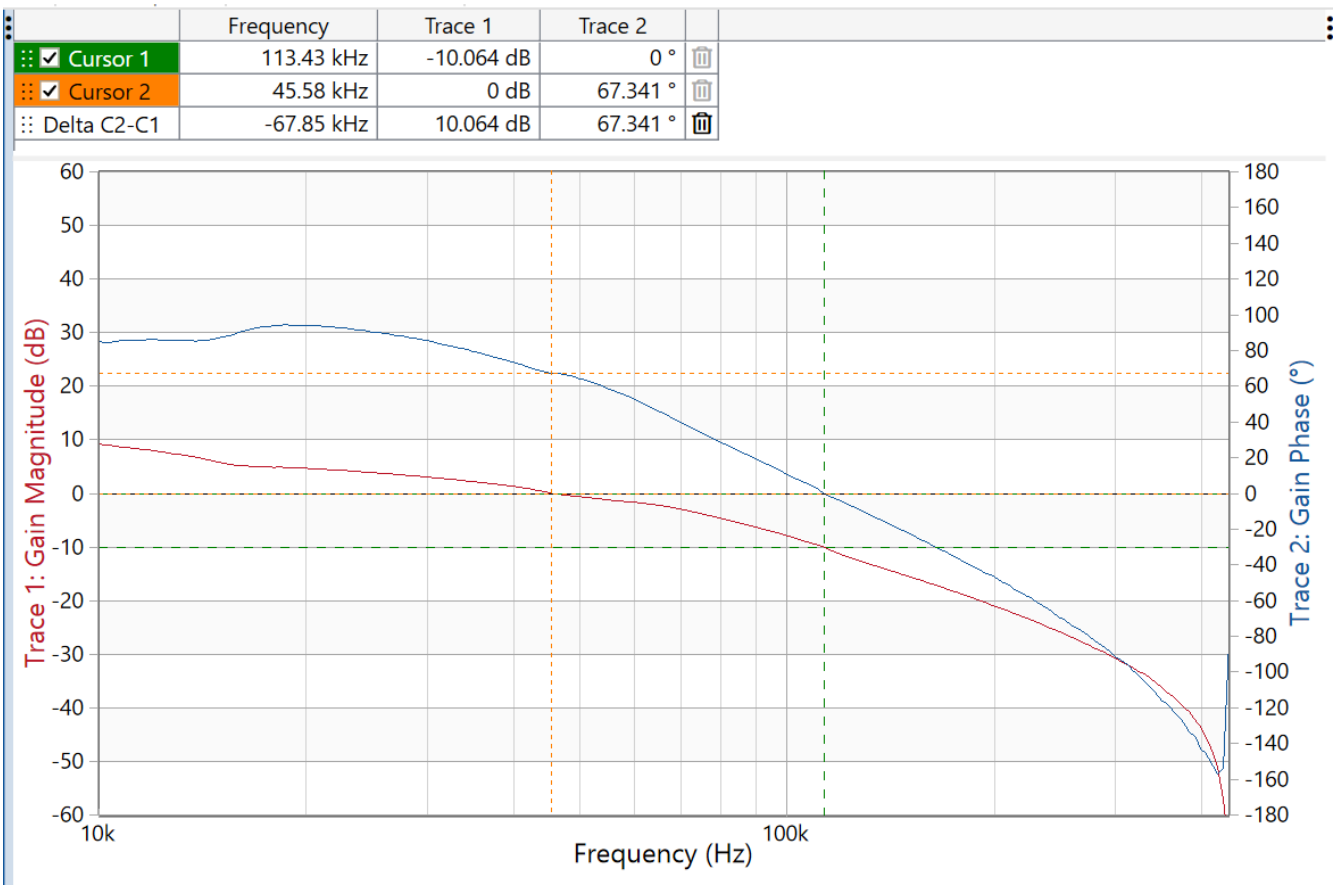


Figure 2-10. Bode Plot: 20V_{IN} at 50A

3 Waveforms

3.1 Switching

Figure 3-1 displays the main switching waveform that is representative of worst case scenario. The waveform in Figure 3-2 is captured at 60V_{IN} while operating under a maximum load of 50A. The waveform is characterized by the following conditions: a switching frequency of 442.3kHz, an overshoot of 0.5V, a rise time of 7.7ns, and a fall time of 3.5ns.

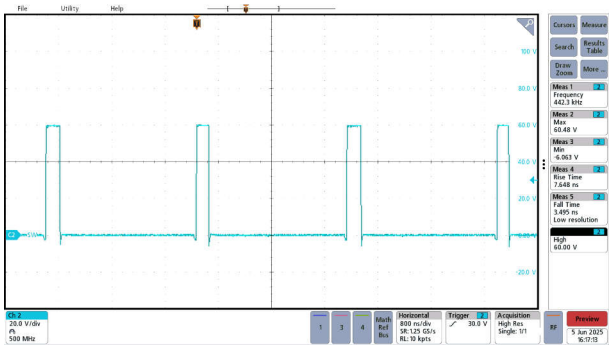


Figure 3-1. 60V_{IN} Switch Node at 800ns/div

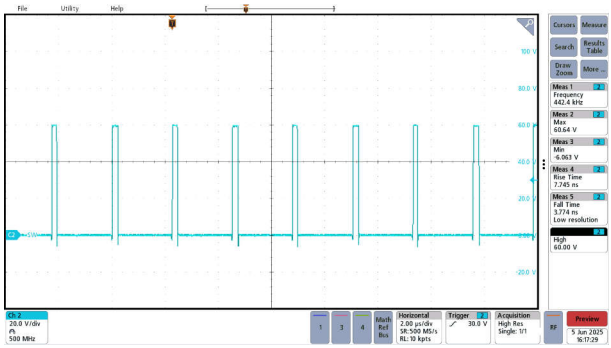


Figure 3-2. 60V_{IN} Switch Node at 2us/div

3.2 Output Voltage Ripple

Figure 3-3 displays the output voltage ripple. The waveform in Figure 3-3 is captured at $48V_{IN}$ while operating under a maximum load of 50A. The waveform is characterized by the following conditions: a maximum value of 5mV, minimum value of –3.6mV, and a total peak-to-peak ripple of 8.6mV.

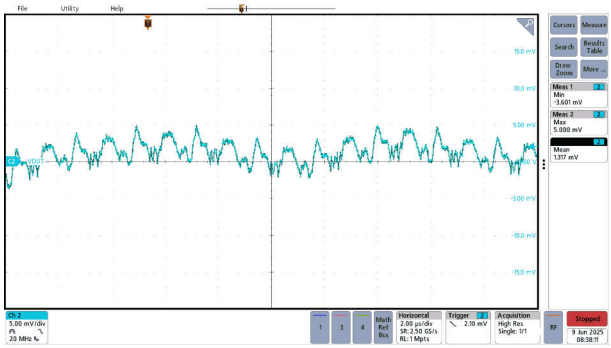


Figure 3-3. Output Voltage Ripple at Full Load

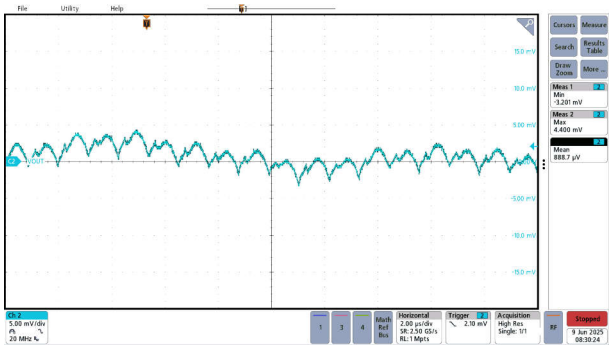


Figure 3-4. Output Voltage Ripple at No Load

3.3 Load Transients

Figure 3-5 represents a load transient at $48V_{IN}$ with a 12.5A to 37.5A load step, and then a 37.5A to 12.5A load dump. The load transient is totaling a 25% to 75% step at about an 4A/us slew rate and demonstrates an overshoot and undershoot of about 5% or less.

Figure 3-6 represents a load transient at $48V_{IN}$ with a 25A to 50A load step, and then a 50A to 25A load dump. The load transient is totaling a 50% to 100% step at about an 4A/us slew rate and demonstrates an overshoot and undershoot of about 5% or less.

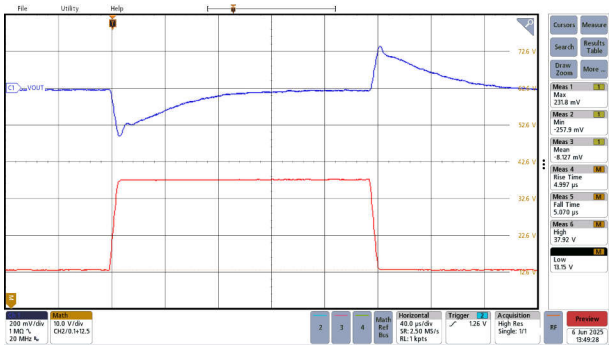


Figure 3-5. Load Transient 1: 12.5A - 37.5A at 4A/us

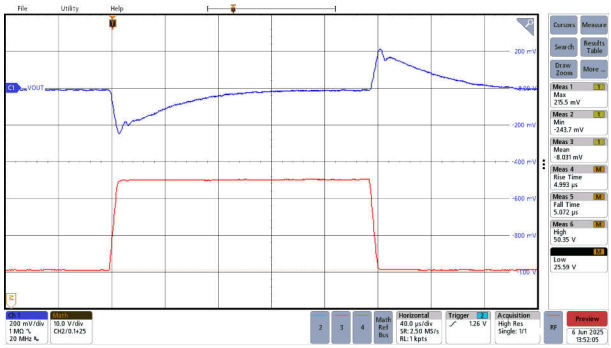


Figure 3-6. Load Transient 2: 25A to 50A at 4A/us

3.4 Start-up and Shutdown Sequence

Figure 3-7 displays the start-up waveform at 48V_{in} input into a no load. The total rise time is 3.4ms, insinuating total start-up totaling about 4.25ms.

Figure 3-8 displays the shutdown waveform at 48V_{in} input into a ⅓Ω constant-resistance load using an electronic load. The total fall time is 37.2ms, insinuating total shutdown totaling about 46.4ms.

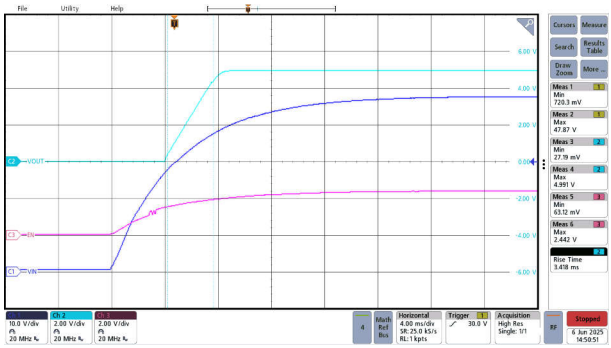


Figure 3-7. Start-up

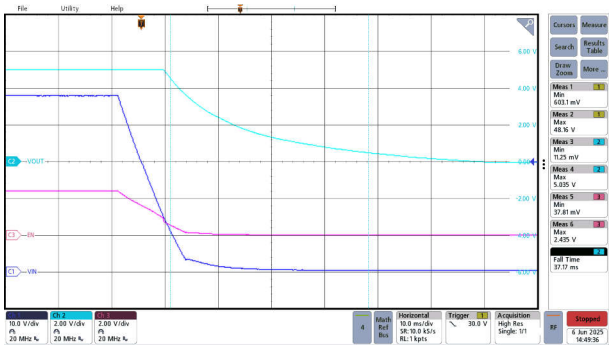


Figure 3-8. Shutdown

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