

TPS7H5001-SP 12 V to 0.8 V / 80 A Buck Converter Design Detailing Methodology and Results



Daniel Hartung

ABSTRACT

The TPS7H5001-SP EVM uses the TPS7H5001-SP and LMG1210 to create a synchronous buck with error amplification, current sensing and overcurrent protection. The design is meant to convert a 12 V rail into a 0.8 V rail appropriate for FPGA core voltage rails. The TPS7H5001-SP is used to switch the FET's of the synchronous buck and provides voltage and current to the output.

Table of Contents

1 Introduction	2
2 System Design Theory	2
2.1 Switching Frequency.....	2
2.2 Leading Edge Blanking.....	3
2.3 Dead Time.....	3
2.4 Enable and UVLO.....	3
2.5 Output Voltage Programing.....	3
2.6 Soft Start.....	3
2.7 Sensing Circuit.....	3
2.8 FAULT Mode.....	4
2.9 HICCUP Mode.....	4
2.10 Slope Compensation.....	4
2.11 Output Capacitance.....	4
2.12 Compensation.....	4
3 Test Results	5
4 Bill of Materials	8
5 Schematics	14
6 PCB Layouts	20
7 References	26

List of Figures

Figure 3-1. Efficiency vs. Current.....	5
Figure 3-2. Start-up Loaded (30 A).....	5
Figure 3-3. Shutdown.....	6
Figure 3-4. Voltage Transient.....	6
Figure 3-5. Thermal Image of Board with 80 A Output Current.....	7
Figure 3-6. Switch Node Voltage with Full Output Current.....	7
Figure 5-1. Controller Card Schematic.....	14
Figure 5-2. Daughter Card Schematic (Page 1).....	15
Figure 5-3. Daughter Card Schematic (Page 2).....	16
Figure 5-4. Mother Board Schematic (Page 1).....	17
Figure 5-5. Mother Board Schematic (Page 2).....	18
Figure 5-6. Mother Board Schematic (Page 3).....	19
Figure 6-1. Controller Card Top Overlay.....	20
Figure 6-2. Controller Card Top Solder.....	20
Figure 6-3. Controller Card Top Layer.....	20
Figure 6-4. Controller Card Signal Layer 1.....	20
Figure 6-5. Controller Card Signal Layer 2.....	20

Figure 6-6. Controller Card Bottom Solder.....	20
Figure 6-7. Controller Card Bottom Solder Mask.....	20
Figure 6-8. Controller Card Bottom Overlay.....	20
Figure 6-9. Controller Card Drill Drawing.....	21
Figure 6-10. Daughter Card Top Overlay.....	21
Figure 6-11. Daughter Card Top Solder.....	21
Figure 6-12. Daughter Card Top Layer.....	21
Figure 6-13. Daughter Card Signal Layer 1.....	21
Figure 6-14. Daughter Card Signal Layer 2.....	21
Figure 6-15. Daughter Card Signal Layer 3.....	22
Figure 6-16. Daughter Card Signal Layer 4.....	22
Figure 6-17. Daughter Card Signal Layer 5.....	22
Figure 6-18. Daughter Card Signal Layer 6.....	22
Figure 6-19. Daughter Card Bottom Layer.....	22
Figure 6-20. Daughter Card Bottom Solder.....	22
Figure 6-21. Daughter Card Bottom Overlay.....	23
Figure 6-22. Daughter Card Drill Drawing.....	23
Figure 6-23. Mother Board Top Overlay.....	23
Figure 6-24. Mother Board Top Solder.....	23
Figure 6-25. Mother Board Top Layer.....	23
Figure 6-26. Mother Board Signal Layer 1.....	23
Figure 6-27. Mother Board Signal Layer 2.....	24
Figure 6-28. Mother Board Signal Layer 3.....	24
Figure 6-29. Mother Board Signal Layer 4.....	24
Figure 6-30. Mother Board Signal Layer 5.....	24
Figure 6-31. Mother Board Signal Layer 6.....	24
Figure 6-32. Mother Board Bottom Layer.....	24
Figure 6-33. Mother Board Bottom Solder.....	25
Figure 6-34. Mother Board Bottom Overlay.....	25
Figure 6-35. Bottom Overlay.....	25
Figure 6-36. Board Dimensions.....	25

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1 Introduction

The TPS7H5001-SP EVM uses the TPS7H5001-SP and LMG1210 to create a synchronous buck with error amplification, current sensing and overcurrent protection. The design converts a 12 V rail into a 0.8 V rail meant for high current FPGA designs, and is created to meet the tight regulation requirements that FPGA core voltage rails require. The TPS7H5001-SP is used to switch the FET's of the synchronous buck and provides voltage and current to the output. Due to the roughly 150-mA peak current capability of the TPS7H5001's primary switching outputs, the LMG1210 gate driver is used to amplify the current to provide the FET's of the synchronous buck with sufficient current. The system uses the TPS7H5001-SP to generate a 80-A output. These outputs are not dependent on the TPS7H5001-SP itself, and can be increased or decreased depending on the design. The full design was created as part of a testing platform and spans across 3 separate boards. There is a controller card with the TPS7H5001-SP, a daughter card with the powerstage, and a motherboard with large capacitance. The design is meant to show the feasibility of the system, and is not optimized for size.

2 System Design Theory

Throughout the design process of the converter equations were used to determine the values to create an initial circuit to test. Note that sometimes the value in this section do not exactly match what is shown in the schematic. Most of the time, this is due to rounding caused by values available in lab or optimizations only known after thorough testing.

2.1 Switching Frequency

Choosing a switching frequency has a tradeoff between efficiency and bandwidth. Higher switching frequencies have larger bandwidth, but a lower efficiency than lower switching frequencies. First, the maximum switching frequency for the requirements had to be calculated. For the calculation, the minimum on time for the device was determined by adding 75 ns for controller on time and 100 ns of LEB.

$$f_{sw_max} = \frac{1}{T_{sw_max}} = \frac{\text{Duty Cycle}}{t_{min_on_time}} = \frac{0.0667}{175 \text{ ns}} = 381 \text{ kHz} \quad (1)$$

To make sure the max switching frequency was not approached, the switching frequency was set to 275 kHz. Using equations provided by the data sheet for the TPS7H5001-SP, the RT resistor was chosen to be 392 k. The equation for the switching frequency used is [Equation 2](#).

$$RT = \frac{112,000}{f_{sw} \text{ (kHz)}} - 19.7 = \frac{112,000}{275 \text{ kHz}} - 19.7 = 388 \text{ k}\Omega \quad (2)$$

2.2 Leading Edge Blanking

Leading edge blank time is utilized to remove any transient noise from the current sensing loop after the primary switching outputs, OUTA or OUTB, go high. The leading-edge blank time was selected to be 100 ns. [Equation 3](#) shows the calculation to program the LEB resistor for a chosen LEB time:

$$R_{LEB} = 1.212 \times LEB - 9.484 = 1.212 \times 100 \text{ ns} - 9.484 = 112 \text{ k}\Omega \quad (3)$$

2.3 Dead Time

The TPS7H5001-SP allows for the user to program two independent dead times. This allows for the dead times to be optimized by the user to prevent shoot-through between the primary and synchronous switches while attaining the best possible converter efficiency. The equation for determining the values of and for a desired dead time is shown in [Equation 4](#).

$$R_{PS} = R_{SP} = 1.207 \times DT - 8.858 = 1.207 \times 25 \text{ ns} - 8.858 = 21.3 \text{ k}\Omega \quad (4)$$

2.4 Enable and UVLO

The TPS7H5001-SP EVM uses two resistors to program the controller to enable the device when VIN surpasses a user determined threshold. The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AVSS. Using [Equation 5](#), the user can calculate the value for a chosen value of . Once the resistor values are determined, [Equation 6](#) can be used to determine the minimum startup voltage.

$$R_{UVLO_TOP} = R_{UVLO_Bottom} \left(\frac{V_{Start_Max}}{V_{EN_Rising_Max}} - 1 \right) = \left(\frac{10 \text{ V}}{0.65 \text{ V}} - 1 \right) = 71.9 \text{ k}\Omega \quad (5)$$

$$V_{START,MIN} = V_{EN_FALLING_MIN} \left(\frac{R_{UVLO_TOP}}{R_{UVLO_BOT}} + 1 \right) = \left(\frac{75 \text{ k}\Omega}{5 \text{ k}\Omega} + 1 \right) = 16 \text{ V} \quad (6)$$

2.5 Output Voltage Programming

The output voltage of the power converter is set by using a resistor divider from of the converter to the VSENSE pin. For a selected value of , the value of can be found using [Equation 7](#).

$$R_{bottom} = \frac{V_{ref}}{V_{out} - V_{ref}} \times R_{top} = \frac{0.613 \text{ V}}{1 \text{ V} - 0.613 \text{ V}} \times 10 \text{ k}\Omega = 15.8 \text{ k}\Omega \quad (7)$$

2.6 Soft Start

Using a capacitor between the soft start (SS) pin and AVSS, the soft start of the device is programmed. [Equation 8](#) shows the calculation of the SS capacitor:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{ref}} = \frac{12 \text{ ms} \times 2.7 \mu\text{A}}{0.613 \text{ V}} = 52.9 \text{ nF} \quad (8)$$

2.7 Sensing Circuit

The sensing circuit of the buck converter was set-up with a similar time period to the inductance and parasitic resistance of the output inductor. This process allows for a triangle wave similar to the output current to be generated from a resistor and capacitor in parallel with the output inductor. This is then directly fed into the CS_ILIM pin of the controller.

2.8 FAULT Mode

FAULT mode was disabled by connecting the pin to AVSS.

2.9 HICCUP Mode

For the design, the value of the hiccup capacitor used is 100 nF. Based on this value, the delay and hiccup times of the converter after an overcurrent are detected can be calculated using [Equation 9](#) and [Equation 10](#), respectively.

$$t_{delay} = \frac{C_{HICC} \times 0.6 V}{80 \mu A} = \frac{100 nF \times 0.6 V}{80 \mu A} = 75 \mu s \quad (9)$$

$$t_{HICC} = \frac{C_{HICC} \times (1 V - 0.3 V)}{1 \mu A} = \frac{100 nF \times (1 V - 0.3 V)}{1 \mu A} = 70 ms \quad (10)$$

2.10 Slope Compensation

To avoid errors associated with subharmonic oscillation as well as give noise immunity, slope compensation is used. The signal of the current ramp from the current sense was small enough that a large amount of slope compensation was needed to give the needed noise immunity to the circuit. These factors lead to 50 k Ohms being used for the RSC resistor.

2.11 Output Capacitance

The output capacitance value is picked such that there is enough capacitance for the required voltage ripple and output current load step. **Equation 17** shows the calculation to find the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient. **Equation 19** determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design. Due to these calculations 20 mF was chosen for the design.

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_c} = \frac{\Delta 33.3 A}{2\pi \times 18 mV \times 15 kHz} = 19.6 mF \quad (11)$$

$$C_{OUT} > \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times f_{sw}} = \frac{80 \times 0.0667}{1 mV \times 275 kHz} = 19.4 mF \quad (12)$$

2.12 Compensation

Before the compensator component values can be found, the power stage transconductance was calculated as shown in [Equation 13](#).

$$gm_{ps} = \frac{R_{CS} \times C_{CS} \times f_{SW}}{L_{OUT}} = \frac{1 k\Omega \times 100 nF}{560 nH} = 179 \quad (13)$$

The following equations were used to achieve the desired crossover frequency, and values used as a starting value. These values were optimized during lab testing and movement of the poles and zeros further out in frequency were determined to work better for the converter as a whole. Note that the resistor used in calculations is the value that was settled on in lab and not the answer provided by the equation.

$$R_{COMP} = \frac{2\pi \times f_c \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{ps}} = \frac{2\pi \times 15 kHz \times 0.8 V \times 20 mF}{1800 \mu S \times 0.613 V \times 179 S} = 7.6 k\Omega \quad (14)$$

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}} = \frac{0.8 V \times 20 mF}{80 \times 6.98 k\Omega} = 28 nF \quad (15)$$

$$f_{esr} = \frac{1}{2\pi \times C_{OUT} \times ESR} = \frac{1}{2\pi \times 20 mF \times 0.1 m\Omega} = 79.6 kHz \quad (16)$$

$$C_{HF} = \frac{1}{2\pi \times R_{comp} \times f_{esr}} = \frac{1}{2\pi \times 6.98 k\Omega \times 79.6 kHz} = 285 pF \quad (17)$$

3 Test Results

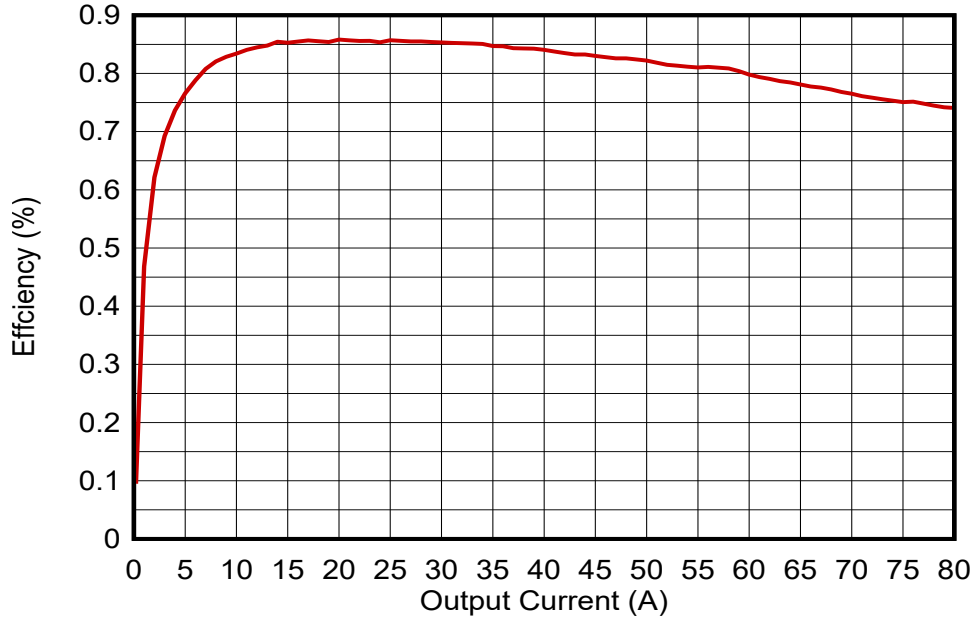


Figure 3-1. Efficiency vs. Current

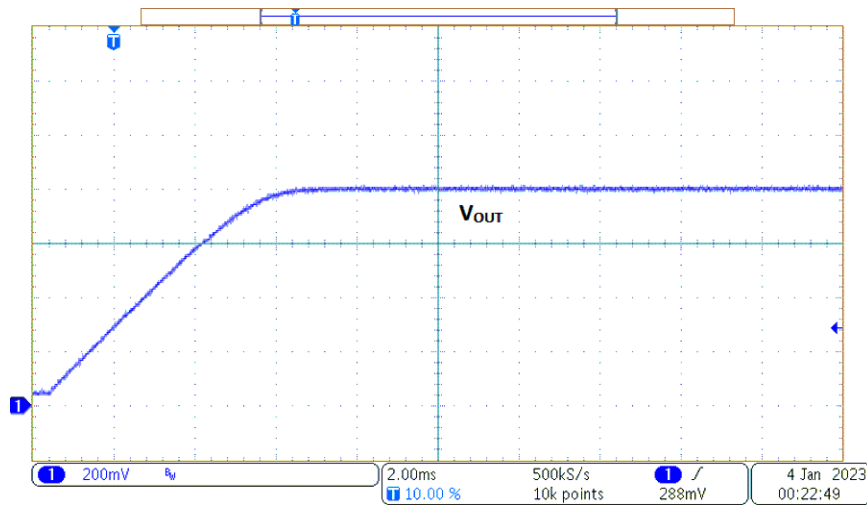


Figure 3-2. Start-up Loaded (30 A)

Figure 3-2 shows start-up of the converter when unloaded.

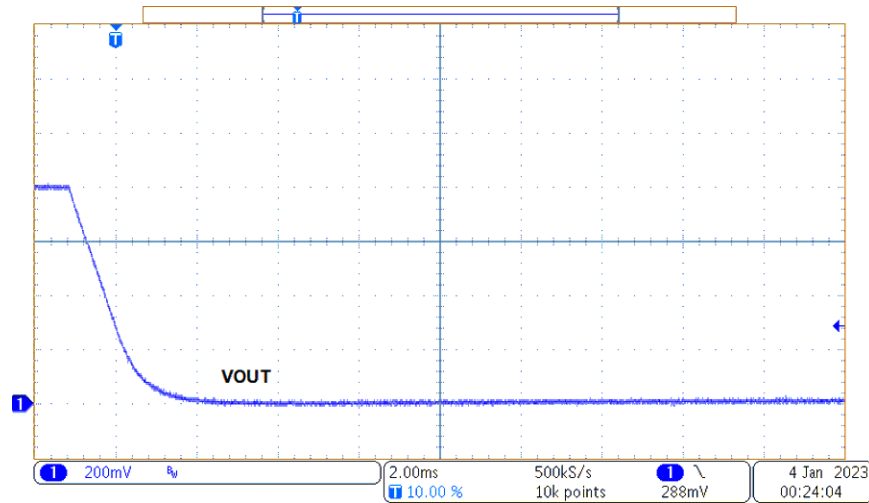


Figure 3-3. Shutdown

Figure 3-3 shows shutdown of the converter when loaded with 30 A on the output current.

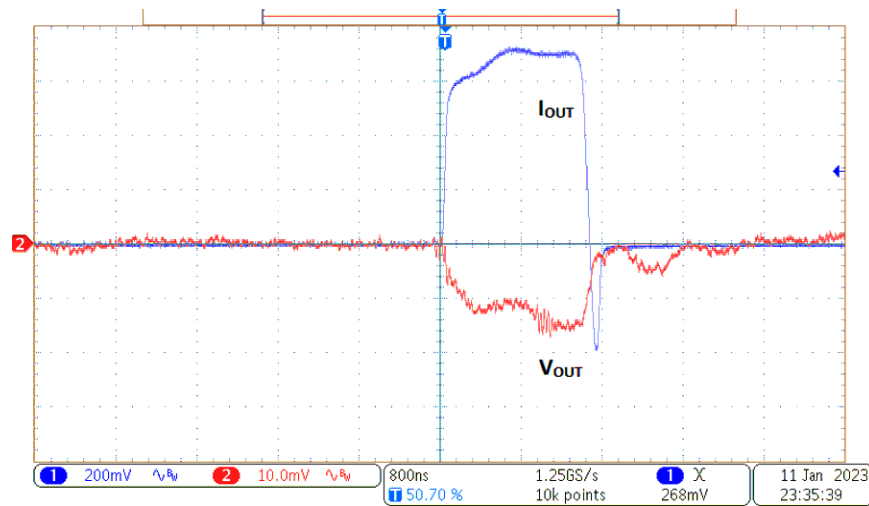


Figure 3-4. Voltage Transient

Figure 3-4 shows the output voltage dip of the converter to a 33 A output current transient. The output current is measured across a 0.01 Ohm resistor that a FET is pulsing the current through.

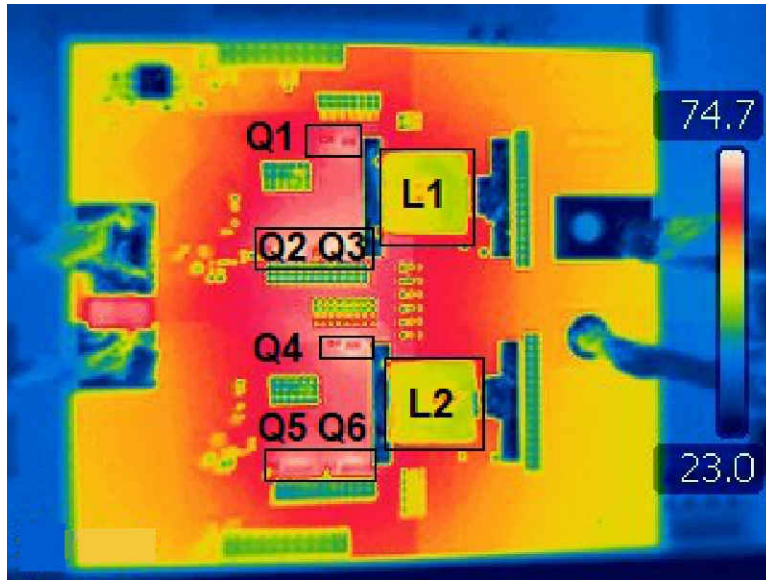


Figure 3-5. Thermal Image of Board with 80 A Output Current

Figure 3-5 shows the thermal image of the board with 80 A of output current.

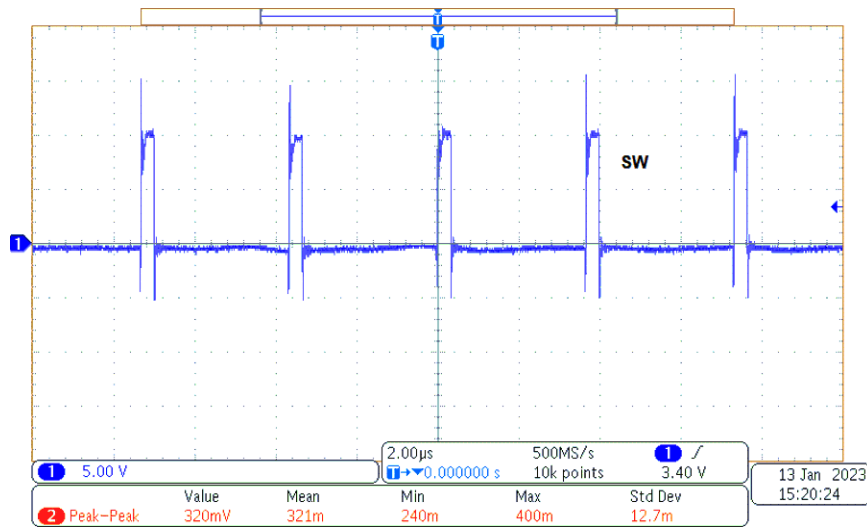


Figure 3-6. Switch Node Voltage with Full Output Current

Figure 3-6 shows the maximum voltage on the switch node of the converter with an output current of 80 A.

4 Bill of Materials

Table 4-1. Controller Card Bill of Materials

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C1, C10	2	CAP, CERM, 1 μ F, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK		
C2, C11	2	CAP, CERM, 10 μ F, 50 V, +/- 10%, X7R, 1210	1210	GRM32ER71H106KA12L	MuRata		
C3, C12, C15	3	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603C104K5RACAUTO	Kemet		
C4, C13	2	CAP, CERM, 0.47 μ F, 25 V, +/- 10%, X7R, 0603	0603	C1608X7R1E474K080AE	TDK		
C5	1	CAP, CERM, 0.1 μ F, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RAC	Kemet		
C6	1	3300pF \pm 5% 100V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	06031C332J4Z2A	AVX Corporation		
C7	1	CAP, CERM, 330 pF, 100 V, +/- 10%, X7R, 0603	0603	GRM188R72A331KA01D	MuRata		
C8	1	CAP, CERM, 0.056 μ F, 16 V, +/- 5%, X7R, 0603	0603	C0603C563J4RACTU	Kemet		
C9, C14	2	CAP, 1 μ F, 25V, \pm 10%, X7R, 0603	0603	CL10B105KA8NNNC	Samsung		
C16, C17	2	CAP, CERM, 100 pF, 25 V, +/- 10%, X7R, 0603	0603	06033C101KAT2A	AVX		
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J2	2	Receptacle, 2.54mm, 10x2, Tin, TH	Receptacle, 2.54mm, 10x2, TH	SSQ-110-03-T-D	Samtec		
R1, R4, R13, R15, R19	5	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc		
R2	1	RES, 75.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0775KL	Yageo		
R3	1	RES, 4.99 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K99L	Yageo		

Table 4-1. Controller Card Bill of Materials (continued)

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R5	1	RES, 35.7 k, 1%, 0.1 W, 0603	0603	RC0603FR-073 5K7L	Yageo		
R6, R7, R16, R17	4	RES, 30.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF3002 V	Panasonic		
R8	1	RES, 261 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD07 261KL	Yageo America		
R9	1	RES, 49.9, 1%, 0.1 W, 0603	0603	M55342K12B49 D9T	TT Electronics/IRC		
R10, R18	2	RES, 110 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603110 KFKEA	Vishay-Dale		
R11, R20	2	RES, 887 k, 1%, 0.1 W, 0603	0603	RC0603FR-078 87KL	Yageo		
R12	1	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-103-B-T5	Susumu Co Ltd		
R14	1	RES, 15.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-071 5K8L	Yageo		
R21, R22	2	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-071 0RL	Yageo		
TP1, TP4, TP6	3	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP2, TP3, TP5	3	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP13, TP14, TP15, TP16	4	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1, U2	2	Radiation-Hardness-Assured Si and GaN Dual Output Controller	CFP22	TPS7H5001HK Y-EM	Texas Instruments		

Table 4-2. Daughter Card Bill of Materials

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C1, C2, C12, C15, C25, C28	6	CAP, CERM, 1 μ F, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK		
C3, C4, C5, C6, C7, C8, C9, C10, C11, C14, C16, C17, C18, C19, C20, C21, C22, C23, C24, C27	20	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603C104K5RACAUTO	Kemet		
C13, C26, C29, C30	4	CAP, CERM, 10 μ F, 25 V, +/- 10%, X7R, 0805	0805	GRM21BZ71E106KE15L	MuRata		
C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54	24	CAP, CERM, 4.7 μ F, 25 V, +/- 10%, X7R, 0805	0805	C2012X7R1E475K125AB	TDK		
D1, D3	2	Diode, Schottky, 100 V, 0.25 A, SOD-123F	SOD-123F	BAT46WH,115	Nexperia		
D2, D4	2	Schottky Barrier Diode 30V 40A 3-Pin TO-263S Emboss T/R	TO263S	RB238NS-30TL	ROHM		
J1, J2	2	Receptacle, 2.54mm, 10x2, Tin, TH	Receptacle, 2.54mm, 10x2, TH	SSQ-110-03-T-D	Samtec		
L1, L2	2	Inductor 560nH 10% 43A 625nOhm	SMT_30MM48_25MM62	PQC2717	Standex Electronics		
MP1, MP2, MP3, MP4	4	Terminal Connector Rectangular Lug, Grounding 6-14 AWG 1/4 Stud	TERMINAL_CO NN	LAMA6-14-QY	Panduit		
Q1, Q4	2	N-Channel Enhancement Mode Power Transistor ID 60A 100 V - - Surface Mount Die	SMT_3MM5_1 MM95	EPC2218	EPC		
Q2, Q3, Q5, Q6	4	MOSFET, N-CH, 30 V, 60 A, 6.05x2.3mm	6.05x2.3mm	EPC2023ENGR	EPC		None
R1	1	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-103-B-T5	Susumu Co Ltd		
R2	1	RES, 3.16 k, 1%, 0.1 W, 0603	0603	RC0603FR-073K16L	Yageo		

Table 4-2. Daughter Card Bill of Materials (continued)

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R3, R4, R5, R6, R8, R9, R10, R11, R12, R13, R15, R16, R17, R19, R21, R23, R24, R27	18	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0 R00	Stackpole Electronics Inc		
R7, R14	2	RES, 169, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603169 RFKEA	Vishay-Dale		
TP1, TP2	2	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
U1	1	Wide Vin Low-Dropout Voltage Regulator, HKU0010A (CFP-10)	HKU0010A	TPS7A4501HK U/EM	Texas Instruments		Texas Instruments
U2, U3	2	200-V, 1.5-A, 3-A Half-Bridge GaN Driver With Adjustable Dead Time, RVR0019A (WQFN-19)	RVR0019A	LMG1210RVRR	Texas Instruments	LMG1210RVRT	Texas Instruments
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
R18, R20, R22, R25, R26	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0 R00	Stackpole Electronics Inc		

Table 4-3. Motherboard Bill of Materials

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1	Printed Circuit Board		M1234	Any		
C1, C2, C3, C4, C5, C6, C7, C11, C12, C13, C14, C15, C16, C17	14	CAP, TA, 220 μ F, 16 V, +/- 10%, 0.025 ohm, SMD	7343-43	TPME227K016R0025	AVX		
C8, C9, C10, C18, C19, C20, C21, C23, C30, C31, C32, C34, C35, C36, C37, C38, C41, C42, C43, C44, C45, C47, C48, C49, C50, C51, C52, C53, C60, C64, C76, C77, C78, C80, C92, C93, C96, C97, C98, C99, C100, C101, C102, C103, C104, C107	46	CAP, TA, 470 μ F, 6.3 V, +/- 10%, 0.03 ohm, SMD	7343-43	T495X477K006ATE030	Kemet		
C39	1	CAP, CERM, 2.2 μ F, 50 V, +/- 10%, X7R, 0805	0805	UMK212BB7225KG-T	Taiyo Yuden		
C40	1	CAP, CERM, 4.7 μ F, 25 V, +/- 10%, X7R, 0805	0805	C2012X7R1E475K125AB	TDK		
C62	1	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805	CEU4J2X7R1H104K125AE	TDK		
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 4400025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J4, J5, J6	4	Receptacle, 2.54mm, 10x2, Tin, TH	Receptacle, 2.54mm, 10x2, TH	SSQ-110-03-T-D	Samtec		
J2	1	Fixed Terminal Blocks MKDSP 10 HV/ 2-10	HDR2	1929517	Phoenix Contact		
J3, J7	2	Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe	131-5031-00	Tektronix		
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		

Table 4-3. Motherboard Bill of Materials (continued)

Designator	Quantity	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
MP1, MP2, MP3, MP4, MP5, MP6, MP7, MP8, MP9, MP10, MP11, MP12	12	Terminal Connector Rectangular Lug, Grounding 6-14 AWG 1/4 Stud	TERMINAL_CO NN	LAMA6-14-QY	Panduit		
Q1	1	MOSFET, N-CH, 30 V, 100 A, DQH0008A (VSON-CLIP-8)	DQH0008A	CSD17559Q5	Texas Instruments		None
R1	1	RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031R00FKEA	Vishay-Dale		
R2	1	RES, 49.9, 1%, 0.1 W, 0603	0603	M55342K12B49D9T	TT Electronics/IRC		
R3	1	RES, 10.0 k, 1%, 0.1 W, 0603	0603	M55342K12B10E0T	TT Electronics/IRC		
R4, R5	2	RES, 0.02, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	LRMAM2512-R02FT4	TT Electronics/IRC		
TP1	1	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP2	1	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
TP24, TP25	2	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
C22, C24, C25, C26, C27, C28, C29, C33, C46, C54, C55, C56, C57, C58, C59, C61, C63, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C79, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C94, C95, C105, C106	0	CAP, TA, 470 uF, 6.3 V, +/- 10%, 0.03 ohm, SMD	7343-43	T495X477K006 ATE030	Kemet		
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		

5 Schematics

Figure 5-1 through Figure 5-6 show the EVM schematics.

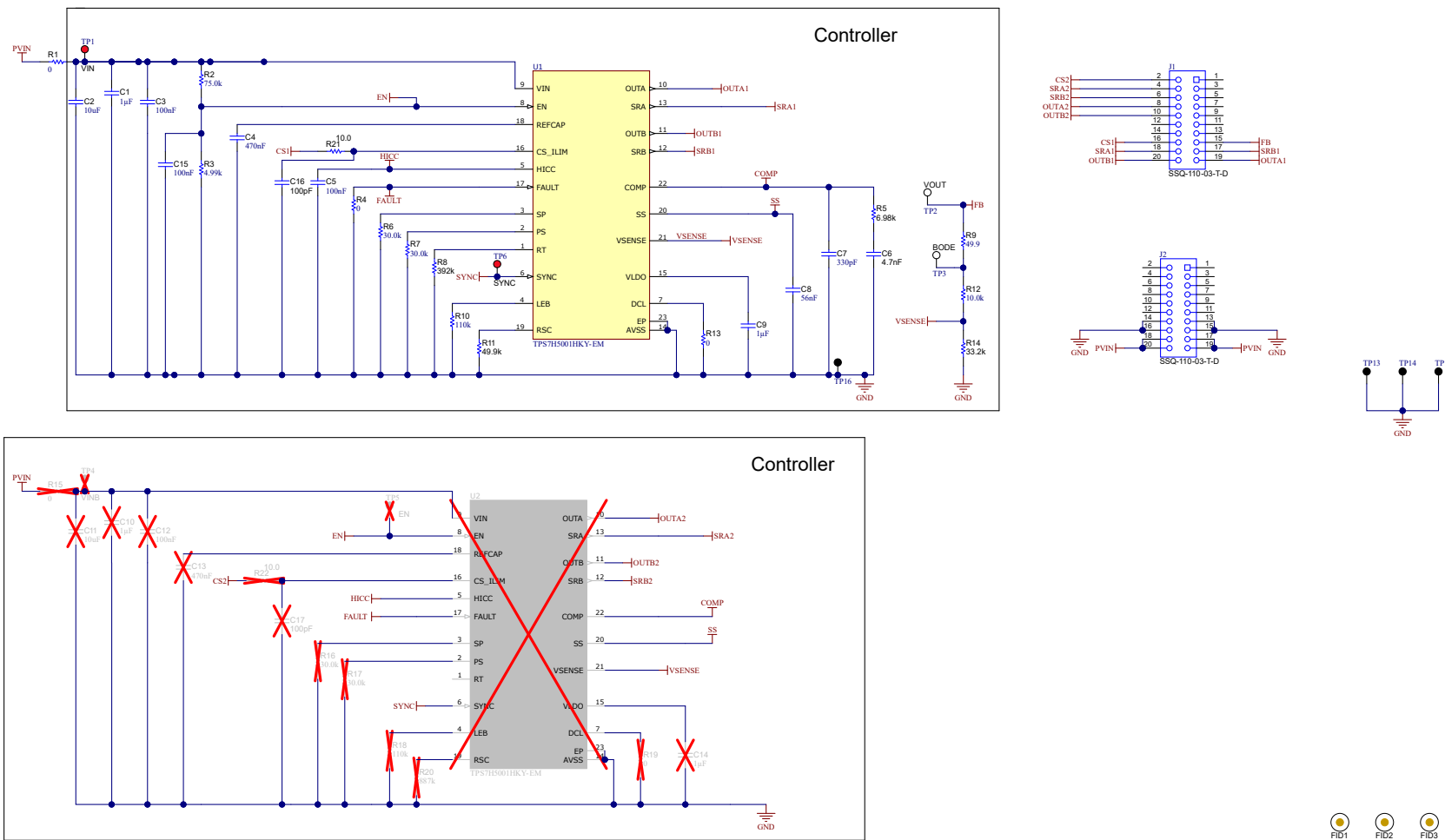


Figure 5-1. Controller Card Schematic

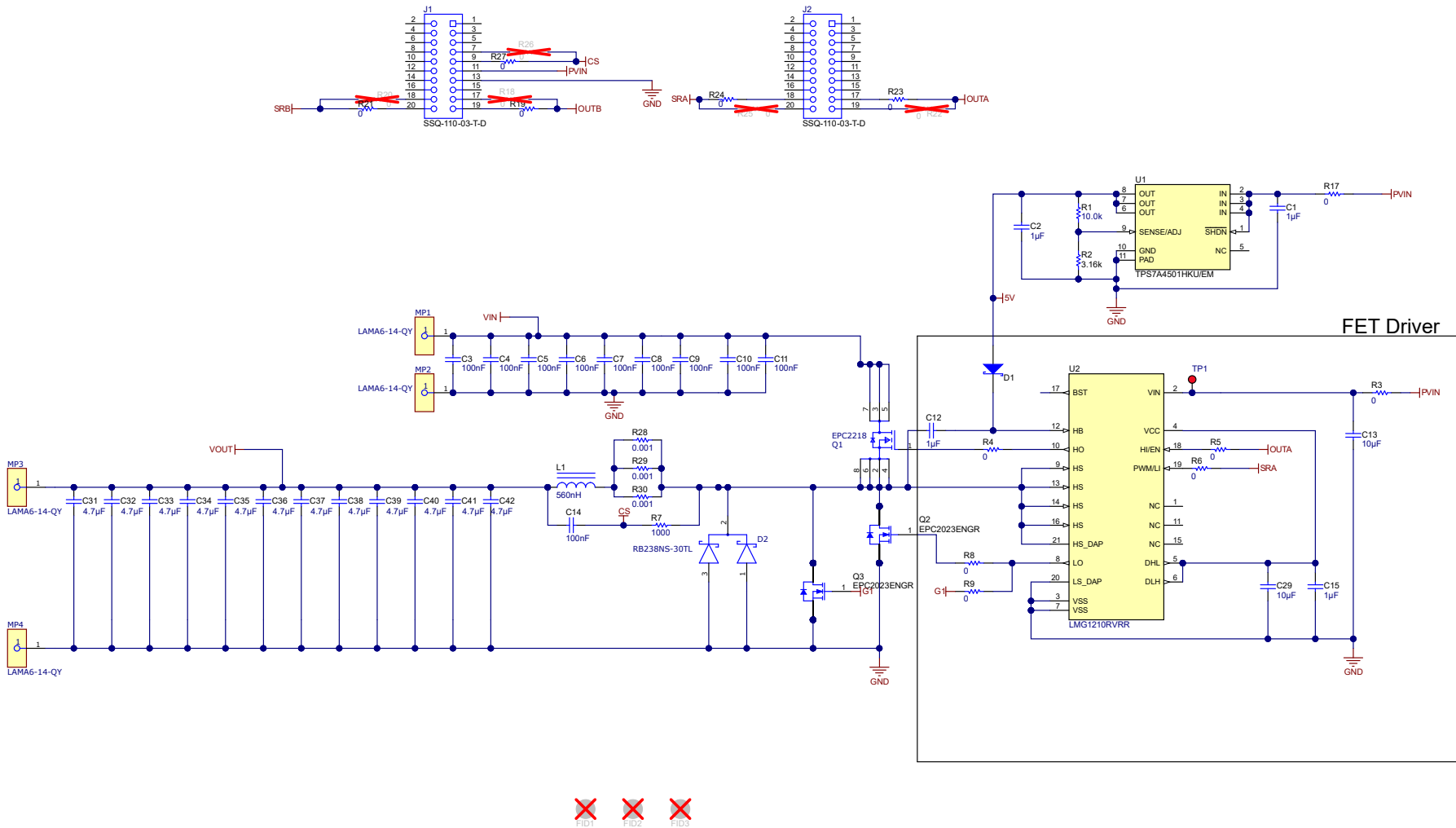


Figure 5-2. Daughter Card Schematic (Page 1)

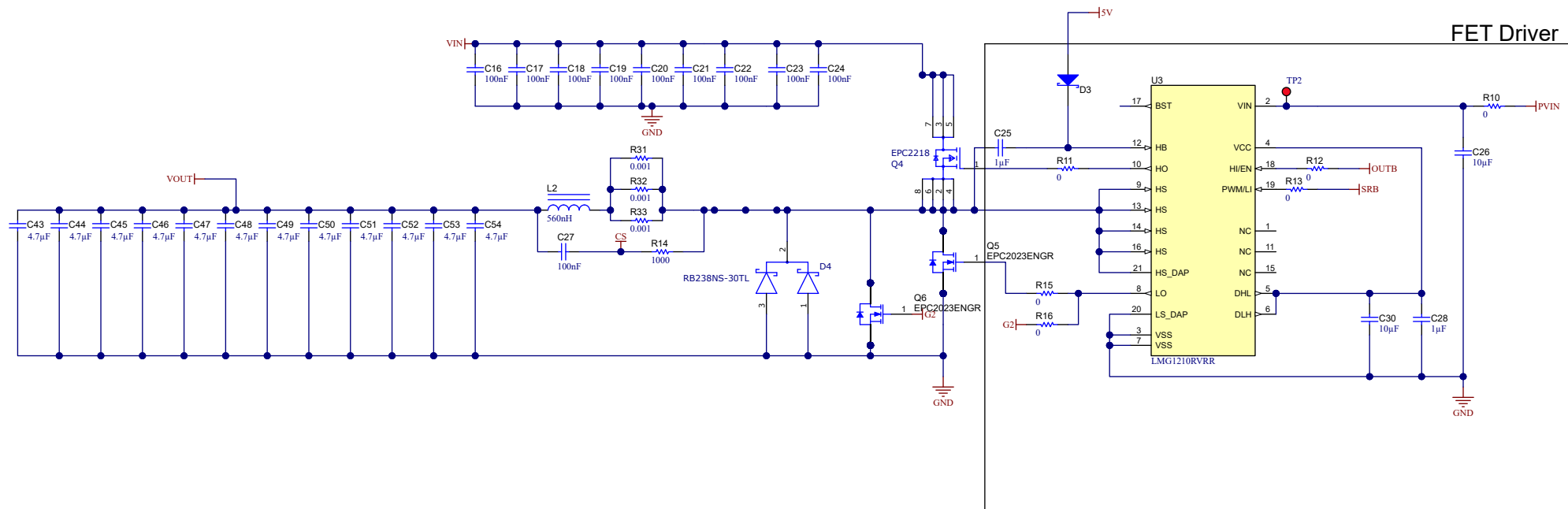


Figure 5-3. Daughter Card Schematic (Page 2)

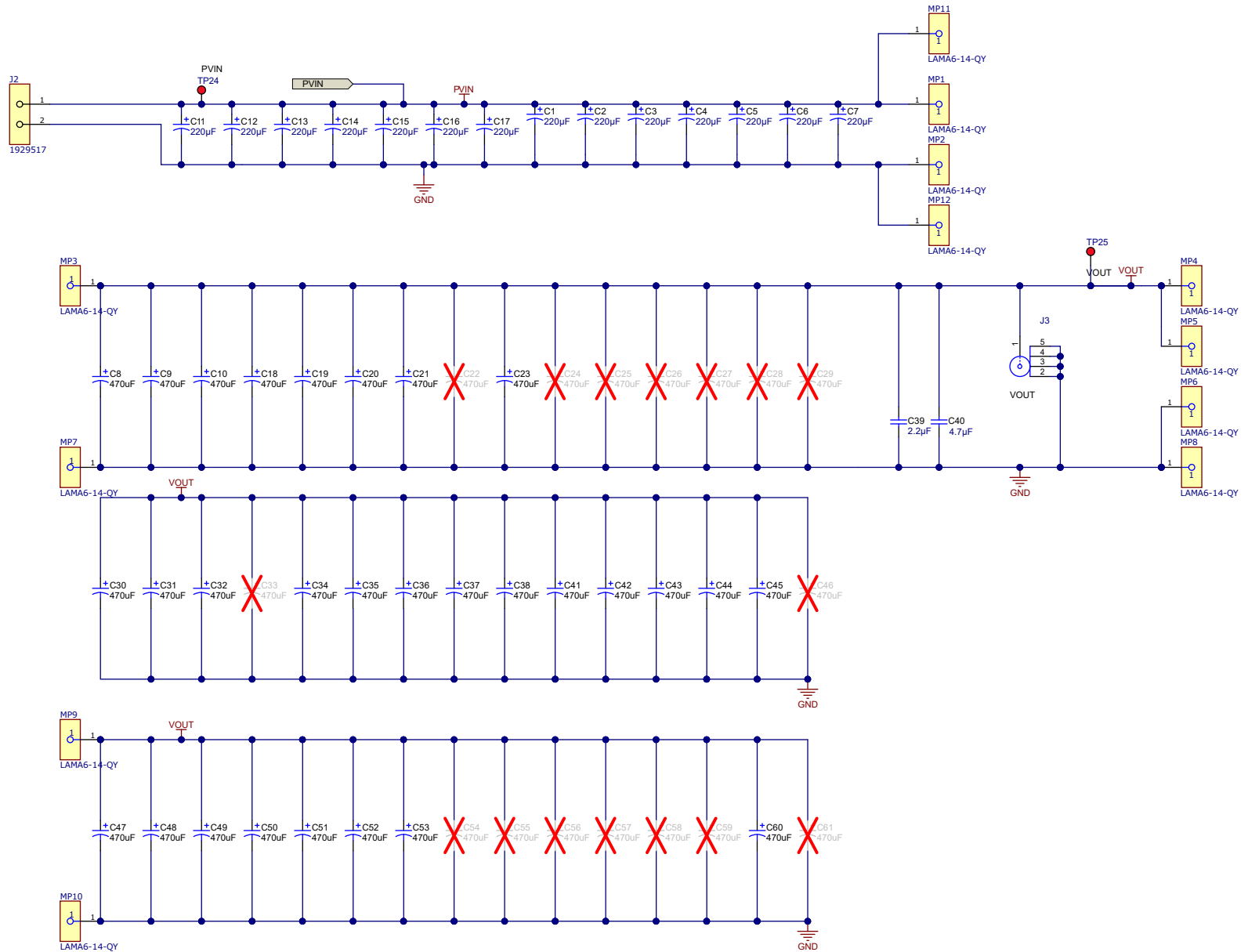


Figure 5-4. Mother Board Schematic (Page 1)

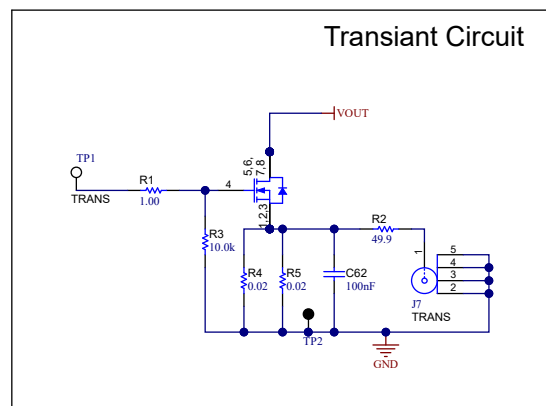
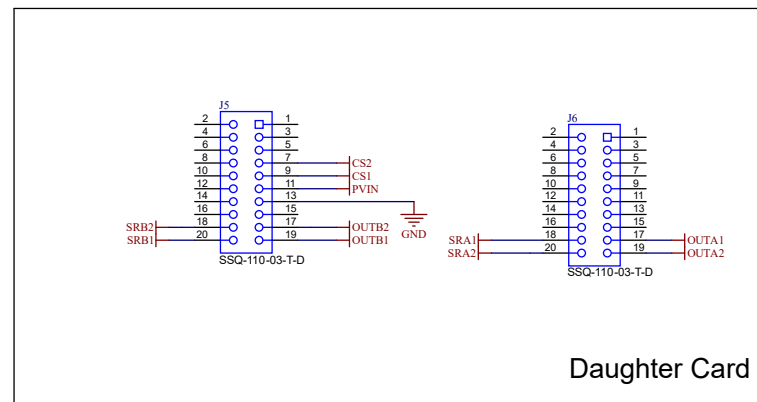
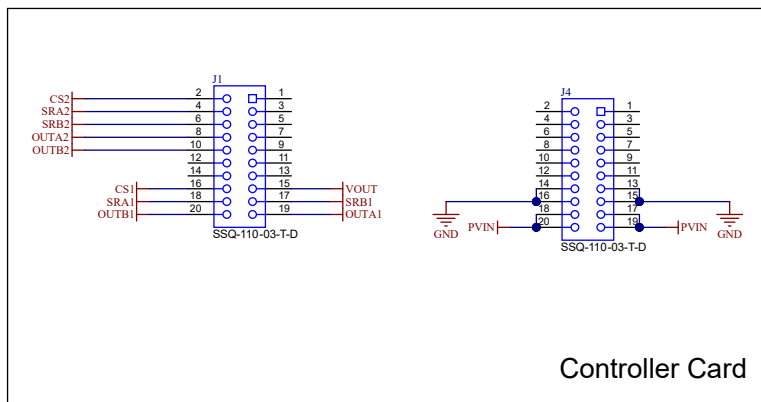


Figure 5-5. Mother Board Schematic (Page 2)

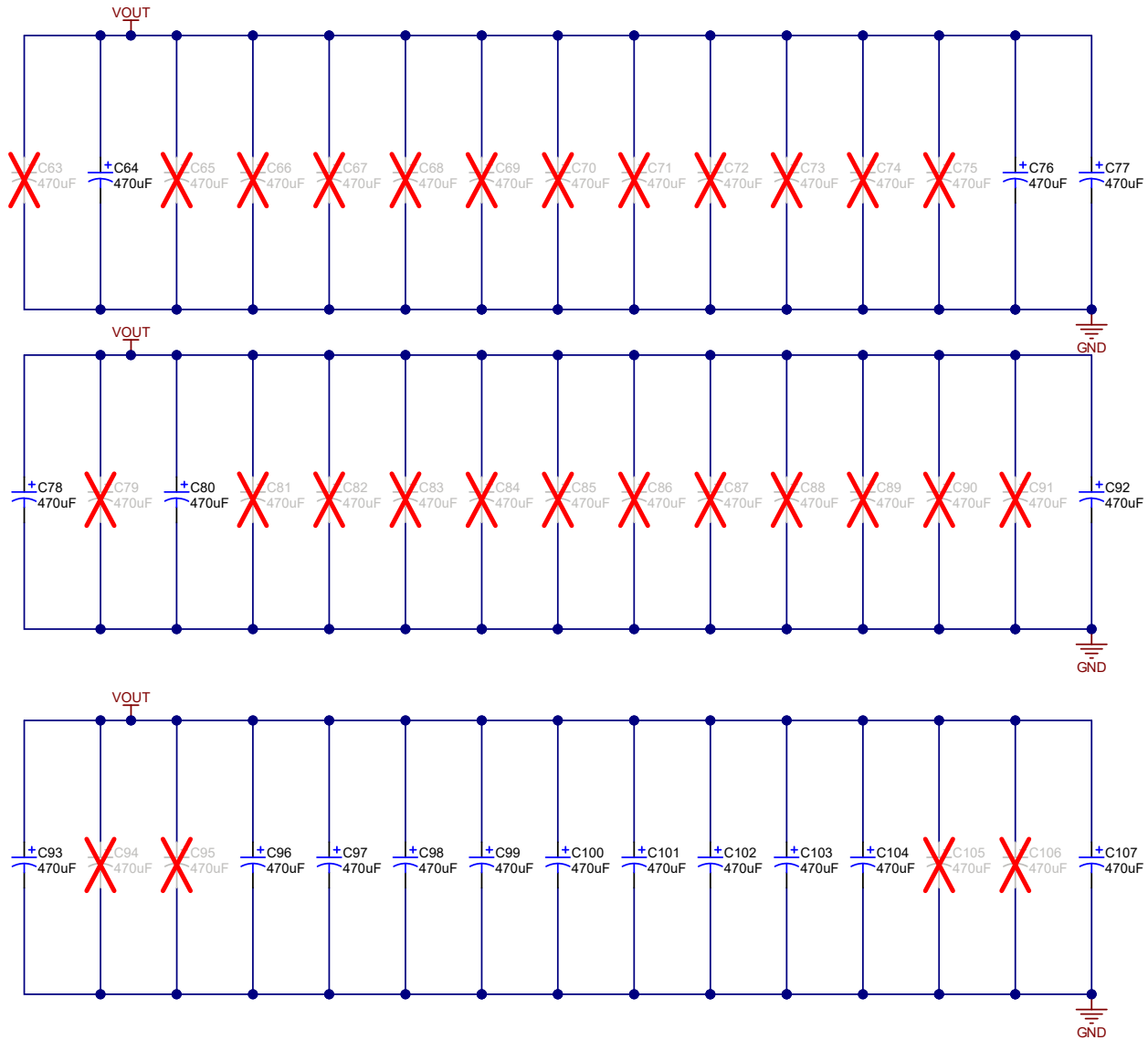


Figure 5-6. Mother Board Schematic (Page 3)

6 PCB Layouts

Figure 6-1 through Figure 6-9 show the PCB layout images of the multiple boards.

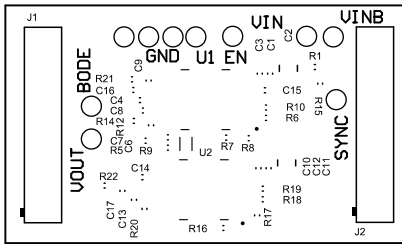


Figure 6-1. Controller Card Top Overlay

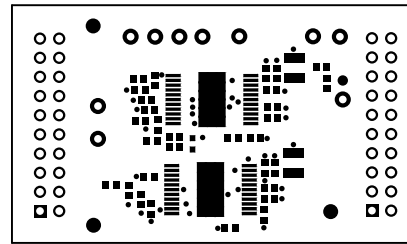


Figure 6-2. Controller Card Top Solder

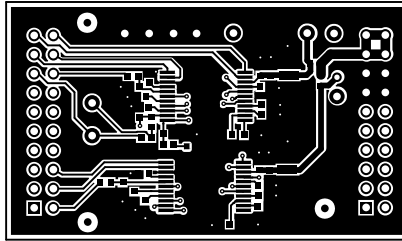


Figure 6-3. Controller Card Top Layer

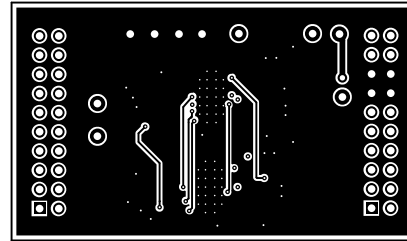


Figure 6-4. Controller Card Signal Layer 1

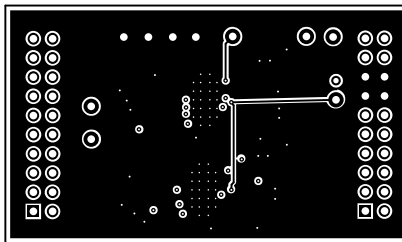


Figure 6-5. Controller Card Signal Layer 2

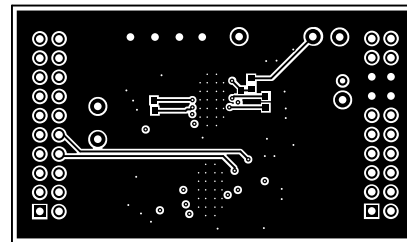


Figure 6-6. Controller Card Bottom Solder

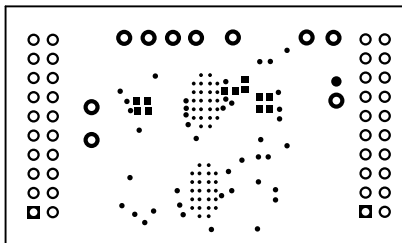


Figure 6-7. Controller Card Bottom Solder Mask

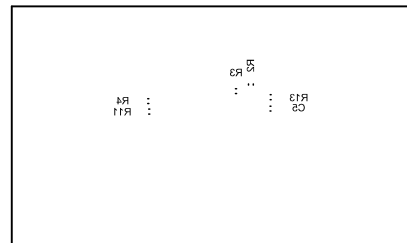


Figure 6-8. Controller Card Bottom Overlay

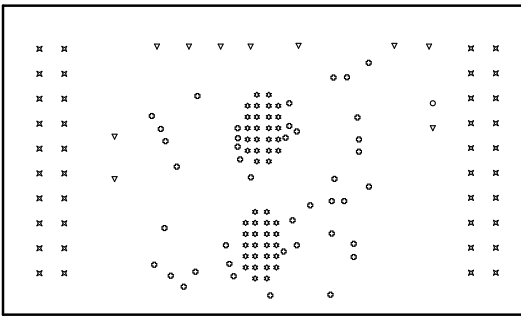


Figure 6-9. Controller Card Drill Drawing

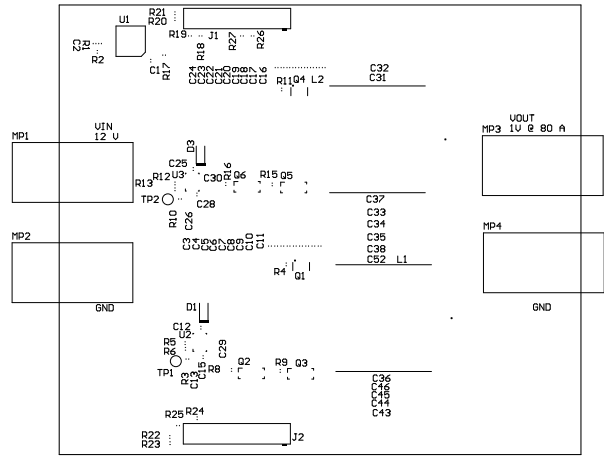


Figure 6-10. Daughter Card Top Overlay

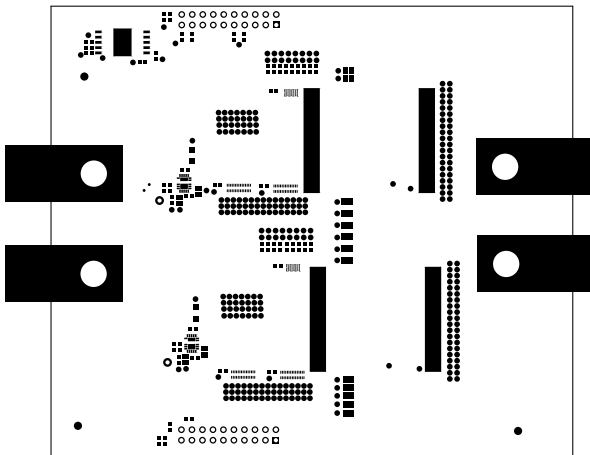


Figure 6-11. Daughter Card Top Solder

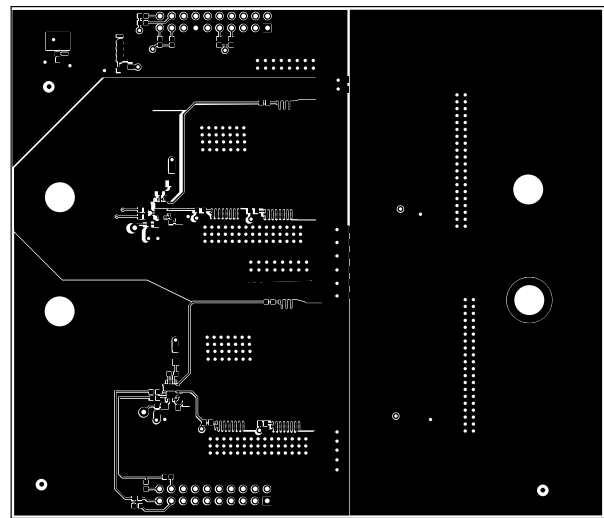


Figure 6-12. Daughter Card Top Layer

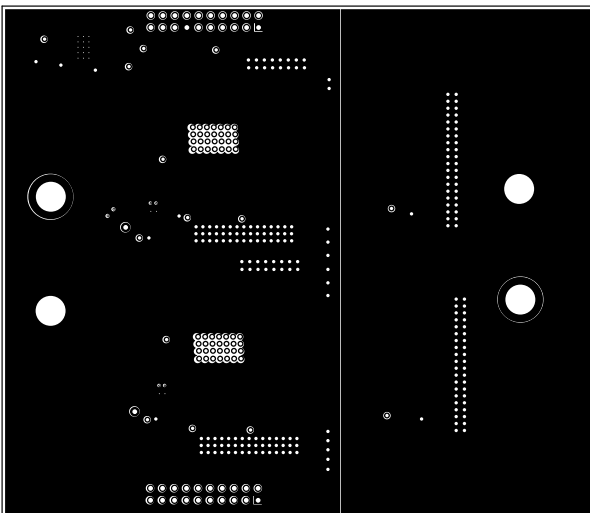


Figure 6-13. Daughter Card Signal Layer 1

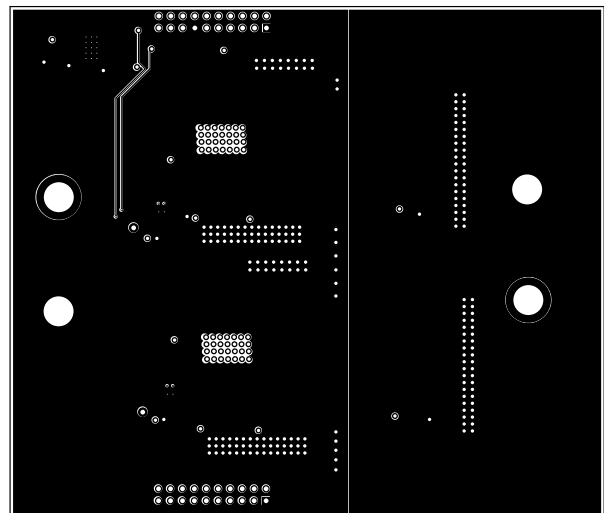


Figure 6-14. Daughter Card Signal Layer 2

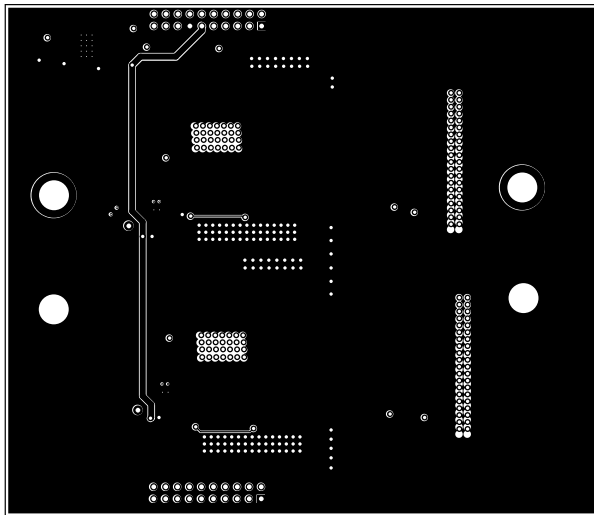


Figure 6-15. Daughter Card Signal Layer 3

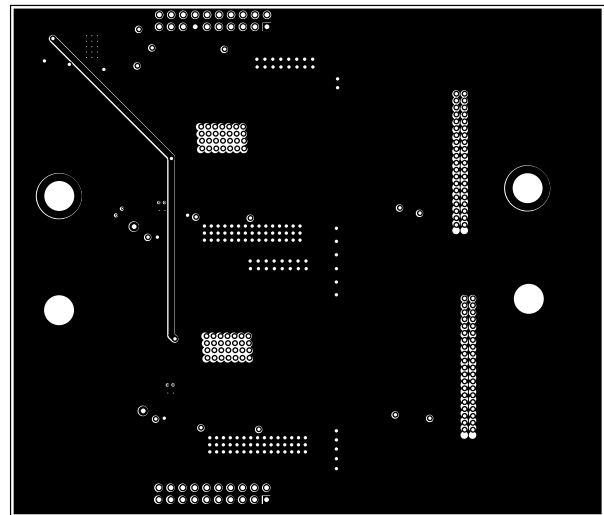


Figure 6-16. Daughter Card Signal Layer 4

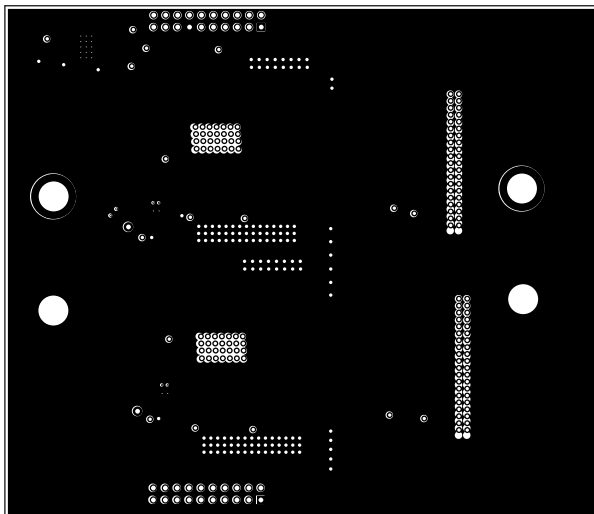


Figure 6-17. Daughter Card Signal Layer 5

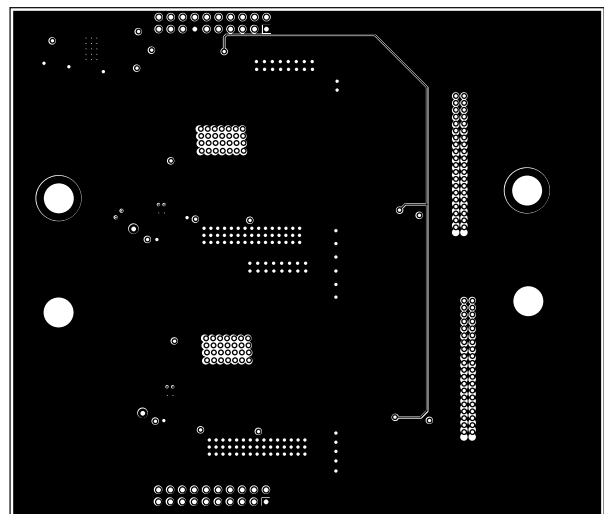


Figure 6-18. Daughter Card Signal Layer 6

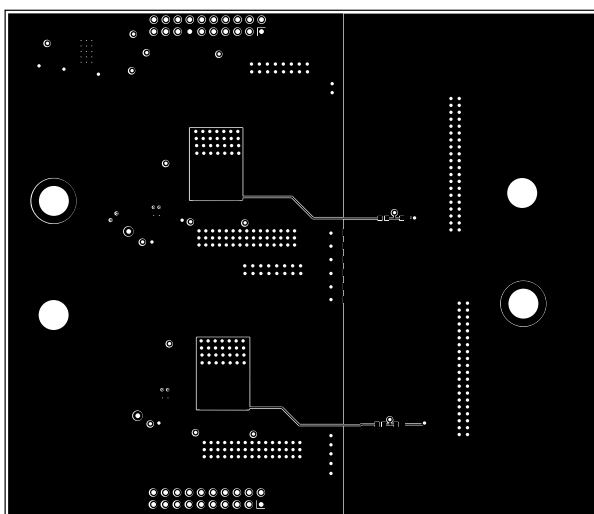


Figure 6-19. Daughter Card Bottom Layer

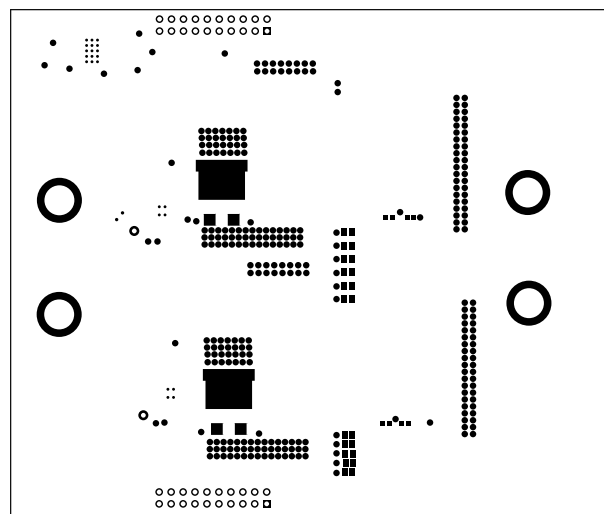


Figure 6-20. Daughter Card Bottom Solder

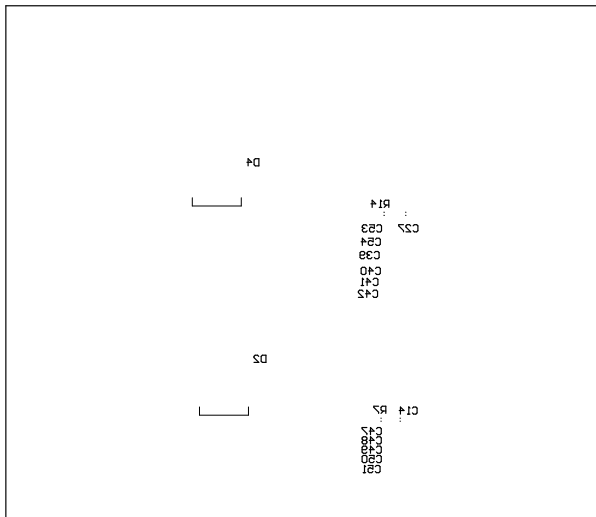


Figure 6-21. Daughter Card Bottom Overlay

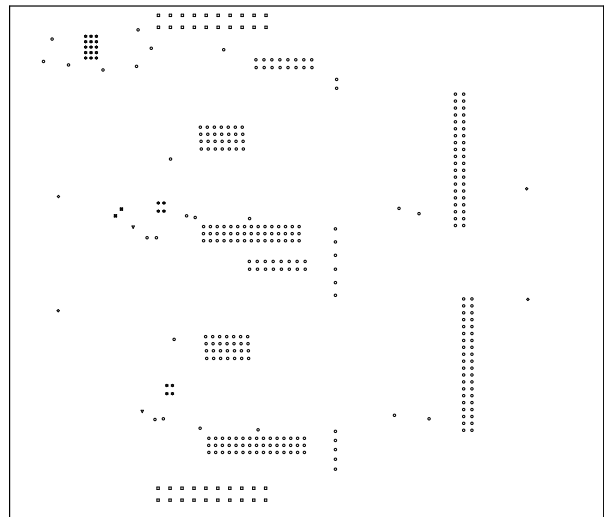


Figure 6-22. Daughter Card Drill Drawing

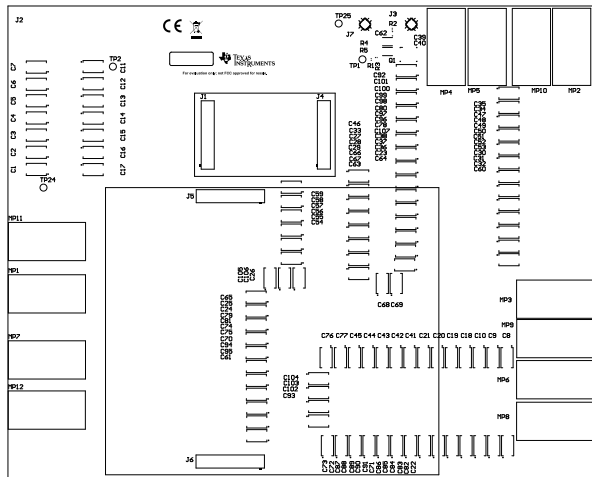


Figure 6-23. Mother Board Top Overlay

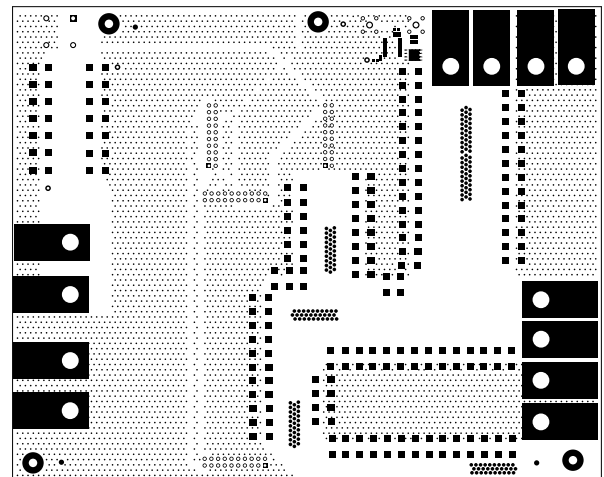


Figure 6-24. Mother Board Top Solder

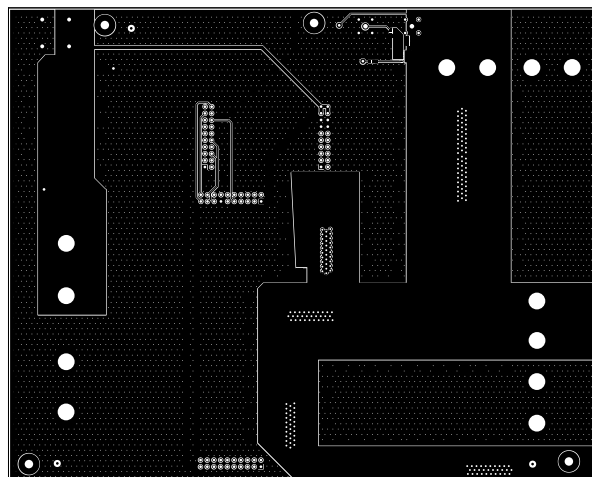


Figure 6-25. Mother Board Top Layer

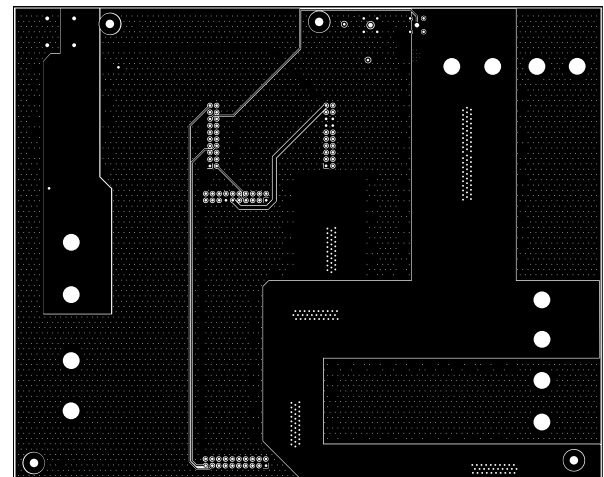


Figure 6-26. Mother Board Signal Layer 1

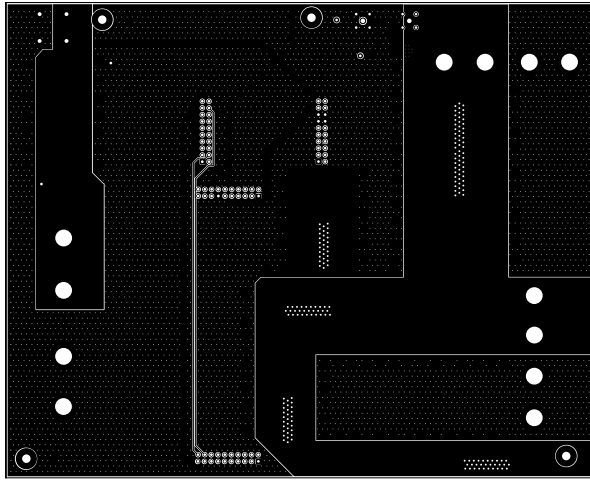


Figure 6-27. Mother Board Signal Layer 2

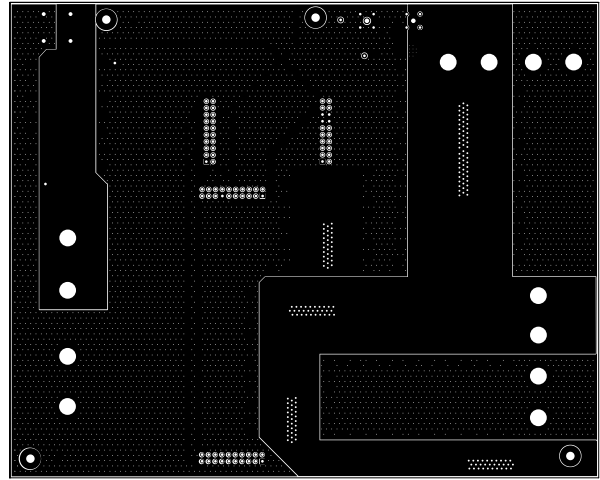


Figure 6-28. Mother Board Signal Layer 3

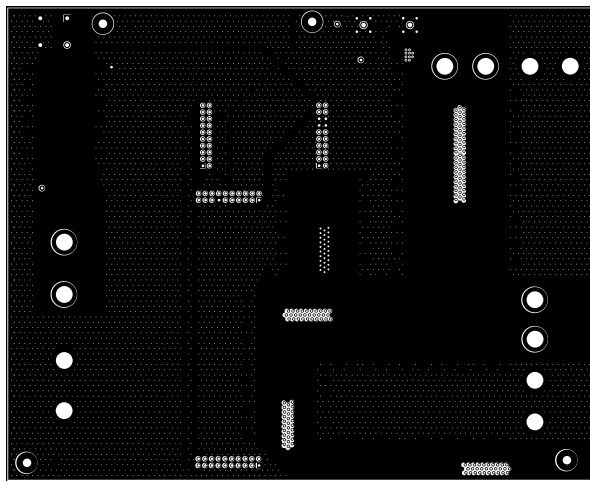


Figure 6-29. Mother Board Signal Layer 4

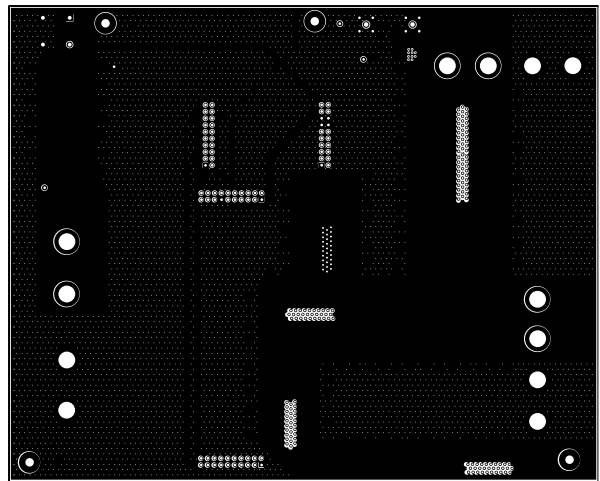


Figure 6-30. Mother Board Signal Layer 5

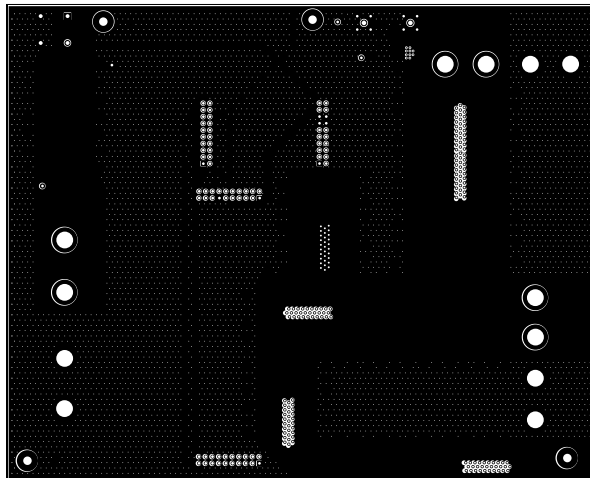


Figure 6-31. Mother Board Signal Layer 6

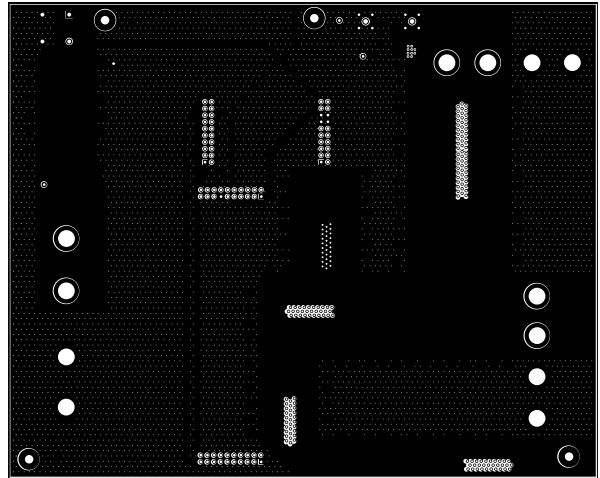


Figure 6-32. Mother Board Bottom Layer

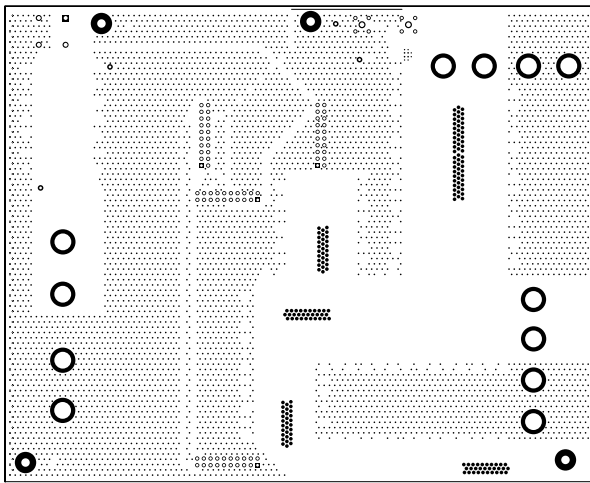


Figure 6-33. Mother Board Bottom Solder

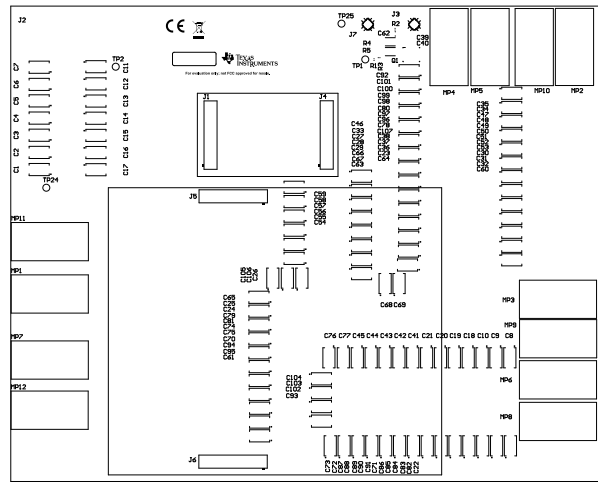


Figure 6-34. Mother Board Bottom Overlay

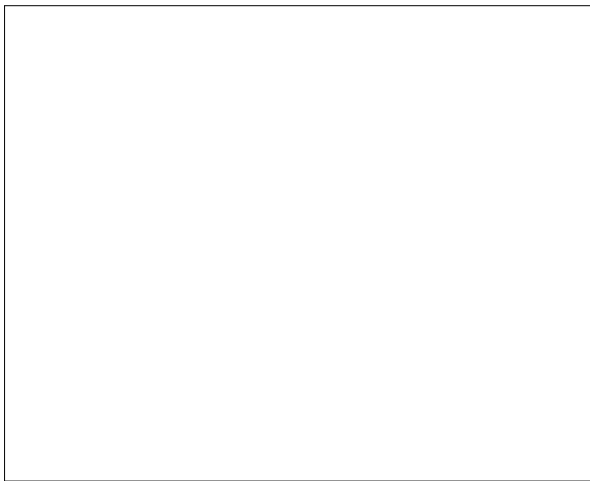


Figure 6-35. Bottom Overlay

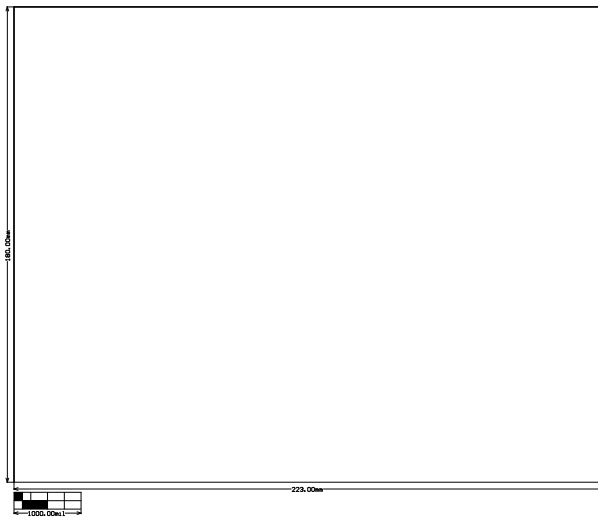


Figure 6-36. Board Dimensions

7 References

- Texas Instruments, [TPS7H500x-SP Radiation-Hardness-Assured 2-MHz Current Mode PWM Controllers](#), data sheet.
- Texas Instruments, [LMG1210 200-V, 1.5-A, 3-A Half-Bridge MOSFET and GaN FET Driver With Adjustable Dead Time for Applications up to 50 MHz](#), data sheet.

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