Application Note

Discrete Fault Detection Circuit for the TPS9261x-Q1

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ABSTRACT

Vehicle electronic fault detection is an important capability implemented in vehicles today to report what specific fault has occurred in an electronic system. This fault detection allows the vehicle to communicate the detected fault through LED indicators on the cluster, the onboard diagnostics port (OBD), and potentially over a wireless Wi-Fi®, 4GLTE, or 5G connection. Currently, the TPS9261x-Q1 family of devices features built in fault detection for open load (OL), short to ground (SG), short to battery (SB), and overtemperature (OT) faults that can occur on the LED driver output. However; there is only a single generic fault output to signal when any of the previously-listed faults have occurred in the system and therefore no way for the local MCU to distinguish what specific fault has taken place. This application note demonstrates a cost-effective method to implement a discrete fault detection circuit to report what specific fault has occurred on the TPS9261x-Q1 output to a local MCU.

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Trademarks

1 Introduction

Vehicle manufacturers greatly benefit from implementing circuits with detailed fault detection capabilities because this fault information can be shared with the driver through screen or LED indicators, with mechanics through the OBD port, and even to an OEM database or smart phone application over Wi-Fi, 4GLTE, or 5G wireless connections. The TPS9261x-Q1 family of LED drivers has the capability to detect an over temperature (OT), short to ground (SG), and open load (OL) or short to battery (SB) condition. However, there is only a single fault output to indicate if any of the above faults has occurred. This application note covers a method to detect these faults when implementing the TPS9261x-Q1 to drive off board LEDs.

2 TPS9261x-Q1 Fault Detection and Discrete Fault Detection Introduction

Before covering discrete fault detections, the device behavior during each fault condition must be understood.

Table 2-1 as published in the *TPS92611-Q1 Automotive Single-Channel Linear LED Driver* data sheet shows the expected behavior of the device during the four different fault conditions (OL,SB, SG, and OT).

Table 2-1. Fault Table With DIAGEN = HIGH

FAULT BUS STATUS	FAULT TYPE	DETECTION MECHANISM	CHANNEL STATE	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY
$\overline{\text{FAULT}}$ floating or externally pulled up	Open-circuit or short-to-supply	$V_{(IN)} - V_{(OUT)} < V_{(OPEN\_th\_rising)}$	On	$t_{(OPEN\_deg)}$	Constant-current pulldown	Device works normally with $\overline{\text{FAULT}}$ pin pulled low. Device sources $I_{(retry)}$ current when PWM is LOW. Device keeps output normal when PW M is HIGH.	Auto recover
	Short-to-ground	$V_{(OUT)} < V_{(SG\_th\_rising)}$	On	$t_{(SG\_deg)}$	Constant-current pulldown	Device turns output off and retries with constant current $I_{(retry)}$, ignoring the PWM input.	Auto recover
	Over-temperature	$T_J > T_{(TSD)}$	On or off	$t_{(TSD\_deg)}$	Constant-current pulldown	Devices turns output off.	Auto recover
Externally pulled low	Device turns output off						

When the device PWM pin input is high (output is on) during an open load or short to battery condition, the TPS9261x-Q1 detects an open load or short to battery has occurred and pull the fault pin low. The device continues to try and source the set current to the output every time PWM is set high. However, little to no current flows through the device due to the output voltage being equal to the input voltage (battery). In a short to battery condition, it is clear that the output voltage equals the battery but during an open load condition, the output also equals battery due to the constant current control of the TPS9261x-Q1. With a high impedance on the output, the TPS92611x tries to source the designed output current but because the output has infinite impedance, the output voltage is limited to the input voltage of the device. When PWM is set low and DIAG EN pin is high, the device sources a 1-mA $I_{(retry)}$ current to check if the open load or short to battery condition has been removed.

During a short to ground condition, when the PMW pin is high, the TPS9261x-Q1 detects a short to ground and pull the fault pin low. Before the fault is reported, the output voltage drops to approximately 0 V due to the TPS9261x-Q1 output sourcing the designed current into ground or close to 0 Ω. The output then is disabled once the fault is detected after $t_{(SG\_deg)}$ and the device tries to source the 1-mA $I_{(retry)}$ current, regardless of the PWM pin, to detect if the short to GND has been removed.

Lastly, for an overtemperature condition, the device simply shuts off the output regardless of the state of the PWM pin. In this case, the output is disabled and there is no voltage on the output due to no current flowing from the device.

2.1 Discrete Fault Detection

Now that the expected behavior of the TPS9261x-Q1 is understood along with the condition of the OUT pin or output of the device, the discrete fault detection circuit must consider the fault behavior and expected output current or voltage during each fault condition. Figure 2-1 shows the discrete fault detection circuit block diagram.

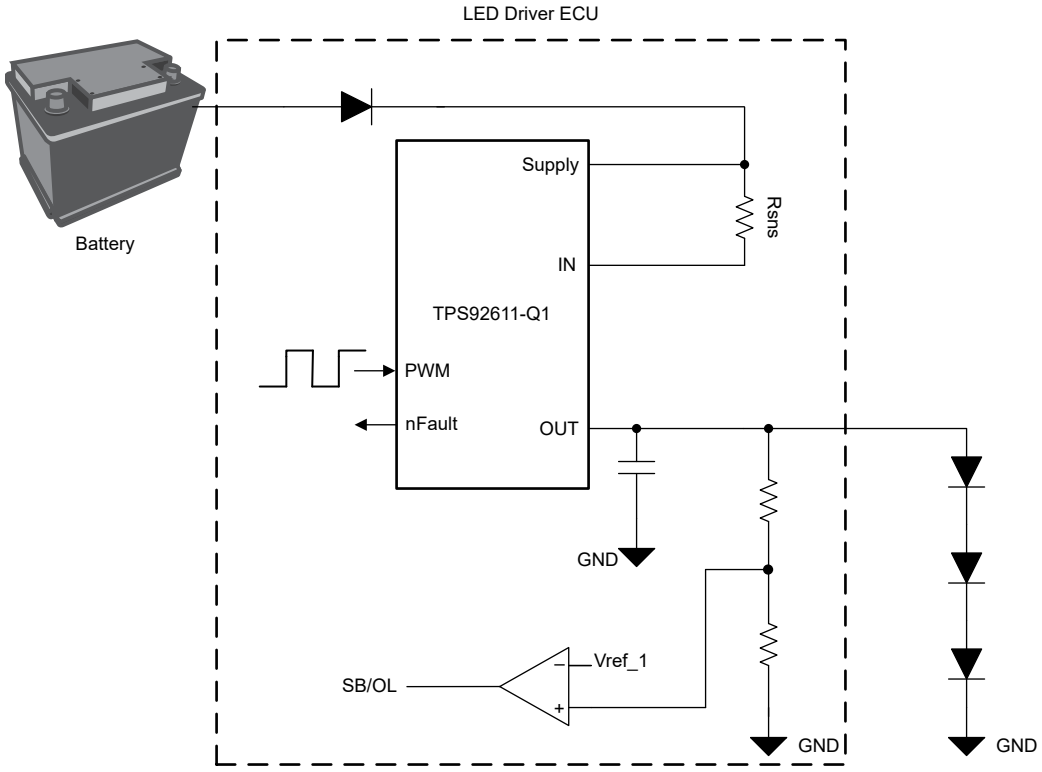

Figure 2-1. Discrete Fault Detection Block Diagram

2.2 Open Load vs Short-to-Battery Detection

The main approach for detecting between open load (OL) and short to battery (SB) is to measure the output voltage when the device output is disabled as shown in Figure 2-1. To do this, a voltage divider is required on the output of the TPS9261x-Q1 to verify that the comparator input is within a reasonable range and is not damaged. Remember, this pulls the output low in an open-load condition. Therefore, when a SB has occurred, the output voltage equals the battery, but in an OL condition, the output is pulled to ground. This now creates a detectable logical difference between the SB and OL conditions when the TPS9261x-Q1 output is disabled as shown in Figure 2-2.

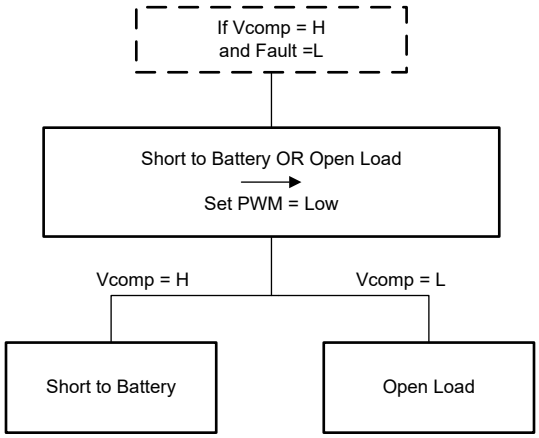

Figure 2-2. Short to Battery (SB) or Open Load (OL) Logic Flowchart

If the fault pin is initially triggered and the comparator output V_{comp} is HIGH, then a SB or OL has occurred. Thus, to differentiate between the two faults, the PWM pin must be pulled LOW. Then, if Vcomp stays HIGH a short to battery has occurred and if Vcomp is LOW an open load fault has occurred. However, if DIAGEN is pulled high, the device sources the 1-mA $I_{(retry)}$ current preventing the output from ever being disabled in either OL or SB conditions. Nevertheless, the $I_{(retry)}$ current can be compensated for by the voltage divider on the output. The resistor values can be selected so that when the 1-mA current is sourced by the LED driver, the voltage on the output is lower than the battery voltage during an OL condition. Now the comparator can be configured to compare the output voltage and the voltage expected during OL conditions when $I_{(retry)}$ is sourced through the resistive divider. Additionally, the fault pin is now released during an OL condition after the PWM pin is pulled low and the $I_{(retry)}$ current is sourced due to the output voltage dropping below battery voltage and causing the $V_{in} – V_{out}$ to be greater than $V_{(OPEN\_th\_rising)}$ (OL, SB fault condition from Table 2-1). Figure 2-3 and Figure 2-4 show the SB and OL conditions with the 1-mA $I_{(retry)}$ when PWM is LOW.

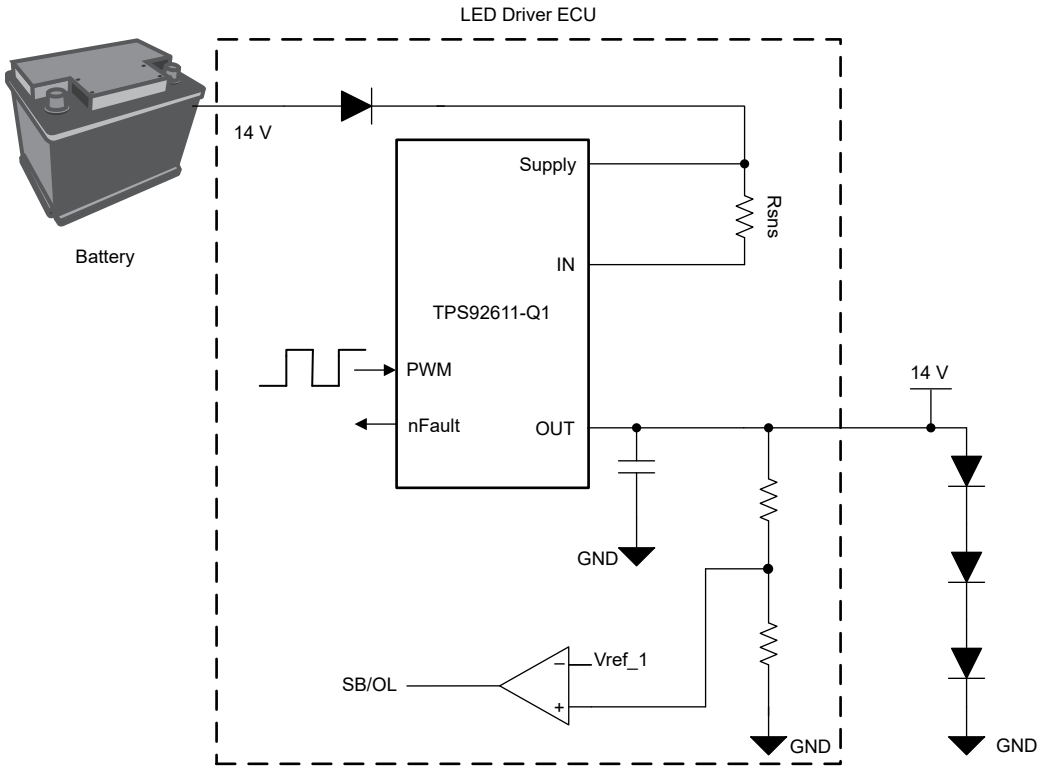

Figure 2-3. Short to Battery (SB) Condition

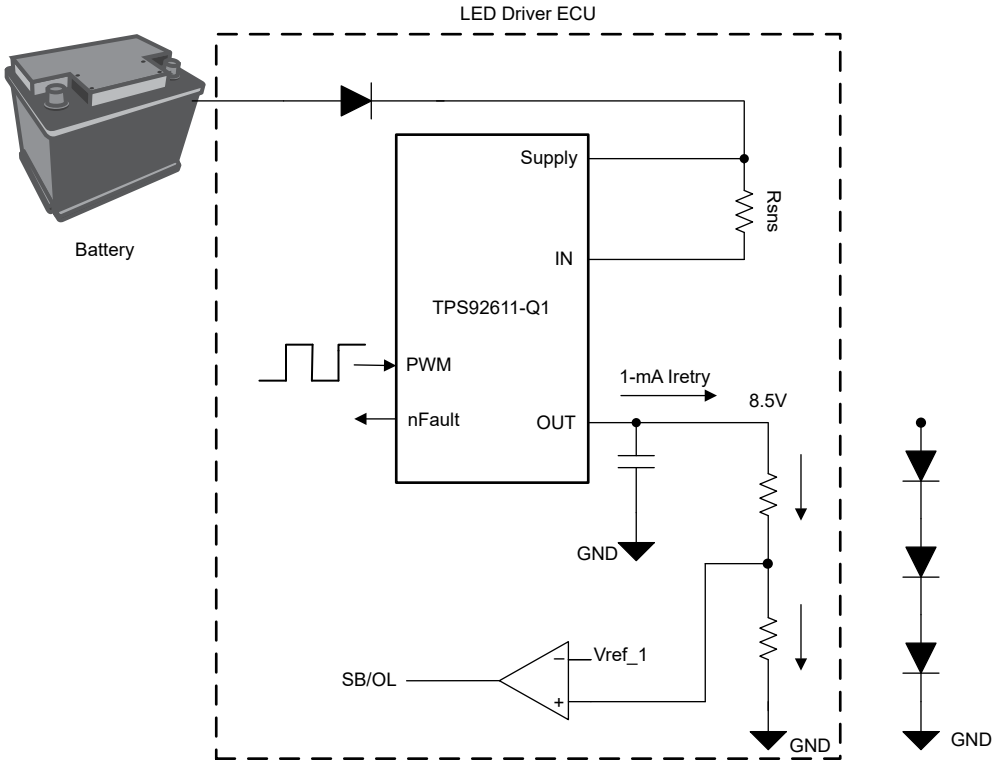

Figure 2-4. Open Load (OL) Condition

Another method to avoid $I_{(retry)}$ completely is to disable the OL and SB fault detection by pulling the DIAGEN pin LOW. However, the device no longer pulls fault LOW in an OL or SB condition. This can be valid due to the comparator detecting this fault but when the DIAGEN pin is set HIGH the fault pin adds an additional level of robustness to the fault detection scheme.

2.3 Short to Ground vs Overtemperature Detection

The next faults to detect are short-to-ground (SG) and overtemperature (OT) conditions. Figure 2-5 shows the SG condition.

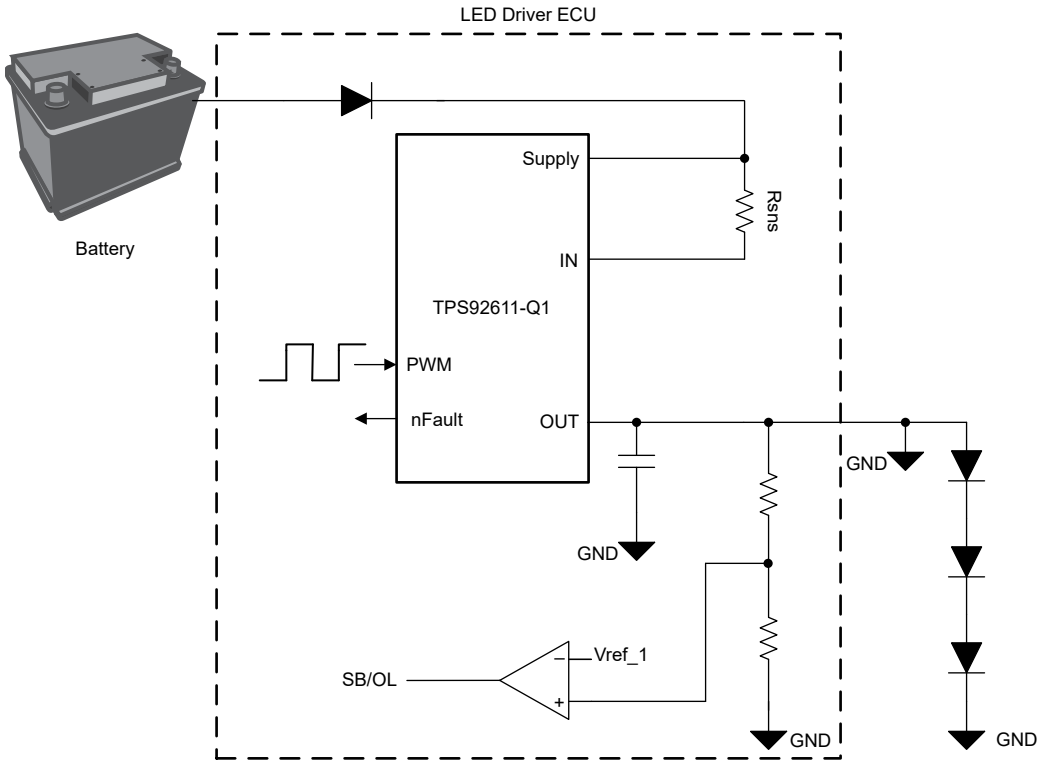

Figure 2-5. Short-to-Ground (SG) Condition

In both SG and OT conditions, the output is disabled and the output voltage either drops to 0 V if either fault occurs when PWM is high, or stays at 0 V when transitioning the PWM pin from low to high during either fault condition. Therefore, the output voltage comparator does not help distinguish between the SG and OT faults. However, the devices built-in detection of SG and OT detects both faults and pulls the fault pin LOW. To distinguish between a SG and OT condition, the local MCU can simply adjust the PWM pin control of the TPS9261x-Q1 output. If the fault pin is pulled low by the LED driver but the comparator output has not triggered a SB or OL condition, the MCU can logically conclude that either a SG or OT condition has occurred. Next, the MCU can hold the PWM pin low for 300 ms to 500 ms to check if the LED driver has overheated. By pulling the PWM pin low, the MCU allows the TPS9261x-Q1 time to cool off and avoid any self-heating. If an OT condition has occurred, during the 200-ms to 500-ms wait time, the LED driver clears the fault after the 15°C hysteresis has been cleared (specified in the TPS9261x-Q1 data sheet). The MCU can then drive the PWM pin high at the dedicated PWM frequency and duty cycle to monitor if the fault pin is triggered again due to the LED driver overheating. Figure 2-6 shows the logic flowchart for distinguishing between SG and OT.

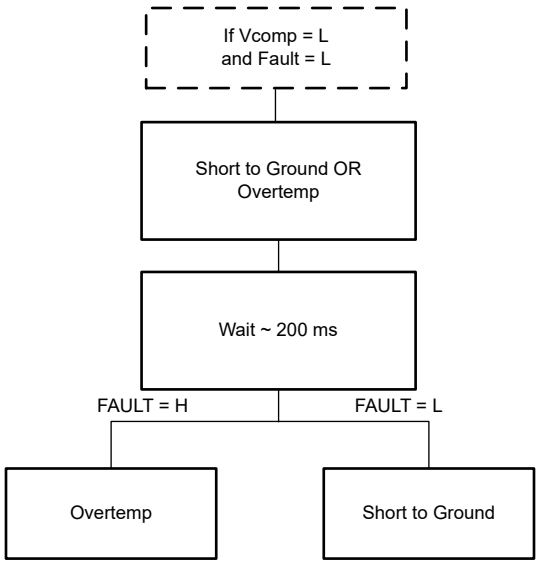

Figure 2-6. Short to Ground (SG) or Overtemperature (OT) Logic Flowchart

If the PWM pin is held HIGH and the comparator output (V_{comp}) is LOW while the fault pin is LOW then a SG or OT has occurred. After the MCU holds the PWM pin low for 200 ms as shown in Figure 2-6, the fault pin state can be checked to determine if an OT event has occurred. If there is a SG, the fault pin stays low unless the short has been cleared. Therefore, some simple logic and control of the PWM pin can be implemented to detect if a SG or OT condition has occurred. Testing can be performed to understand what conditions cause the TPS9261x-Q1 to overheat.

2.4 Fault Detection Logic Summary

Figure 2-7 illustrates final flow of logic of the fault detection circuit.

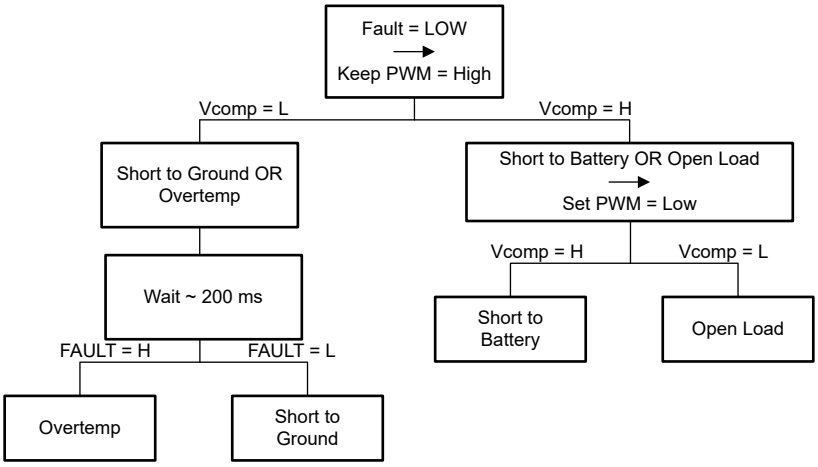

Figure 2-7. Discrete Fault Detection Logic Flowchart

As Figure 2-7 shows, the comparator output (V_{comp}), is used to distinguish if a SG, OT or SB, OL has occurred. If a SB or OL has occurred, V_{comp} can be used to further distinguish between the two after PWM is pulled LOW. For SG, OT conditions, the fault pin is used along with the PWM pin to distinguish between a SG or OT fault.

3 Discrete Fault Detection Circuit Details

The discrete fault detection circuit utilizes the ATL431LI-Q1 device as a comparator to monitor the TPS9261x-Q1 output voltage. The ATL431LI-Q1 is a high bandwidth low I_Q programmable shunt regulator that can act as a comparator in open loop mode. Additionally, the device has an internal reference voltage of 2.5 V and works well across temperature providing an accurate output voltage measurement. For more information on the ALT431LI-Q1 performance across temperature, see *Using the TL431 for Undervoltage and Overvoltage Detection* application note. The ATL431LI-Q1 output (V_{comp}) is used to differentiate between OL, SB, and SG or OT conditions. Figure 3-1 illustrates the initial schematic with the fault detection circuit added on to the TPS9261x-Q1.

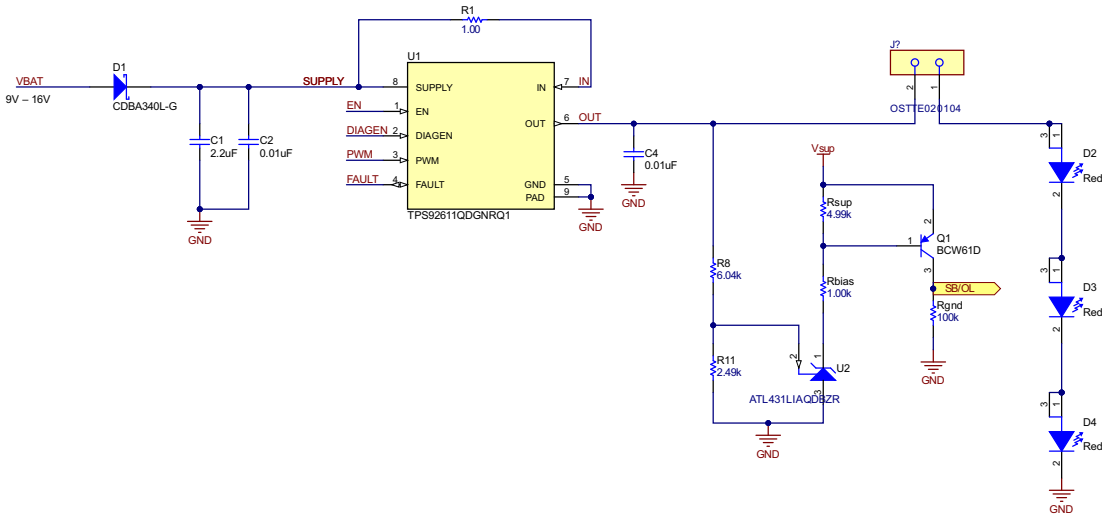

Figure 3-1. Discrete Fault Detection Schematic

A resistor divider must be used to properly divide the voltage going into the ATL431LI-Q1 from the output of the TPS9261x-Q1. This is to properly compare the OUT voltage to the reference voltage. In addition, this resistor ladder creates the trip point (where the comparator output changes). A trip point of 8.5 V was used for the tests in Section 3.1 to Section 3.4. To verify the resistor ladder behaves as expected, the total series resistance (R_{total}) of the resistive divider R8 and R11 must be approximately 8.5 kΩ. Due to the $I_{(retry)}$, a R_{total} that is too large causes the output and input voltages to be close to equal and therefore the ATL431LI-Q1 comparator does not trigger. R_{sup} and R_{bias} are used in accordance to *Using the TL431 for Undervoltage and Overvoltage Detection* application note to verify that the BJT has an appropriate voltage drop and that the ATL431LI-Q1 is not sinking excess current. R_{gnd} is utilized to pullup the SB, OL output to V_{sup}. Additionally, a BJT is used to verify that the ATL431LI-Q1 output swings from Vsup (3.3 V) to 0 V as described in the previously-referenced *application note*. Table 3-1 documents the logic truth table associated with the fault detection circuit. Each unique outcome is highlighted to show the logic for a microcontroller to differentiate between each fault scenario.

Table 3-1. Fault Detection Circuit Truth Table

Condition	PWM	nFault	Comparator Output (V_{comp})
Normal Operation	L	H	L
	H	H	L
Short to GND, Over Temperature	L	L	L
	H	L	**L**
Short to V_{bat}	**L**	L	**H**
	H	L	H
Open Load	**L**	H	**L**
	H	L	H

3.1 Simulation

The fault detection circuit was created on PSpice® and an independent voltage source was used to simulate different voltage conditions on the TPS9261x-Q1 output. Figure 3-2 shows the circuit when the TPS9261x-Q1 output voltage is below the trip point of 8.5 V.

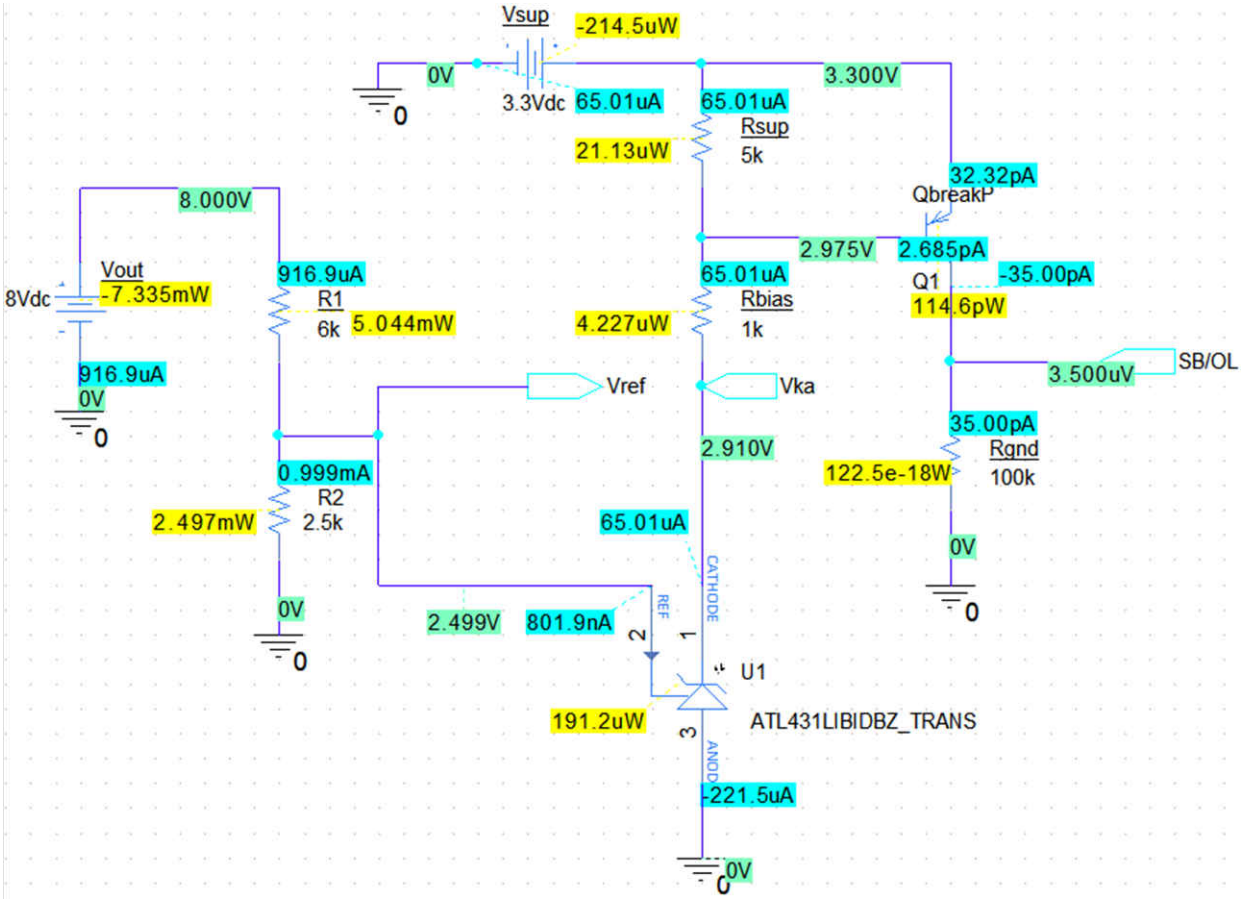

Figure 3-2. Simulation With TPS9261x-Q1 Vout Below the Trip Point

An 8-V voltage was applied to the fault detection circuit and with accordance to the truth table in Table 3-1. A proper LOW output is shown at SB/OL. Figure 3-3 shows the circuit when a voltage above the trip point of 8.5 V is present.

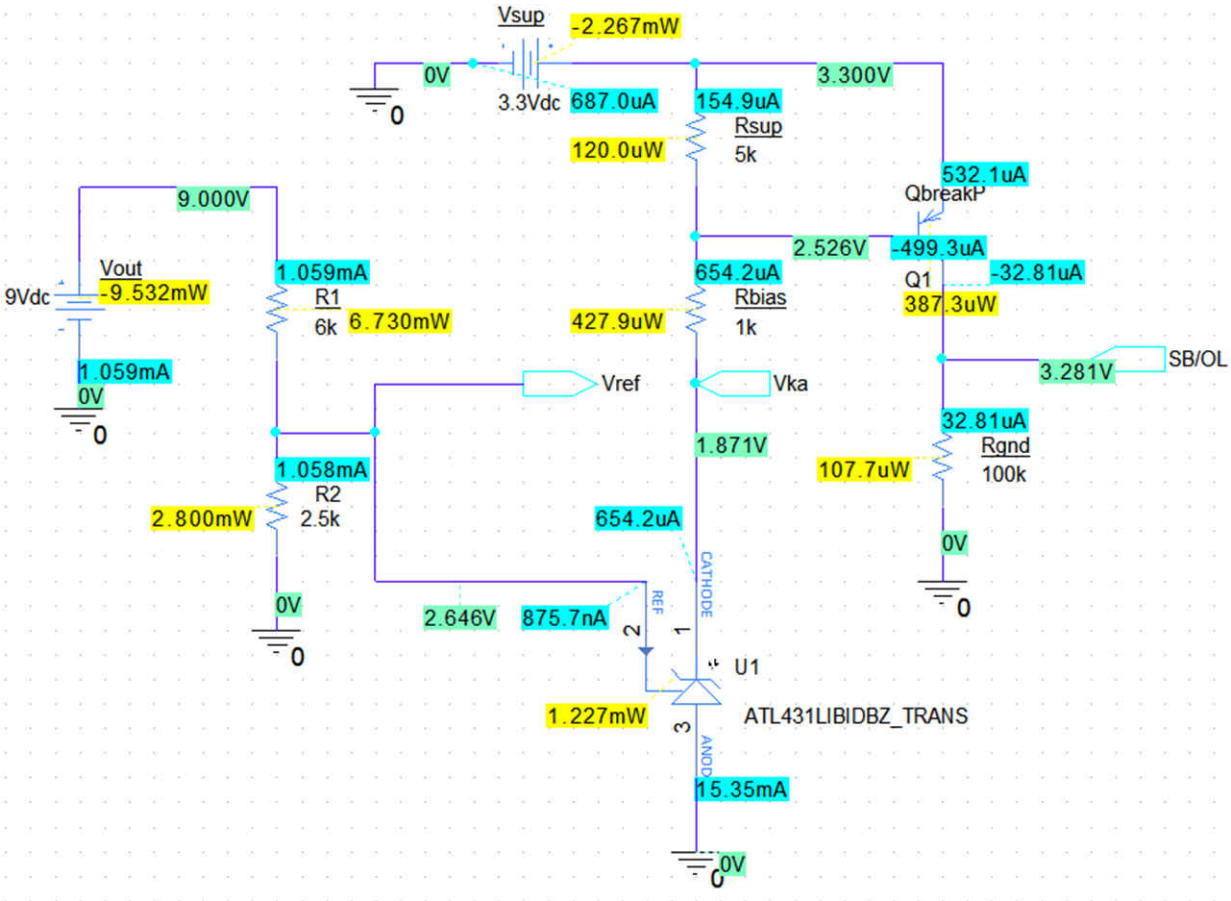

Figure 3-3. Simulation With TPS9261x-Q1 Vout Above the Trip Point

A voltage of 9 V was applied to the fault detection circuit and with accordance to Table 3-1 the Vcomp output is HIGH as shown on SB/OL.

3.2 PCB Implementation

Figure 3-4 illustrates the PCB layout in a 2D view and Figure 3-5 utilizes a 3D view.

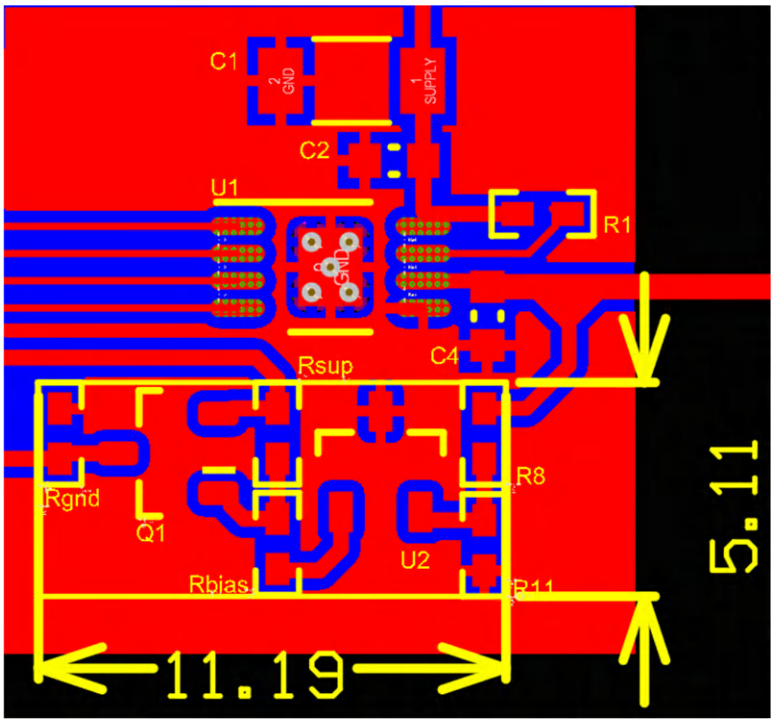

Figure 3-4. 2D Fault Detection Circuit Layout

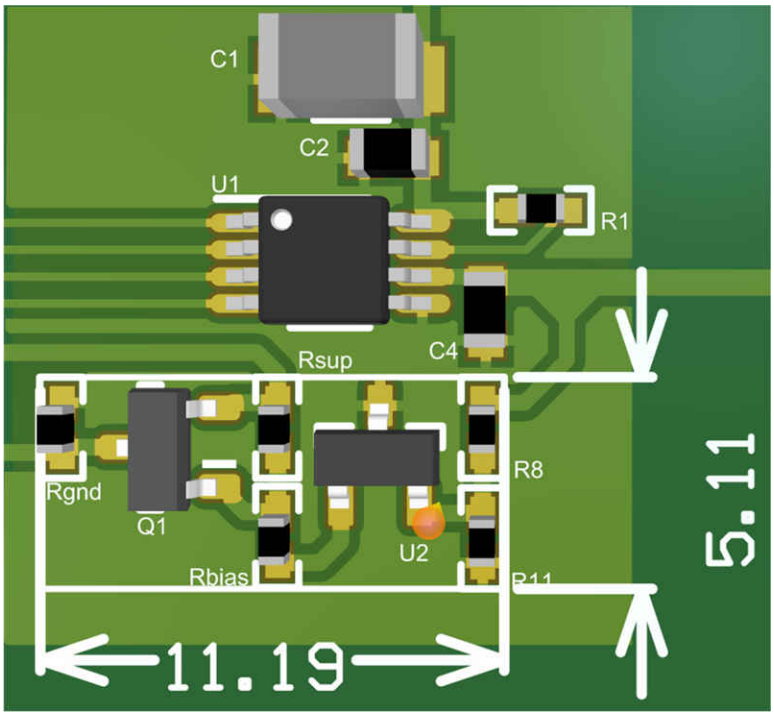

Figure 3-5. 3D Fault Detection Circuit Layout

The fault detection circuit was added in conjunction to the TPS92611-Q1 EVM and highlighted in silk screen on the layout. As shown in the layout, the footprint for the fault detection circuit is compact, only requiring an area of 11.19 mm × 5.11 mm (440.55 mil × 201.18 mil).

3.3 Test Setup

The proposed fault detection circuit was tested utilizing the TPS92611-Q1 and ATL431LI-Q1 EVMs. Figure 3-6 illustrates the block diagram of how the boards were connected for testing.

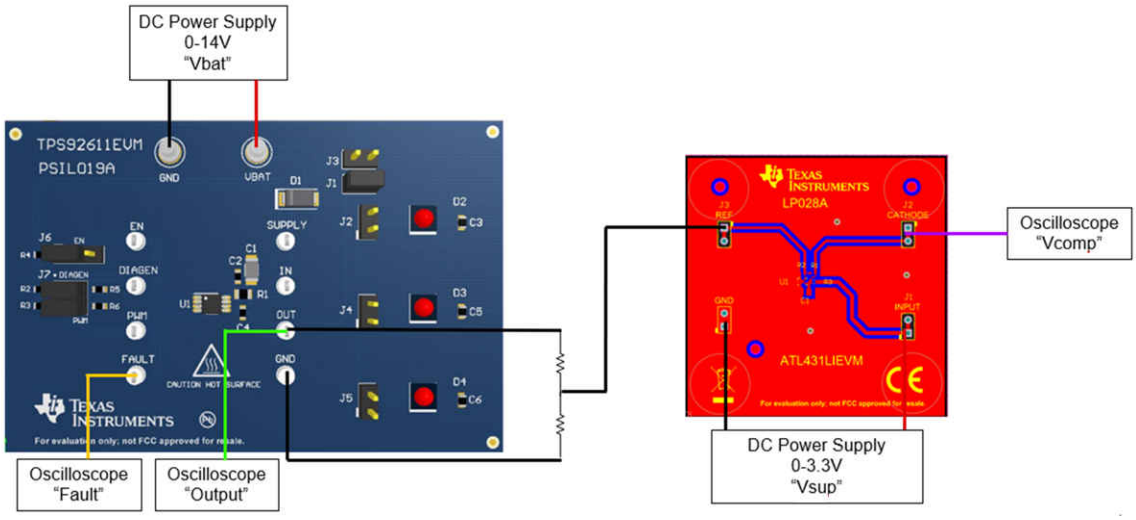

Figure 3-6. Test Setup Block Diagram

The two EVMs were connected through an external resistor ladder and the proper supplies were utilized are shown. Additionally, the test points taken are labeled as shown in the Figure 3-7. The EVMs had multiple jumpers that allowed the testing of each fault condition. For more information on the TPS92611-Q1 EVM, see the *TPS92611-Q1 Evaluation Module* and *ATL431 Adjustable Shunt Regulator EVM* user guides.

Figure 3-7 illustrates how the test setup was utilized during testing.

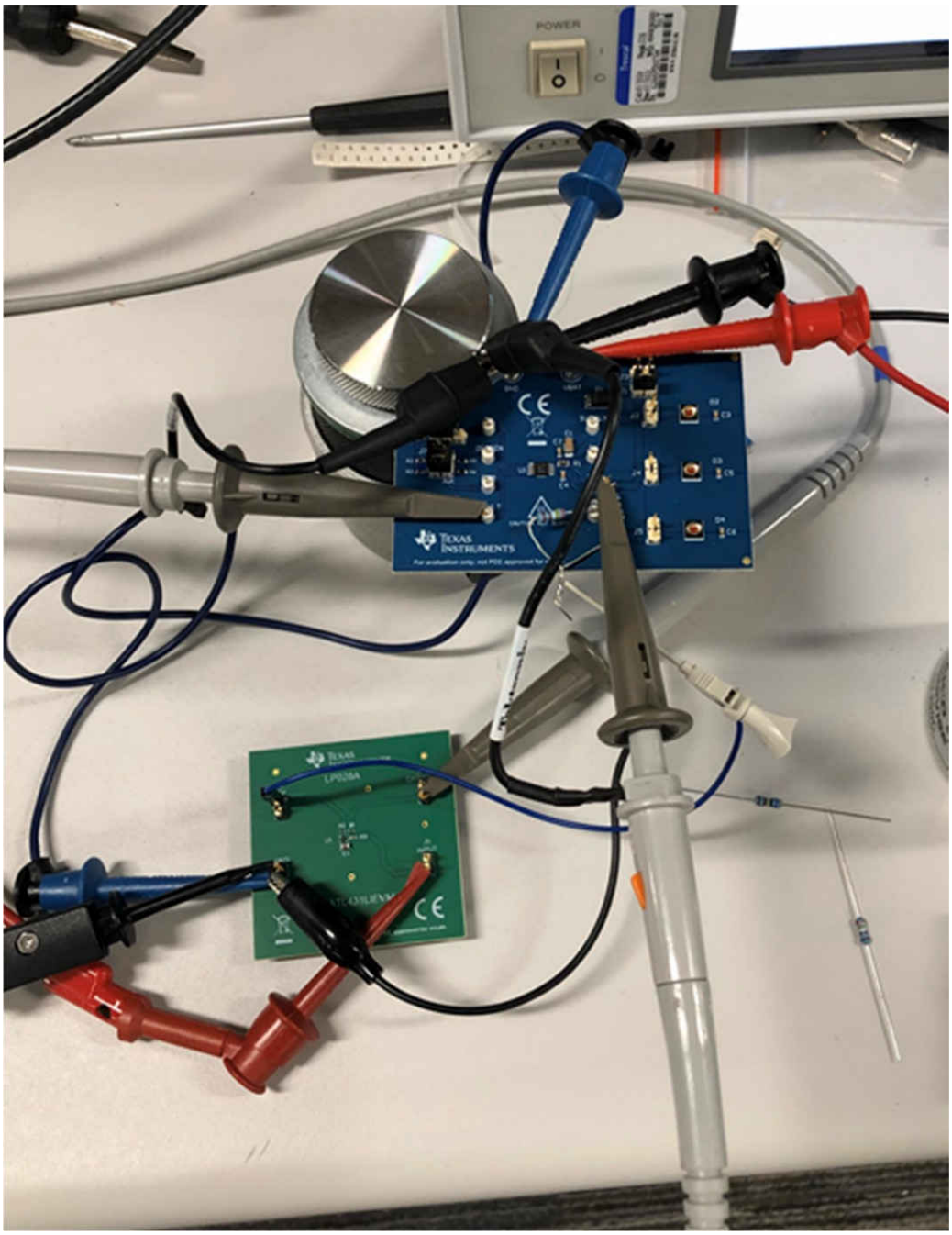

Figure 3-7. Lab Test Setup

In the test setup, the Q1 BJT was not included on the cathode of the ATL431LI-Q1 device so the V_{comp} results are going to be inverted of what Figure 2-7 and Table 3-1 show. In addition, the output for low is about 2.5 V instead of ground and the output for high is still a standard 3.3 V. Table 3-2 is included with an inverted V_{comp} to assist the comparison of the truth table and scope shots provided.

Table 3-2. Fault Detection Circuit Truth Table Without Q1 BJT

Condition	PWM	nFault	Comparator Output (V_{comp})
Normal Operation	L	H	L
	H	H	L
Short to GND, Overtemperature	L	L	L
	H	L	**H**
Short to V_{bat}	**L**	L	**L**
	H	L	H
Open Load	**L**	H	**H**
	H	L	H

Testing was conducted under multiple circumstances to verify that the fault detection circuit behaved as expected. Figure 3-8 illustrates the device under normal operation with the PWM pin on.

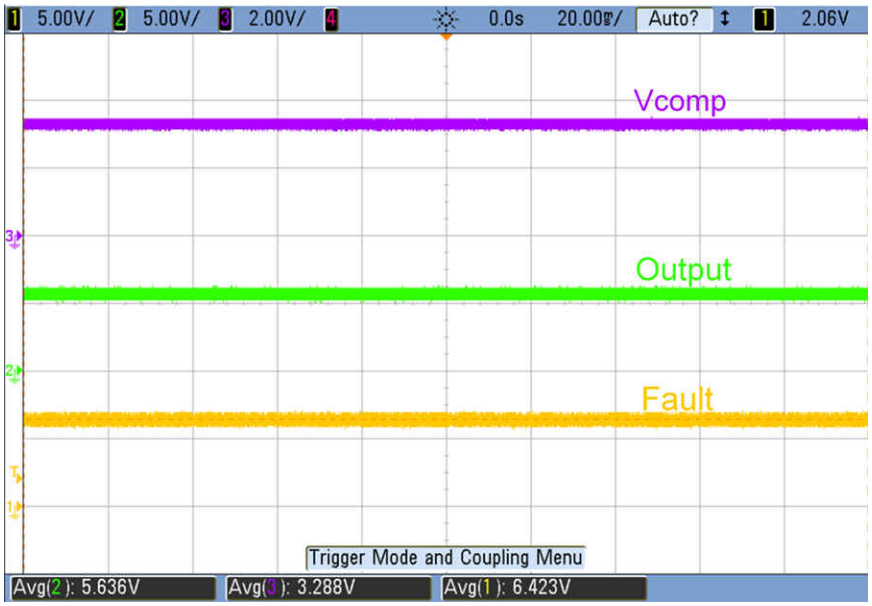

Figure 3-8. Normal Operation

Under normal operation the fault pin stays high. With three LEDs connected to the TPS92611-Q1 there is a constant output of approximately 5.4 V. Additionally, due to no BJT in the testing circuit the V_{comp} stays high. Figure 3-9 illustrates device behavior when a SG fault occurs.

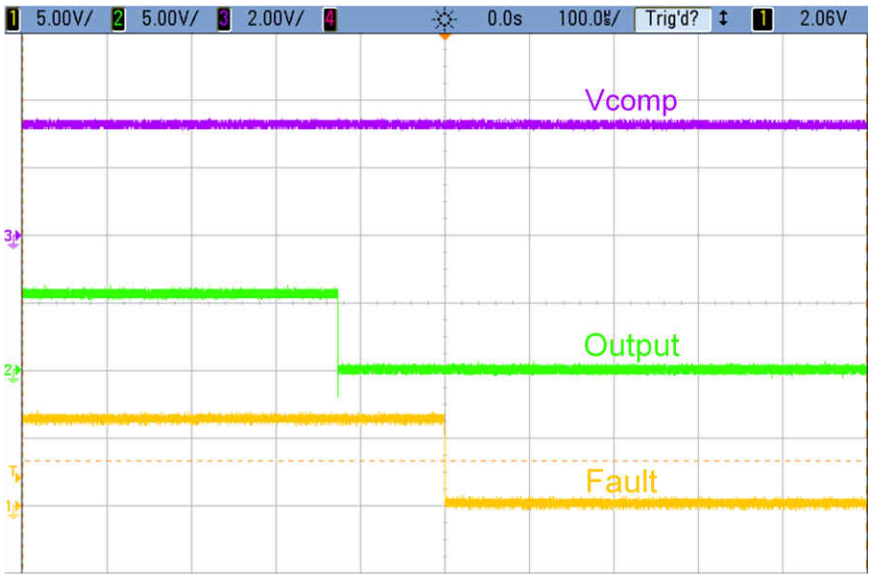

Figure 3-9. Short-to-Ground Fault

When the SG condition is triggered with PWM high the output drops to ground followed by the fault pin after $t_{(SG\_deg)}$. Furthermore, the V_{comp} stays high in this condition. Figure 3-10 illustrates device behavior when an open load condition is initially triggered.

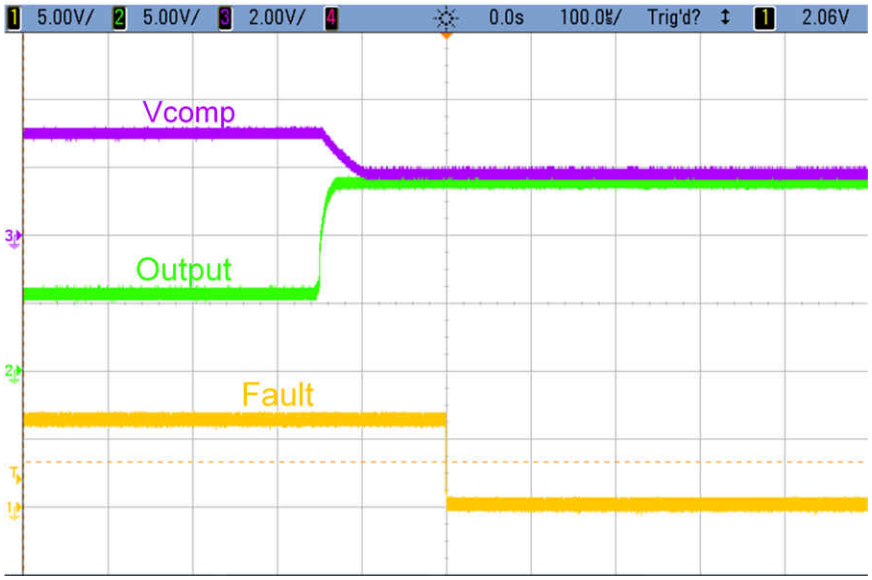

Figure 3-10. Open Load Fault

When the OL condition is triggered with PWM high, the output rises to approximately 14 V due to the TPS92611-Q1 trying to drive 100 mA into infinite impedance. Additionally, the V_{comp} drops to low state with the fault triggering low after $t_{(OPEN\_deg)}$. Figure 3-11 illustrates when the PWM is pulled low in the open load condition.

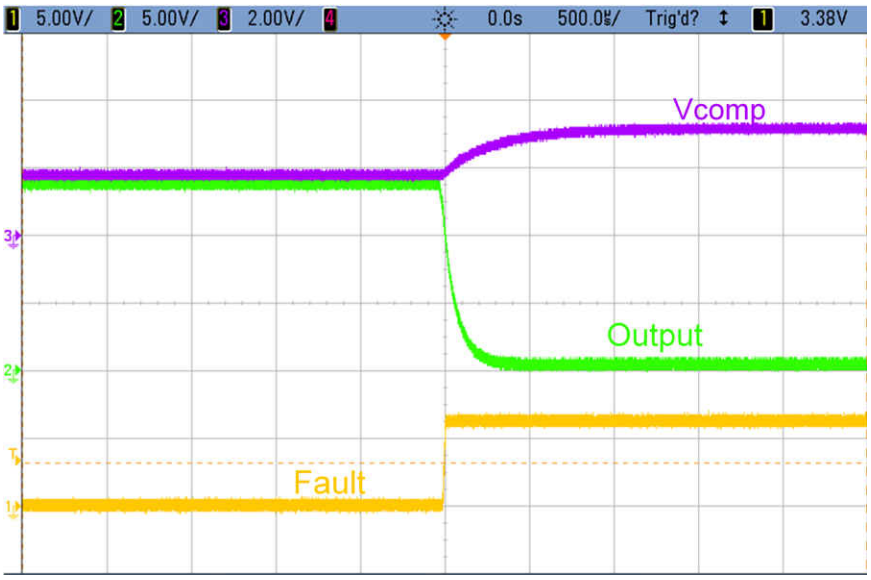

Figure 3-11. Open Load Condition When PWM is Set Low

When the PWM is pulled low during an OL condition, the fault clears immediately. Additionally, the V_{comp} returns to a high state with the output dropping to 0 V. Figure 3-12 illustrates device behavior when a SB condition is initially triggered.

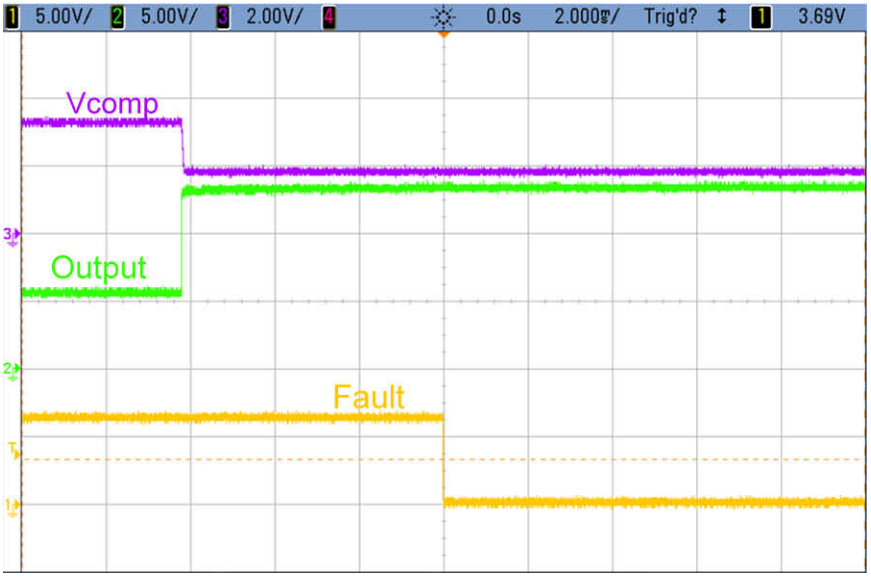

Figure 3-12. Short to Battery Fault Condition

When the SB condition is initially triggered with PWM high, the output increases to the battery voltage (14 V) and V_{comp} goes low. Moreover, the fault triggers low following $t_{(OPEN\_deg)}$. Figure 3-13 illustrates when the PWM is set low in the SB condition.

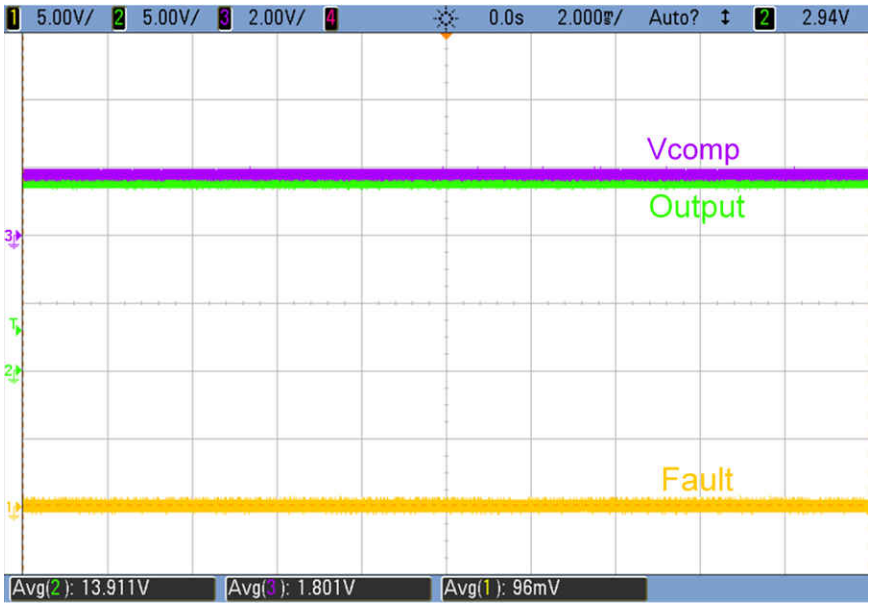

Figure 3-13. Short to Battery Fault When PWM is Set Low

When the PWM is pulled low in the SB condition, nothing changes. V_{comp} stays in a high state, the output remains at the supply of 14 V, and the fault remains triggered low. All tests follow Table 3-2 and verify the behavior of the discrete fault detection circuit.

3.4 Thermal Testing for Overtemperature Conditions

To test the time needed to wait for the TPS92611-Q1 to cool after an OT condition, a thermal camera was used to measure the temperature rise of the TPS92611 when driving a 100 mA through the three LEDs on the TPS92611-Q1 EVM. Figure 3-14 shows the IC at room temperature and Figure 3-15 shows when the IC has fully self-heated.

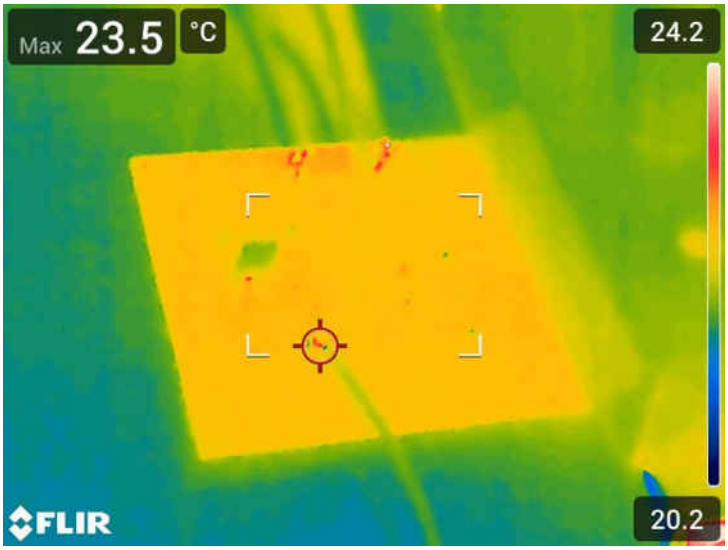

Figure 3-14. TPS92611-Q1 at Room Temperature

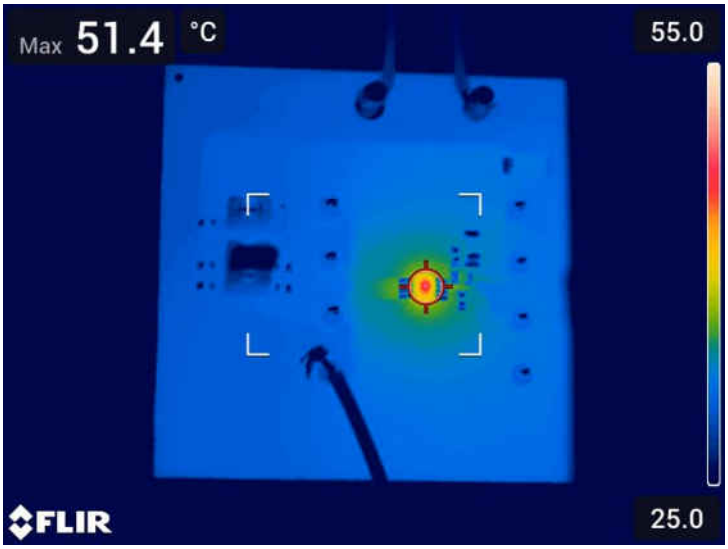

Figure 3-15. TPS92611-Q1 Self-Heating Driving 100 mA at Room Temperature

As shown by the thermal camera photographs, the self-heating is about 28°C. Once the self-heating was determined, the TPS92611-Q1 EVM was placed inside a thermal stream to test behavior in high ambient temperature conditions. The EVM was first heated to 150°C after which the PWM was toggled on for the EVM allowing the TPS92611-Q1 to self-heat to the thermal shutdown threshold. Once the OT occurred, the TPS92611-Q1 output and fault pin turns on and off periodically at an approximately constant rate. The time the fault is low (output disabled due to OT) is the time needed to allow the device to cool down from an overtemperature event. Figure 3-16 shows the fault pin switching at 150°C. The device turns off for approximately 180 ms each time.

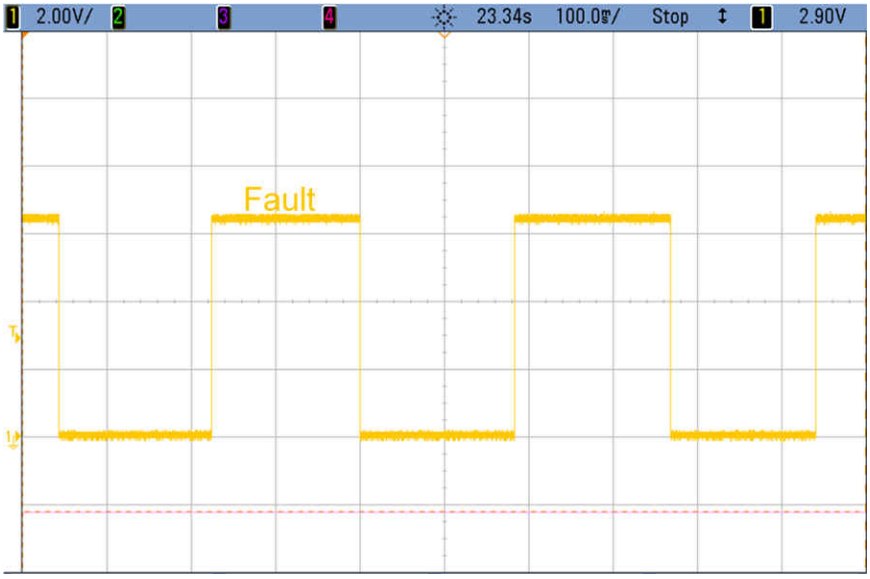

Figure 3-16. 150°C Ambient Overtemperature Fault Output

An additional test was conducted at 165°C to compare results. Figure 3-17 illustrates fault switching at 165°C.

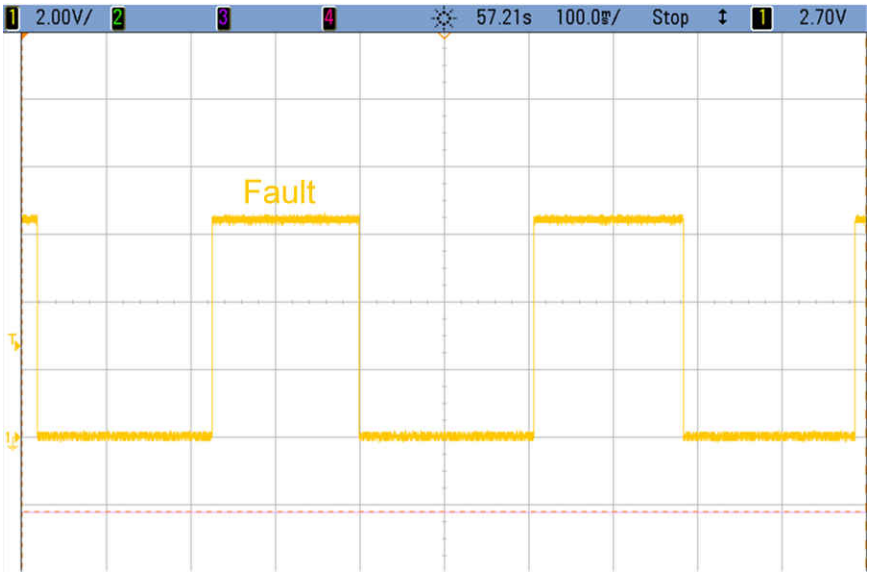

Figure 3-17. 165°C Ambient Overtemperature Fault Output

In this case, the device turns off slightly longer than 200 ms each time. Given these results, a turn off time between 220 ms to 400 ms is viable but the recommendation is to test the thermals in the expected conditions of the use-case.

4 Conclusion

The discrete fault detection circuit utilizes the ATL431LI-Q1 to differentiate fault conditions that affect the TPS9261x-Q1 output. With the addition of the ATL431L1-Q1 and simple MCU logic, the MCU can differentiate between an overtemperature, short to battery, short to ground, and open load condition. Furthermore, this discrete solution is both cost-effective and compact requiring only a single additional comparator and minimal passive components. By implementing this simple fault detection circuit customers can detect specific faults that occur on the TPS9261x-Q1 output and report this information to the driver and other vehicle electronic control units.

5 References

1. Texas Instruments, *TPS92611-Q1 Automotive Single-Channel Linear LED Driver* data sheet
2. Texas Instruments, *TPS92611-Q1 Evaluation Module* user's guide
3. Texas Instruments, *ATL431 Adjustable Shunt Regulator EVM* user's guide
4. Texas Instruments, *Using the TL431 for Undervoltage and Overvoltage Detection* application note

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