Application Report

Measuring and Understanding the Output Voltage Ripple of a Boost Converter

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ABSTRACT

The output ripple waveform of a boost converter is normally larger than the calculation result because of the voltage spike. Such behavior is related to the measurement method, the operating principle and the non-ideal characteristics of the boost circuit. The application note analyzes the root cause of the spike in the output ripple and proposes a simple solutions to solve the problem.

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Trademarks

1 Introduction

A boost converter circuit such as TPS61022 is shown in Figure 1-1. With alternate turning on and off of the two integrated MOSFET, the inductor stores energy and then released to VOUT which is higher than the input voltage. The average value of VOUT is set by the FB pin and R1, R2 resistors.

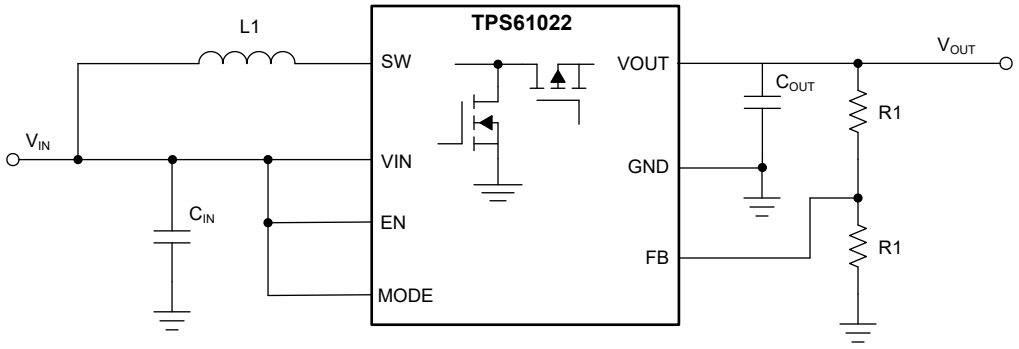

Figure 1-1. Simplified Schematic of TPS61022

The ideal operating waveform at heavy loading condition are shown in Figure 1-2. In the image:

- I_L is the inductor current.
- I_{OUT} is the output current of the boost converter.
- I_D is the current through the synchronous rectification MOSFET.
- SW is voltage waveform in SW pin.
- ΔV_{OUT} is output voltage ripple.

The output voltage drops when the inductor is storing energy, and increases when the inductor energy is released. This behavior results in output voltage ripple ΔV_{OUT} defined by Equation 1. This formula is commonly found in boost converter data sheet. The ΔV_{OUT} is typically lower than 1% of the average output voltage if the boost converter is properly designed.

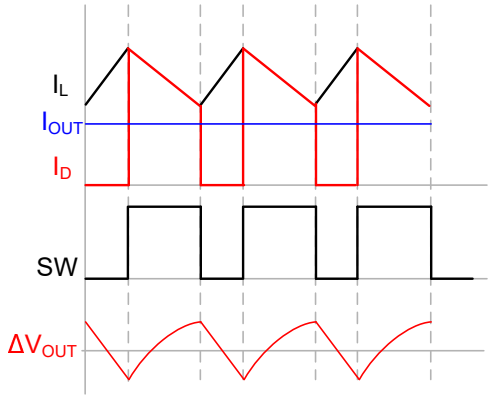

Figure 1-2. Ideal Operating Waveform of a Boost

$$\Delta V_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (1)$$

In this equation:

- C_{OUT} is the effective output capacitance.
- f_{SW} is the switching frequency of the boost.

However, one may observe much larger output voltage ripple than the calculation result in real circuits. This application details the root cause of the observation and proposes solution to solve the problem.

2 Observation in Bench Test

The Equation 1 assumes that the output capacitor is ideal and capacitor ripple is perfectly measured by the voltage probe. However, the actual ripple waveform would be related to the setting of oscilloscope bandwidth and voltage probe grounding method.

The bandwidth of a Tektronix oscilloscope can be set to 20 MHz or full bandwidth, which could be 500 MHz or higher depending on the oscilloscope model. The voltage probe grounding loop could be as in Figure 2-1. The left probe has long grounding wire and the test point is not closed to the capacitor. The right probe has very short grounding wire and the test point is on the terminals of the capacitor.

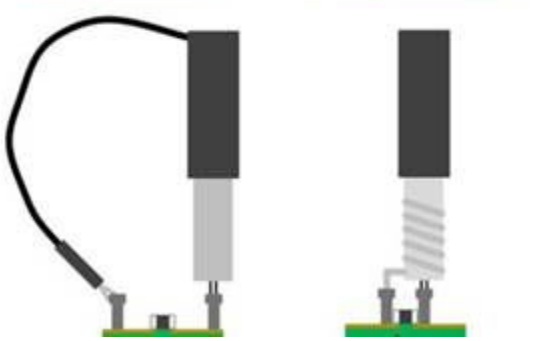

Figure 2-1. Setup of Voltage Probe

Taking TPS61022 as an example, the output ripple waveform with different setting are shown from Figure 2-2 to Figure 2-4. From the waveform, three conclusions can be derived :

1. The loop between the probe tip and its ground must be as small as possible, to avoid any noise coupling.
2. In additional to the switching frequency ripple, there is large and high frequency voltage spike across the output capacitor.
3. The voltage spike is much small at 20-MHz bandwidth setting as the oscilloscope acts at low pass filter.

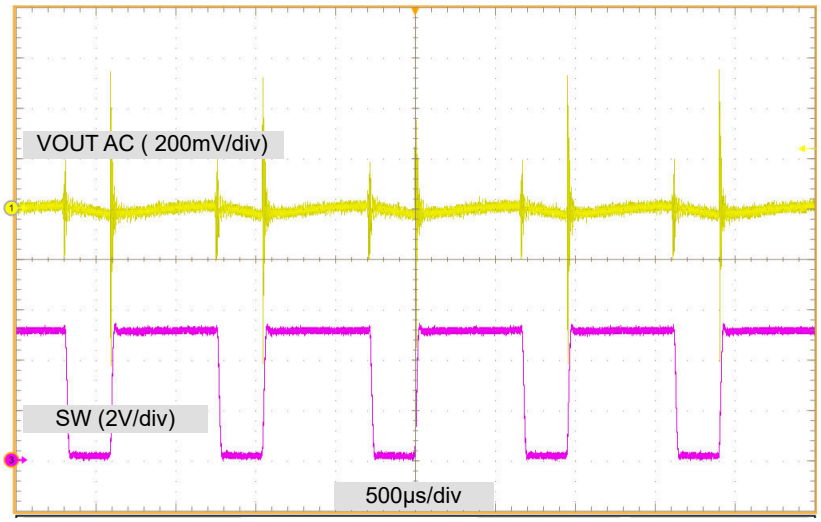

Figure 2-2. Voltage Ripple with Long Ground Cable and Full Bandwidth

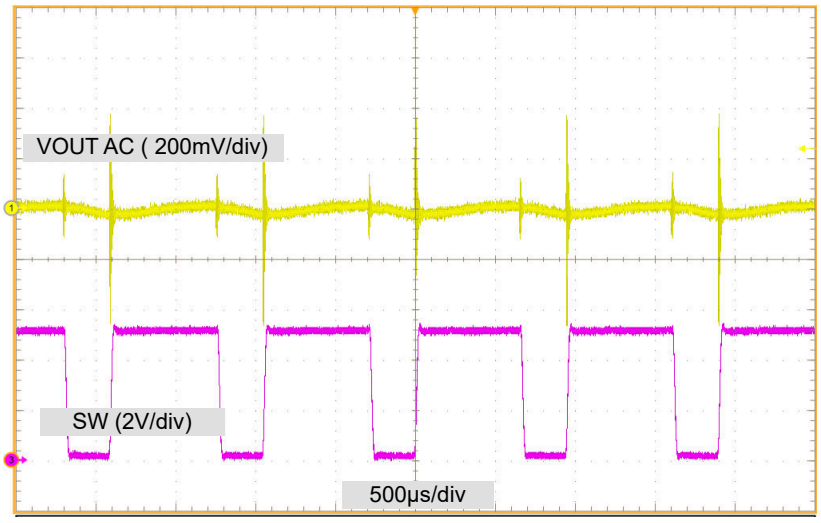

Figure 2-3. Voltage Ripple with Short Ground Cable and Full Bandwidth

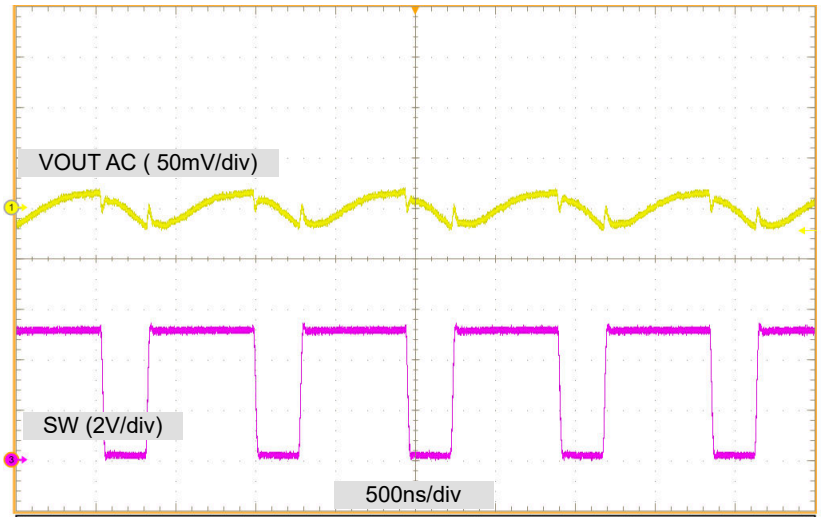

Figure 2-4. Voltage Ripple with 20-MHz Bandwidth

3 Root Cause Analysis

The voltage spike shown in Figure 2-3 is caused by the ESR (effective series resistance) and ESL (effective series inductance) of the output capacitor. The Figure 3-1 shows the impedance of a 0805-package ceramic capacitor over frequency. Point A is the resonant frequency of the ESL and the capacitor.

The impedance of the capacitor is equal to its ESR which is approximately 3.5mΩ. The impedance of the capacitor increases linearly once the frequency is higher than 10 MHz. This is behavior of the ESL. From the impedance of point B and point C, the ESL is estimated to be 0.27nH.

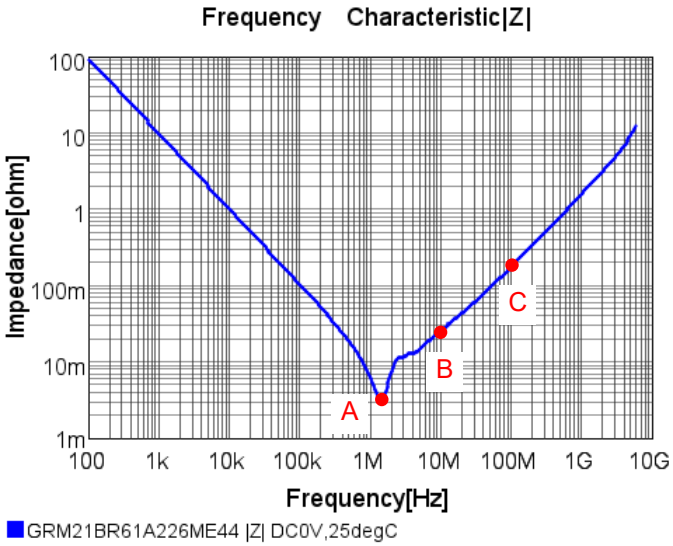

Figure 3-1. Characteristic of a Ceramic Capacitor

The voltage crossing the ESR is in proportion to the current through capacitor. A ceramic capacitor has only several milliohm resistances and normally there will be several ceramic capacitors in parallel. Thus, this voltage ripple caused by ESR is small and can be neglected.

The voltage crossing the ESL is in proportional to its di/dt, which could be very large. Because the switching frequency of a boost converter always tends to be as large as possible to reduce the solution size. The di/dt will also increase with the switching frequency to reduce the power loss in the IC.

Considering the ESL and the parasitic inductance of the PCB trace and IC package, the schematic of the boost converter power stage is shown in Figure 3-2 where L_{PAR1} is the sum of pin-out and PCB parasitic inductor and L_{PAR2} is the parasitic inductor of the GND pin;

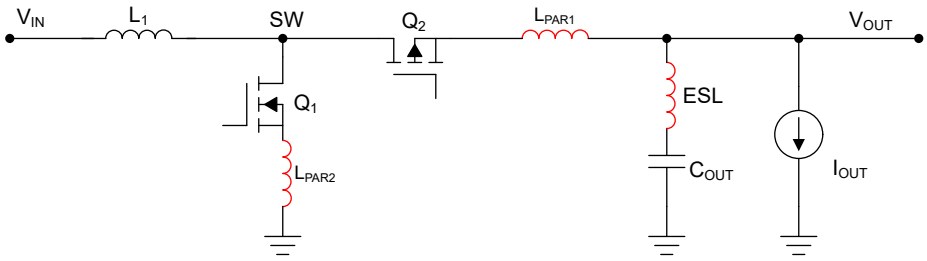

Figure 3-2. Boost Converter Power Stage With Parasitic Inductor

When Q_1 turns off and SW node voltage is higher than V_{OUT}, the inductor current starts to transit from Q_1 to Q_2. During the current transition period, the equivalent circuit is shown in Figure 3-3, where

- C_{Q1} represents parasitic capacitor of Q_1. The turning-off time of Q_1 is neglected.
- I_{L1} represents the inductor as inductor current is almost constant during the short transition period.

- V_{COUT} represent the voltage in the ideal capacitance portion of the output capacitor. the voltage is almost constant during this transition period.

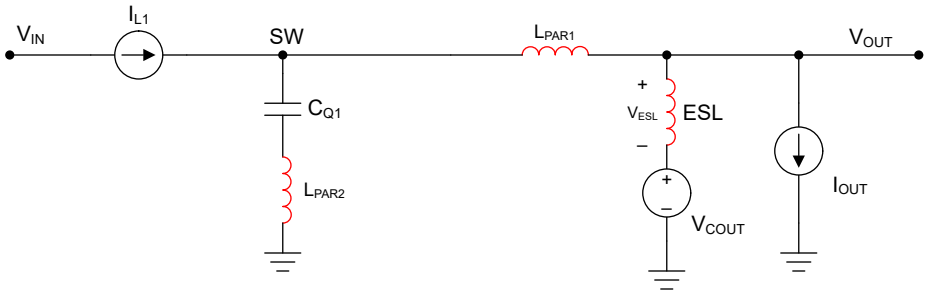

Figure 3-3. Simplified Model at Low Side MOSFET Turning Off

The Figure 3-3 can be further simplified to a LC circuit with initial inductor current I_{L1}. The inductor value is the sum of all the parasitics inductor in the circuit. The capacitor is C_{Q1}. So the voltage spike of the ESL is defined by Equation 2. The voltage spike is in proportinal to inductor current.

$$V_{ESL} = I_{L1} \cdot \sqrt{\frac{(L_{PAR1} + L_{PAR2} + ESL)}{C_{Q1}}} \cdot \frac{ESL}{(L_{PAR1} + L_{PAR2} + ESL)} \tag{2}$$

And the oscillation frequency is defined by Equation 3.

$$f_{ESL} = \frac{1}{2\pi \cdot \sqrt{(L_{PAR1} + L_{PAR2} + ESL) \cdot C_{Q1}}} \tag{3}$$

When Q_1 turns on, the inductor current firstly transits from Q_2 to Q_1, then voltage Q_1 quickly declines to zero. The simplified schematic during this period is shown in Figure 10, where C_{Q2} represents the parasitic capacitance of Q_2 when it turns off.

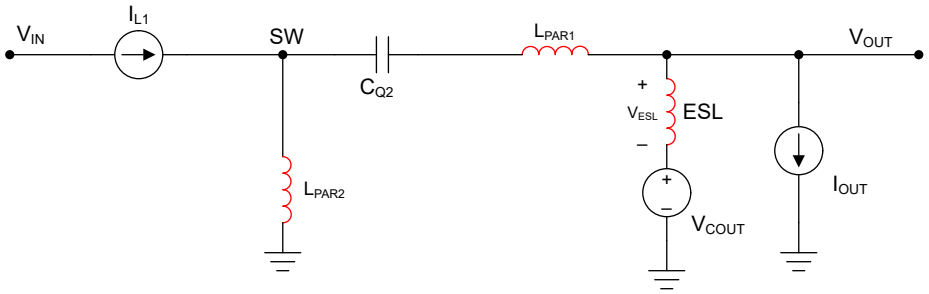

Figure 3-4. Simplified Model at Low Side MOSFET Turning On

The maximum voltage spike at ESL is defined by Equation 4. The circuit can also be simplified to a LC circuit. The V_{ESL} voltage level is in proportion to the boost output voltage, and the oscillation frequency is the same as Equation 3 because the C_{Q2} and C_{Q1} is similar.

$$V_{ESL} = V_{COUT} \cdot \frac{ESL}{(L_{PAR1} + L_{PAR2} + ESL)} \tag{4}$$

Taking TPS61022EVM as example, C_{Q1} and C_{Q2} are approximately 0.4 nF. L_{PAR1} is closed to 0.3 nH; L_{PAR2} is approximately 0.05 nH; ESL is approximately 0.09 nF as there are three capacitors in parallel. Thus, the LC oscillation frequency is up to 300 MHz.

At VIN=3.6V, VOUT=5V, IOUT=3A condition, the I_{L1} is about 4.4 A. The V_{ESL} spike at both Q_1 turning on and turning off condition are approximately 0.75 V. however, the actual voltage spike from Figure 2-3 is lower than this calculation result, especially at Q_1 turning-on condition. The main factor leading to the gap is the turning on/off time of the Q_1. The turning on/off time of Q_1 is at 5ns level. The greatly impacts the voltage spike caused by a 300-MHz LC ringing. It is hard to have an equation to calculate the voltage spike if considering the turning on/off time. A better method is simulation with PSPICE-FOR-TI or other tools.

4 A Simple Solution

The actual output ripple in real system circuit is not always equal to the value measured in the EVM. And this high frequency noise doesn't always impact the system loading:

- If there is an LDO between the boost output and the loading, The LDO and its input and output capacitor would help to filter such high frequency noise.
- If there is long cable between the boost output and the loading, the ESR, ESL of the cable and the bypass capacitor closed to the loading forms RLC filter to reduce the high frequency noise.
- Such high frequency noise may not impact the performance the system loading.

But if the loading is sensitive to the high frequency noise, or EMI performance is critical to system, a ferrite bead with high impedance at high frequency can greatly reduce such noise. The location of the ferrite bead is shown in Figure 4-1. The impedance of the FB should be much higher than C_{OUT2} at frequency closed to 300 MHz.

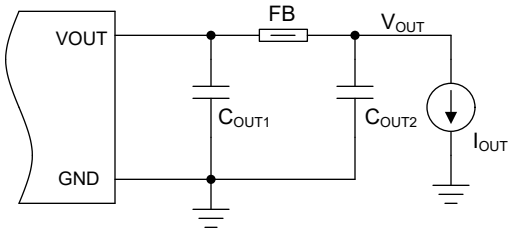

Figure 4-1. Location of the Bead

Taking BLM18KG30TH1 as an example, its impedance is higher than 35Ω at frequency from 200 MHz to 1000 MHz. the impedance is much higher than a capacitor as in Figure 4-2.

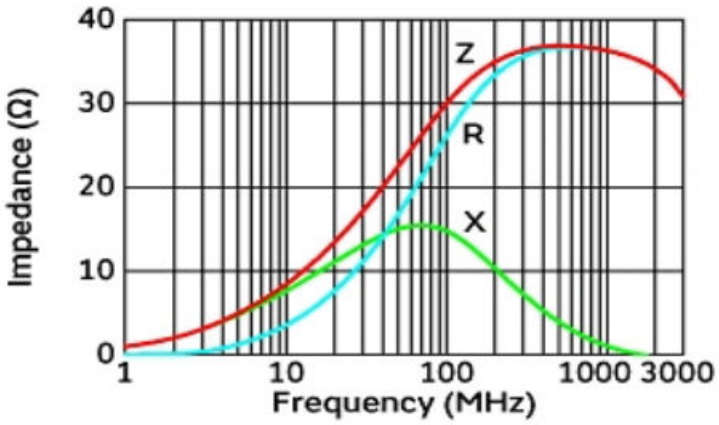

Figure 4-2. Characteristic of a Bead

After adding ferrite bead and moving one of three capacitors to location C_{OUT2} in the TPS61022EVM, The output voltage ripple is shown in Figure 4-3. The high frequency noise is greatly reduced and the ripple is mainly the switching frequency ripple.

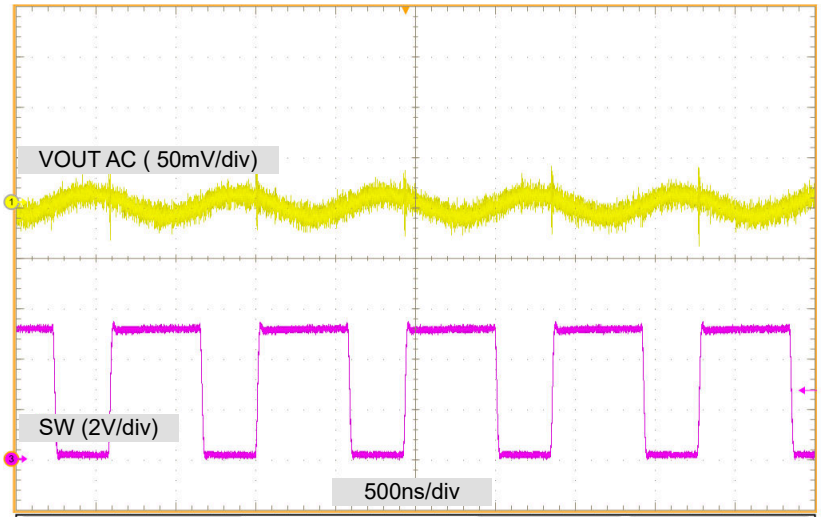

Figure 4-3. Output Voltage Ripple With a Bead

5 Summary

The voltage spike in the boost converter output voltage is mainly caused by the ESL of the output capacitor. Setup of the probe and the oscilloscope also impact the output voltage ripple waveform. This application details the root cause of voltage spike and proposes ferrite bead reduce the spike if required.

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