Application Report

Mitigating Procedure on Voltage Spike of Switching Node from Flyback Converter

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ABSTRACT

Flyback converter is being widely adopted in many applications, covering from personal electronics to industrial and automotive area. It usually supports from very small to mid-ranged power and requires fewer external components rather than other topologies. But conventional flyback still generates an unwanted voltage spike during normal operation by hard switching operation. This kind of voltage spike has high frequency noise harmonic and usually is related to EMI issue in system level. The other problem is that this voltage spike can damage to the switching device once its' peak voltage stress is higher than device's maximum absolute rating. This note will show how this voltage spike could be mitigated and contained through design example with TPS55340.

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Trademarks

1 Switching Node Voltage Stress from Flyback

1.1 Reflected Voltage, VOR

In a typical flyback converter, there is voltage which is reflected from secondary side when the primary side switch is turned off and the stored energy is transferring to the load through transformer. This reflected voltage, VOR will form voltage stress to the switching device after adding maximum input VDC, VIN in worst case. So the amplitude of the reflected voltage, VOR will be a key design factor, affecting voltage stress to the switching device.

$$V_{OR} = \frac{Np}{Ns} Vout \quad \text{(Np: Number of Turns in Primary, Ns: Number of Turns in Secondary)} \tag{1}$$

From the simple equation above, VOR is set by primary to secondary turn ratio once output voltage is set. And then Flyback controller or convert will set its' duty ratio by inductor's volt-sec balance if VOR is fixed. Figure 1-1 shows the comparison voltage and current stress according to VOR level.

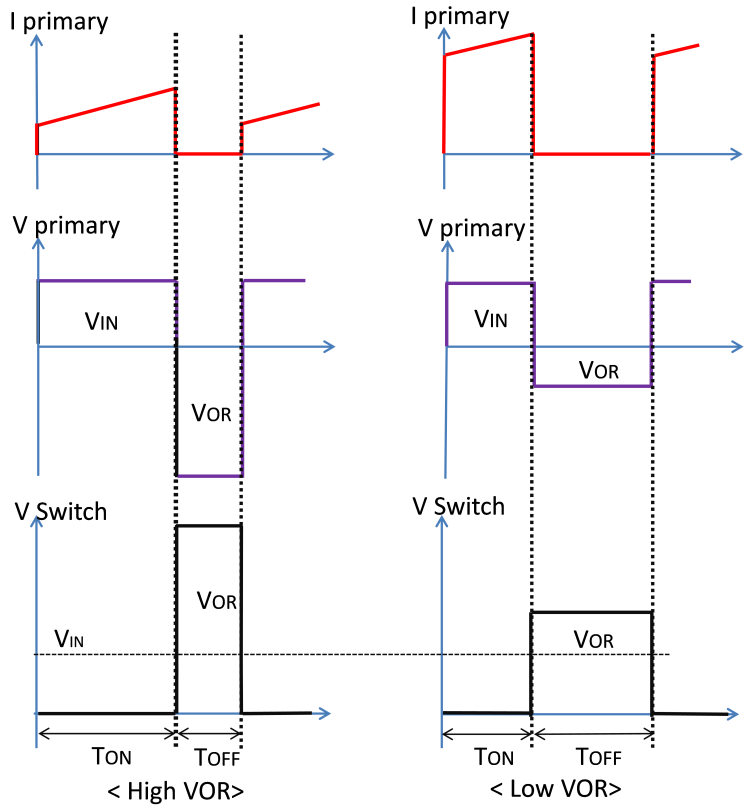

Figure 1-1. Flyback Converter's Primary Side Current, Voltage, and Switch Note Voltage

By adjusting turn ratio, VOR could be contained if it tops a limited level that is required by system. But a lower VOR will cause a higher peak current stress and make system have lower efficiency due to an increased conduction loss. Also, it is possible for higher peak to trigger internal current limit of the device which integrates FET inside.

1.2 Leakage Inductance Factor

In addition to voltage stress (VIN + VOR), there is a large voltage spike at turned off moment that is caused by the stored energy in leakage inductance of primary winding. Basically, it is a fact that magnetic flux from one winding that does not couple to other winding 100%, so it remains as a leakage inductance in the circuit. One of methods to reduce leakage factor is to improve transformer winding structure such as interleaving winding. Figure 1-2 is the simulated result after adding a small amount of leakage inductance in primary side equivalently.

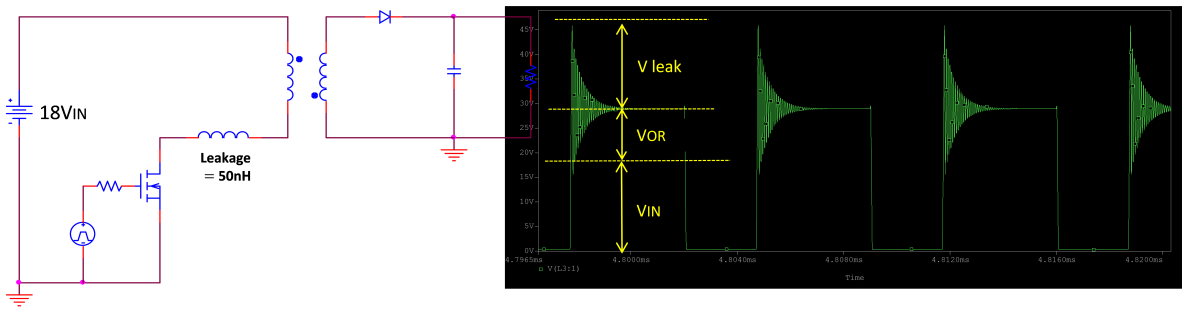

Figure 1-2. Switch Note Waveform with Leakage Inductance

As the simulated result, the stored energy in the leakage inductance turns to voltage spike immediately at turn off transient moment and then mainly resonates with the capacitance on the node. Usually it resonates under a few hundreds of MHz so it may cause EMI problems in the systems and need additional snubbing measures. Plus, if the voltage peak is higher than device's AMR (Absolute Maximum Rating), it will lead to IC or FET's damage issue either in the design stage or field.

2 Mitigating Voltage Spike on Switch Node

2.1 Zener or TVS Clamping

There are several ways to contain voltage spike by adding some snubber circuits but Zener / TVS clamping is strong candidate for the solution if the peak level should be limited so as to protect the switching device. This means that user easily controls peak level of voltage spike that is caused by leakage inductance from transformer by selecting proper zener diode's Vz rating. Figure 2-1 is the simulation results about how the voltage spike could be mitigated according to zener voltage rating under a same leakage inductance, VOR and VIN condition. It shows how voltage shape on SW node is being changed. From left, Zener rating is 1.5 times of VOR, 1.3 times and 1.1 times of VOR. (VOR is 10 V, VIN is 18 V) Noticeably, voltage peak and ringing is being mitigated if Zener rating is getting close to VOR value.

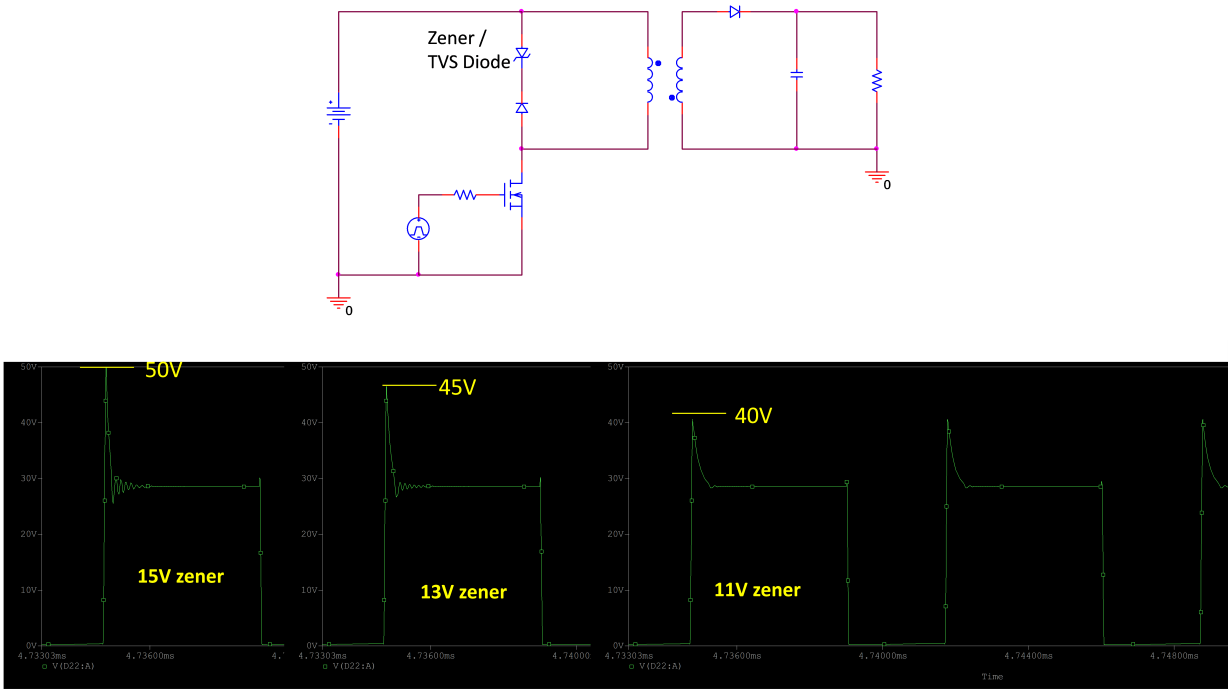

Figure 2-1. Voltage Spike on Switching Node with Zener Rating

The main purpose of zener clamping is to absorb energy from leakage inductance when main switch is turned off, but it also could clamp some of energy from magnetizing inductance of primary winding if zener rating is very close to VOR level. It means some of the stored energy in the primary which is supposed to be delivered to secondary load during turn-off period may disappear in the zener block as Figure 2-2. So this should be optimized in the system, considering required voltage stress versus system efficiency.

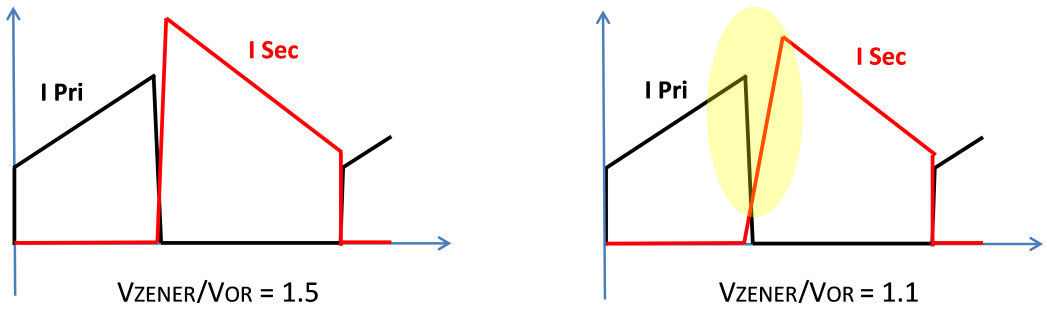

Figure 2-2. Secondary Current Shape According to Zener Rating

2.2 Forward Recovery Characteristic of Blocking Diode

At turn off transient, the stored energy in leakage inductance should be dissipated through zener as fast as possible. Before the turn off stage, the blocking diode is in reverse biased and then it should immediately flow the current from leakage inductance to zener diode when the main switch is turned off. So the path to zener in the layout should be decent, but the forward recovery time of blocking diode is also important factor as well. If the blocking diode's speed is not enough to handle this transient energy, it will bring up an unwanted voltage peak. Figure 2-3 highlights the portion which is being built during blocking diode's forward recovery period. In a real test result from Figure 3-1, around 5 V of the voltage peaking is linked to this time.

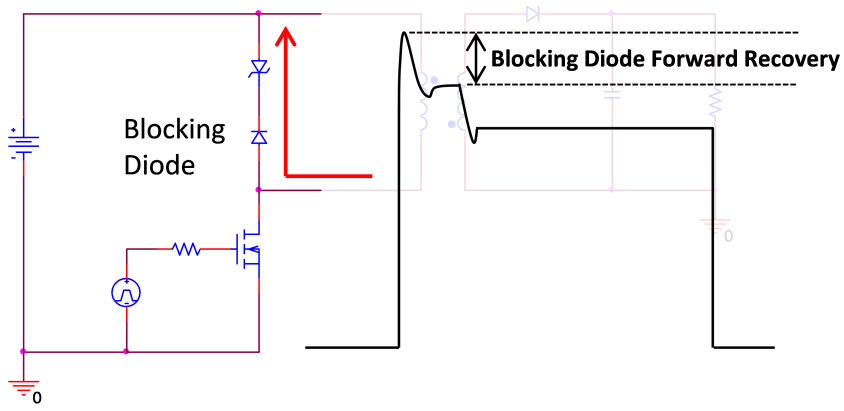

Figure 2-3. Voltage Peaking from Forward Recovery of blocking Diode

3 Design Example with TPS55340

3.1 Initial Key Designs and Test Results

- VIN_Max: 18VDC, VOUT: 14 V, IOUT: 1.6A
- Set VOR to 10 V from Vout and turn ratio of Np, Ns (Np : Primary turns, Ns: Secondary turns)
- Main check lists from TPS55430 D/S (5A, 40 V Current mode Integrated-FET DC converter)

Table 3-1. Primary Peak Current Should Not Touch IC's Internal Current Limit Once VOR is Set

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
OCP and SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	5.25	6.6	7.775	A

Table 3-2. Absolute Maximum Rating of Vsw should be less than 40 V

		MIN	MAX	UNIT
Output voltage	SW(2)	-0.3	40	V
	SW (10<10 ns transient)(2)	-5	40	V

Figure 3-1 is scope image of Vsw on TPS55340 with initial design. Peak Vsw is measured to 38 V. So it has only 2 V margin to its' AMR rating. Sometimes,in the field, the peak Vsw is required to be less than 80~85% of IC's AMR to reinforce reliability for mass production. So it needs to be reduced by redesign parameters around TPS55340.

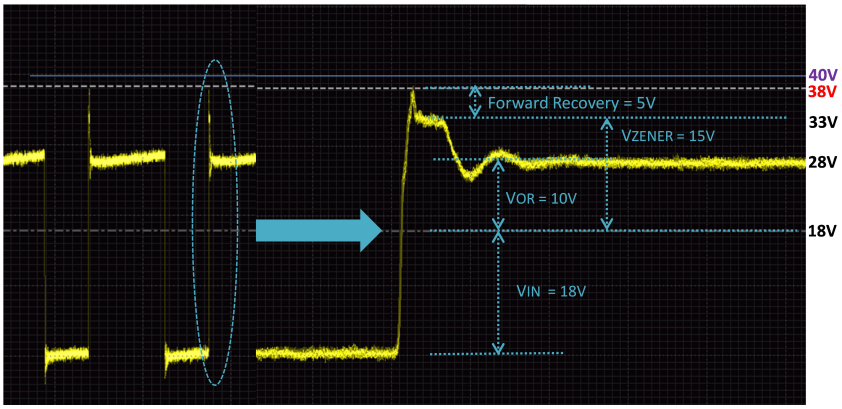

Figure 3-1. Scope Image on VSW of TPS55430 from Initial Design

3.2 Redesign Procedure to Mitigate Vsw

The first step is to check the VOR level and reduce it after ensuring the peak primary current does not touch IC's internal current limit level because if we reduce VOR, as Figure 1-1, current will be increased. This then changes the zener diode rating accruing to VOR level again.

Figure 3-2. Design change about VOR and Zener Diode

	Before	After
VOR	10 V	8 V
Zener Rating	15 V	10 V

Figure 3-3 plots more mitigated Vsw's peak voltage. It reduced from 38.4 V to 34.5 after redesign reflected voltage and zener diode rating. But it still needs some additional margin to 40V AMR

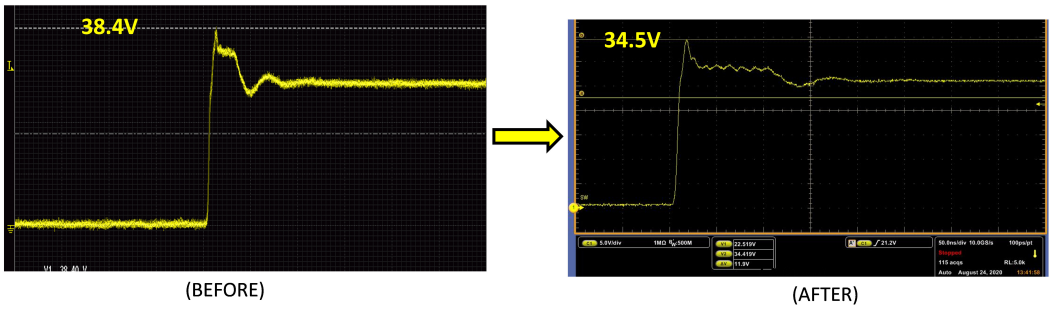

Figure 3-3. Scope Image After Changing VOR and Zener Diode Rating

3.3 Using Blocking Diode that has a good T_{fr}

Use Blocking Diode (MURS105T3G, On-semi) from TPS55340EVM-148 that has a characteristic as shown in Figure 3-4.

Maximum Forward Recovery Time (i_F = 1.0 A, di/dt = 100 A/µs, Rec. to 1.0 V)	t_{fr}	25ns

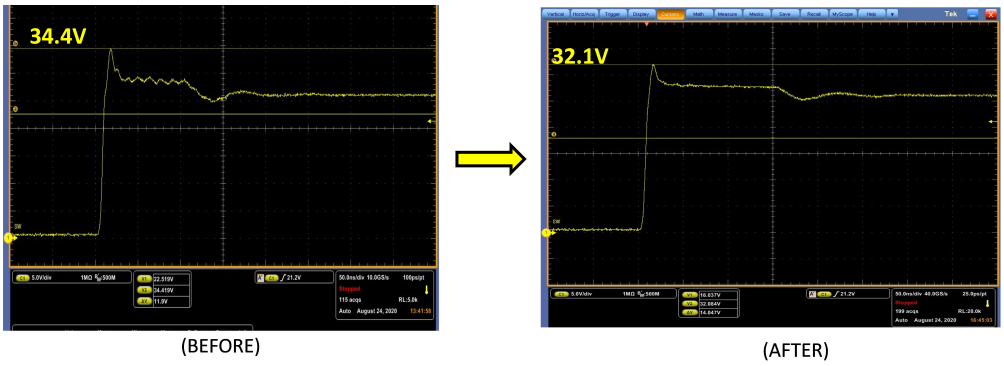

Figure 3-4. Final Test Result After changing Blocking Diode

After changing blocking diode, Vsw was measured to around 32 V which has up to 80~85% of it's AMR, 40 V with some margin.

4 Summary

If there is a strict requirement regarding to switching node waveform in the flyback converter, the user needs to check whether the reflected voltage is optimized at first and then consider proper snubbing methods. There also should not be a pcb design error that usually generates parasitic inductance in the critical path. Lastly, keeping correct measurements is also important to receive exact voltage waveform on SW node as well.

5 References

- Texas Instruments, Isolated Flyback Topology Module for TPS55340 5A, 40 V Current Mode Integrated-FET DC Converter

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