Application Note

Op Amp ESD Protection Structures

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ABSTRACT

All operational amplifier (op amp) input stages feature some sort of protection against electrostatic discharge (ESD). Most amplifiers accomplish this with diodes from both inputs and the output to both supply rails. While these diodes offer protection against ESD strikes, the diodes can also lead to undesirable current through the ESD structure when one, or both, of the inputs exceeds the V+ rail. Fortunately, there are a select few op amps with an alternative input ESD structure designed to prevent this undesired current. This application report covers the standard ESD protection structure and an alternative ESD protection structure. The document also shows different testing methods for observing the behavior of the ESD protection under device shutdown and measurement data from devices with protection structures that do not have diodes from the inputs to the V+ supply pin.

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1 Introduction

To help deal with short-term, high-voltage events, amplifiers have electrostatic discharge (ESD) protection structures. These structures typically feature diodes that protect amplifier inputs and outputs from unintended damage by clamping these pins to the supply rails under ESD conditions.

However, these diodes are not designed to be relied upon for electrical overstress (EOS) events where the input voltage significantly exceeds the supply rail for a longer period of time. Under such a scenario, current can flow from the inputs to the supply rails. This can have undesirable effects including, but not limited to, *back-powering the amplifier*, device damage, and complete device failure. Understanding these scenarios and what can be done to avoid them is important in op amp circuit design.

This application note considers the standard amplifier ESD protection structure as well as an alternative structure that does not have diodes from the inputs to the V+ supply rail. Then, some Texas Instruments devices are highlighted with this alternative input protection structure and how the behavior of the protection structure of an op amp can be measured for certain scenarios.

2 Standard Op Amp ESD Protection

2.1 Standard Op Amp ESD Protection: Structure

The majority of op amps have input structures that include a protection diode between each input and each supply rail, as shown in Figure 2-1. The purpose of these diodes is to protect the amplifier from sudden ESD strikes by clamping the rising voltage and redirecting the current surge away from the input stage transistors. If either input reaches a voltage greater than V+ plus the forward voltage of the ESD protection diode, the protection diodes become forward biased and the current flows from the input, through the ESD cell. In a similar manner, if either input reaches a voltage lower than V– minus the forward voltage of the ESD protection diode, the protection diodes become forward biased and the current flows through the ESD cell, to the input. Note that the forward voltage drop of the ESD diode is about 500 mV in many data sheets.

During an ESD event, several current paths are available, including through the absorption device, and the path taken depends on the voltages at the pins. An example is shown in Figure 2-1 where the IN+ pin takes a large, positive voltage with respect to V–.

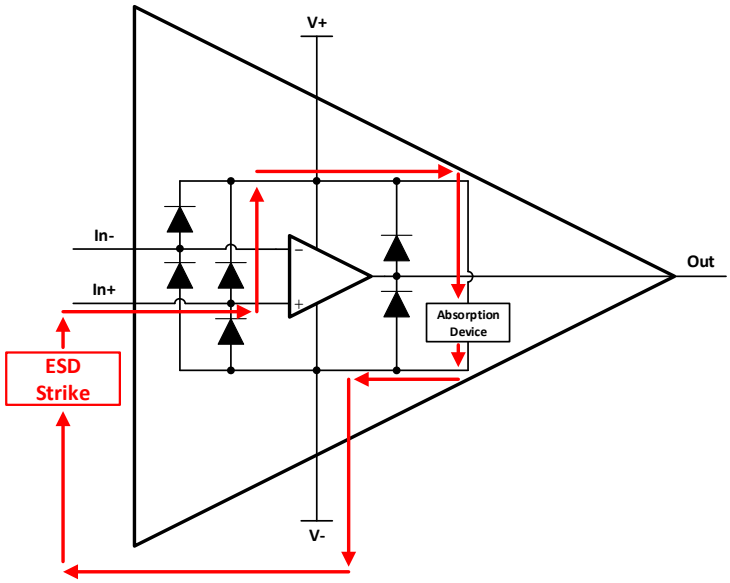


Figure 2-1. Path of Current During ESD Strike From In+ to V– for Op Amp With Standard ESD Protection

The behavior of the output protection diodes, also seen in Figure 2-1, mirrors that of the input protection diodes. If the output reaches a voltage higher than V+ plus the forward voltage of the ESD diode, a current path forms and current flows from the output, through the ESD cell. The same occurs if the output reaches a voltage lower than V– minus the forward voltage of the ESD diode, a current path forms and current flows through the ESD cell, to the output.

Note that ESD protection is for out-of-circuit events, such as ESD events that can occur during handling or assembly, and is not intended for in-circuit events. Because this protection structure is designed for high-energy, short-duration ESD events, the diodes must be protected from destruction during the longer instances of Electrical Overstress (EOS). During EOS events, the applied voltage can be a lot lower. For example, the voltage can be in the region of 500 mV over the supply voltage rather than 1 kV. However, these scenarios also last for much longer periods of time. The level of current that the protection diodes can sustain under EOS is often given in the *Absolute Maximum Ratings* section of the data sheet as ±10 mA. Nonetheless, keep this number under ±1 mA, when possible.

If the circuit designer anticipates the possibility of either input going outside the minimum or maximum common-mode voltage range in the Absolute Maximum Ratings table of the data sheet, a common practice is to include series resistors at the IN+ and IN– pins that are sized to limit the input current. Additional ESD and EOS scenarios are covered in more depth in the TI Precision Labs presentations on ESD and EOS.

Table 2-1 shows an example Absolute Maximum Ratings table from the *TLV9051 / TLV9052 / TLV9054 5-MHz, 15-V/µs High Slew-Rate, RRIO Op Amp* data sheet. Limit the common-mode voltage to be no less than (V–) – 0.5 V and no more than (V+) + 0.5 V. If these limits are exceeded, the diode starts conducting current. If the current is high enough, the current can potentially damage the diodes themselves and cause subsequent damage to the amplifier inputs.

Table 2-1. Absolute Maximum Ratings for the TLV905x

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				7	V
Signal input pins	Voltage(1)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		V_S + 0.2	V
	Current(1)		–10	10	mA
Output short-circuit(2)			Continuous		
Operating ambient temperature, T_A			–40	150	°C
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(2) Short-circuit to ground, one amplifier per package.

2.2 Standard Op Amp ESD Protection: Considerations

The TLV9051 device has the traditional ESD diode protection shown in Figure 2-2. For certain applications, such as a battery-powered system, the circuit designer can choose to save power by temporarily turning off the amplifier. This is usually done by either floating V+ or, preferably, setting V+ to ground. When the amplifier is turned off, the input can continue to detect a voltage, such as a signal being generated by a sensor.

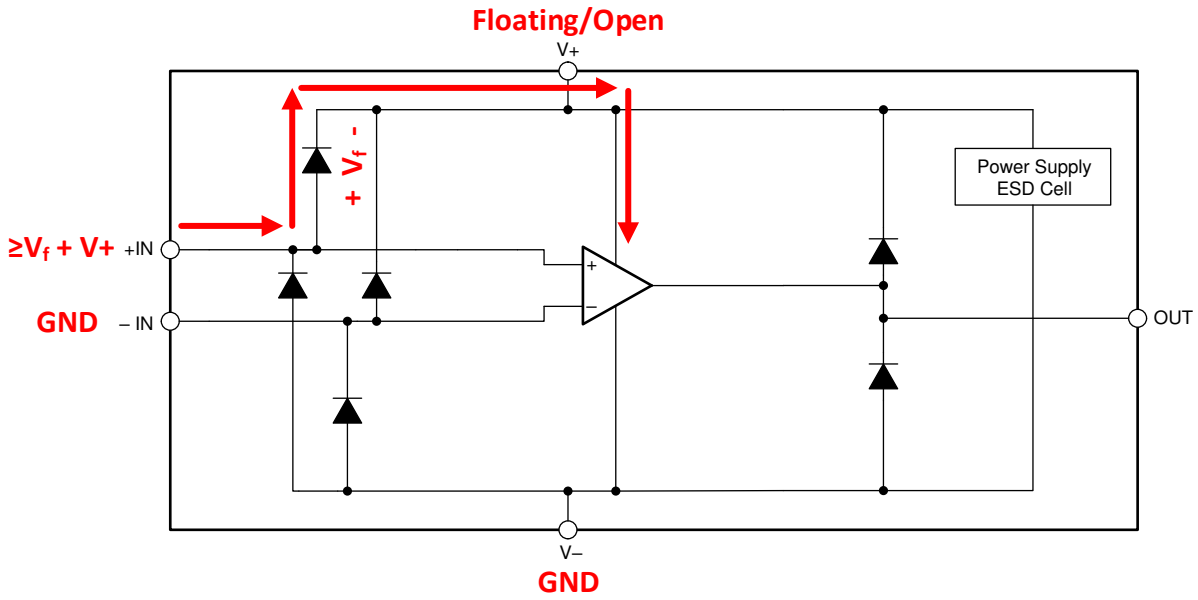


Figure 2-2. Input Current Path of a Back-Powered Op Amp

When V+ is high impedance or floating, there exists the possibility of back-powering the amplifier. Back-powering can happen when the input experiences a voltage greater than the forward voltage of the ESD diode plus the voltage at the V+ rail, then the diode can begin to conduct current through the input to the supply pin. If the V+ pin is not being driven, the voltage can float up, especially if there is an impedance to ground at this node from another section of the circuit. The device is then turned on using the input signal as a means to power on the amplifier through the ESD diode. The output of the amplifier begins to provide undesired output signals, which can then feed to downstream components. A similar scenario can occur in a sensor circuit when the sensor turns on and sends a signal that reaches the inputs of the amplifier before the supply pins of the amplifier have fully ramped.

One way to help protect against accidentally back-powering the device is not to leave the V+ pin floating. When the pin is left floating or open, the voltage of the pin is unpredictable and it can be impossible to tell when the protection diode to V+, or even to V–, is likely to turn on. By grounding this pin, the circuit designer can help prevent the voltage of the V+ pin from floating upward and turning on the amplifier.

Even if grounding the V+ pin prevents the amplifier from being back-powered, in such a scenario, there still exists the possibility of unwanted current going into the diode. The input protection diode to V+ can still be turned on if the input voltage is higher than GND by the forward voltage drop of the protection diode. The best way to prevent back-powering of the amplifier in the presence of an input signal when V+ is left floating or grounded, is to avoid turning on the ESD diodes entirely. For cases when an input voltage is unavoidable while the supply pins of the amplifier are grounded or left floating, an alternate ESD protection scheme is needed.

3 Op Amp ESD Protection Without Input Diodes to V+

There are several op amps with an alternative input ESD protection structure that does not have a protection diode from both IN+ and IN– pins to V+. This protection behaves differently than the standard protection. Parts with this structure include: OPA310 | OPA2310 | OPA4310, OPA348 | OPA2348 | OPA4348, TLV341 | TLV341A, TLV342 | TLV342A.

3.1 Op Amp ESD Protection Without Input Diodes to V+: Structure

Figure 3-1 shows an example of an alternate input protection structure for the IN+ and OUT pins. The same structure is present on the IN– pin as on the IN+ pin, though the structure is not shown here for the sake of simplicity. In contrast, the output pin has diode paths to both rails. Not all of the input protection is shown here, instead, this figure shows only the portion most relevant to this application report.

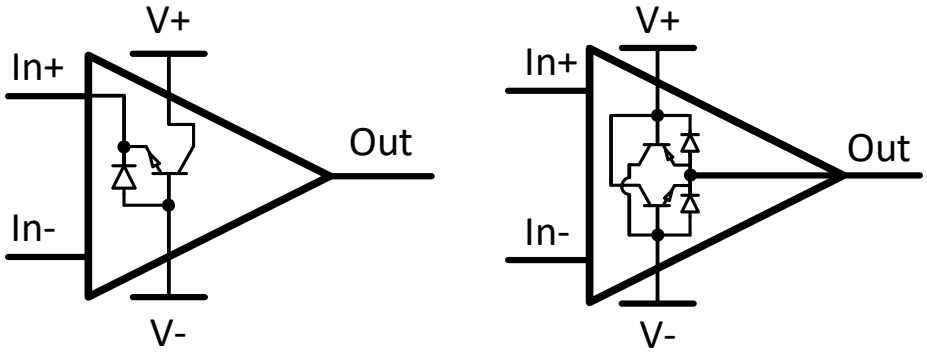


Figure 3-1. Current Paths for IN+ (also present for IN–) and OUT

With this type of structure, IN+ and IN- can exceed V+ without turning on a diode protection path and conducting current. For example, if V+ and V- are grounded, then a current path from the input to the supplies is prevented in the case of a positive input signal. Similarly, if V+ is left floating and V- is grounded while a positive input signal is seen, then input current to the positive supply and the possibility of back-powering the amplifier are avoided. The voltage on the inputs and supply pins still need to stay below the absolute maximum ratings mentioned in the data sheet.

Table 3-1 shows an example *Absolute Maximum Ratings* table from the OPAx310 High Output Current, Fast Shutdown, Low Voltage (1.5 V to 5.5 V), RRIO, 3-MHz Operational Amplifier. Unlike what was seen with a standard ESD protection structure table, where the absolute input common-mode voltages can only go 0.5 V past the supply rails, the input common-mode voltages of this alternative protection scheme do not have that limitation. There still is a limit to how far the input voltage can be taken beyond V+. Eventually, the input is driven too far and significant current begins to flow. Example test setups and sample data are provided later in this document.

Table 3-1. Absolute Maximum Ratings for the OPAx310

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	7	V
Signal input pins	Common-mode voltage (1) (2)	– 0.5	6.0	V
	Differential voltage(1) (2)		±6.0	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Input pins can swing beyond (V+) as long as the pins stay with in 6.0 V. No diode structure from input pins to (V+).
(2) Input pins are diode-clamped to (V–). Input signals that 0.3 V below (V–) must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

Finally, remember that the devices with this alternative ESD protection structure still start to turn on their diode protection paths if one of the input pins falls below V– minus 0.5 V. Therefore, consider what type of input signals are present while the amplifier is turned off.

3.2 Op Amp ESD Protection Without Input Diodes to V+: Considerations

As mentioned in the previous section, if the input voltage continues to rise beyond the absolute maximum ratings, a deep snap-back effect occurs at the input. The effect causes the voltage of the protection circuitry to suddenly fall and clamp the input voltage at a much lower level while raising the input current to higher levels and damaging the input structure itself. Furthermore, the device can become stuck in this state, a phenomenon known as *latch-up*.

While ESD protection structures without input diodes to the V+ rail can work well in applications where the amplifier must be turned off while an input signal is present, the possibility of a deep snap-back effect needs to be considered when the input voltages can potentially go beyond the absolute maximum ratings. The best practice is to avoid entering the high-current conduction regions altogether. Add input resistors that limit the input current to ±10 mA, or even ±1 mA.

Figure 3-3 shows an example of this effect. In this example, the OPA348 amplifier has the V– pin at ground and the V+ pin connected to a supply at 0 V. The output and inverting input are left open, while the non-inverting input is driven with a positive voltage. The corresponding input ESD structure current is then measured. The test configuration is shown in Figure 3-2.

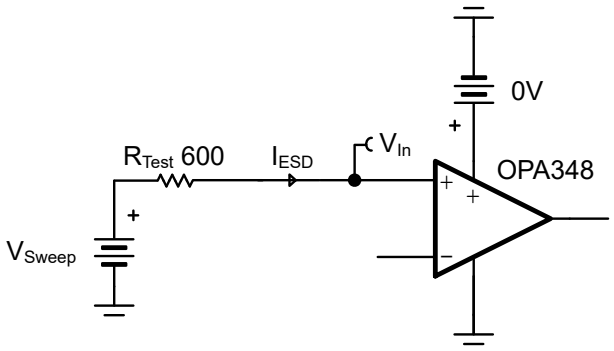


Figure 3-2. OPA348 - Test Setup of ESD Structure Current for Extended Applied Input Voltage

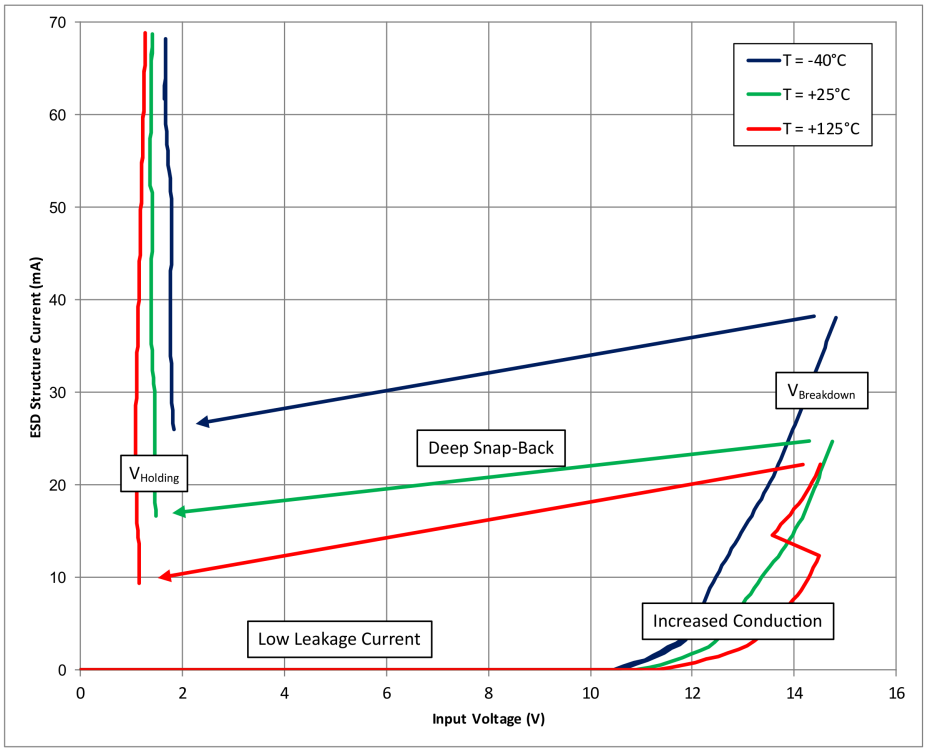
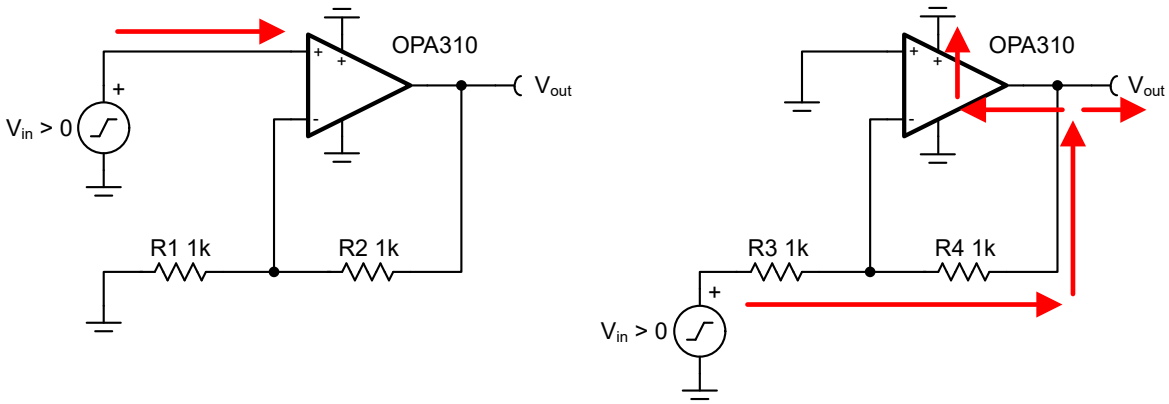


Figure 3-3. OPA348 - ESD Structure Current for Extended Applied Input Voltage

From an input voltage of 0 V to about 10 V, there is low current passing through the ESD structure. In this region, the alternate ESD protection structure prevents an input signal from back-powering the amplifier or creating significant current. After about 10.5 V, the input current begins to rise rapidly. When the input is driven even further, deep snap-back occurs. The voltage suddenly drops and is clamped at a lower level. Simultaneously, the input current rises to very high levels. Avoid the operating regions of higher current to prevent damage. For the purpose of demonstration, the input current in this experiment was allowed to exceed the data sheet limit of 10 mA. Do not exceed the absolute maximum ratings in your design.

Effectiveness of the alternative input structure depends on the amplifier circuit configuration, even when the amplifier is turned off. For example, if a TLV341 amplifier is placed in a non-inverting configuration while the supplies are grounded and the device turned off, the input is able to handle some positive voltage without leaking current to the V+ rail or output (Figure 3-4 left). However, if the same amplifier under the same scenario is put into an inverting configuration, current does not pass through the input pin but is passed to the output through the feedback loop (Figure 3-4 right). Furthermore, the diodes at the output pin can turn on and pass into the V+ pin. So, care must be given not just to the op amp, but also to the circuit setup.



Non-Inverting Amplifier Configuration Inverting Amplifier Configuration

Figure 3-4. Circuit Configuration Can Influence Current Through the ESD Structure

4 How to Measure the ESD Structure Current of an Op Amp

The ESD structure current of an op amp can be measured to better understand the behavior of its ESD protection circuitry. One method of measurement involves picking an amplifier, grounding the supply pins, and sweeping the voltage at the input and output pins, one pin at a time. The pins not under test can be left open. Measuring the corresponding current passing through the V+ and V- pins shows the amount of ESD structure current. This setup is shown in Figure 4-1 and gives an idea of the amplifier behavior when the amplifier is turned off with grounded supply pins and an input or output signal is still present. To avoid damaging the device during testing, it is a good idea to limit the current available from the voltage source to ±10 mA. In production, it is better to limit the current to ±1mA when possible. This test method was used to confirm the input structure behavior of some devices and the sample data can be found in Appendix A.

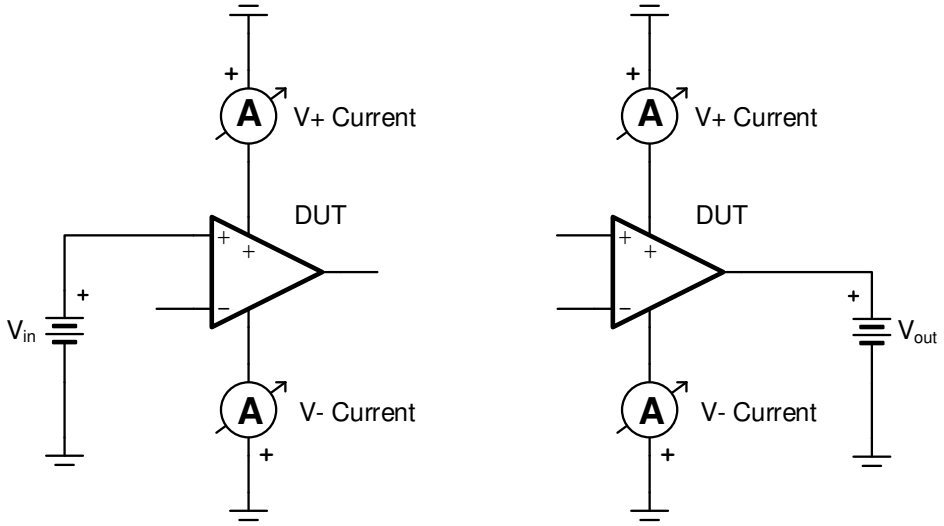


Figure 4-1. Setup 1 - Example Schematic for Testing IN+ and OUT Pins With Grounded Supplies

Depending on how the amplifier is turned off, a different test setup may be more appropriate for accurately observing the ESD structure current while an input or output voltage is present. For example, a shutdown pin may allow the circuit designer to put the amplifier into shutdown mode while the V+ supply pin still has a voltage present. Alternatively, some circuit designers look to turn off their amplifiers by switching open the V+ pin. Alternate ESD structure current test setups for some of the more popular scenarios are shown in Figure 4-2 through Figure 4-4. Sample data for these test setups is also available in Appendix A.

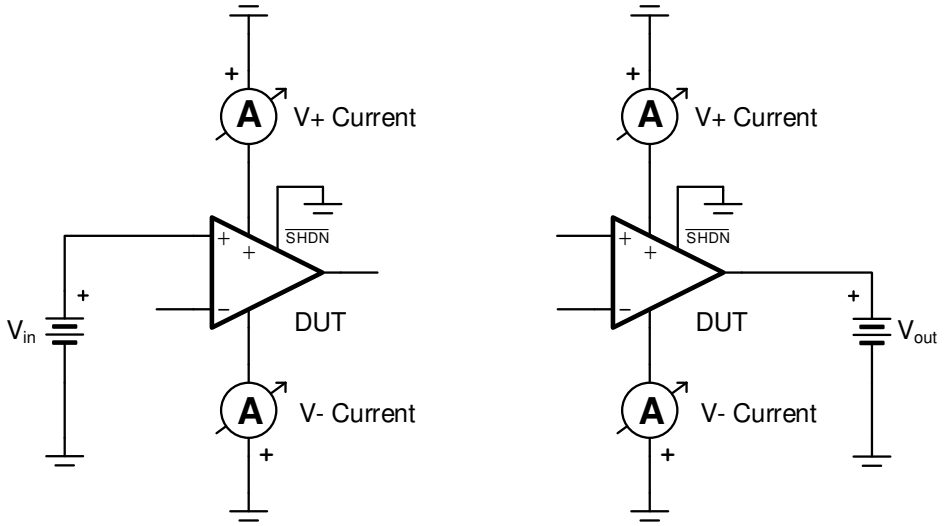


Figure 4-2. Setup 2 - Example Schematic for Testing IN+ and OUT Pins With Grounded Supplies and Shutdown Pin

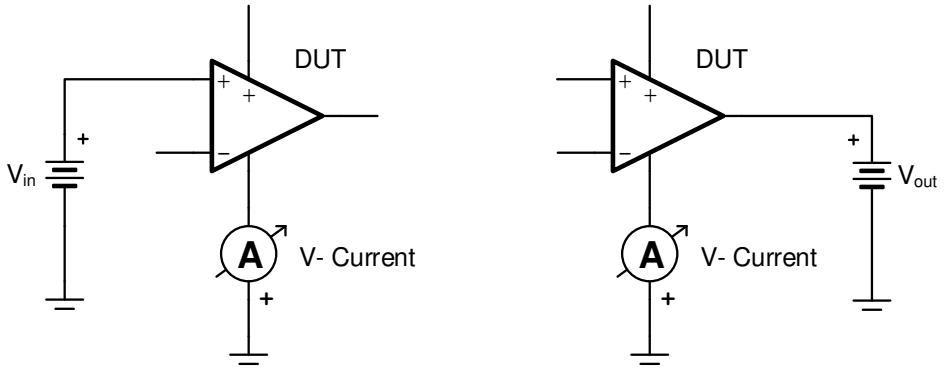


Figure 4-3. Setup 3 - Example Schematic for Testing IN+ and OUT Pins With Open V+ Pin and Grounded V- Pin

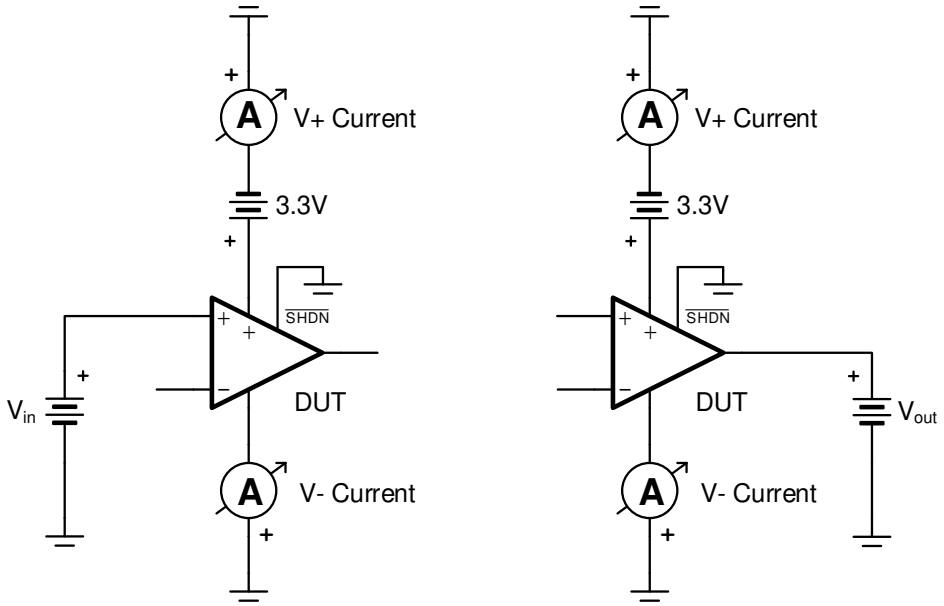


Figure 4-4. Setup 4 - Example Schematic for Testing IN+ and OUT Pins With Power on V+ Pin, Grounded V- Pin and Shutdown Pin Low

5 Summary

Most amplifiers come with standard ESD diode structures to protect them from sudden, high-voltage discharges. Although these are robust circuits, alternative protection structures are preferable in some applications. It is important for analog circuit engineers to understand the strengths and limits of different ESD protection circuits and to be able to verify the type of protection structure of an op amp depending on the input voltage behavior and power supply sequencing.

6 References

1. To learn more about back-powering amplifiers, see Tim Claycomb's Precision Hub blog post titled, *The self-powering device?*
2. To learn more about ESD and the effects on op amps, visit the TI Precision Labs Presentation on Electrostatic Discharge (ESD).
3. To learn more about EOS and the effects on op amps, visit the TI Precision Labs Series on Electrical Overstress (EOS).
4. For more information on ESD protection snap-back, see Matthew Xiong's blog post, *The dangers of deep snap-back ESD circuit-protection diodes*.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (January 2023)	Page
• Revision A includes the ESD structure of one of the newer TI devices and updates to the nomenclature and graphs	1

A Measured Data for Op Amps With Alternate ESD Protection

The results in the appendix were gathered using the test setups described in Section 4. Data was taken at room temperature. To learn about changes over temperature, see Figure 3-3.

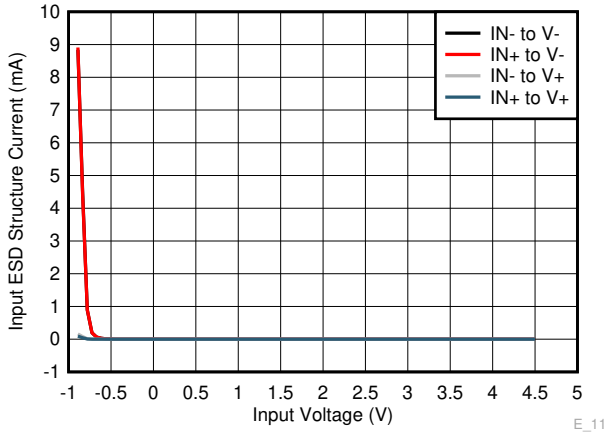


Figure A-1. OPA310 - Setup 1 - ESD Diode Current for Applied Input Voltage

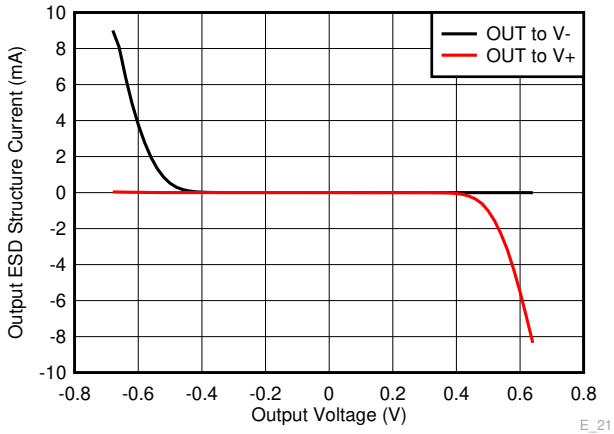


Figure A-2. OPA310 - Setup 1 - ESD Diode Current for Applied Output Voltage

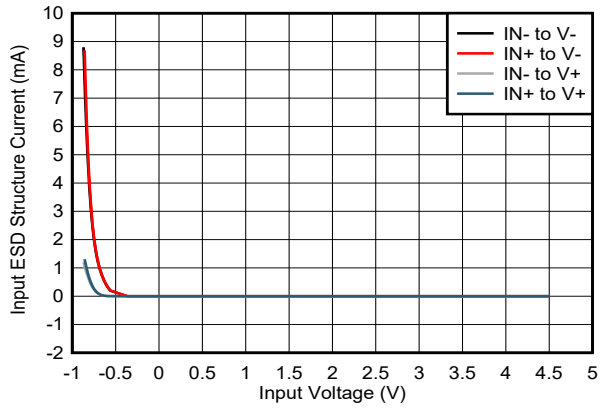


Figure A-3. OPA348 - Setup 1 - ESD Diode Current for Applied Input Voltage

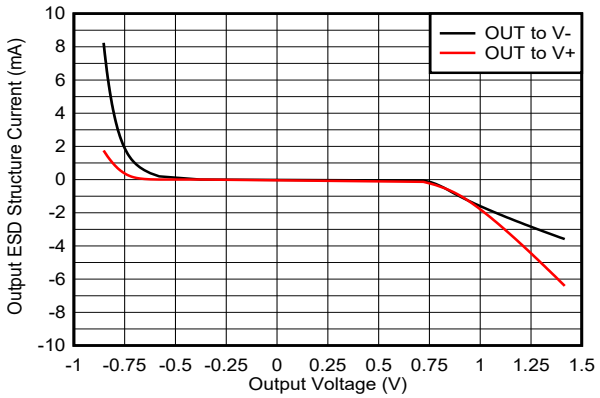


Figure A-4. OPA348 - Setup 1- ESD Diode Current for Applied Output Voltage

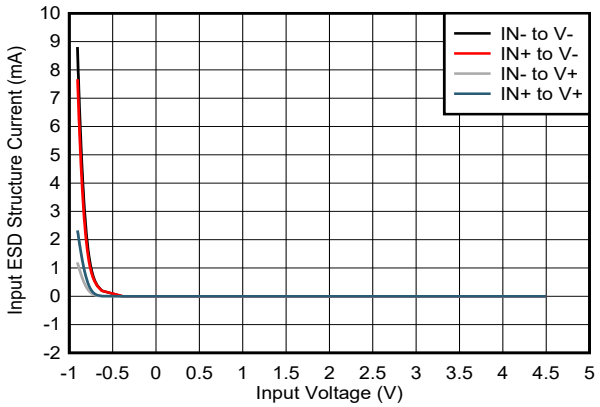


Figure A-5. TLV342/TLV342A - Setup 1- ESD Diode Current for Applied Input Voltage

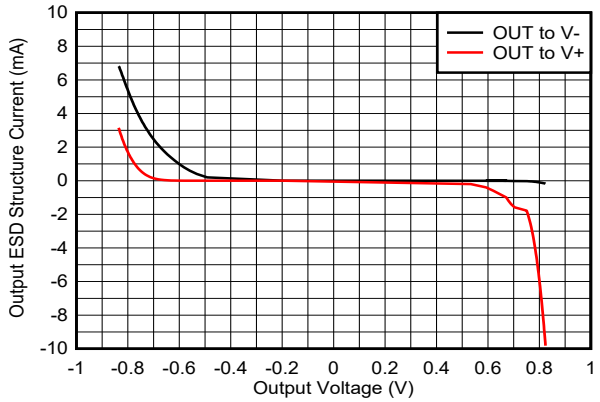


Figure A-6. TLV342/TLV342A - Setup 1 - ESD Diode Current for Applied Output Voltage

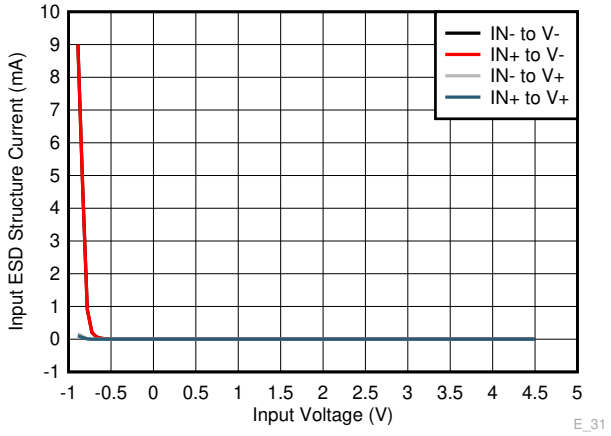


Figure A-7. OPA310 - Setup 2 - ESD Diode Current for Applied Input Voltage

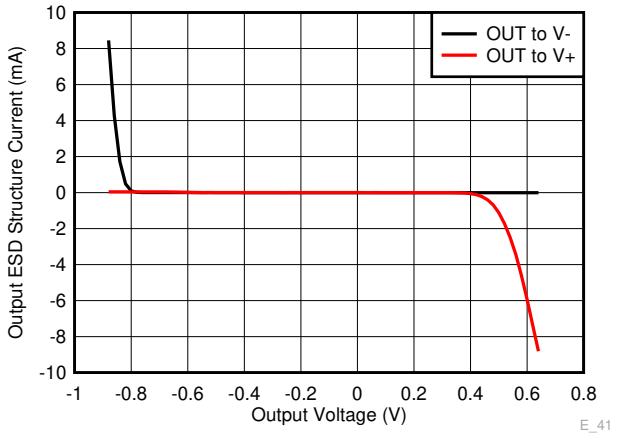


Figure A-8. OPA310 - Setup 2 - ESD Diode Current for Applied Output Voltage

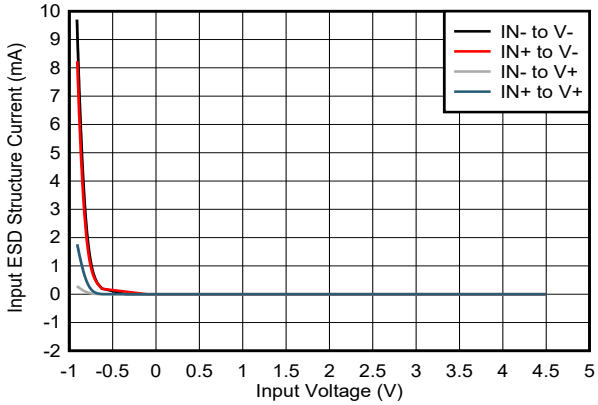


Figure A-9. TLV341/TLV341A - Setup 2 - ESD Diode Current for Applied Input Voltage

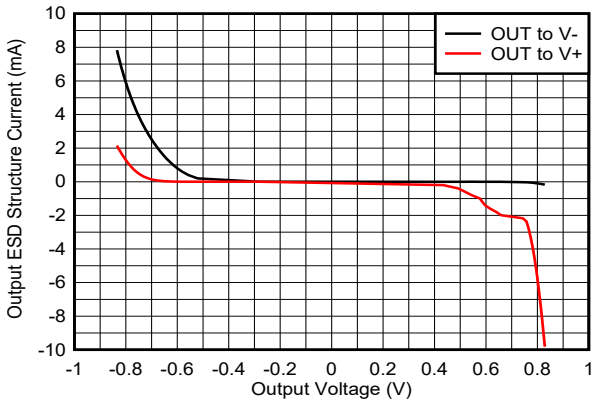


Figure A-10. TLV341/TLV341A - Setup 2 - ESD Diode Current for Applied Output Voltage

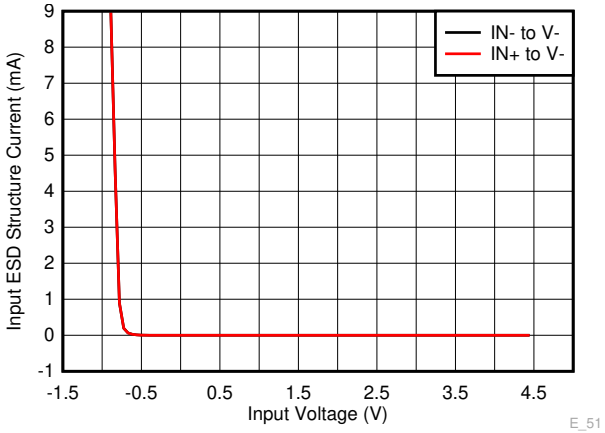


Figure A-11. OPA310 - Setup 3 - ESD Diode Current for Applied Input Voltage

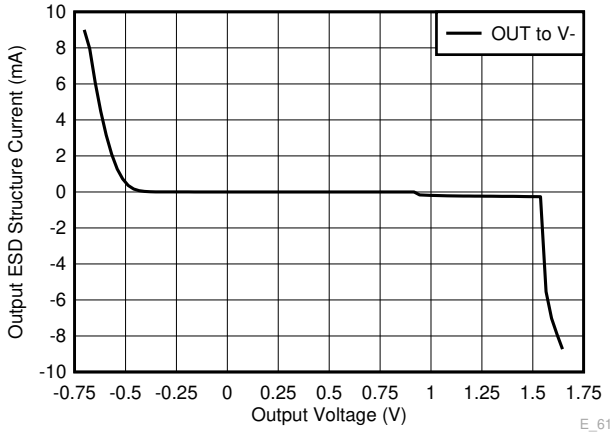


Figure A-12. OPA310 - Setup 3 - ESD Diode Current for Applied Output Voltage

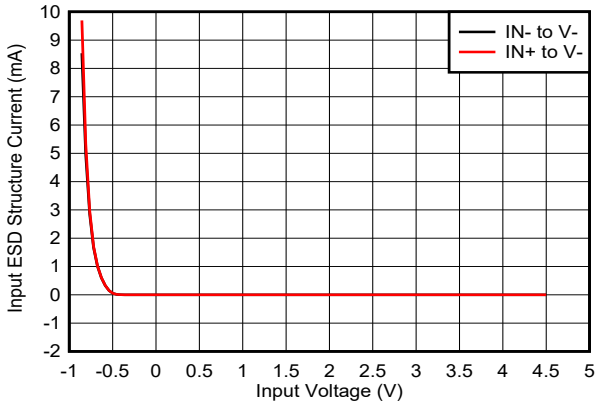


Figure A-13. OPA348 - Setup 3 - ESD Diode Current for Applied Input Voltage

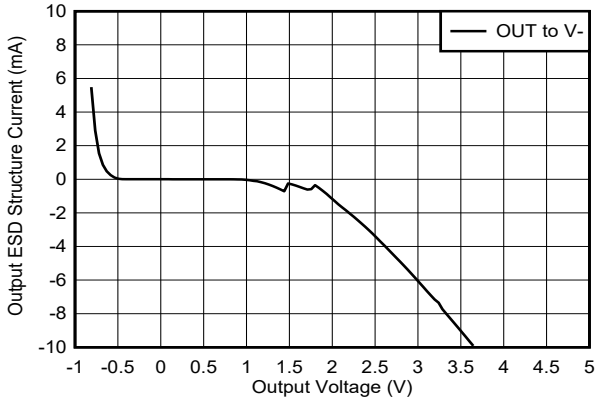


Figure A-14. OPA348 - Setup 3 - ESD Diode Current for Applied Output Voltage

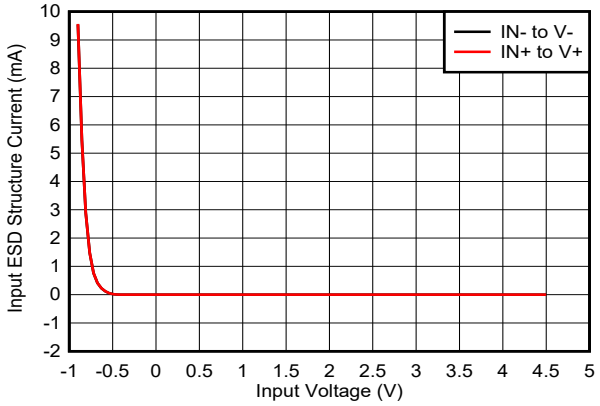


Figure A-15. TLV342/TL342A - Setup 3 - ESD Diode Current for Applied Input Voltage

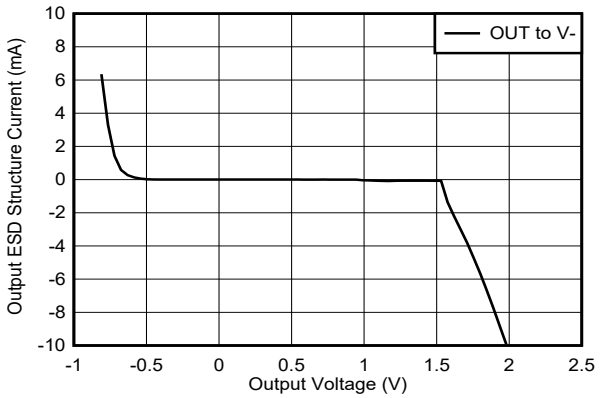


Figure A-16. TLV342/TLV342A - Setup 3 - ESD Diode Current for Applied Output Voltage

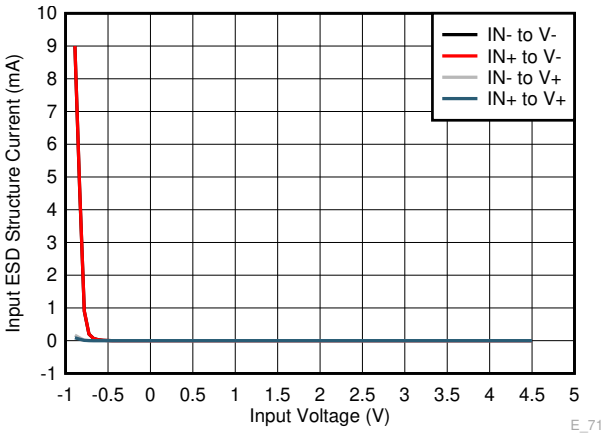


Figure A-17. OPA310 - Setup 4 - ESD Diode Current for Applied Input Voltage

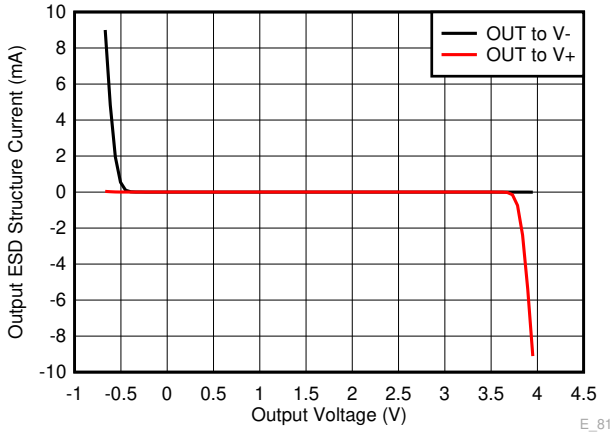


Figure A-18. OPA310 - Setup 4 - ESD Diode Current for Applied Output Voltage

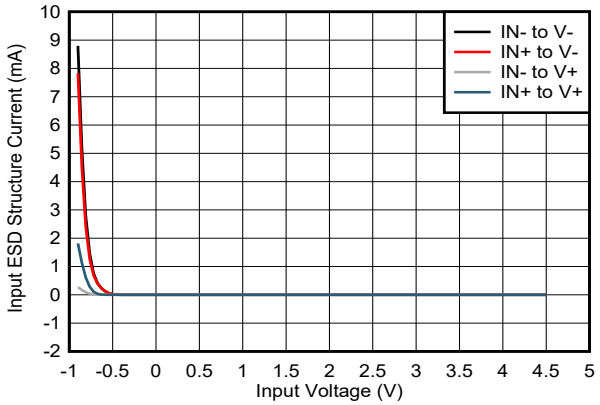


Figure A-19. TLV341/TLV341A - Setup 4 - ESD Diode Current for Applied Input Voltage

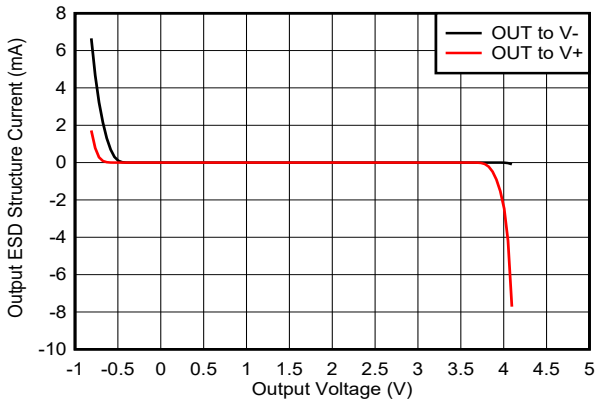


Figure A-20. TLV341/TLV341A - Setup 4 - ESD Diode Current for Applied Output Voltage

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