Functional Safety Information

TPS61175-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS61175-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

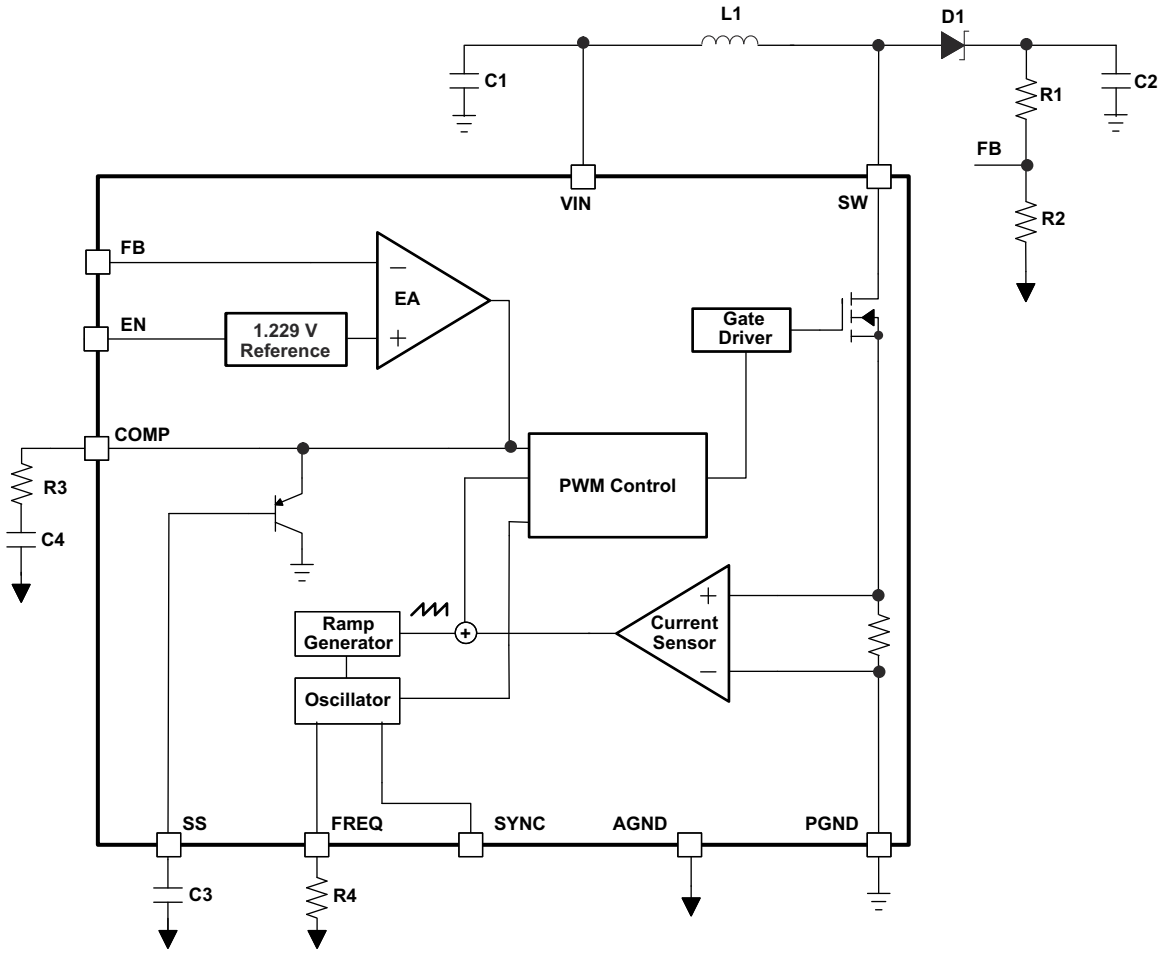

Figure 1-1. Functional Block Diagram

TPS61175-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS61175-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	5
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 550 mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed ≤50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS61175-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35
SW output not in specification voltage or timing	50
SW FET stuck on	5
EN fails or false enable	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS61175-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS61175-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS61175-Q1 datasheet.

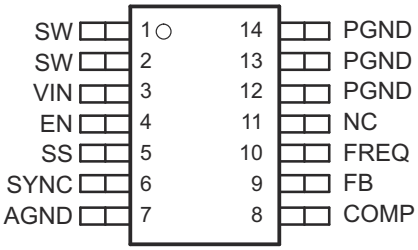

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* sections found in the TPS61175-Q1 datasheet.
- The configuration is as shown in the *Application and Implementation* section found in the TPS61175-Q1 datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	The power supply is short. There is potential damage to the inductor and pin.	A
	2	The power supply is short. There is potential damage to the inductor and pin.	A
VIN	3	The power supply is short. The device does not operate.	B
EN	4	There is a loss of the ENABLE function. The device remains in shut-down mode.	B
SS	5	The device does not operate.	B
SYNC	6	The output voltage is correct. There is a loss of the SYNC function.	C
AGND	7	There is no effect on the device.	D
COMP	8	The device does not operate.	B
FB	9	The output voltage is extremely high. The device is potentially damaged.	A
FREQ	10	The switching frequency is extremely high. The device is potentially damaged.	A
NC	11	There is no effect on the device.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGND	12	There is no effect on the device.	D
	13	There is no effect on the device.	D
	14	There is no effect on the device.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	The device is potentially damaged.	A
	2	The device is potentially damaged.	A
VIN	3	There is a loss of power supply. The device does not operate.	B
EN	4	There is a loss of the ENABLE function. The device remains in shut-down mode.	B
SS	5	There is a loss of the soft start function.	C
SYNC	6	The device is easily coupled by noise.	B
AGND	7	The internal signals have no reference ground. The device is potentially damaged.	A
COMP	8	The output voltage cannot regulate. The device is potentially damaged.	A
FB	9	The output voltage cannot regulate. The device is potentially damaged.	A
FREQ	10	The device does not operate.	B
NC	11	The device is potentially damaged.	A
PGND	12	When one of the repetitive pins is left open, there is no effect to the function of the pin.	D
	13	When one of the repetitive pins is left open, there is no effect to the function of the pin.	D
	14	When one of the repetitive pins is left open, there is no effect to the function of the pin.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SW	1	SW	There is no effect on the device.	D
SW	2	VIN	The device is potentially damaged.	A
VIN	3	EN	The output voltage is correct. There is a loss of the ENABLE function.	C
EN	4	SS	The SS pin is damaged if the voltage of the EN pin is higher than 7V.	A
SS	5	SYNC	The device does not operate.	B
SYNC	6	AGND	The output voltage is correct. There is a loss of the SYNC function.	C
COMP	8	FB	The output voltage cannot regulate. The device is potentially damaged.	A
FB	9	FREQ	The output voltage cannot regulate. The device is potentially damaged.	A
FREQ	10	NC	The switching frequency is extremely high. The output voltage is incorrect.	B
NC	11	PGND	There is no effect on the device.	D
PGND	12	PGND	There is no effect on the device.	D
PGND	13	PGND	There is no effect on the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	The device is potentially damaged.	A
	2	The device is potentially damaged.	A
VIN	3	There is no effect on the device.	D
EN	4	The output voltage is correct. There is a loss of the ENABLE function.	D
SS	5	The SS pin is damaged if the supply voltage is higher than 7V.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SYNC	6	The SYNC pin is damaged if the supply voltage is higher than 7V.	A
AGND	7	There is high current out of the power supply. The device does not operate.	B
COMP	8	The COMP pin is damaged if the supply voltage is higher than 3V.	A
FB	9	The FB pin is damaged if the supply voltage is higher than 3V.	A
FREQ	10	The FREQ pin is damaged if the supply voltage is higher than 3V.	A
NC	11	The device is potentially damaged.	A
PGND	12	There is high current out of the power supply. The device does not operate.	B
	13	There is high current out of the power supply. The device does not operate.	B
	14	There is high current out of the power supply. The device does not operate.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 1, 2020 to November 3, 2025 (from Revision * (June 2020) to Revision A (November 2025)) **Page**

- Updated document title....0
- Added table of contents....0
- Updated the numbering format for tables, figures, and cross-references throughout the document....2
- Added the *Pin Failure Mode Analysis (Pin FMA)* section....5

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