TPS7B63-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TPS7B63-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

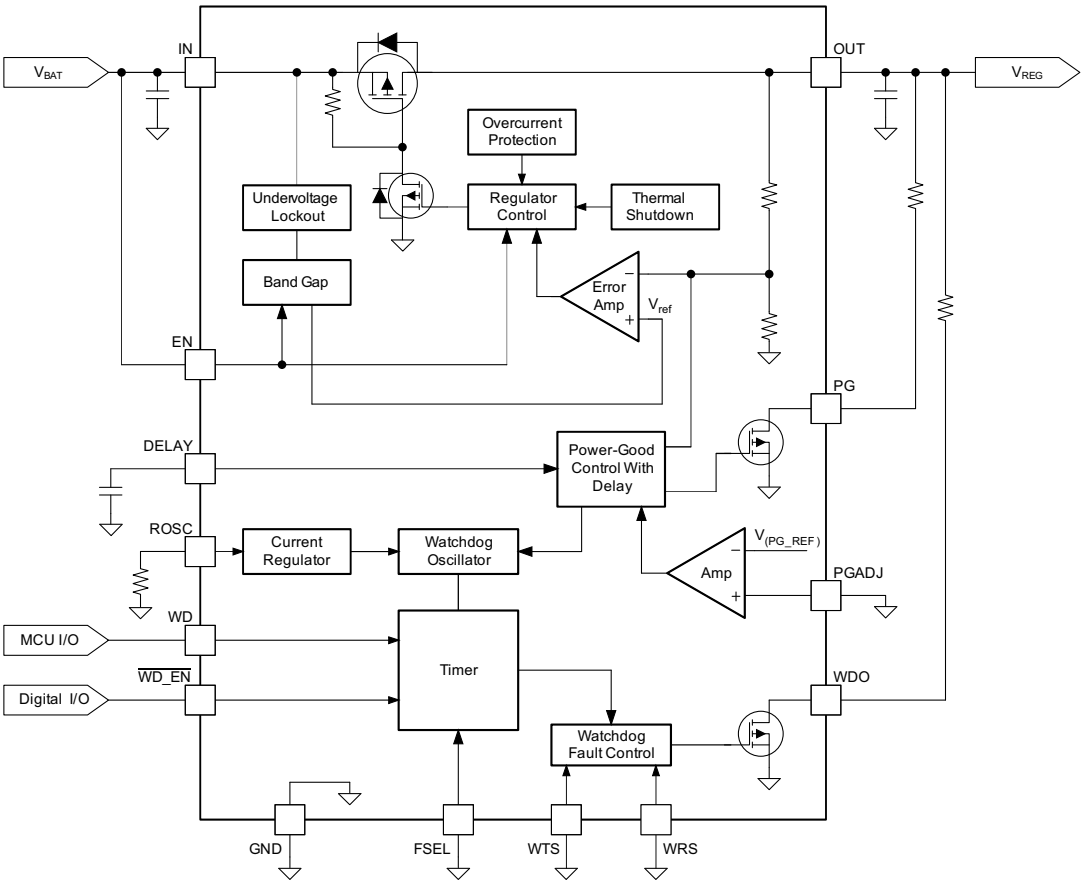

Figure 1. Functional Block Diagram

TPS7B63-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS7B63-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	8
Package FIT Rate	8

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 2700 mW; Delta T_J 65ºC
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog & Mixed ≤ 50 V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS7B63-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No V_{OUT} (V_{OUT} low)	40%
V_{OUT} high (Following V_{IN})	25%
V_{OUT} not in specification	20%
WDO or PG false enable	5%
WDO or PG enable fails	5%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS7B63-Q1 . The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin short-circuited to an adjacent pin (see Table 6)
- Pin short-circuited to supply (see Table 7)

Table 5 through Table 7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the TPS7B63-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS7B63-Q1 datasheet.

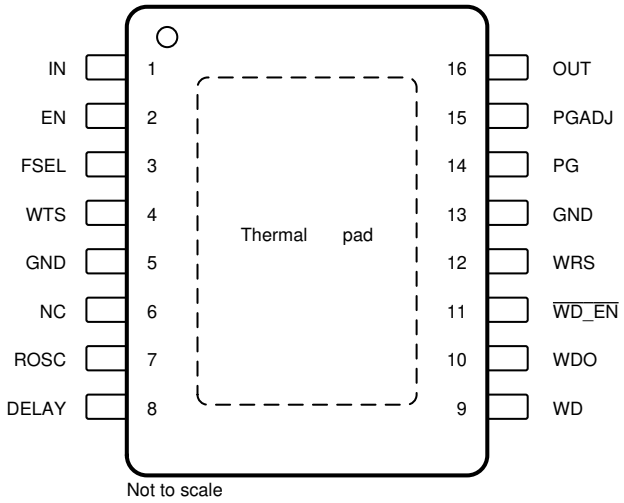

Figure 2. Pin Diagram

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	IN	Output will be at or near GND.	B
2	EN	Device will be disabled.	B
3	FSEL	Select the high-frequency oscillator.	D
4	WTS	Select the window watchdog timer.	D
5	GND	N/A	D
6	NC	No impact.	D
7	ROSC	A fault will be reported at WDO.	B
8	DELAY	PG delay timer will not work; PG will never assert high.	B
9	WD	The watchdog timer will not receive the service-signal and report an error.	B
10	WDO	WDO will not be able to assert high.	B
11	/WD_EN	The watchdog timer is enabled.	D
12	WRS	Set the watchdog window ratio to 8:1.	D
13	GND	N/A	D
14	PG	PG will not be able to assert high.	B
15	PGADJ	Set the PG threshold to 91.6% of V_{OUT}.	D
16	OUT	Output will be at or near GND. If IN is biased, the device will be in current limit. It may cycle in and out of thermal shutdown depending on the power dissipation.	B

Table 6. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	2 - EN	LDO will startup when V_{IN} is above EN threshold. LDO will shut down when V_{IN} is below the EN threshold.	D
EN	2	3 - FSEL	Device can be enabled or disabled depending on FSEL pin voltage. The low-frequency or high-frequency oscillator can be selected depending on the EN pin voltage.	B
FSEL	3	4 - WTS	The low-frequency or high-frequency oscillator can be selected depending on the WTS pin voltage. The standard or window watchdog timer can be selected depending on the FSEL pin voltage.	C
WTS	4	5 - GND	Selects the window watchdog timer.	C
GND	5	6 - NC	No impact.	D
NC	6	7 - ROSC	No impact.	D
ROSC	7	8 - DELAY	A fault can be reported at WDO depending on the DELAY pin voltage. PG will not have a delay.	B
WD	9	10 - WDO	The watchdog service signal could drive WDO to go low and the watchdog function will be affected.	C
WDO	10	11 - /WD_EN	WDO flag state may be incorrect depending on the WDO pin voltage.	C
/WD_EN	11	12 - WRS	Depending on the driving capabilities of the supplies/GND on these pins, the watchdog function could be off when both pins are driving high; the watchdog function could be on with open:closed windows ratio to 1:1.	C
WRS	12	13 - GND	Sets the watchdog window ratio to 8:1.	D
GND	13	14 - PG	PG will not be able to assert high.	B
PG	14	15 - PGADJ	PG flag state may be incorrect depending on the PGADJ pin voltage. PGADJ threshold may be affected.	C
PGADJ	15	16 - OUT	The PG function will be affected because PGADJ voltage will be set by the OUT voltage instead of by the internal charging circuit.	C

Table 7. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	IN	N/A	D
2	EN	LDO will startup when V_{IN} is above EN threshold. LDO will shut down when V_{IN} is below the EN threshold.	D
3	FSEL	Selects the low-frequency oscillator.	D
4	WTS	Selects the standard watchdog timer.	D
5	GND	Output will be at or near GND.	B
6	NC	No impact.	D
7	ROSC	Watchdog timer will not operate properly. ROSC will become damaged if V_{IN} exceeds ROSC maximum voltage.	A
8	DELAY	PG will not have a delay. DELAY will become damaged if V_{IN} exceeds DELAY maximum voltage.	A
9	WD	The watchdog timer will not receive the service-signal and report an error. WD will become damaged if V_{IN} exceeds WD maximum voltage.	A
10	WDO	WDO will not be able to assert low. WDO will become damaged if V_{IN} exceeds WDO maximum voltage.	A
11	/WD_EN	Disables the watchdog timer. WD_EN will become damaged if V_{IN} exceeds WD_EN maximum voltage.	A
12	WRS	Set the watchdog window ratio to 1:1. WRS will become damaged if V_{IN} exceeds WRS maximum voltage.	A
13	GND	Output will be at or near GND.	B
14	PG	PG will not be able to asset low. PG will become damaged if V_{IN} exceeds PG maximum voltage.	A
15	PGADJ	PGADJ will become damaged if V_{IN} exceeds PGADJ maximum voltage.	A
16	OUT	No V_{OUT} regulation. Output is the same as the input voltage. OUT will become damaged if V_{IN} exceeds OUT maximum voltage.	A

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2019) to A Revision	Page
• Added *Component Failure Rates per Siemens Norm SN 29500-2* table and a pin FMEA table	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265