Functional Safety Information

TPS7B68-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7B68-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

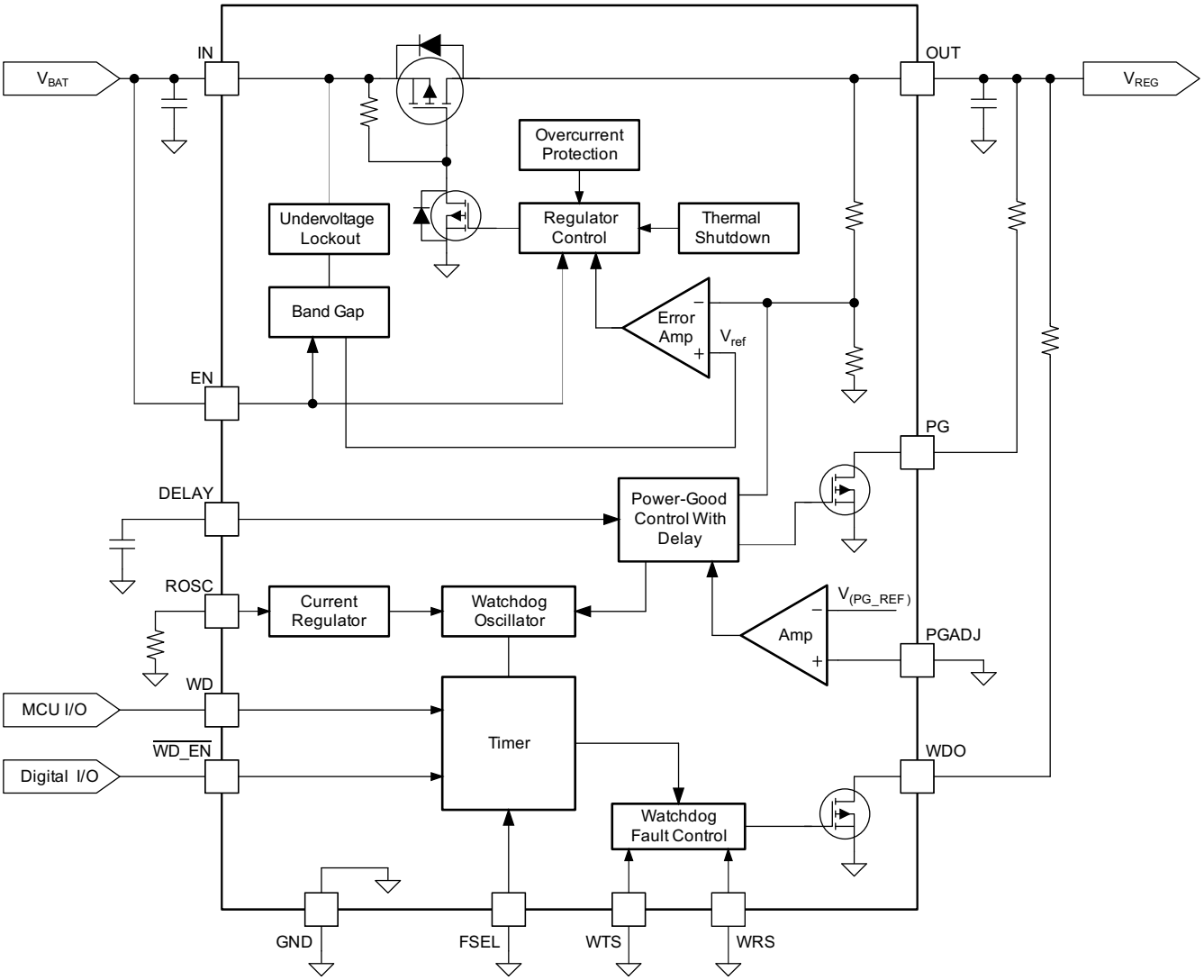

Figure 1-1. Functional Block Diagram

The TPS7B68-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B68-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	4
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and mixed ≤ 50-V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B68-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	55
VOUT not in specification (voltage or timing)	10
VOUT low (no output)	15
Short circuit any two pins	10
PG not in specification (voltage or timing)	5
WDO not in specification (voltage or timing)	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B68-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7B68-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B68-Q1 data sheet.

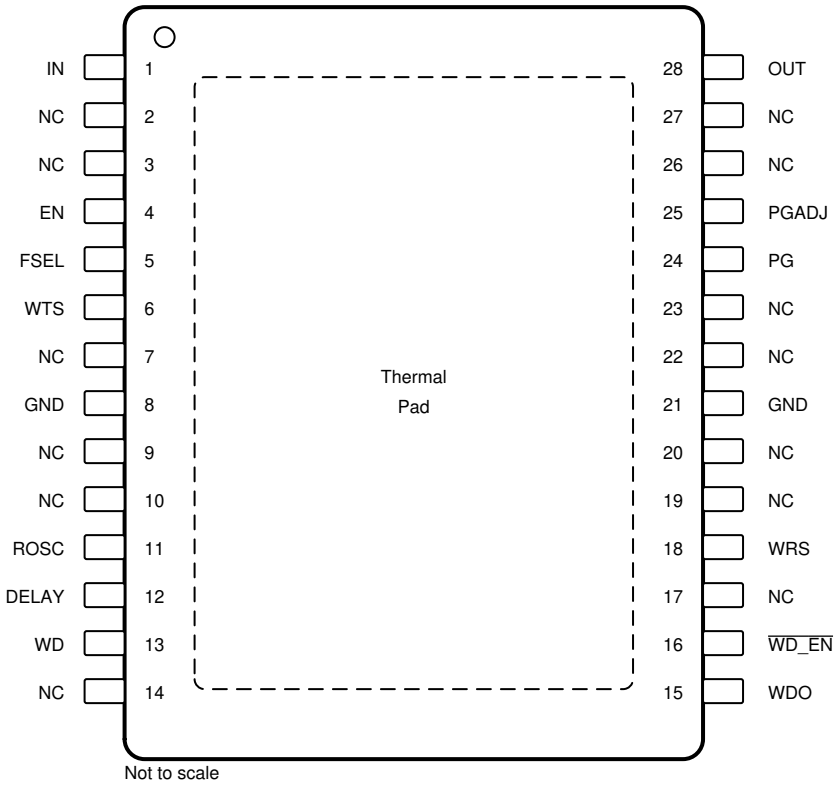

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating within ROC conditions
- The watchdog is being serviced correctly following the EC table specifications

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No power is supplied to the device, resulting in no output voltage.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
EN	4	The device is disabled, resulting in no output voltage.	B
FSEL	5	The device operates with the high-frequency oscillator selected.	B
WTS	6	The device operates with the window watchdog-timer.	B
NC	7	No effect. Normal operation.	D
GND	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
ROSC	11	A fault is reported at WDO.	B
DELAY	12	The power-good delay becomes infinite. PG is unable to assert high.	B
WD	13	Watchdog functionality is never serviced, resulting in error reported at WDO.	B
NC	14	No effect. Normal operation.	D
WDO	15	Watchdog cannot assert high.	B
$\overline{\text{WD\_EN}}$	16	Watchdog functionality is always enabled.	B
NC	17	No effect. Normal operation.	D
WRS	18	Sets the open:closed window ratio to 1:1.	B
NC	19	No effect. Normal operation.	D
NC	20	No effect. Normal operation.	D
GND	21	No effect. Normal operation.	D
NC	22	No effect. Normal operation.	D
NC	23	No effect. Normal operation.	D
PG	24	PG is unable to assert high.	B
PGADJ	25	Sets the PG threshold to 91.6% of VOUT.	B
NC	26	No effect. Normal operation.	D
NC	27	No effect. Normal operation.	D
OUT	28	Regulation is not possible, the device operates at current limit and can cycle in and out of thermal shutdown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No power is supplied to the device, resulting in no output voltage.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
EN	4	The enable circuit is in an unknown state. The device is either enabled or disabled.	B
FSEL	5	The frequency-select circuitry is in an unknown state. The watchdog timer window is either high-frequency or low-frequency.	B
WTS	6	The watchdog type selection circuitry is in an unknown state. The watchdog is either in windowed mode or standard operation.	B
NC	7	No effect. Normal operation.	D
GND	8	There is no current loop for the supply voltage. The device is not operational and does not regulate. There is also a possibility that the absolute maximum value of the device pins are exceeded, causing internal damage to the transistors.	A
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
ROSC	11	A fault is reported at WDO.	B
DELAY	12	The power-good circuitry responds with no delay.	B
WD	13	The watchdog timer does not receive the service-signal and reports an error at WDO.	B
NC	14	No effect. Normal operation.	D
WDO	15	The watchdog output signal is unconnected and unreadable. The watchdog output on the device is not representative of the watchdog fault control behavior.	B
$\overline{\text{WD\_EN}}$	16	The watchdog enable circuitry is in an unknown state. The watchdog is either enabled or disabled.	B
NC	17	No effect. Normal operation.	D
WRS	18	(Standard watchdog operation.) No effect. Normal operation. (Window watchdog operation.) The watchdog ratio select circuitry is in an unknown state. The watchdog ratio is either 1:1 or 8:1.	D/B
NC	19	No effect. Normal operation.	D
NC	20	No effect. Normal operation.	D
GND	21	There is no current loop for the supply voltage. The device is not operational and does not regulate. There is also a possibility that the absolute maximum value of the device pins are exceeded, causing internal damage to the transistors.	A
NC	22	No effect. Normal operation.	D
NC	23	No effect. Normal operation.	D
PG	24	The PG signal is unconnected and unreadable. The PG flag state on the device is not representative of VOUT.	B
PGADJ	25	The PGADJ circuitry is in an unknown state. The PG trip threshold is unknown and the PG output becomes unreliable.	B
NC	26	No effect. Normal operation.	D
NC	27	No effect. Normal operation.	D
OUT	28	The device output is disconnected from the load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	NC (pin 2)	No effect. Normal operation.	D
NC	2	NC (pin 3)	No effect. Normal operation.	D
NC	3	EN (pin 4)	No effect. Normal operation.	D
EN	4	FSEL (pin 5)	The device can be enabled or disabled depending on the FSEL pin voltage. The low-frequency or high-frequency oscillator option can be selected depending on the EN pin voltage.	B
FSEL	5	WTS (pin 6)	The low-frequency or high-frequency oscillator option can be selected depending on the WTS pin voltage. The standard or window watchdog timer can be selected depending on the FSEL pin voltage.	B
WTS	6	NC(pin 7)	No effect. Normal operation.	D
NC	7	GND (pin 8)	No effect. Normal operation.	D
GND	8	NC (pin 9)	No effect. Normal operation.	D
NC	9	NC (pin 10)	No effect. Normal operation.	D
NC	10	ROSC (pin 11)	No effect. Normal operation.	D
ROSC	11	DELAY (pin 12)	A fault can be reported at WDO depending on the DELAY pin voltage. PG has no delay.	B
DELAY	12	WD (pin 13)	The PG delay time is affected depending on the WD pin voltage. The watchdog timer does not receive a service-signal properly, causing a fault to be output at WDO.	B
WD	13	NC (pin 14)	No effect. Normal operation.	D
WDO	15	$\overline{\text{WD\_EN}}$ (pin 16)	The WDO flag state is always low if enabled, and is DNC when disabled. The watchdog can be disabled or enabled depending on the voltage level of the WDO pin.	B
$\overline{\text{WD\_EN}}$	16	NC (pin 17)	No effect. Normal operation.	D
NC	17	WRS (pin 18)	No effect. Normal operation.	D
WRS	18	NC (pin19)	No effect. Normal operation.	D
NC	19	NC (pin 20)	No effect. Normal operation.	D
NC	20	GND (pin 21)	No effect. Normal operation.	D
GND	21	NC (pin 22)	No effect. Normal operation.	D
NC	22	NC (pin 23)	No effect. Normal operation.	D
NC	23	PG (pin 24)	No effect. Normal operation.	D
PG	24	PGADJ (pin 25)	The PG flag state can be incorrect, depending on the PGADJ pin voltage. The PGADJ threshold can be affected.	B
PGADJ	25	NC (pin 26)	No effect. Normal operation.	D
NC	26	NC (pin 27)	No effect. Normal operation.	D
NC	27	OUT (pin 28)	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
EN	4	The device is always on when VIN is supplied.	B
FSEL	5	The device operates with the low-frequency oscillator when VIN is supplied.	B
WTS	6	The device operates with the standard watchdog timer when VIN is supplied.	B
NC	7	No effect. Normal operation.	D
GND	8	No output voltage. System performance depends on upstream current limiting.	B
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
ROSC	11	The watchdog timer does not operate properly. ROSC becomes damaged if VIN exceeds the ROSC maximum voltage.	A
DELAY	12	PG does not have a delay. PG becomes damaged if VIN exceeds the PG maximum voltage.	A
WD	13	The watchdog timer does not receive the service signal and reports and error at WDO. WD becomes damaged if VIN exceeds the WD maximum voltage.	A
NC	14	No effect. Normal operation.	D
WDO	15	WDO is unable to assert low. WDO becomes damaged if VIN exceeds the WDO maximum voltage.	A
$\overline{\text{WD\_EN}}$	16	The watchdog timer is always disabled. $\overline{\text{WD\_EN}}$ becomes damaged if VIN exceeds the $\overline{\text{WD\_EN}}$ maximum voltage.	A
NC	17	No effect. Normal operation.	D
WRS	18	Sets the watchdog window ratio to 1:1. WRS becomes damaged if VIN exceeds the WRS maximum voltage.	A
NC	19	No effect. Normal operation.	D
NC	20	No effect. Normal operation.	D
GND	21	No output voltage. System performance depends on upstream current limiting.	B
NC	22	No effect. Normal operation.	D
NC	23	No effect. Normal operation.	D
PG	24	PG is unable to assert low. PG becomes damaged if VIN exceeds the PG maximum voltage.	A
PGADJ	25	PGADJ becomes damaged if VIN exceeds the PGADJ maximum voltage.	A
NC	26	No effect. Normal operation.	D
NC	27	No effect. Normal operation.	D
OUT	28	No VOUT regulation. Output voltage is the same as the input voltage. OUT becomes damaged if VIN exceeds the OUT maximum voltage.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (October 2022)	Page
• Changed entire document and added *pin FMA* information	2

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265