

# How to Cascade Multiple UCD90xxx Sequencers

Yihe Hu

## ABSTRACT

The UCD90xxx family of digital power supply sequencers, also known as system health monitors are flexible and powerful enough to meet users sequencing, monitoring, margining, and other needs. TI's [Fusion Digital Power™](#) designer is a dedicated Graphical User Interface (GUI) tool that helps users configure and monitor UCD90xxx sequencers and health monitors with limited coding knowledge.

In the advanced application, the system requires more rails than a single UCD90xxx can support. Therefore, multiple UCD90xxx devices are required. This document is to describe how to cascading multiple to ensure that proper sequencing across these devices.

## Contents

1	Function Required for Cascading.....	2
2	Cascading Multiple UCD90xxx .....	11
3	Conclusion .....	13

## List of Figures

1	Boolean Logic Combination .....	2
2	System POWER_GOOD Logic Builder .....	3
3	System POWER_GOOD_OFF Logic Builder .....	3
4	Sequencing On and Off Dependencies .....	4
5	Fault Shutdown Slaves .....	5
6	GPI Fault Response for UCD9090A and UCD90160A .....	6
7	GPI Fault Response For UCD90240 and UCD90320 - Step 1 .....	7
8	GPI Fault Response for UCD90240 and UCD90320 - Step 2 .....	8
9	Fault Pin Configuration for UCD9090A and UCD90160A .....	9
10	Configure Fault Pin UCD90240 and UCD90320 - Step 1 .....	10
11	Configure Fault Pin UCD90240 and UCD90320 - Step 2 .....	10
12	POWER_GOOD Cascading Case 1 .....	11
13	Power Good Cascading Case 2.....	12
14	POWER_GOOD and POWER_GOOD_OFF Cascading .....	12
15	Fault Pin Cascading.....	13

## List of Tables

1	Sequencing Dependencies Events .....	4
---	--------------------------------------	---

## Trademarks

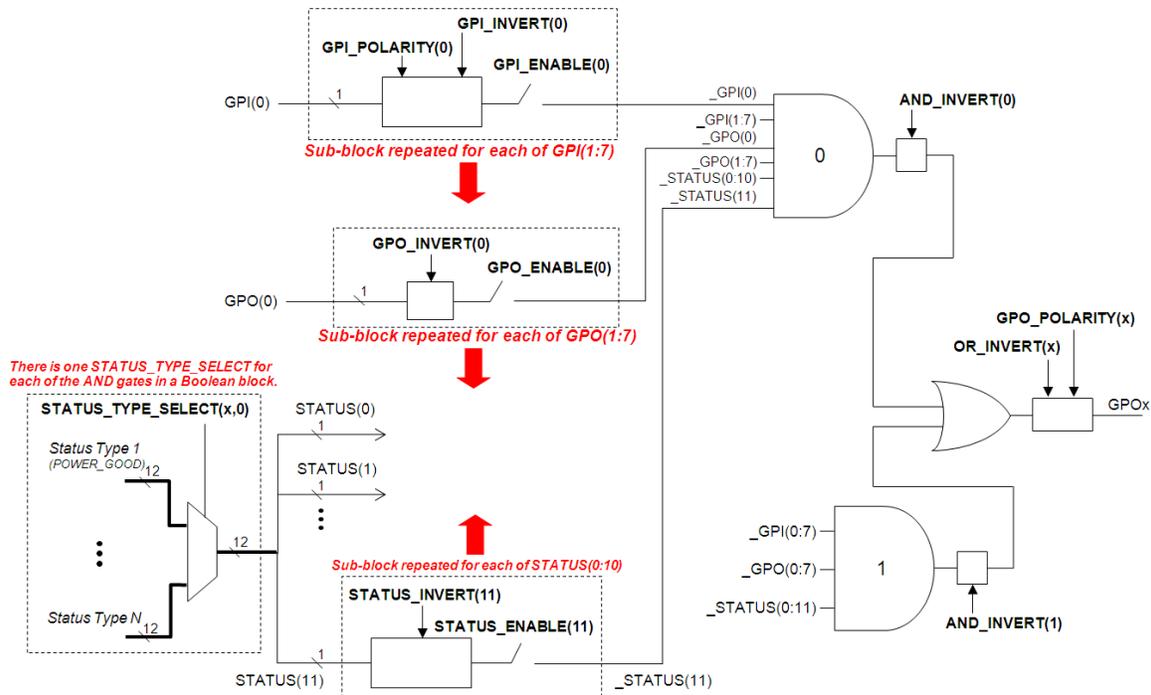
Fusion Digital Power is a trademark of Texas Instruments.  
 All other trademarks are the property of their respective owners.

## 1 Function Required for Cascading

The following features are required to implement cascading among multiple UCD90xxx devices:

### 1.1 Logical Controlled GPO (LGPO)

All UCD90xxx devices have a feature called logic general-purpose output (LGPO). General-purpose I/Os (GPIO) can be configured as outputs that are based on the Boolean combination of up to two ANDs, ORed together as shown in Figure 1. Inputs to the logic blocks can include the first 8 defined LGPOs, general-purpose inputs (GPI), and rail-status flags. One rail status type is selectable as an input for each AND gate.



**Figure 1. Boolean Logic Combination**

With LGPO function, a proper signal can be generated based on the rail status from any given UCD90xxx device in the chain. So the other UCD device can determine this if the signal is connected to GPI pins. Figure 2 and Figure 3 demonstrates how to configure a GPIO to output when all rails are reaching POWER\_GOOD and POWER\_GOOD\_OFF, respectively.

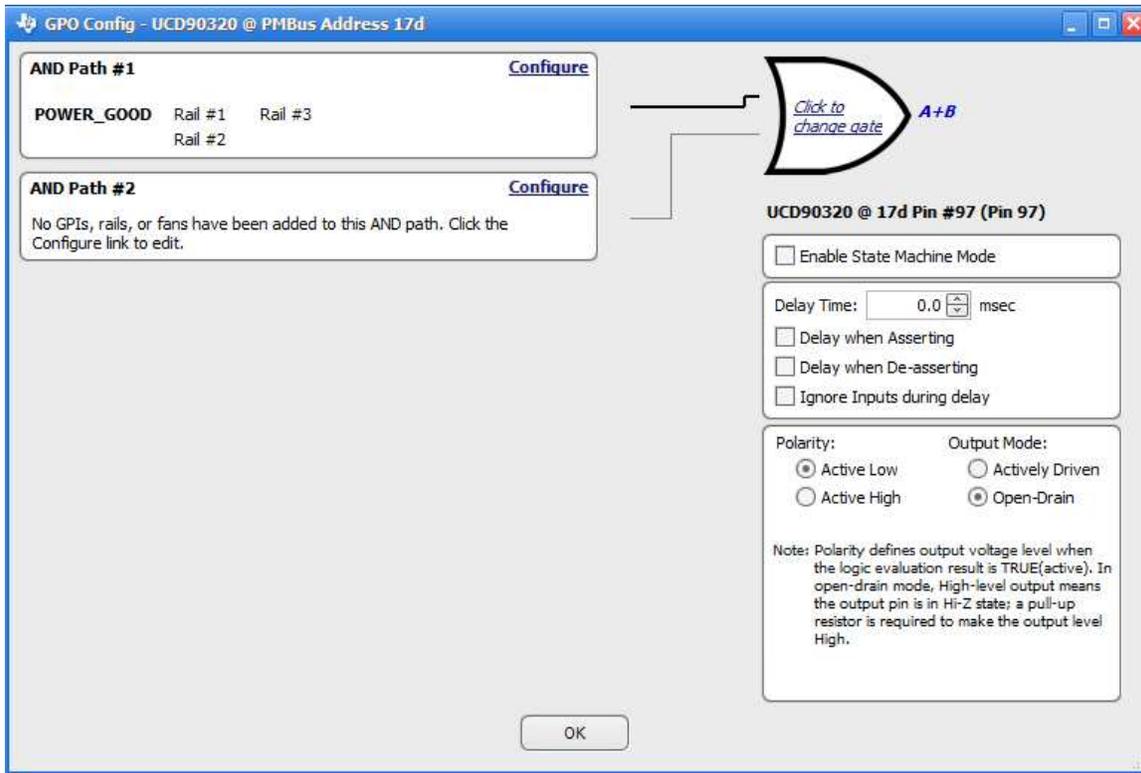


Figure 2. System POWER\_GOOD Logic Builder

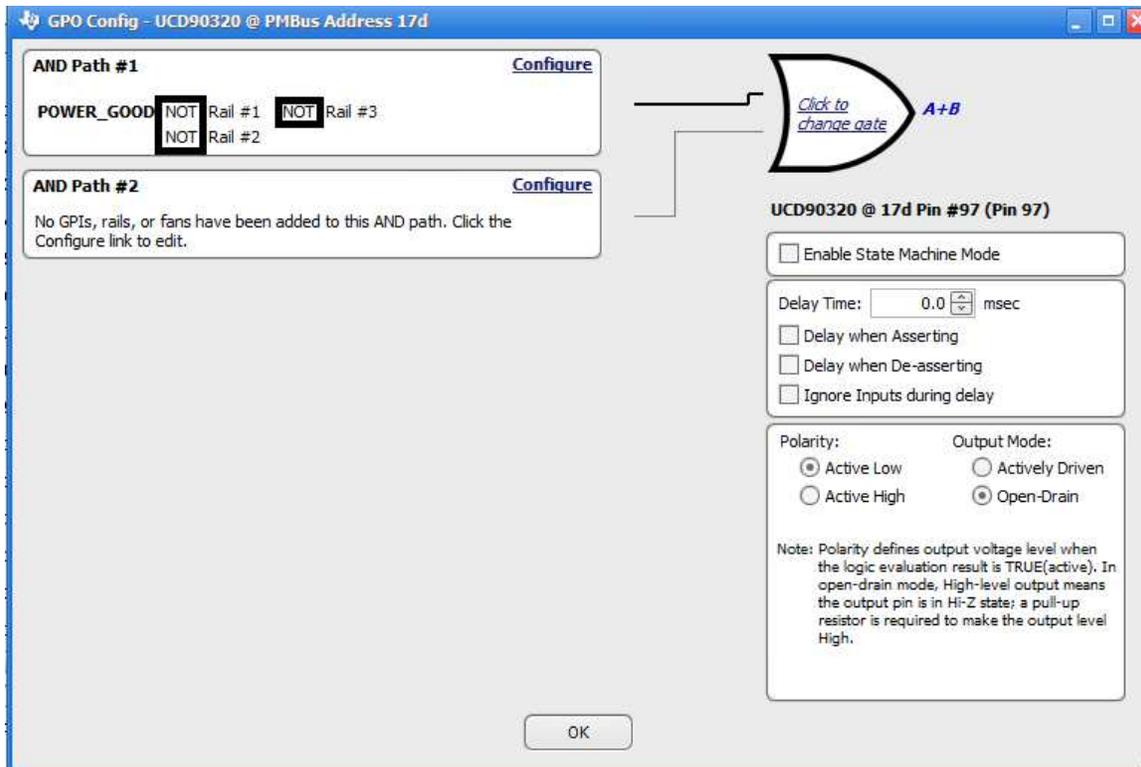


Figure 3. System POWER\_GOOD\_OFF Logic Builder

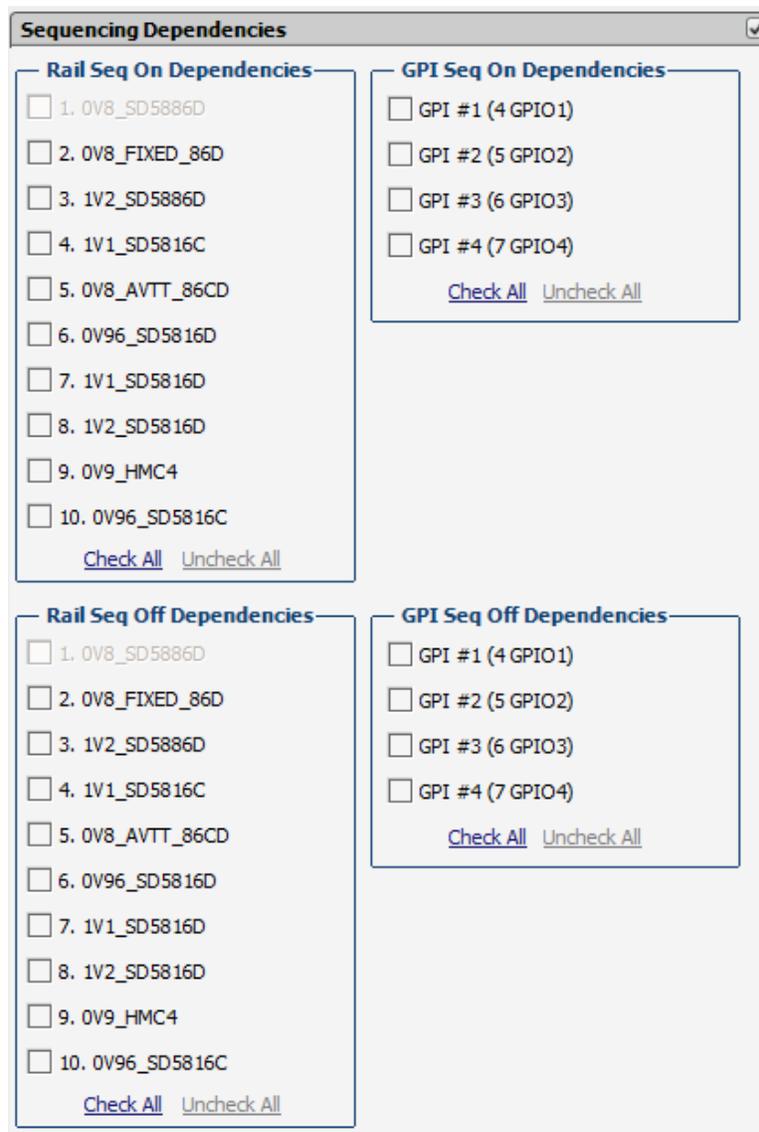
## 1.2 Sequencing On and Off Dependencies

The other important feature to cascade is the sequencing on and off dependencies (Figure 4). Those rails that have dependencies will not be on or off, unless the dependencies are met.

**Table 1. Sequencing Dependencies Events**

Event	Rail		GPI	LGPO
Sequence ON condition met	Voltage monitoring: Above POWER_GOOD threshold	Other monitoring: EN signal is asserted	ASSERTED <sup>(1)</sup>	The logic output is TRUE
Sequence OFF condition met	Voltage monitoring: Below POWER_GOOD_OFF threshold	Other monitoring: EN signal is de-asserted	DE-ASSERTED <sup>(1)</sup>	The logic output is FALSE

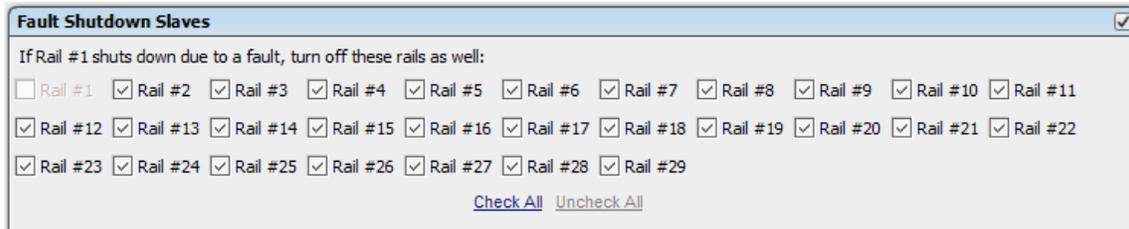
<sup>(1)</sup> The input signal is ASSERTED if it matches the defined active polarity, otherwise it is DE-ASSERTED.



**Figure 4. Sequencing On and Off Dependencies**

### 1.3 UV, GPI Fault Response

All analog Monitor pin can be used to monitor digital signal such as POWER\_GOOD output from other devices. A proper external voltage divider is required to meet the ADC reference. The de-assertion of a POWER\_GOOD output can trigger a UV fault of the next device. When device detects the UV fault, the UV fault response of the rail can be configured to shut down other rails controlled by the same UCD90xxx device via setting other rails as fault shutdown slaves of the faulted rail.



**Figure 5. Fault Shutdown Slaves**

The UCD9090A, UCD90160A, UCD90240, and UCD90320 devices support GPI fault response; therefore, the POWER\_GOOD output signal can be connected to GPI instead of MON to save the MON for normal monitoring. The de-assertion of the POWER\_GOOD output can trigger GPI fault on the next device. The fault response of the GPI fault can be configured to shut down rails controlled by the same device. Configure the GPI fault response as shown in the following paragraphs. There are some differences to set the GPI fault response between the UCD9090A, UCD90160A and the UCD90240, UCD90320.

For the UCD9090A and UCD90160A, the Fault response is centralized at GPI configure as shown in [Figure 6](#). Only one GPI can be assigned to have Fault response.

But for UCD90240 and UCD90320 devices, the Fault response is separated into two places. The user first must enable the GPI Fault Enable feature on the GPI Configure as shown in [Figure 7](#). Next, select the corresponding response for the given rail as shown in [Figure 8](#). All GPI can be assigned to have the fault response function.

**Configure**

GPI Polarity:  Active Low  Active High

Note: Polarity defines output voltage level when the logic evaluation result is TRUE(active). In open-drain mode, High-level output means the output pin is in Hi-Z state; a pull-up resistor is required to make the output level High.

**GPI Fault Enable**  
When this bit is set, the de-assertion of the GPI is treated as fault and can shutdown rails if together either "Fault Shutdown Rails" or "Fault Pin" bit is also set.

Latched Statuses Clear Source  
When a GPO uses a latched status type (\_LATCH) , you can configure a GPI that will clear the latched status.

Input Source for Margin Enable  
When the Margin Enable pin is asserted, this pin determines if the margined state is low or high.

Input Source for Margin Low/Not-High  
When this pin is asserted, all rails with margining enabled will be put in a margined state (low or high).

**Fault Shutdown rails**  
When this bit and the GPI Fault Enable bit are set, the de-assertion of the GPI is treated as fault and can be used to shutdown rails according to the below Fault Responses setting

How device responds to GPI fault:  
Max glitch time: 0.5 ms  
Resequencing: Enabled; Glitch filter: Disabled; Response: Shut down immediately; Restart: Do not restart Edit

When pin has fault, will shut down these rails:  
 Rail 01  Rail 02  Rail 03  Rail 04  
 Rail 05  Rail 06  Rail 07  Rail 08  
 Rail 09  Rail 10

**Options**

Enable glitch filter  
If checked, when the fault is first detected the device continues operation for the per-rail GPI max glitch time, Disabled. If the fault is still present after this time, the response configured below is taken.

**Enable re-sequencing**  
If checked, when the retries have been exhausted the associated rail and any Fault Slaves will be shutdown in a manner based on the Response selected. There will be a delay, and then all of those rails will be re-sequenced.

**Response**

Ignore fault and continue operation  
 Shut down immediately  
 Shut Down with delay configured using TOFF\_DELAY

**Restart**

Do not restart  
The unit does not attempt to restart. The output remains disabled until the fault is cleared.

Restart up to 1 times  
The device attempts to restart up to the specified number of times, with a maximum of 14 restarts permitted.  
If the device fails to restart in the allowed number of retries, it disables the output and remains off until the fault is cleared.  
The time between each restart attempt is configured globally for the rail  
If configured to restart and the rail does not come back within regulation, the TON\_MAX fault response will apply.

Restart continuously  
The device attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

Figure 6. GPI Fault Response for UCD9090A and UCD90160A

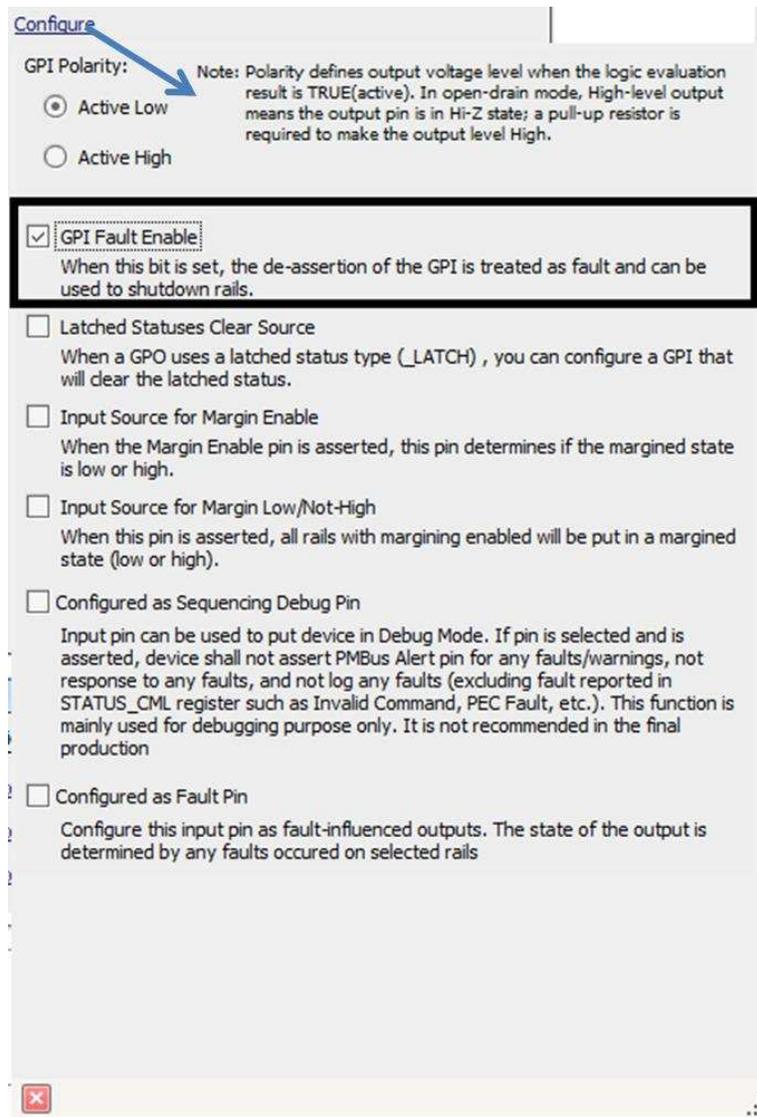


Figure 7. GPI Fault Response For UCD90240 and UCD90320 - Step 1

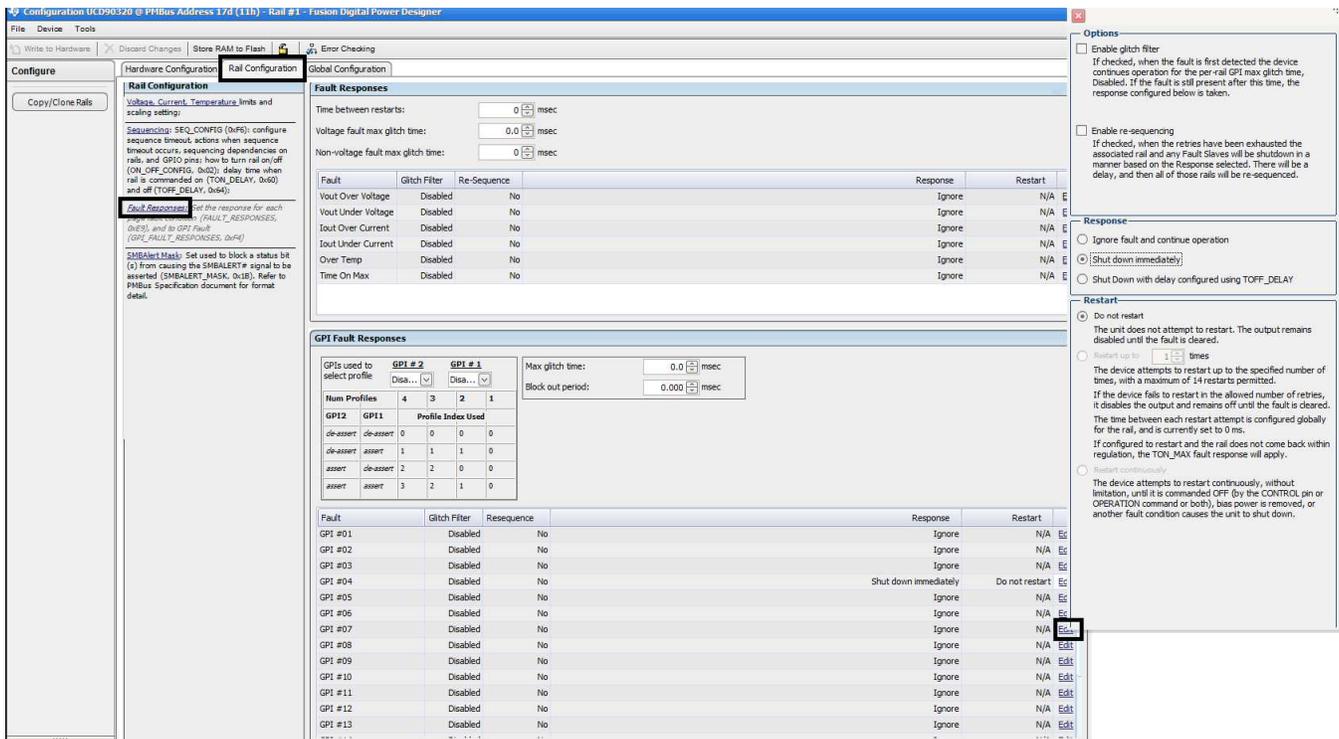


Figure 8. GPI Fault Response for UCD90240 and UCD90320 - Step 2

## 1.4 Fault Pin

The UCD9090A, UCD90160A, UCD90240, and UCD90320 devices support the FAULT PIN feature. Fault pin is a bi-directional signal and can form a fault bus when pulled up to 3.3 V. When there is no fault on a Fault Bus, the Fault Pins are digital input pins and respond to the Fault Bus. When one or multiple UCD devices detect a rail fault, the corresponding Fault Pin is turned into active driven low state, pulling down the Fault Bus and communicating to all other UCD devices of the corresponding fault. This way, a coordinated action can be taken across multiple devices. After the fault is cleared, the state of the Fault Pin of the given device is turned back to an input pin. There are some differences to set GPI fault response between the UCD9090A, UCD90160A devices and the UCD90240, UCD90320 devices.

For the UCD9090A and UCD90160A devices, only one GPI pin can be assigned as FAULT PIN, the configuration of the fault pin is shown in Figure 9. For the UCD90240 and UCD90320 device, the fault pin configuration is separated at three places. Please follow Figure 10 to enable the GPI fault and Fault Pin (UCD90320 Only). Figure 11 demonstrates how to configure a Fault pin, for UCD90240, the Fault pin selection is done at this step. Once previous two steps, please follow Figure 8 to configure the corresponding fault response for the fault pin.

**Must check this box** →  GPI Fault Enable

**Configure which rails impact Fault pin out** →

When these rails have fault, will output signal on pin:

<input checked="" type="checkbox"/> Rail 01	<input checked="" type="checkbox"/> Rail 02	<input checked="" type="checkbox"/> Rail 03	<input checked="" type="checkbox"/> Rail 04
<input checked="" type="checkbox"/> Rail 05	<input checked="" type="checkbox"/> Rail 06	<input type="checkbox"/> Rail 07	<input type="checkbox"/> Rail 08
<input type="checkbox"/> Rail 09	<input type="checkbox"/> Rail 10		

**Configure which rails respond the external Fault event** →

When pin has fault will shutdown these rails:

<input checked="" type="checkbox"/> Rail 01	<input checked="" type="checkbox"/> Rail 02	<input checked="" type="checkbox"/> Rail 03	<input checked="" type="checkbox"/> Rail 04
<input checked="" type="checkbox"/> Rail 05	<input checked="" type="checkbox"/> Rail 06	<input type="checkbox"/> Rail 07	<input type="checkbox"/> Rail 08
<input type="checkbox"/> Rail 09	<input type="checkbox"/> Rail 10		

**Response Options:**

- Enable glitch filter
- Enable re-sequencing

**Response:**

- Ignore fault and continue operation
- Shut down immediately
- Shut Down with delay configured using TOFF\_DELAY

**Restart:**

- Do not restart
- Restart up to 1 times
- Restart continuously

Figure 9. Fault Pin Configuration for UCD9090A and UCD90160A

**Configure**

GPI Polarity: Note: Polarity defines output voltage level when the logic evaluation result is TRUE(active). In open-drain mode, High-level output means the output pin is in Hi-Z state; a pull-up resistor is required to make the output level High.

Active Low

Active High

**GPI Fault Enable**  
When this bit is set, the de-assertion of the GPI is treated as fault and can be used to shutdown rails.

Latched Statuses Clear Source  
When a GPO uses a latched status type (`_LATCH`), you can configure a GPI that will clear the latched status.

Input Source for Margin Enable  
When the Margin Enable pin is asserted, this pin determines if the margined state is low or high.

Input Source for Margin Low/Not-High  
When this pin is asserted, all rails with margining enabled will be put in a margined state (low or high).

Configured as Sequencing Debug Pin  
Input pin can be used to put device in Debug Mode. If pin is selected and is asserted, device shall not assert PMBus Alert pin for any faults/warnings, not response to any faults, and not log any faults (excluding fault reported in STATUS\_CML register such as Invalid Command, PEC Fault, etc.). This function is mainly used for debugging purpose only. It is not recommended in the final production

**Configured as Fault Pin**  
Configure this input pin as fault-influenced outputs. The state of the output is determined by any faults occurred on selected rails

Enable GPI fault

Configure GPI as Fault Pin(UCD90320 Only)

Figure 10. Configure Fault Pin UCD90240 and UCD90320 - Step 1

Rail Config | Hardware Configuration | Global Configuration | All Config

**Global Configuration**

**Enable Fault Log:** Select which faults will get written to the detail fault log in non-volatile flash memory. Because there is a limit to the total number of faults that can be logged in detail, use this setting to log the most critical faults in your system.

**Misc Config:** Resequencing options, enable Brownout, set Fault Log FIFO Scheme, manually set temperature, enable Sync Clock between devices, and set ADC Reference.

**System Reset:** allows device to provide an external reset signal to the system. This signal can be based on time, the power-good state of selected rails, the state of selected GPI pins, or a combination of these things... This ensures that key devices are held in reset until other dependent devices (ex: peripherals) are fully powered.

**System Watchdog:** keeps a timeout counter running. That counter is reset when the watchdog input (WDI) pin is toggled or when the SYSTEM\_WATCHDOG\_RESET command is written.

**Pin Selected Rail Status:** use up to 3 GPI pins to determine the state of the rails if rails' ON\_OFF\_CONFIG are configured using OPERATION command.

**Fault Pin Config:** allows pins to be configured as fault-influenced outputs. The state of the output pin is determined by a selection of GPI pins and any faults of a selection of rails.

**Run Time Clock:** the time kept by this clock is used within data flash-based fault logging to note the time that a fault occurred. You can sync the device clock to PC, mimicking techniques your host microcontroller might use.

**Fault Pins Config**

Pin #	Enable	Pin Selection	Pin Polarity	System Watchdog	Timeout	Resequencing Error
1	<input checked="" type="checkbox"/>	Pin E4 MAR06(GPIO) Pages	Active Low	<input type="checkbox"/>	<input type="checkbox"/>	
2	<input type="checkbox"/>	<Click to Assign> Pages	Active Low	<input type="checkbox"/>	<input type="checkbox"/>	
3	<input type="checkbox"/>	<Click to Assign> Pages	Active Low	<input type="checkbox"/>	<input type="checkbox"/>	
4	<input type="checkbox"/>	<Click to Assign> Pages	Active Low	<input type="checkbox"/>	<input type="checkbox"/>	

Configurable for UCD90240 Only

This Read/Write block command configures the function of a given fault pin. This command allows pins to be configured as fault-influenced outputs. The state of the output pin is determined by a selection of GPIs and any faults of a selection of rails. The same fault pin could also be configured as GPI pin. In this way, when there is no fault, the pin behaves as a GPI and once there is fault inside the system, this pin is changed to a fault pin and output a signal based on the configuration

Figure 11. Configure Fault Pin UCD90240 and UCD90320 - Step 2

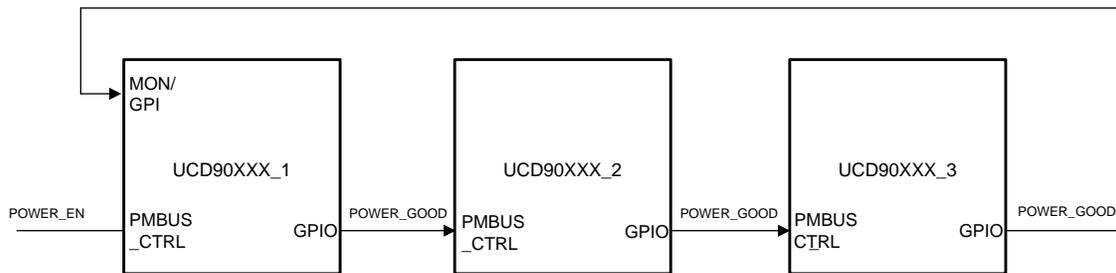
## 2 Cascading Multiple UCD90xxx

There are many different ways to cascade multiple UCD90xxx devices, which is up to system power sequencing requirements.

### 2.1 Only Power On Sequencing is Required

For systems where only the power-on sequencing among multiple UCD90xxx devices is a concern, the following connection description works well.

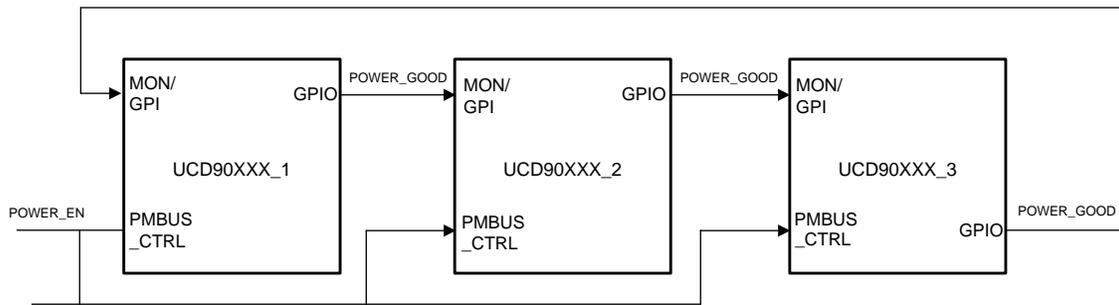
An LGPO pin can be used to coordinate multiple controllers by using it as a POWER\_GOOD output from one device and connecting it to the PMBUS\_CNTRL pin of another. Connect the POWER\_GOOD signal of the last UCD in the chain back to either MON/GPI pin of the first UCD. This imposes a master and slave relationship among multiple devices. During startup, the slave controllers initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off, it de-asserts the POWER\_GOOD signals to its slaves. A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers. The fault on slaves cannot only shutdown its own rails, but also de-assert the POWER\_GOOD signal to shutdown the rails of other slaves. For the last devices in the chain, when there is a fault, it de-asserts the POWER\_GOOD signals. The first (master) device in the chain will treat this as a UV fault (connected on the MON pin). A proper fault response could be set to shutdown rails. The other option here is to use GPI instead of the MON pin. GPI fault response is available on the UCD9090A, UCD90160A, UCD90240, and UCD90320. Therefore, GPI can be used for those devices to achieve the same function if there are not enough MON pins left. For this configuration the power-off sequencing is not ensured since all rails controlled by multiple UCDs will be sequenced off together. If there is a requirement for the power down sequence to cross different devices, this configuration may not be applicable.



Copyright © 2017, Texas Instruments Incorporated

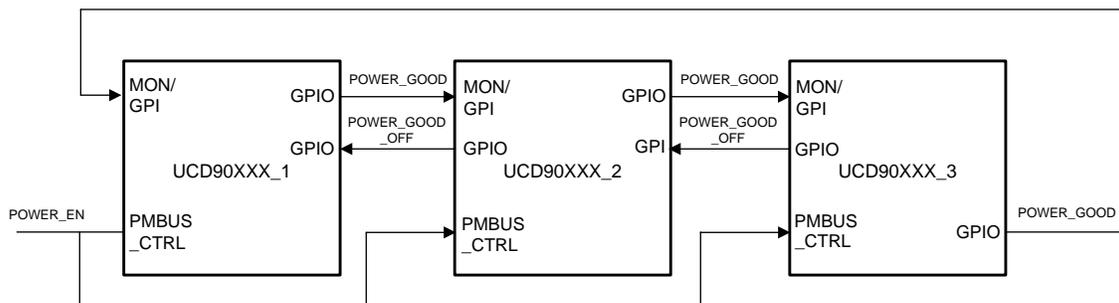
Figure 12. POWER\_GOOD Cascading Case 1

Another method to cascade multiple devices is to connect the power-good output of the first device to a MON/GPI pin of the second device; connect the power-good output of the second device to a MON/GPI pin of the third device, and so on. Optionally, connect the power-good output of the last device to a MON pin of the first device. The rails controlled by a device have dependency on the power-good output of the previous device. This way, the rails controlled by multiple devices can be sequenced. Also, the de-assertion of a power-good output can trigger a UV fault of the next device. The UV fault response can be configured to shut down other rails controlled by the same device. This way, when one rail has a fault shutdown, rails controlled by other devices can be shut down accordingly. Optionally, connect to the GPI pin instead of the MON pin if the UCD9090A, UCD90160A, UCD90240, and UCD90320 devices are used in the cascading method to save the MON pin for other uses.


**Figure 13. Power Good Cascading Case 2**

## 2.2 Both Power On and Off Sequencing Are Required

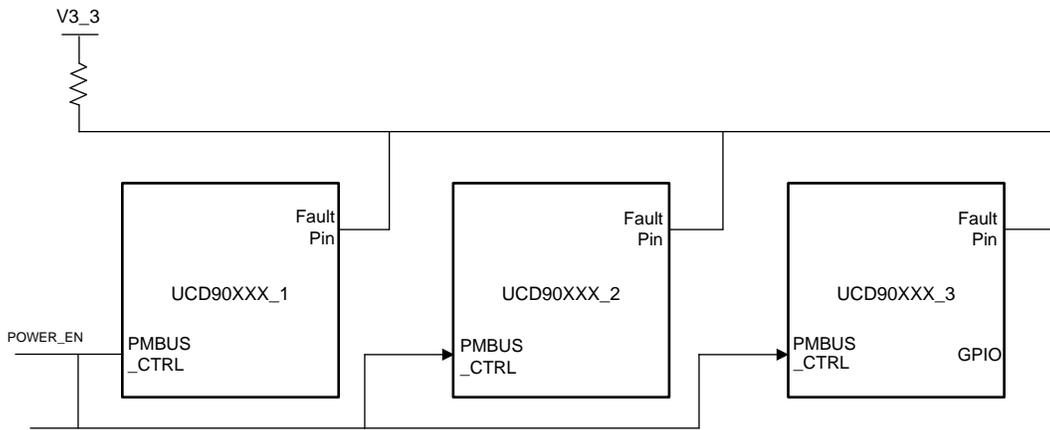
The 2 use-cases in [Section 2.1](#) do not ensure the power down sequence since there is no such information communicated among the devices. To ensure that the first rail on is the last one off among multiple devices, an additional LGPO pin is required. The new LGPO pin outputs a `POWER_GOOD_OFF` when all the rails controlled by the same devices are below the `POWER_GOOD_OFF` threshold, indicating that the rails are properly shutdown. The upstream UCD can take this signal from downstream UCD as sequencing off dependencies via the GPI pin. When the hosts de-assert the `POWER_EN` pin to power down the whole system, the rails controlled by the last UCD in the chain will be off first. All rails controlled by the first (master) UCD start shutting down its rails when all slave rails are off. This can ensure a proper shutdown sequence.


**Figure 14. POWER\_GOOD and POWER\_GOOD\_OFF Cascading**

## 2.3 Fault Pin Cascading

The UCD9090A, UCD90160A, UCD90240, and UCD90320 devices have a new feature “Fault Pin”.

The Fault pin is a bi-directional signal and can form a fault bus when pulled up to 3.3 V. When there is no fault on a Fault Bus, the Fault Pins are digital input pins and listen to the Fault Bus. When one or multiple UCD devices detect a rail fault, the corresponding Fault Pin is turned into active driven low state, pulling down the Fault Bus and informing all other UCD devices of the corresponding fault. This way, a coordinated action can be taken across multiple devices. The action is programmable. After the fault is cleared, the state of the Fault Pin is turned back to an input pin. The fault pin cascading connection does not provide power on or power off dependencies among multiple UCD devices, but it lets multiple devices response to the same fault event.



**Figure 15. Fault Pin Cascading**

### 3 Conclusion

The UCD90xxx family provides versatile approaches for users to implement cascading multiple devices. The best approach can be selected based on the power requirements and sequencer solution of the system.

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2017, Texas Instruments Incorporated