Application Report

Simplifying EFT, Surge and Power-Fail Protection Circuits in PLC Systems

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ABSTRACT

The Programmable Logic Controller (PLC) system is usually connected to an external DC power supply to provide power to the controller unit, backplane and I/O modules. The input protection circuits are required to protect the PLC from various faults that may occur either on the field or the PLC side. Traditionally, discrete or semi-integrated circuits have been the solution and require a lot of external components to provide protection and to pass stringent electromagnetic compatibility (EMC) tests. Industry's first high-voltage eFuse, the TPS266x devices, integrate all of the necessary functions required to simplify the complete protection needs. This application report describes how the TPS266x devices simplify protection circuits for the EFT, surge and power-fail requirements.

Table of Contents

List of Figures

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1 Surge Test (IEC 61000-4-5)

The surge test is performed to make sure the system is immune to surges produced by lightning strikes and power system transients such as capacitor bank switching, short circuits and arcing faults. Surge testing is one of the highest energy pulse tests done on the system.

Typical traditional surge and front-end protection circuits used in a PLC system are shown in Figure 1-1. Input side passive components like common mode choke, series inductor and capacitors are used to reduce slew rate of the surge pulse. A string of TVS diodes is used to clamp the surge magnitude to an acceptable level. A series diode or an OR-ing controller with an external FET is used to protect the downstream from negative voltages. Negative voltages are most common either due to miswiring or a negative surge pulse. Discrete or semi-integrated solutions are used for hot-swap, inrush control, monitoring, undervoltage (UV) and overvoltage (OV) protection.

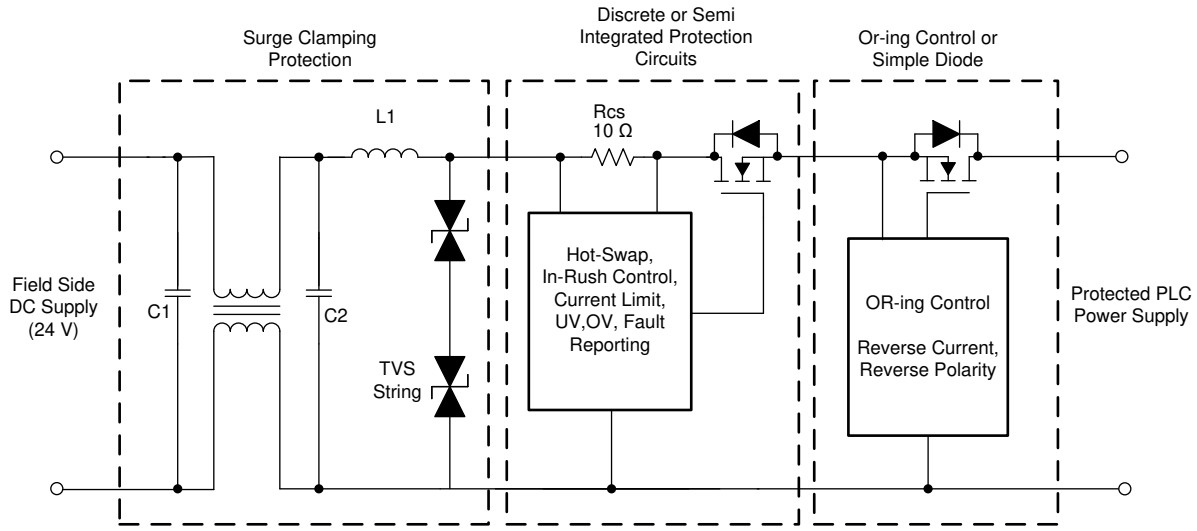

Figure 1-1. Traditional Input Protection Circuits

Figure 1-2 shows catastrophic damage of the board due to protection circuits failure. Probability of the failure is high in a discrete components-based implementation. Selecting a proper integrated protection solution is critical to avoid possible system failure, unwanted downtime and bad reputation of the product.

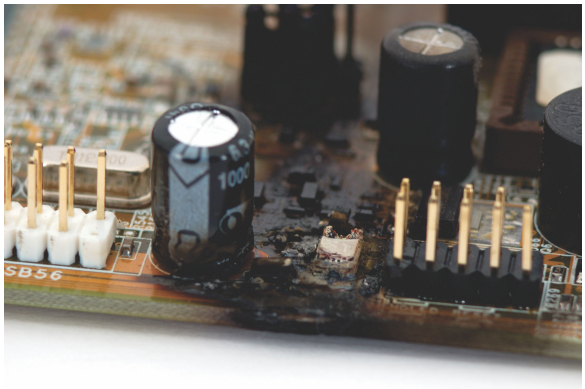

Figure 1-2. Impact of the Improperly Designed Protection Circuits

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2 EFuse Solution for Surge Protection

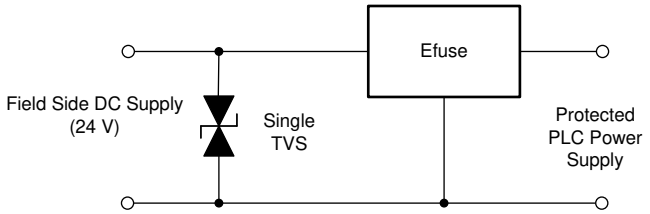

Figure 2-1. EFuse Integrated Solution

The eFuse-based surge protection solution is shown in Figure 2-1. It requires only a single TVS diode to protect the PLC from surges. The device does not need any passive wave shaping circuits to reduce slew rate of the surge. It can handle slew rates as fast as 20 V/µs. Built-in back-to-back FETs and reverse polarity protection circuits effectively block negative voltage that can be generated due to a negative surge.

The ±70 V transient absolute maximum ratings of the device enables the use of a single TVS diode for clamping the surge. Overvoltage and undervoltage protection makes sure that the downstream converters are isolated from input when the surge is at peak or valley level. A proprietary high-speed protection algorithm immediately disconnects the output from the input and prevents the surge passing from the input to the output.

3 EFuse Solution Schematic for Surge Protection

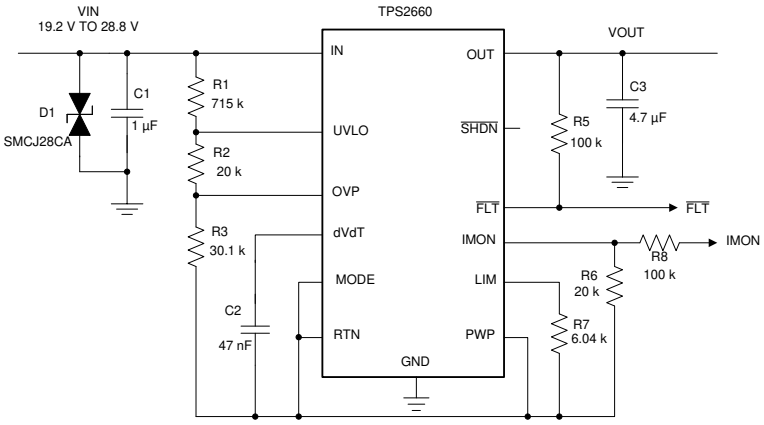

Figure 3-1. Efuse Solution Schematic for Surge Protection

The complete schematic of the surge protection solution is shown in Figure 3-1. This protection circuit is designed for a 19.2 V to 28.8 V supply voltage range and 2-A load current. A 28-V reverse standoff voltage TVS in SMC package is used to clamp the surge voltage. When a ±500 V, 2Ω surge pulse is applied, the input voltage clamps to a ±44 V maximum. The Internal FET experiences maximum stress during the negative surge event. Maximum voltage across the device is the sum of the input clamp voltage and the output voltage under no load conditions. The maximum device stress at nominal test input voltage is less than the transient absolute maximum rating of the device with the selected TVS.

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4 Circuit Performance for Surge Tests

Figure 4-1 to Figure 4-4 shows the performance of the TPS2660 for positive and negative 500-V, 2-Ω, 8/20-µs surge pulses. The output voltage waveform shows that the device shuts-down and re-starts without operator intervention after all of the surge related oscillations are over and provides criteria B performance. For circuits to give criteria A performance, contact the application engineer on the E2E Forum.

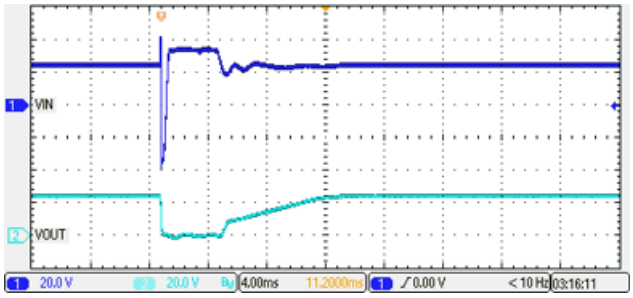

Figure 4-1. +500 V, 2-Ω Surge Performance at V_{IN} = 24 V and Load = 16 Ω

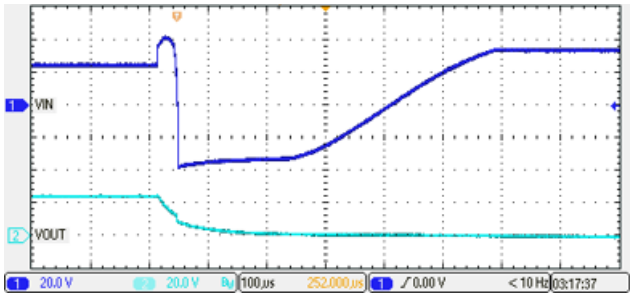

Figure 4-2. Zoom at the Instance of Surge Application

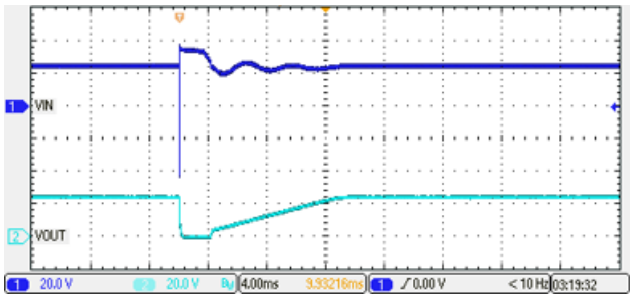

Figure 4-3. –500 V, 2-Ω Surge Performance at V_{IN} = 24 V and Load = 16 Ω

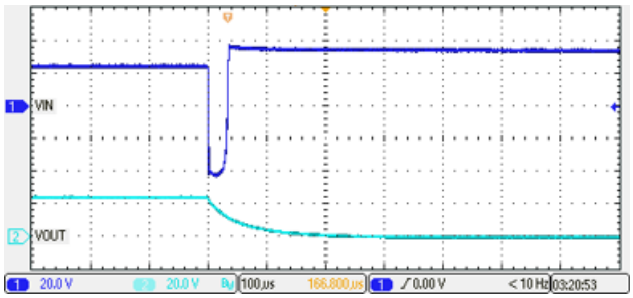

Figure 4-4. Zoom at the Instance of Surge Application

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5 EFT Test (IEC 61000-4-4)

The PLC system is surrounded by cables carrying power and data. EFT events can occur from the surrounding cables and can interrupt data or power through inductive or capactive couplings. Therefore EFT immunity becomes an important requirement for PLC systems. The IEC 61000-4-4 standard defines the EFT immunity tests, set-up procedures, and test levels. Depending on the application environment, the pulse generator has varying test voltage levels depending on the application. Table 5-1 provides different test levels for EFT test for power supply ports. Test pulses are defined in Figure 5-1 by IEC 61000-4-4 standard. EFT in IEC 61000-4-4 standard are specified as repeated pulses and bursts for 15 ms with each single pulse 5 × 50 ns, as in Figure 5-1.

Table 5-1. IEC61000-4-4 stress levels

	Peak Amplitude (For Power Supply Port)	
Level	V_{CC} (kV)	Isc (A)
1	0.5	10
2	1	20
3	2	40
4	4	80

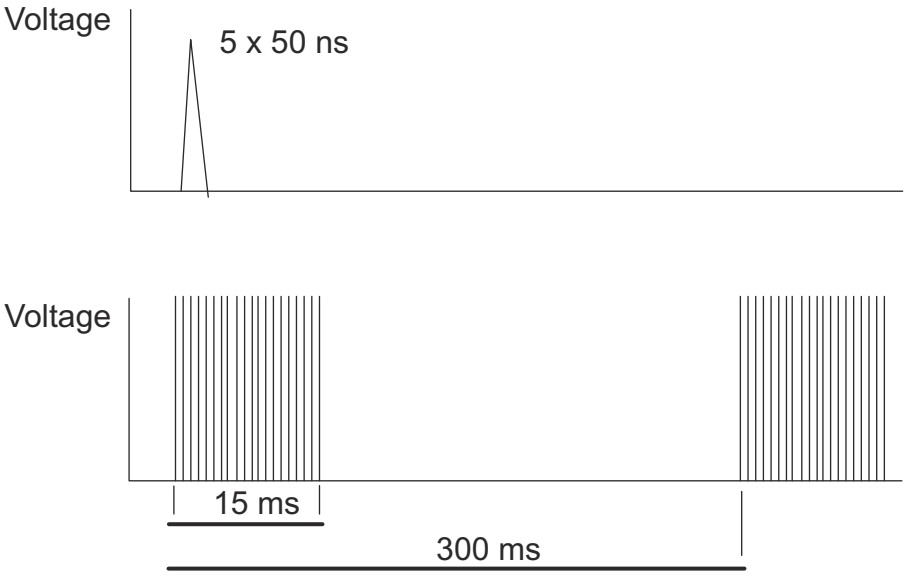

Figure 5-1. IEC61000-4-4 Bursts and Waveforms

Systems are classified based on their immunity to EFT, Table 5-2 provides different classifications for EFT immunity.

Table 5-2. EFT Immunity Criteria Levels

Criteria Level	Description
A	Normal performance within the limits specified by the manufacturer, requestor or purchaser
B	Temporary loss of function or temporary degradation of performance not requiring an operator
C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention
D	Loss of function or degradation of performance which is not recoverable, owing to damage of the hardware of software, or loss of data

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6 EFuse Solution Schematic for EFT protection

Figure 6-1 illustrates the schematic with TPS2662x device for EFT protection.

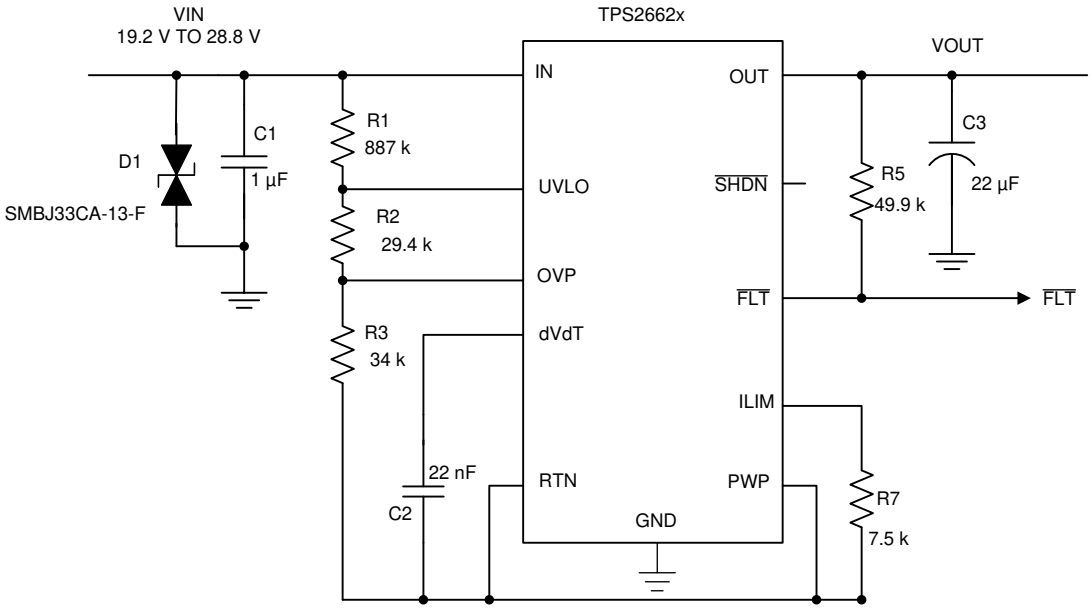

Figure 6-1. Efuse Solution Schematic for EFT protection

7 Circuit Performance for EFT Tests

The TPS2662 device has integrated back to back MOSFETs which provide overvoltage protection, reverse input polarity protection, reverse output polarity protection and fast reverse current blocking to achieve a Criteria-A performance for EFT tests. Table 7-1 summarizes the results for circuit performance for EFT protection with TPS2662.

Table 7-1. Circuit perfprmance with TPS2662 for EFT protection

EFT level	Voltage (kV)	Pass/Fail on input (VIN)	Pass/Fail on output (VOUT)
1	±0.5	Pass with Criteria-A performance(1)	Pass with Criteria-A performance(1)
2	±1	Pass with Criteria-A performance(1)	Pass with Criteria-A performance(1)
3	±2	Pass with Criteria-A performance(1)	Pass with Criteria-A performance(1)

(1) See Table 5-2

8 Power-Fail Test (IEC 61000-4-29)

The PLC system must be immune to voltage dips, short interruptions or voltage variations on the DC power ports. Typically, systems are designed to be immune to 5 ms to 10 ms short power interruptions. Major challenges in designing the protection circuits are reverse current blocking and inrush current control. Again, the discrete protection circuits as shown in Figure 1-2 are traditionally used. The TPS2660 based eFuse solution schematic is shown in Figure 9-1. When power fails, integrated back-to-back FETs and high-speed reverse current blocking circuitry prevents bulk capacitor discharge from the output to the input. If the input supply resumes, TPS2660 starts in the current limit mode to quickly ramp up the system bus voltage to the input voltage level. The circuit also provides inrush current control during startup.

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9 EFuse Solution Schematic for Power-Fail Applications

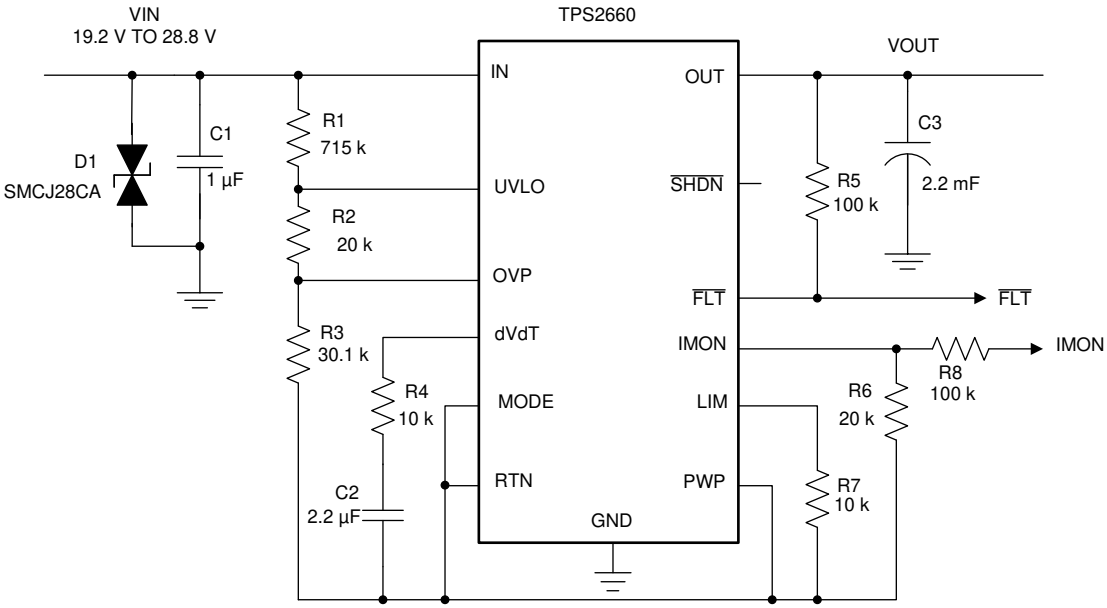

Figure 9-1. Efuse Solution Schematic for Power-Fail

10 Circuit Performance for Power-Fail Tests

Figure 10-1 shows the performance of the TPS2660 for 10 ms supply interruption. During power-fail, the output bulk capacitor supplies the system load. When supply voltage resumes, the TPS2660 charges the output capacitance with the current limit.

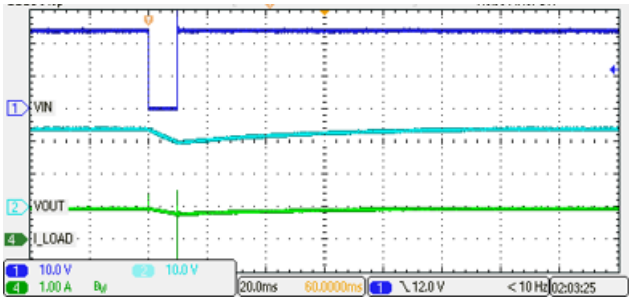

Figure 10-1. 10 ms Input Power-Fail at V_{IN} = 24 V, Load = 24 Ω (IEC 61000-4-29 Level -1)

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Figure 10-2 shows the startup of the TPS2660 when the supply voltage is ramped up. The circuit limits charging current to the bulk capacitor and simultaneously provides the required load current.

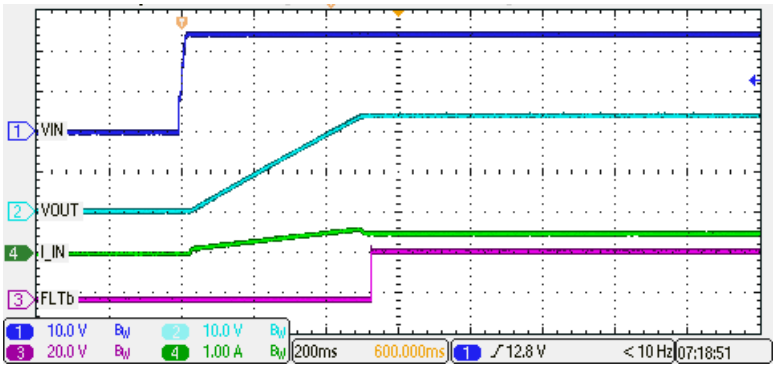

Figure 10-2. Startup With V_{IN} = 24 V and Load = 48 Ω

11 EFT, Surge and Power-Fail Test Setup

Figure 11-1 shows the test setup of the surge and power fail tests. The test setup is made compatible with IEC standards. UCS500N is used for generating the EFT, surge and power fail waveforms.

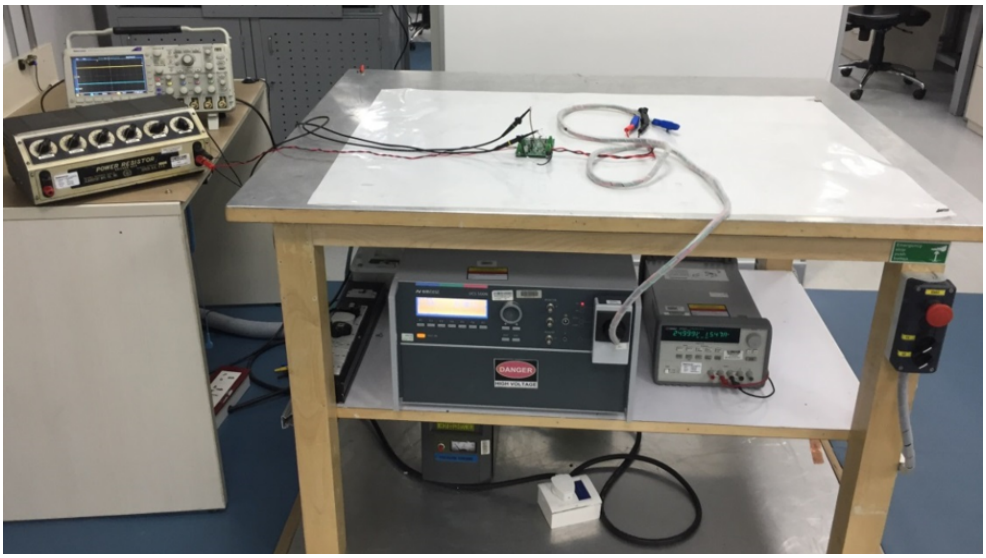

Figure 11-1. Test Setup

12 Conclusion

The TPS2660 and TPS2662 devices are highly integrated protection circuit which solve the system level issues such as EFT, surge and power fail with minimum external components. These save board space and improve reliability of the overall system.

13 References

- TPS2660
- TPS2662

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14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2018) to Revision D (May 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

Changes from Revision B (November 2018) to Revision C (December 2018)	Page
• Updated the Abstract	1

Changes from Revision A (April 2018) to Revision B (November 2018)	Page
• Updated title	1
• Updated Figure 2-1	3
• Added Section 5	5
• Added Section 6	6
• Added Section 7	6
• Updated *Section 12*	8

Changes from Revision * (October 2016) to Revision A (April 2018)	Page
• Changed title of the *Application Report* to Simplifying Surge and Power-Fail Protection Circuits in PLC Systems	1

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