Application Report
SLVA812C–August 2016–Revised August 2019

Extracting Maximum Power from an Adapter with Input Current Optimization Feature

BCP SCS

ABSTRACT

To maximize the output power of any adaptor that charges a battery, some battery chargers include the input current optimization (ICO) feature. This application note explains how the ICO feature configures the current limit of the charger input to the maximum allowed without overloading the power source of the charger.

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Trademarks

1 Background

Wall adapters that power portable electronic devices come in a variety of voltage and current ratings. Most battery chargers inside these portable devices include one or more fast-response feedback control loops. These prevent the charger from pulling too much current from the wall adapter, which collapses it. One such loop is the input current-limit dynamic power management (I_{INDPM}) loop. The designer, through an external resistor, I2C register, or the D+/D- circuitry of the charger, automatically sets a predetermined value for the amount of input current the charger is allowed to pull from the adapter. The dynamic power-path management circuitry of the charger then distributes this input power to the system load and uncharged battery, reducing charge current if necessary, to provide the demanded DC, or transient system load. In the event the adapter cannot provide the rated output current, or because of highly resistive connections from the source to the charger, the charger input pin voltage droops. This can also happen when an adapter unknown to D+/D- detection (for example, a third-party adapter) is attached, and the charger sets the I_{INDPM} setting too high. When this happens, the second feedback loop, input voltage dynamic power management (V_{INDPM}), activates. As highlighted in Figure 1, this reduces the charge current to prevent the charger from crashing the adapter.

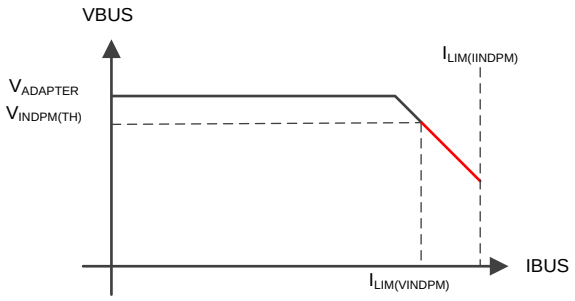

Figure 1. Effective Input Current Limit Set by V_{INDPM}

At start-up, the charger sets a default V_{INDPM} threshold (for example, the BQ25890 sets $V_{INDPM(TH)}$ to 600 mV below the unloaded input voltage). The host software can change the desired input current limit, or V_{INDPM}voltage thresholds, via I2C anytime. If the input voltage droop is due to highly resistive connections, allowing the V_{INDPM} loop of the charger to continuously control and regulate the charger input voltage, therefore preventing further droop, is acceptable. If, however, the droop is due to an adapter overload, reducing the input current limit of the charger to a level at which the adapter is not in overload is preferable. More details about I_{INDPM} and V_{INDPM} can be found in the Dynamic Power-Path Mgmt & Dynamic Power Mgmt Application Report.

The ICO circuitry identifies and sets the maximum (optimal) current the charger can pull from the adapter without collapsing the adapter.

2 Operation

The actual input-current limit is the lower value set by the ILIM pin resistor, or as reported by the input current limit register bits, unless the host-controlled EN_ILIM bit of the charger is disabled. In other words, the ILIM pin resistor clamps the maximum input current limit value. The remainder of the application note assumes that the host-controlled EN_ILIM = 0 of the charger, or that the ILIM resistor is set higher than the ICO determined current limit. This results in the ICO input current limit register reporting the actual input current limit in use.

When ICO is disabled, or until the ICO algorithm has optimized the input current limit, the ICO status bits indicate that optimization is disabled, in progress, or complete. The ICO-optimized input current register reports the same value as configured in the input current limit register by the D+/D- algorithm, the PSEL pin at start-up, or the host software.

If ICO is enabled, the charger waits for the first V_{INDPM} event to occur. This is the desired system, plus charge current power, to exceed the output power capability of the power source. It reports, per the ICO status bits, that ICO optimization is in progress. When V(BAT) > V_{MINSYS} and a V_{INDPM} event occurs, the ICO algorithm does the following:

1. Reduces the input current limit register, and the charger maximum allowed input current, to 500 mA
2. Steps up the current limit until the input voltage drops to the V_{INDPM} threshold
3. Lowers the input current limit register slightly below the point where V_{INDPM} is reached
4. Updates the ICO input current limit register to this input current limit value
5. Updates the ICO status bits

Figure 2 is a graphical representation of the ICO algorithm list discussed previously. It is assumed that the system load, or charge current, increases at the point where the VBUS voltage is no longer at the adapter voltage (V_{ADPTR}).

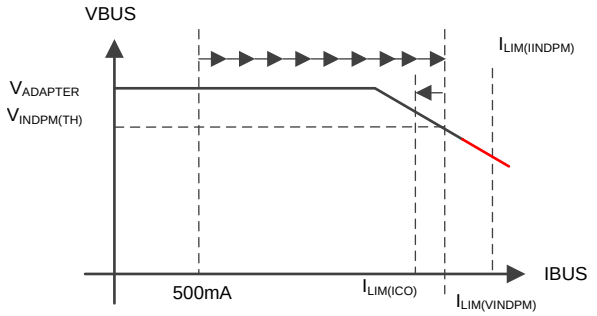

Figure 2. Graphical Representation of ICO During Operation

Figure 3 is a scope shot of the BQ25890 ICO circuitry, on a board with a 0.5-Ω input resistance from a 6-V supply, and a 5.3-V V_{INDPM} threshold. The charge current increases from 1 A to 4 A, causing the input voltage to droop to V_{INDPM} and trigger an ICO.

When V(BAT) < V_{MINSYS}, the battery voltage can be too low to supplement a large system load if the charger buck converter is limited to 500 mA, then ramped up by the ICO algorithm. Therefore, when a V(BAT) < V_{MINSYS} and a V_{INDPM} event occurs, the ICO algorithm works by:

1. Setting the input current equal to the input current-limit register value (which is clamped to a lower value by the V_{INDPM} control loop)
2. Stepping down the current limit until the charger exits V_{INDPM} control
3. Updating the ICO input current-limit register to this input current-limit value
4. Updating the ICO status bits

Figure 4 is a scope shot of the same BQ25890 board, but with a V(BAT) < V_{MINSYS}.

The input current limit remains optimized, and does not automatically run the ICO detection algorithm again, unless the following occurs:

- Another V_{INDPM} event
- Input current-limit register changes
- V_{INDPM} offset or the absolute V_{INDPM} registers changes
- Force V_{INDPM} register changes

Additionally, if a DCP or HVDCP adapter is detected at start up by the D+/D- circuitry, the ICO algorithm automatically runs.

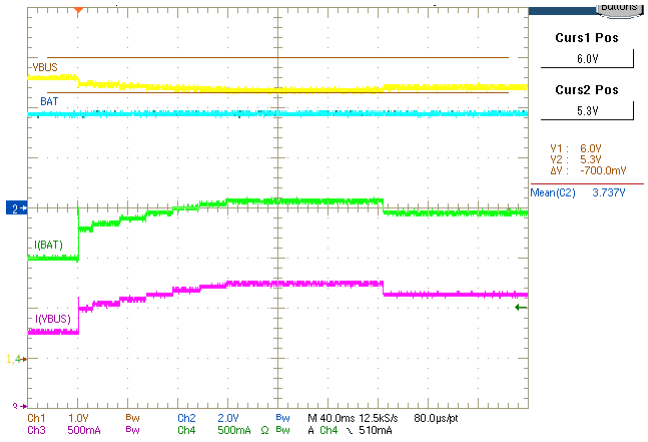

Figure 3. Automatic ICO Detection After Charge Current Increase With V(BAT) > V_{MINSYS}

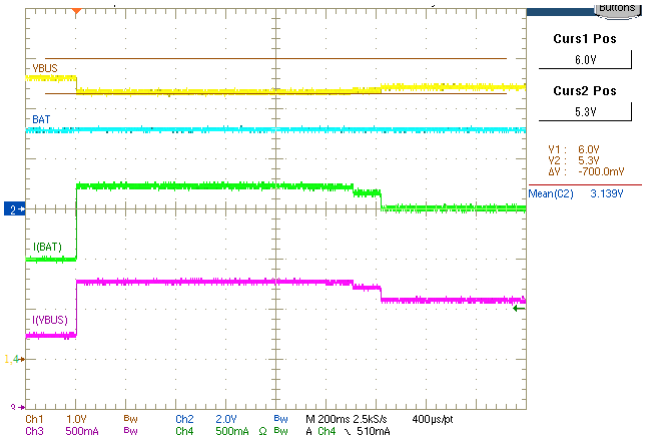

Figure 4. Automatic ICO Detection After Charge Current Increase With V(BAT) < V_{MINSYS}

The host software can also force ICO detection using the FORCE_ICO bit, or by toggling the ICO enable bit (which defaults to 1). As shown in Figure 5, when forcing detection in the BQ25890, the ICO detection algorithm first disables charge for 10 ms. Then, it applies a 10 mA sink on the BAT to determine whether V(BAT) is greater than or equal to V_{MINSYS}, and proceeds as previously described.

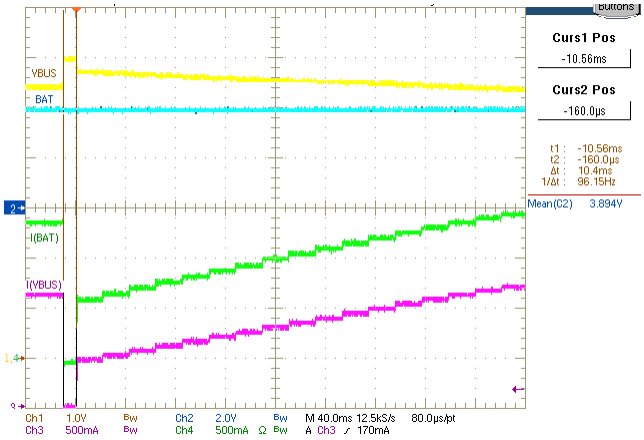

Figure 5. Forced ICO Detection With V(BAT) > V_{MINSYS}

shows which battery chargers have ICO, the relevant I2C registers for the host-controlled chargers, and how ICO is activated.

Table 1. Battery Charge ICs With ICO and Relevant Bits

Charger	Desired Input Current-Limit Register Bits	EN_ILIM Pin Register Bit	ICO-Enable Bit	Input Current-Limit When ICO Active Bits Register	ICO Status Bits	Force ICO Bit	V_{INDPM} Register Bits	How/When Activated[1]
BQ25890 BQ25892 BQ25895 BQ25896 BQ25895M	REG00[0:5]	REG00[6]	REG02[4]	REG13[0:5]	REG14[6]	REG09[7]	REG01[0:4] REG0D	Immediately following DCP source detection if enable ICO bit = 1. If DCP input source detected, enable ICO set to 1, EN_HIZ bit toggled, IINDPM register changed, V_{INDPM} register changed, V_{INDPM} event; Force ICO set to 1 even if not DCP input source
BQ25890H BQ25898 BQ25898D	REG00[0:5]	REG00[6]	REG02[4]	REG13[0:5]	REG14[6]	REG09[7]	REG01[0] REG0D	
BQ25882 BQ25883 BQ25887	REG03[0:4]	REG01[6]	REG03[5]	REG0A[0:4]	REG0C[1:2]	REG03[7]	REG02[0:4]	Same as above plus VBUS OVP event
BQ25886	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Only if and immediately following DCP detection by D+/D- algoirthm or if DCP and V_{INDPM} event

(1) Even if activated, ICO may not complete (no input current limit reduction) if SYS + BAT load is not high enough to cause V_{INDPM} event during input current limit sweep

Table 2 summarizes possible cases for input current limit registers for the BQ25890.

Table 2. Example Current Limit Register Results

TEST CONDITIONS				RESULTS		
Adapter	**Max Input Current Limit per ILIM Pin Resistor**	**Input Current-Limit Register**	**ICHG Register**	**ILIM When ICO Active Bits Register**	**ICO Status Register**	**Actual Input Current Limit**
Case 1						
5 V at 3 A	2 A	3.25 A	5 A	3.25 A	1	2 A – clamped by ILIM resistor
Case 2						
5 V at 1.5 A	2 A	3.25 A	5 A	1.5 A	1	1.5 A – ICO finds optimal setting
Case 3						
5 V at 3 A	3 A	2 A	5 A	2 A	1	2 A – clamped to INLIM
Case 4						
5 V at 3 A	3 A	3.25 A	2 A	3.25 A	0 – ICO in progress because ICHG does not require IBUS = 3.25 A	3 A

3 Summary

The V_{INDPM} loop of a charger is the last line of defense in preventing the charger from collapsing the input source (for example, the adapter). While the charger is fully capable of indefinitely regulating the input current limit using the V_{INDPM} loop, running a wall adapter in an overload state is unhealthy for the adapter. The designer sets the input current limit, either through an external ILIM resistor or input current limit I²C register, to match the adapter-rated current. In the event of malfunctioning adapters, or highly resistive adapter cables, the ICO circuitry of the battery charger finds the optimal input current-limit setting of the charger for the maximum power extraction without adapter overload.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (July 2019) to C Revision	Page
• Updated abstract	1
• Edited application report for clarity	1
• Updated *Section 1*	1
• Updated *Section 2*	2
• Deleted BQ2589X family register addresses from body of text and added BQ2588X family in Table 1	4
• Updated *Section 3*	5
• Updated document for additional clarity	5

Changes from A Revision (February 2018) to C Revision **Page**

- Updated abstract 1
- Edited application report for clarity 1
- Updated *Section 1* 1
- Updated *Section 2* 2
- Deleted BQ2589X family register addresses from body of text and added BQ2588X family in Table 1 4
- Updated *Section 3* 5
- Updated document for additional clarity 5

Changes from Original (August 2016) to A Revision **Page**

- Changed 3.25 A to 3 A in the Case 4 Actual Input Current Limit column of Table 2 4

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