Application Report
SLVA764–February 2016

SMT Guidelines for Stacked Inductor on Voltage Regulator IC

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ABSTRACT

In today's *Cloud Infrastructure* systems, board space and power density are challenging particularly in power supply designs where several high-current point-of-load rails are present. End equipment such as enterprise servers and switches, workstations, base stations, network attached storage, FPGA testers, network testers, and other test and measurement equipment employ several high-current CPUs, ASICs, FPGAs, and DDR memory – all of which need high power, while the available board area is steadily decreasing. As long as 11.5-mm height is acceptable, a great opportunity today is stacking the inductor on top of the IC, thus saving PCB area. The following guideline is a step-by-step guide on assembling TI voltage regulator ICs and inductors on top of the IC in a high-volume manufacturing environment where SMT processes are used.

Although this guideline can be applied to many TI voltage regulator ICs, the following ICs are a typical offering for both single- and multi-phase voltage regulators for point-of-load (POL) solutions where inductors on top can be used to reduce the X-Y PCB area on the board.

This guideline is applicable to the following TI devices:

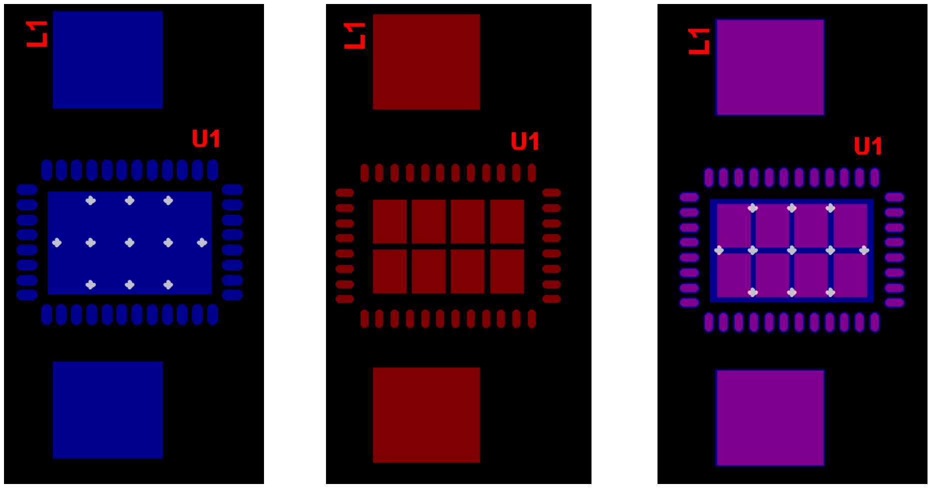
iFET Converters:	TPS54020, TPS54020,TPS544C20/B20, TPS546C20, TPS53513/515/915, TPS548A20/9A20, TPS53318/19/53/55, TPS544B25/C25, TPS548D22
Controllers:	TPS53647, TPS40425/8, TPS40422, TPS53631/41/61, TPS40400, TPS53819A, TPS53219A, TPS40303/4/5, TPS40322

Table 1. Assembly Quick Start Checklist

Operation	Assembly Quick Start Checklist
Solder Paste	TI recommends the use of type 3 or finer solder paste when mounting the devices
Reflow Profile	Measure the peak reflow temperature by placing a fine gauge thermocouple (Type K) on top of the package body center.
	Ensure that the peak reflow temperature does not exceed 260C max. (260°C +/ -5°C) Exceeding the max temperature may damage the part.
	Reflow time within 5°C Peak Temp must not exceed 20 seconds and the reflow time above liquidus must not exceed 60 seconds.
	Minimizing the number of reflow cycles seen by devices is recommended.
Moisture Handling	Depending on the products, the MSL level can be 1, 2, or 3. Refer to the data sheet of the individual product for its MSL level (links to the data sheets are available in Section 8). MSL2 devices have a maximum floor life of 1 year after the devices are removed from the sealed package. MSL3 devices have a maximum floor life of 1 week after the devices are removed from the sealed package.
	See IPC/JEDEC J-STD-020 for additional details.

1 PCB Design Guideline

Figure 1 illustrates the example TPS544C20 layout and Table 2 lists the layout parameters.



Metal Layer   Stencil Opening   Paste on Metal Layer

Figure 1. Example TPS544C20 PCB Layout

Table 2. TPS544C20 PCB Layout Parameters

	U1		L1
	IO	DAP	
Metal	0.24 mm × 0.60 mm	5.30 mm × 3.30 mm	3.50 mm × 3.10 mm
Mask	0.34 mm × 0.70 mm	5.40 mm × 3.40 mm	3.60 mm × 3.20 mm
Stencil	0.24 mm × 0.60 mm	8x 1.08 mm × 1.43 mm	3.50 mm × 3.10 mm

This PCB layout recommendation applies only to the TPS544C20 device. For other device PCB layout recommendations, refer to the individual application note.

Recommended stencil thickness: 0.1 mm.

TI recommends stencil manufacturing by either laser cut, electro polished, or electroform with tapered aperture walls and a 5-degree tapper to facilitate paste release.

2 Inductor Selection

Two inductors are custom made for this board assembly. TI recommends using one of the inductors listed in Table 3 for this application.

Table 3. Electrical Specification

TDK™ Identification	Inductance		Test Frequency (kHz)	DC Resistance		Rated DC	Current
	at 0 A (µH Typ.)	Tol. (%)		Spec. (mΩ)	Tol. (%)	I_{DC} 1 [(1)] (A Typ.)	I_{DC} 2 [(2)] (A Typ.)
VLB10090HT-R10M-B2	0.10	±20%	100	0.33	±10%	100.0	32.8
VLB10090HT-R33K-B2	0.33	±10%	100	0.33	±10%	45.0	32.8

(1) I_{DC} 1: Based on the inductance change (drop 30% typ. from Lo)
(2) I_{DC} 2: Based on the self temperature rise. (+40° C typ.)

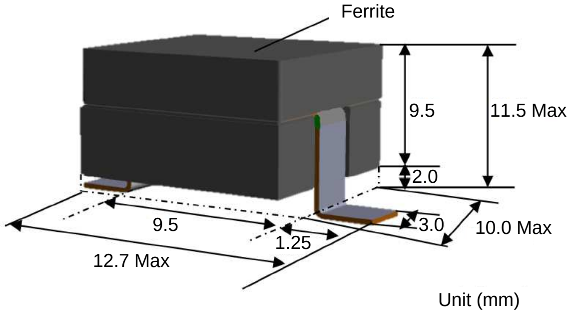


Figure 2. Inductor Dimensions

TDK Corporation of America
Magnetics Business group
Contact information
475 Half Day Road,
Lincolnshire, IL 60069-2934
Phone: (847) 699-2299
http://www.tdk.com/contact.php

3 Solder Paste

TI recommends using type 4 or finer solder paste. Using paste provides the following advantages:

- Paste acts as a flux to aid in wetting the solder ball to the PCB land
- The adhesive properties of the paste hold the component in place during reflow
- Paste contributes to the final volume of solder in the joint, allowing this volume to be varied and providing an optimal joint
- Paste selection is normally driven by overall system assembly requirements. In general, the *no clean* compositions are preferred, due to the difficulty in cleaning under the mounted components.

4 Component Placement

Components are placed by programming the component thickness or by controlling the mounting force. If placement is by programming the component thickness, add 0.05 mm to the actual component thickness so that package is sitting halfway into paste. If placement is by force feedback, utilize minimum force while not exceeding 5 Newton's of force. This control avoids forcing out solder paste or package free fall resulting in solder balling.

5 Board Assembly Flow

Figure 3 illustrates the assembly flow of the board.

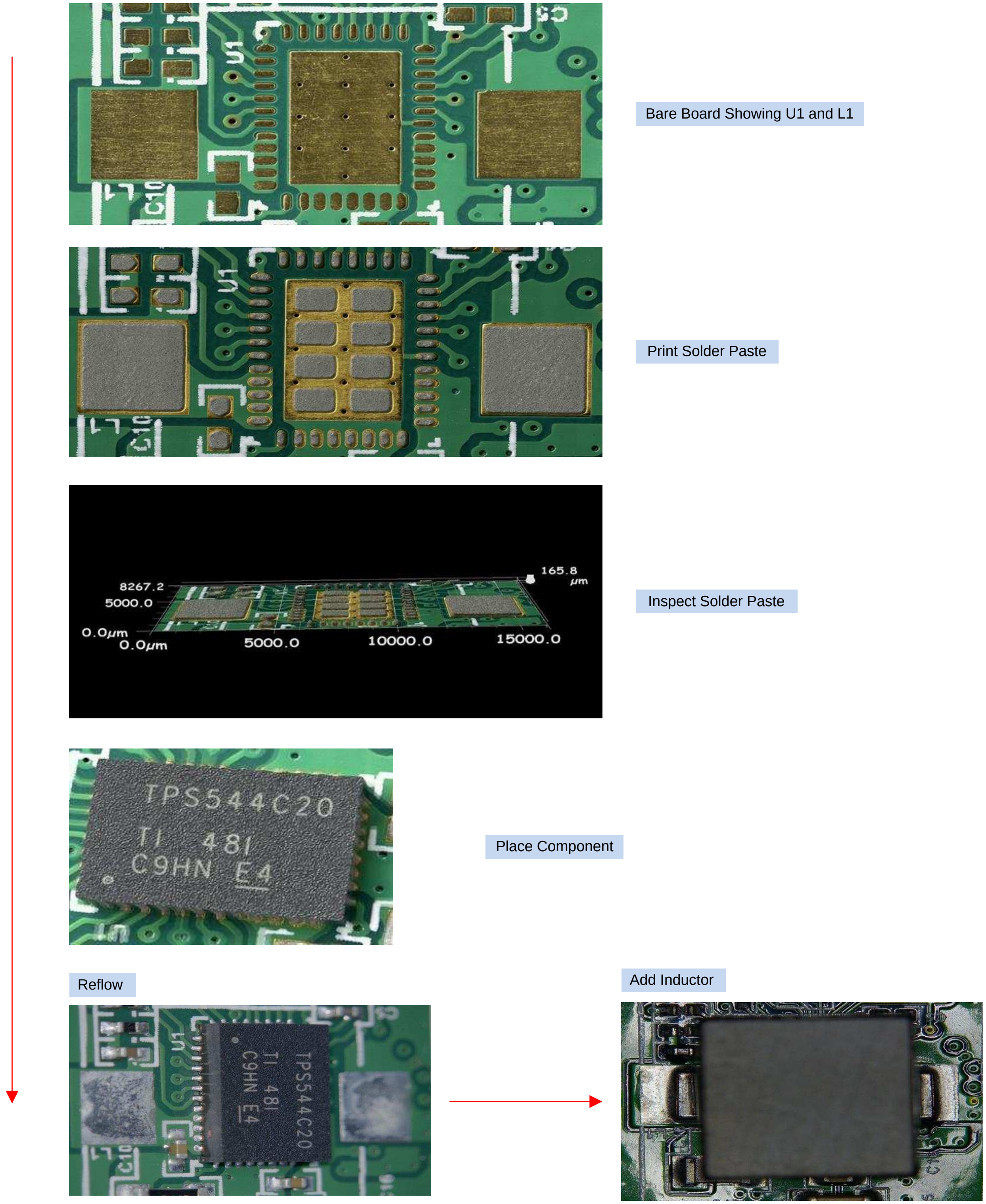


Figure 3. Board Assembly Flow

6 Component Rework Guideline

Repair Procedure

- A package repair/rework station is strongly recommended for this process (that is, Air-Vac Engineering, Metcal, or Den-On Inst.)

Package Replacement Procedure

- Board preheat (package bake recommended)
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PWB lands
- Screening of solder paste (a mini stencil is recommended)
- Placement and reflow of new component
- Inspection of solder joints

Repair Procedure Notes

- Prior to any rework process, TI recommends baking the board 4 hours at 125°C to remove any moisture that might cause delamination or cracking
- Reusing a removed package is not recommended
- Use a new package for the repair process. The new package should be kept dry and should not exceed the stated floor life. Only rebake a package a maximum of 3 times.

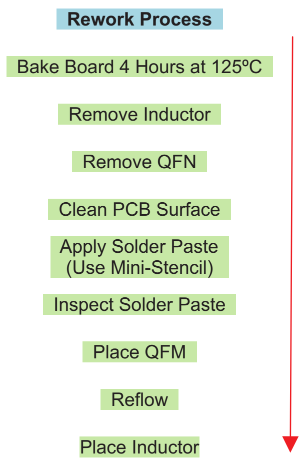


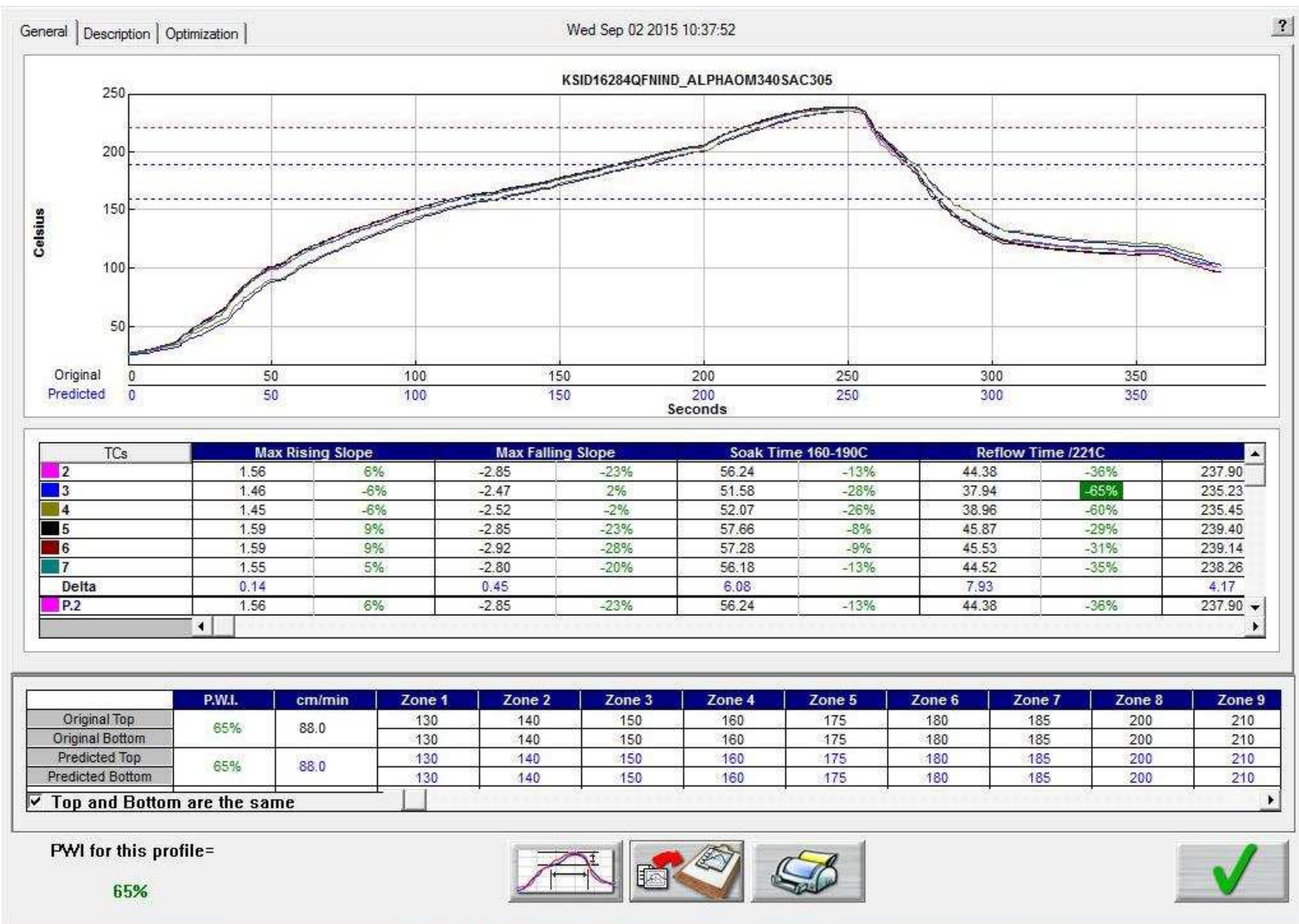
Figure 4. Rework Process

7 Reflow Profile

This reflow profile serves as an example only. The actual profile depends on the various factors such as board size, board thickness, component density, solder paste, and so forth.

Consider the solder paste manufacturer-recommended reflow profile as the optimal source for your specific application.

	JEDEC Pb-Free Profile Example
Ramp Rate	3°C/second maximum
Preheat	150°C to 180°C
	60 to 120 seconds
Time Above Liquidus	220°C
	30 to 90 seconds
Peak Temperature	260°C +0/–5°C
Time Within 5°C Peak Temperature	10 to 20 seconds
Rampdown Rate	6°C/seconds maximum



Temperature profile is JEDEC Pb-free reflow compliant and shown as an example only.

Figure 5. Reflow Profile Example

8 References

1. *QFN/SON PCB Attachment* Application Report (SLUA271)
2. *Moisture Reflow Sensitivity Classification for Nonhermetic Solid State SMD* (J-STD-020)
3. *Handling, Packing, Shipping and Use of Moisture Reflow Sensitive SMD* (J-STD-033)
4. *Design and Assembly Process Implementation for Bottom Termination Components* (IPC-7093)

Data Sheets

1. *TPS54020 Small, 10-A, 4.5-V to 17-V Input, SWIFT™ Synchronous Step-Down Converter With Light-Load Efficiency* (SLVSB10)
2. *TPS544x20 4.5-V to 18-V, 20-A, and 30-A SWIFT™ Synchronous Buck Converters with PMBus™* (SLUSB69) – TPS544B20 and TPS544C20
3. *TPS53513 1.5-V to 18-V (4.5-V to 25-V Bias) Input, 8-A Single Synchronous Step-Down SWIFT™ Converter* (SLUSBP9)
4. *TPS53515 1.5-V to 18-V (4.5-V to 25-V Bias) Input, 12-A Single Synchronous Step-Down SWIFT™ Converter* (SLUSBN5)
5. *TPS53915 1.5 to 18-V (4.5 to 25-V Bias) Input, 12-A Synchronous Step-Down SWIFT™ Converter With PMBus™* (SLUSAS9)
6. *TPS548A20 1.5-V to 20-V (4.5-V to 25-V Bias) Input, 15-A Synchronous Step-Down SWIFT™ Converter* (SLUSC78)
7. *TPS549A20 1.5-V to 20-V (4.5-V to 25-V Bias) Input, 15-A Synchronous Step-Down SWIFT™ Converter With PMBus™* (SLUSC79)
8. *TPS5331x High-Efficiency, 8-A or 14-A, Synchronous Buck Converter with Eco-mode Control* (SLUSAY8) – TPS53318 and TPS53319
9. *TPS53353 High-Efficiency 20-A Synchronous Buck Converter With Eco-mode™* (SLUSAK2)
10. *TPS53355 High-Efficiency 30-A Synchronous Buck Converter With Eco-mode™* (SLUSAE5)
11. *TPS544x25 4.5-V to 18-V, 20-A and 30-A SWIFT™ Synchronous Buck Converters with PMBus™ and Frequency Synchronization* (SLUSC81) – TPS544B25 and TPS544C25
12. *TPS53647 4-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus Interface for ASIC Power and High-Current Point-of-Load* (SLUSC39)
13. *TPS40425 Dual Output, 2-Phase, Stackable PMBus™ Synchronous Buck Driverless Controller with Adaptive Voltage Scaling (AVS) Bus* (SLUSBO6)
14. *TPS40428 Dual Output, 2-Phase, Stackable PMBus™ Synchronous Buck Driverless Controller with Adaptive Voltage Scaling (AVS) Bus* (SLUSBV0)
15. *TPS40422 Dual-Output or Two-Phase Synchronous Buck Controller with PMBus™ Interface* (SLUSAQ4)
16. *TPS40400 3-V to 20-V PMBus Synchronous Buck Controller* (SLUS930)
17. *TPS53819A High-Performance, Eco-mode™, Single Synchronous Step-Down Controller with PMBus™* (SLUSB56)
18. *TPS53219A Wide Input Voltage, Eco-Mode™, Single Synchronous Step-Down Controller* (SLUSAU4)
19. *TPS4030x 3-V to 20-V Input Synchronous Buck Controller* (SLUS964) – TPS40303, TPS40304, and TPS40305
20. *TPS40322 Dual Output or Two-Phase Synchronous Buck Controller* (SLUSAF8)

Inductor on Top – TI Designs

1. Complete PMBus Power System for Enterprise Ethernet Switches Reference Design (PMP10896)
2. High Density 30W DC-DC PMBus Buck Converter with Inductor Mounted Over the Converter to Save Space (PMP10364)
3. High Power Density 12Vin, 100W Synchronous DC/DC Step-Down Buck Converter with Inductor-On-Top (TIDA-00510)
4. TPS53355 12.8W Buck Inductor On Top Design (TIDA-00471)
5. TPS53515 11.8W Buck Inductor On Top Design (TIDA-00595)

9 Questions and Answers

Q. Is package rework possible? Are tools available?

A. Yes, rework is possible, and there are several semi-automatic SMT rework machines and profiles available. However, TI does not guarantee the reliability of reused packages. It is best to discard and replace any package that fails test. Refer to the Component Rework Guideline section of this document for more details.

Q. What size land diameter for these packages should I design on my board?

A. Land size is the key to board-level reliability and Texas Instruments strongly recommends following the design rules included within this summary.

Q. Is a special inspection machine required to X-Ray the IC package leads (optical inspection)?

A. Yes, Nordson Dage X-Plane technology (orbital X-Ray, CT scanner-like) http://www.nordson.com/en/divisions/dage/products/x-ray-inspection-systems/computerized-tomography-option

Q. Is this inductor-on-top solution in high-volume production currently?

A. Yes, by several Tier-1 cloud infrastructure customers.

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?

A. EMI is controlled by minimizing any complex current loops on the PCB trace. Helpful hints include:

- Solid ground and power planes can be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops, increasing radiation.
- Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
- Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other.

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