How to Generate a VCOM Voltage Using a PWM Signal

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ABSTRACT

In an LCD, the backlight shines through the liquid crystal material and the voltage across the liquid crystal controls how much light shines through it. An active matrix LCD (AMLCD) contains many pixels arranged in a grid pattern. The voltage across each pixel is controlled individually so that high resolution images can be created. One terminal of every pixel is connected to a common plane. The voltage on this plane is called the VCOM voltage and it is the reference voltage for each pixel. The VCOM voltage is typically adjusted for best image quality during production and is often generated by a digital-to-analog converter (DAC), such as the LM8342 device, buffered by an amplifier.

A typical VCOM voltage generator has two functions:

- It provides a way to adjust the VCOM voltage
- It buffers the adjusted VCOM voltage

This application note describes how to use a PWM signal to generate the input for a VCOM buffer. Many timing controllers can generate PWM signals which are capable of good performance at low cost.

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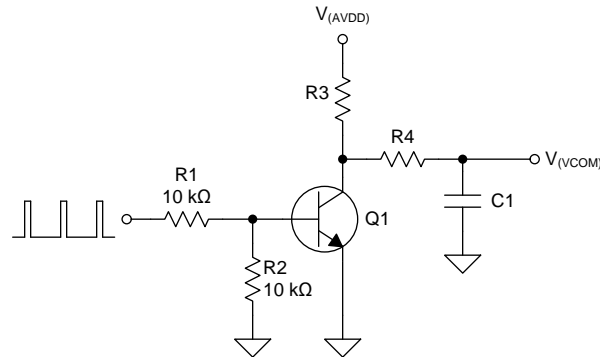# 1   Basic PWM Circuit to Generate the VCOM Voltage

Figure 1. Basic PWM Circuit to Generate the VCOM Voltage

Figure 1 shows a simple circuit that converts the logic-level PWM signal from a microcontroller to an analog VCOM voltage. This circuit is composed essentially of two stages: an amplification stage followed by a low pass filter.

Transistor Q1 amplifies and inverts the input signal. Thus, the output at the collector of Q1 has a duty cycle of 1 – D (where D is the duty cycle of the logic-level input signal) and an amplitude of $V_{(AVDD)}$ volts. The low-pass filter of resistor R4 and capacitor C1 converts the PWM signal at the collector of Q1 to a dc output. If R4 >> R3, high and low signals have an almost equal and opposite effect on the low-pass filter and the output voltage changes almost linearly with duty cycle and is given by Equation 1:

$$V_{(VCOM)} = (1-D)\,V_{(AVDD)}$$

(1)

The collector-emitter saturation voltage ($V_{CE(sat)}$) of transistor Q1 is approximately 100 mV at these current levels, which is small compared with $V_{(AVDD)}$. Because the VCOM voltage of every display is set individually during production, a nonzero collector-emitter saturation voltage does not have an important effect on the circuit performance. During production of the display, if the $V_{CE(sat)}$ of a transistor is different from the nominal value, the operator adjusts the duty cycle of the PWM signal to correct the difference. It is important that $V_{CE(sat)}$ does not change a lot with temperature, because this has an effect on the VCOM voltage. In typical applications, with the components shown, the change of $V_{CE(sat)}$ with temperature is too small to have an important effect.

If the values of R3 and R4 have the same order of magnitude (for example, if the value of R4 is less than ten times the value of R3), then the output voltage changes nonlinearly with duty cycle. For instance if R3 = R4 = 100 kΩ in the circuit of Figure 1, C1 will charge up through 200 kΩ (R3 + R4) when Q1 is off and it will discharge through 100 kΩ (R4) when Q1 is on. This difference in charge and discharge resistance makes the output voltage change nonlinearly with duty cycle:

$$V_{(VCOM)} = \left(\frac{(1-D)(R4)}{D(R3)+R4}\right) V_{(AVDD)}$$

(2)

Inserting R3 = 100 kΩ and R4 = 100 kΩ in Equation 2 gives,

$$V_{(VCOM)} = \left(\frac{1-D}{1+D}\right) V_{(AVDD)}$$

(3)

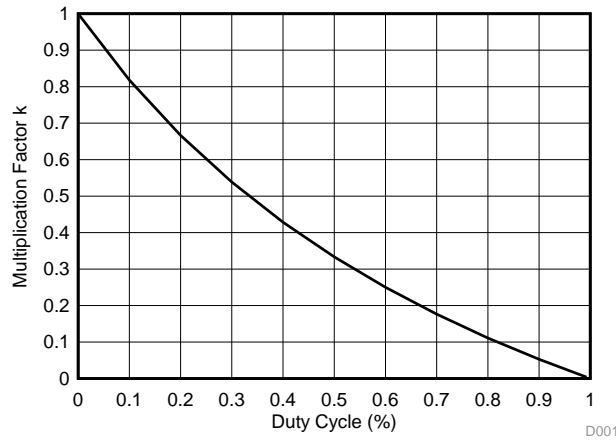Figure 2 shows the nonlinear response of the circuit shown in Figure 1.

Figure 2. VCOM Voltage Characteristic of the Circuit Shown in Figure 1

The VCOM voltage is typically adjusted during the manufacture of the display to get the highest image quality. In most practical applications, a linear relationship between the duty cycle and the VCOM voltage is not necessary.

1.1 Filter Selection

The low-pass filter formed by resistor R4 and capacitor C1 converts the PWM signal at the collector of Q1 to a dc voltage. The cutoff frequency of the low-pass filter sets the output voltage ripple. For example, if a ripple of less than 1 LSB for a resolution of N bits is required, the value of C1 is determined as follows:

- First determine the attenuation needed:

$$a = -20\log\left(\frac{1}{2^N}\right)$$

or $a = 20\log(V_{LSB}/V_{PWM})$
(4)

where

- V_{LSB} is the minimum step size of the PWM signal
- V_{PWM} is the adjustment range of the circuit
(5)

- The cutoff frequency of the low-pass filter is given by Equation 6

$$f_{co} = \frac{f}{\sqrt{\left(10^{\frac{a}{20}}\right)^2 - 1}}$$

where

- f_{co} is the cutoff frequency of a first-order low-pass filter necessary to attenuate sufficiently.
- f is the frequency of the PWM signal
(6)

- Finally, the value of C1 is given by Equation 7

$$f_{CO} = \frac{1}{2\pi(R4)(C1)}$$
(7)

The cutoff frequency of the low-pass filter also sets the rise time of the VCOM voltage during start-up as follows:

$$t_r = (4.6)(R4)(C1)$$

where

- t_r is the VCOM voltage rise time from 0% to 99% of its final value
- R4 is the low-pass filter resistance
- C1 is the low-pass filter capacitance   (8)

Equation 7 and Equation 8 show that a reduction of the rise time of the VCOM voltage will lead to an increase of the voltage ripple amplitude. For this reason, depending on the application, you have to make a tradeoff between the required rise time and the maximum allowed ripple.

2   Modified Circuit With Reduced Adjustment Range

The circuit shown in Figure 1 is sufficient for many applications, but it has the disadvantage that the adjustment range of the VCOM voltage is from 0 V to $V_{(AVDD)}$. In typical display applications, a much smaller adjustment range is used.

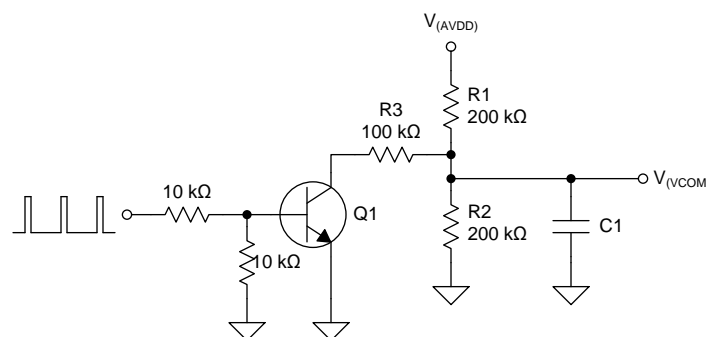Figure 3 shows a circuit that uses an additional resistor to set the adjustment range.

Figure 3. Modified Circuit With Reduced Adjustment Range

The operation of this circuit is best understood with Thévenin equivalent circuits:
- When transistor Q1 is off, capacitor C1 is supplied from an equivalent voltage source of $V_{(AVDD)}/2$ through a resistance of 100 kΩ.
- When transistor Q1 is on, capacitor C1 is supplied from an equivalent voltage source of $V_{(AVDD)}/4$ through an equivalent resistance of 50 kΩ.
- The adjustment range of the VCOM voltage is thus from $V_{(AVDD)}/4$ to $V_{(AVDD)}/2$.

Capacitor C1 makes a low-pass filter with the output resistance of the level shifter. The minimum output resistance of the level shifter is 50 kΩ, and this value must be used to calculate the filter cutoff frequency. Because the output resistance of the level shifter is different when the output is high than when it is low, the VCOM voltage varies nonlinearly, as follows:

$$V_{(VCOM)} = \left(1 + \frac{(1-D)}{(1-D)+D\left(\frac{R1\|R2}{R1\|R2\|R3}\right)}\right)\frac{V_{(AVDD)}}{4}$$

(9)

Inserting R1//R2//R3 = 50 kΩ and R1//R2 = 100 kΩ in Equation 9 gives,

$$V_{(VCOM)} = \frac{1}{2(1+D)} V_{(AVDD)}$$

(10)

Figure 4 shows the nonlinear relationship between the VCOM voltage and the PWM duty cycle of the circuit shown in Figure 3.
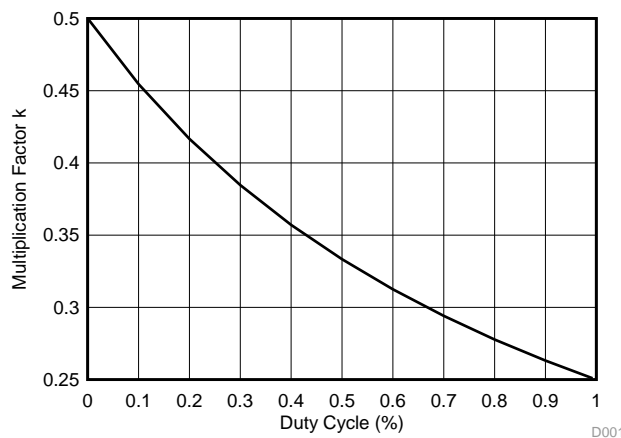

Figure 4. VCOM Voltage Characteristic of the Circuit Shown in Figure 3

The value of capacitor C1 is selected as described in Section 1.1. Because this circuit has an adjustment range of $V_{(AVDD)}/4$ (four times smaller than in the circuit of Figure 1), the output voltage ripple is four times smaller.

2.1 Improvement of Transistor Switching Time

Because of the propagation delay, which occurs during normal switching operation of the transistor, the duty cycle of the input signal differs a little from the duty cycle of the PWM at the collector of Q1. This is observed in Figure 5 where an 100-kHz PWM signal with a duty cycle of 0.35 gives an output with a duty cycle of approximately 0.5.
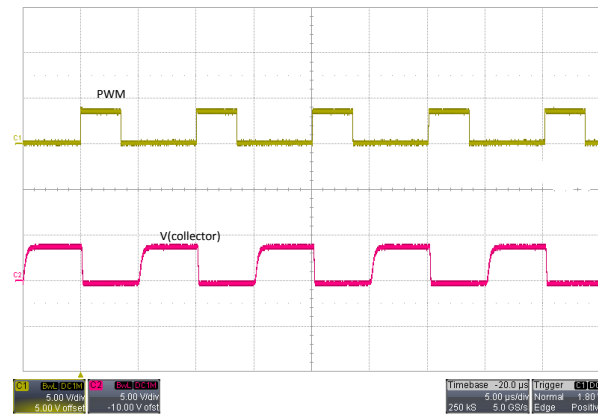
Figure 5. Propagation Delay (50 kHz)

If you use a lower PWM frequency, the delay becomes negligible compared to the period of the PWM signal and the resulting error is very small. For example in Figure 5, the delay is approximately 1.5 µs, which represents an increase of the duty cycle of 15% when the frequency of the PWM is 100 kHz and only 1.5% when it is lowered to 10 kHz (see Figure 6). This solution is simple and does not require additional components. Because of the reduction of the frequency, a bigger filter is necessary to meet the same output voltage ripple requirement.
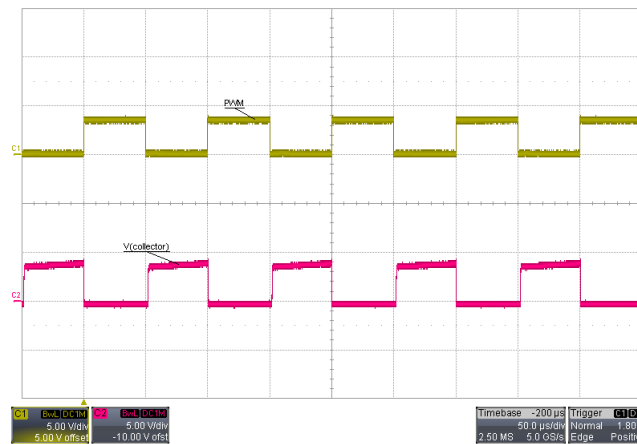
Figure 6. Propagation Delay (10 kHz)

If it is not possible to change the frequency of the PWM signal, another solution is to add a capacitor across the base resistor and a Schottky diode between the base and collector of transistor Q1 (see Figure 7). The capacitor speeds up the removal of charge stored on the base of the transistor and the diode prevents the transistor saturating, thus reducing the overall delay (see Figure 9).
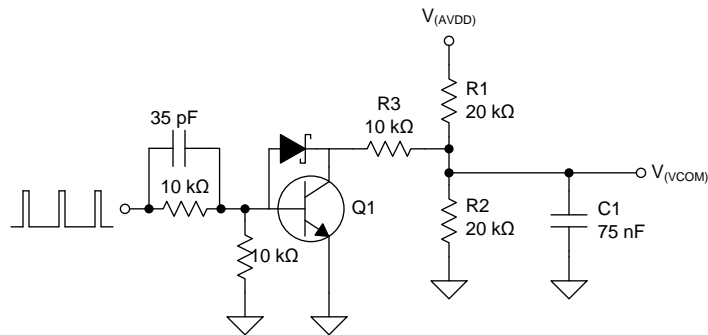
2.2 Application Example

Figure 7. Application Example

In this section the performance of the circuit in Figure 7 is evaluated. The PWM signal frequency is set to 100 kHz and this gives a resolution of approximately 8 bits, that is a minimum step size of 12.5 mV. To achieve a ripple of less than 1 LSB (47-dB attenuation), a 75-nF capacitor is necessary with the minimum output resistance of 5 kΩ. Thus the VCOM voltage takes 1.7 ms to reach 99% of its final value with 0.4% accuracy. This is observed in Figure 8 and Figure 9, which show the fall time and the ripple of the VCOM voltage.

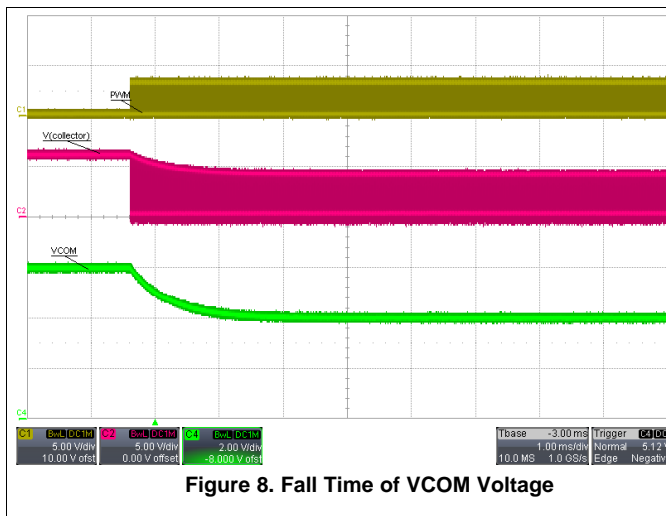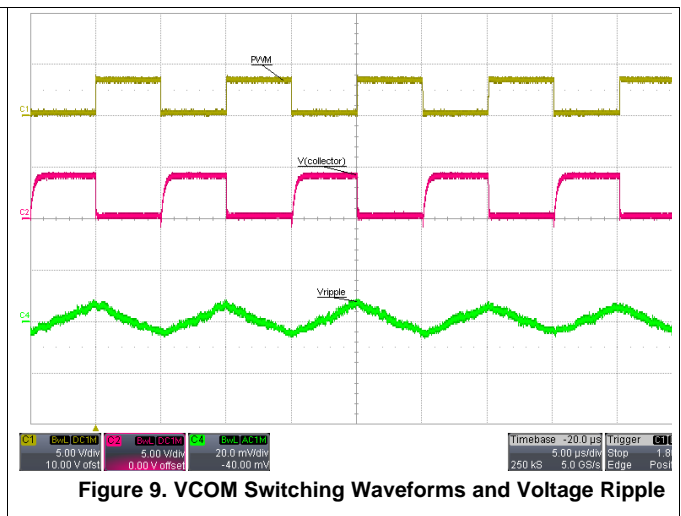**Figure 8. Fall Time of VCOM Voltage**

Figure 9. VCOM Switching Waveforms and Voltage Ripple

Figure 10 shows that a temperature variation lead to a variation of ±0.15% of the VCOM voltage. The considered temperature range is larger than what we would expect on an actual application, which means that the actual variation of the VCOM voltage would be lower than what is shown in Figure 10.
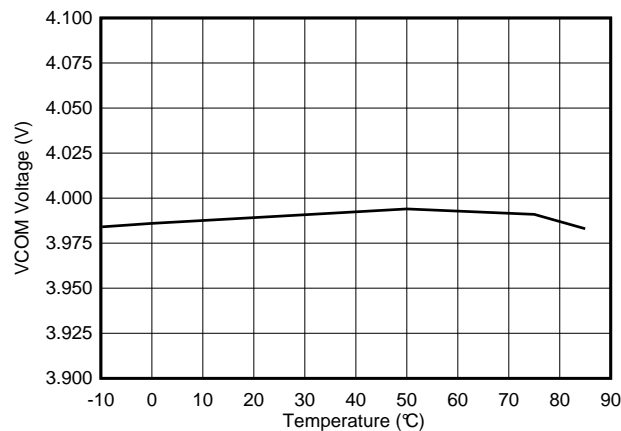
Figure 10. VCOM Voltage Variation over Temperature

3 Using an Operational Amplifier to Generate the VCOM Voltage From a PWM Signal

If your application uses an operational amplifier (that is, not a unity-gain buffer) to generate $V_{(VCOM)}$, you can use the operational amplifier to scale and filter the input PWM signal. The circuit shown in Figure 11 converts a 50-kHz, 3.3-V PWM signal to a dc level in the range 2.5 V to 5 V. Compared to the previous examples, this circuit is more linear, changes less over temperature, and can be used at higher frequencies.
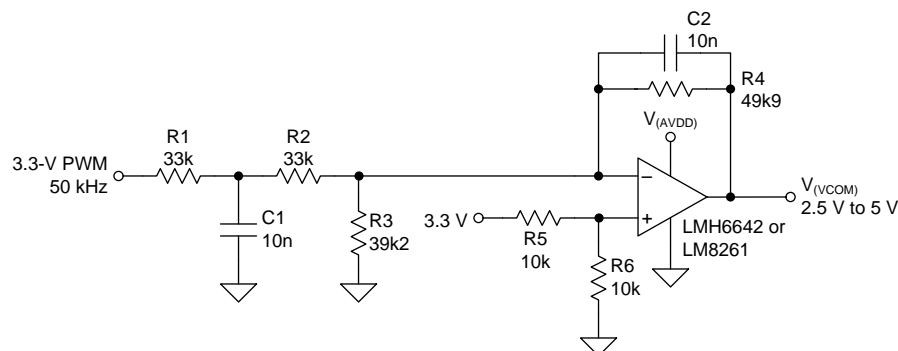
Figure 11. Using an Op-Amp to Generate $V_{(VCOM)}$ Directly

The output voltage of the circuit in Figure 11 is given by Equation 11

$$V_{(VCOM)} = 3.3 \left(\left(\frac{R6}{R5 + R6} \right) \left(1 + \frac{R4}{R3} + \frac{R4}{R1+R2} \right) - D \left(\frac{R4}{R1 + R2} \right) \right)$$

(11)

If the tolerance of the 3.3-V supply is too high, use one of the level shifter solutions shown in Figure 12 to convert the 3.3-V PWM signal to a more steady supply voltage (typically $V_{(AVDD)}$ or $V_{(AVDD+)}$).
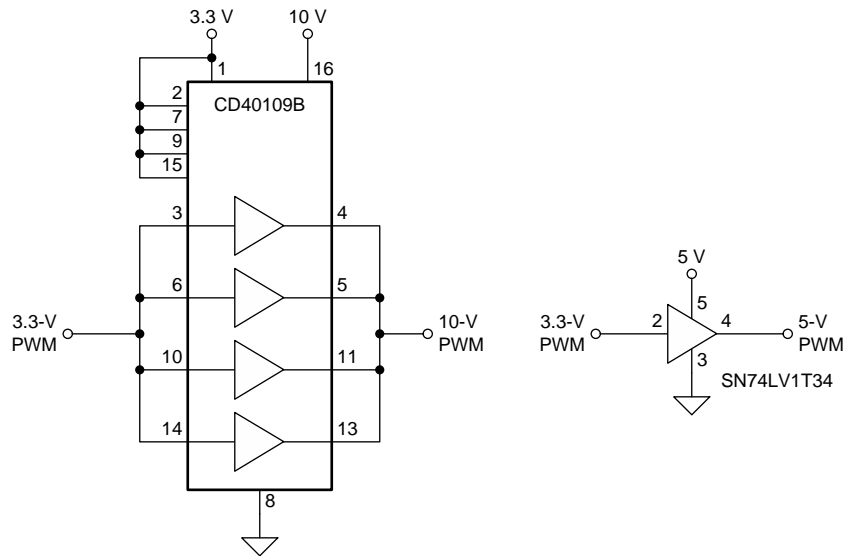
Figure 12. High-Speed Level Shifter Devices

4 VCOM Adjustment Circuit for Bipolar Displays

Figure 13 shows how to generate the VCOM voltage in displays that use $\pm V_{(AVDD)}$ supplies. Unlike the circuits in Figure 1 and Figure 3, where the VCOM voltage decreases as the duty cycle of the PWM signal increases, the VCOM voltage increases as the duty cycle increases with this circuit. The accuracy of this solution also depends on the tolerance of the V_{CC} supply, which must not be too high. With the values shown in Figure 13, the VCOM voltage adjustment range is $-V_{(AVDD)}/2$ to 0 V.
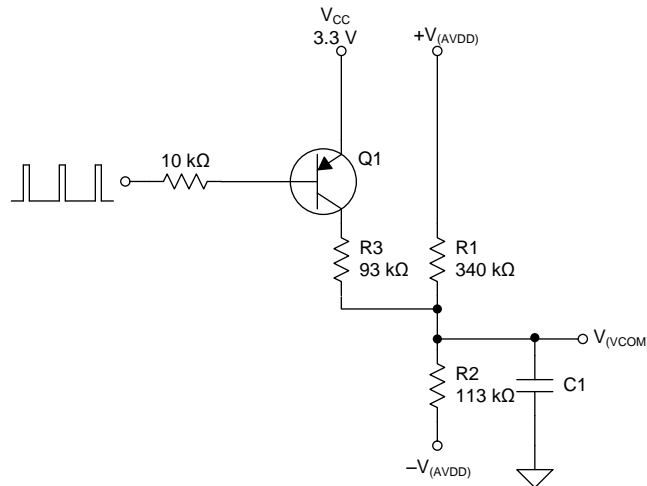

Figure 13. VCOM Adjustment Circuit for Bipolar Displays

The VCOM voltage changes with PWM duty cycle as follows:

$$V_{(VCOM)} = \frac{(R2-R1)(R3)+(1-D)(R1)(R2)\left(\dfrac{V_{CC}}{V_{(AVDD)}}\right)}{(1-D)(R1)(R2)+(R1+R2)(R3)}V_{(AVDD)}$$

(12)

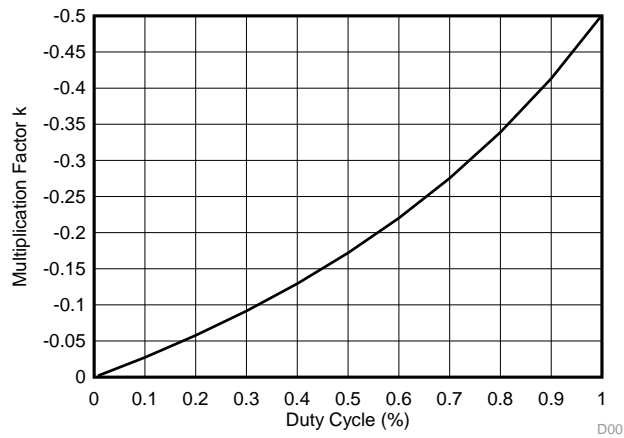Figure 14 shows how the VCOM voltage changes with the PWM duty cycle.

Figure 14. VCOM Voltage Characteristic of Circuit Shown in Figure 13

The cutoff frequency of the low-pass filter is calculated as described in Section 1.1

The circuit in Figure 15 shows how to drive an operational amplifier directly from the PWM signal. As in Figure 11, the accuracy of the $V_{(VCOM)}$ voltage depends on the tolerance of the 3.3-V supply. In most cases, the variation of this supply will be too small to have an effect on image quality, but if the tolerance is too high, you can use one of the level shifter solutions shown in Figure 12 to convert the 3.3-V PWM signal to a more regulated voltage (typically $V_{(AVDD)}$ or $+V_{(AVDD)}$).
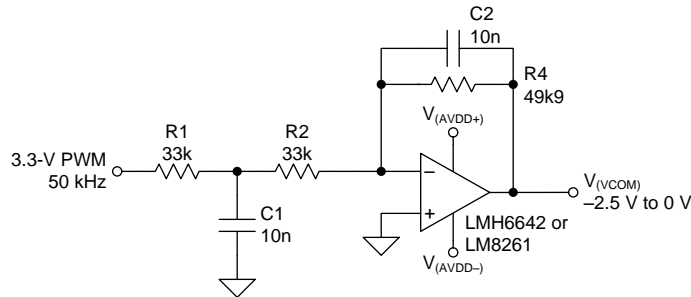
Figure 15. Using an Op-Amp to Generate $V_{(VCOM)}$ Directly

The output voltage of the circuit in Figure 15 is given by Equation 13:

$$V_{(VCOM)} = 3.3 \left(D \frac{R4}{R1 + R2} \right)$$

(13)

5   A Note About Component Selection

The capacitance of a ceramic capacitor changes not only with tolerance and temperature, but also with dc voltage. The change in capacitance with voltage is called the *dc bias effect*, and you must think about it when selecting a capacitor for the low-pass filter.

The circuits described in this application note use 2N3904 and 2N3906 transistors because they are commonly available. The same circuit performance is expected with equivalent transistors. Note that devices are available that include a transistor and two resistors in one package. These devices reduce the component count and minimize the PCB area of the circuit. The FJV4102R and FJV3102R devices from Fairchild Semiconductor are examples of such devices but equivalent devices from other manufacturers are also available.

6   Conclusion

In this application note, different circuits to generate the input of a VCOM buffer with a PWM signal are presented. These circuits are composed of an amplification stage followed by a low-pass filter. The switching delays during the normal operation of the transistor cause a difference between the duty cycle of the PWM signal and the input signal of the filter. To minimize these delays:

*   Reduce the PWM frequency such that the delay is negligible compared to the period of the PWM signal
*   Add a capacitor across the base resistor and a Schottky diode between the base and collector of the transistor

When you choose the low-pass filter components you must decide on the right balance between rise time and output voltage ripple. A lower rise time means higher ripple and vice versa.

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