Application Report
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Optimizing the TPS62097 Output Filter

Pál Bőle

Low Power DC-DC Applications

ABSTRACT

The TPS62097 uses iDCS-Control, which combines the advantages of voltage-mode, current-mode and hysteretic control. This control loop takes information about input and output voltage changes and feeds it directly to a fast comparator stage, providing an immediate response to dynamic load changes. Use of this control topology allows for a wide range of inductor and output capacitor values to accomplish specific design goals. The designer is able to optimize many factors such as control loop stability, transient response, or output voltage ripple, based on the needs of the application. This application report discusses how to adjust the output filter for the TPS62097 in order to meet the requirements of a specific design.

1 Analyzing the Stability of the Design

The TPS62097 datasheet (SLVSCD6) recommends inductance and capacitance ranges which support the majority of designs. If for some specific application requirement these ranges must be exceeded, tradeoffs must be made and the designer should consider many factors when choosing an inductor and output capacitor combination. For example, lower inductances save board space because they can be physically smaller due to fewer windings. However, this causes the peak switch current and output voltage ripple to increase. On the other side, output voltage ripple is lowered by using higher output capacitance, if the design can tolerate the larger size and slower transient response.

The inductor and output capacitor values are also a key influence on stability. Regardless of what goals need to be met through optimizing the output filter, the design has to be stable. The LC filter forms a double pole in the control loop, which has a strong impact on the frequency response and system stability. Equation 1 calculates the corner frequency of the LC filter:

$$f_C = \frac{1}{2\pi\sqrt{LC_{out}}} \qquad (1)$$

The closed-loop crossover frequency of the control loop determines how fast the device responds to changes on the input and output. The control loop responds faster to load or line changes with higher crossover frequencies. The crossover frequency moves lower with lower corner frequencies and vice versa. If the corner frequency is too high, the crossover frequency also moves too high (too close to the switching frequency) and instability results. Additional output capacitance solves this by moving the corner frequency lower.

Table 1 shows the stability of different LC combinations that have been tested in the laboratory with the TPS62097 running in forced PWM mode at the lowest frequency setting, 1.5 MHz. All stability measurements were taken at V_{IN} = 5 V, V_{OUT} = 1.8 V and I_{OUT} = 2 A. The measured crossover frequency of every LC combination is shown. To calculate the corner frequency, use the nominal inductor value and the nominal capacitor value de-rated by 50% to account for DC bias. Capacitors rated for 4 V were used.

Table 1. TPS62097 Stability and Crossover Frequency

Nominal Inductor Value	Nominal Ceramic Capacitor Value (Effective = 1/2 Nominal)					
	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
	Measured Crossover Frequency					
0.47 µH	~~396 kHz~~	310 kHz	164 kHz	145 kHz	95 kHz	52 kHz
1.0 µH	352 kHz	189 kHz	112 kHz	91 kHz	58 kHz	34 kHz
2.2 µH	191 kHz	126 kHz	65 kHz	51 kHz	30 kHz	~~18 kHz~~
4.7 µH	132 kHz	75 kHz	41 kHz	33 kHz	~~20 kHz~~	~~13 kHz~~

(white)	Recommended by the TPS62097 datasheet
(green)	Stable
(yellow)	Unstable, not recommended

Table 1 shows the filter combination recommended by the datasheet colored in white. Additional combinations that are stable are colored in green. Yellow-colored and strikethrough cells indicate combinations which are not recommended.

For more information on control-loop measurement procedures, see the application report How to Measure the Control Loop of DCS-Control™ Devices (SLVA465). A 1-Ω signal injection resistor is recommended for the TPS62097. For more information on determining the stability from the load-step response and Bode plot measurements, see the application report Simplifying Stability Checks (SLVA381).

Using these application reports, the LC filter combinations in Table 1 are determined to be stable. They have at least 60 degrees of phase before and at the crossover frequency, and they do not reach current limit during a heavy load transient.

The required effective inductance is stated as 500 nH minimum in the data sheet. Otherwise, the current ripple might be too high in forced PWM mode and light loads. If a 0.47-µH inductor is desired, Auto Power Save Mode must be used. As well, the maximum output current may be reduced below 2 A due to the higher ripple current.

2 Optimizing Load Transient Response

The load transient response can be optimized for a lower voltage drop or for a faster response. When the load current quickly increases, the output capacitor supplies the load with energy until the regulator reacts to the change and increases its output current. A larger output capacitor provides this current with a smaller amount of output voltage drop. However, a larger capacitor decreases the bandwidth of the system and provides slower response. Figure 1 shows the TPS62097 transient response to a 0 to 2 A load step using a (a) single 22-µF and (b) two 22-µF output capacitors with a 1-µH inductor at 1.2-V output and 5.0-V input voltage. The response (b) with the two 22-µF capacitors has approximately half the voltage overshoot at turn-off. The undershoot at turn-on is similar to the one with the single capacitor.

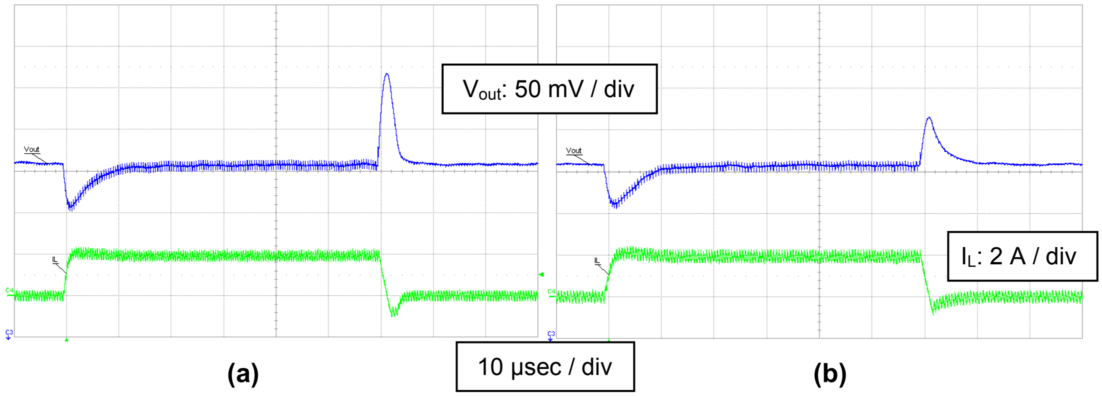

Figure 1. TPS62097 Load Transient Response Using a (a) 22-µF and (b) 2 x 22-µF Output Capacitor

Figure 2 shows the TPS62097 closed-loop frequency response at a 2-A load and 1.2-V output. Both plots show a stable system. Phase is colored blue (-180° to 180°) and magnitude is colored magenta (−40 dB to 40 dB). A yellow vertical bar is placed at the crossover frequency and shows the phase margin.

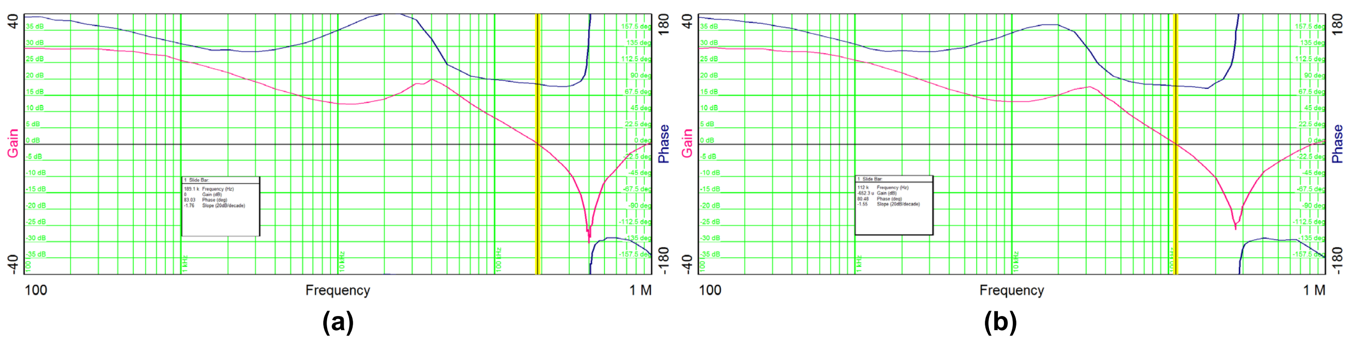

Figure 2. TPS62097 Closed-Loop Frequency Response Using a (a) 22-µF and (b) 2 x 22-µF Output Capacitor

3 Reducing Output Voltage Ripple

Output voltage ripple can pose a problem to processors that have tight voltage tolerances and systems that are sensitive to power supply noise. Worst-case ripple occurs in power save mode when the load is at its lightest.

The dominating cause of power dissipation at light loads is the switching losses in the power stage. To maximize efficiency, switching in power save mode occurs only if the output voltage falls to a certain level. In this operating mode, each switching cycle deliberately transfers too much energy to the output, such that the output voltage rises above its setpoint. This allows the device to enter a standby state between the switching pulses with minimal power consumption. Power save mode keeps efficiency high at these light loads, but it also increases the output voltage ripple.

Increasing either the output capacitance or inductance reduces the ripple in power save mode. Figure 3 shows the output voltage ripple for a 5-V input and 1.2-V output system at 2-mA load with a (a) single 22-µF output capacitor and (b) two 22-µF output capacitors. The extra output capacitor reduces the ripple from 10.3 mV to 5.3 mV as shown in Figure 3.

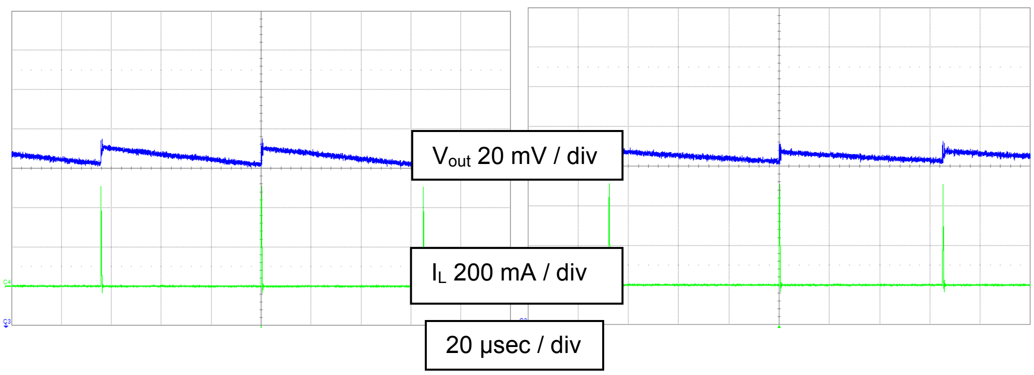

Figure 3. TPS62097 Output Voltage Ripple Using a (a) 22-µF and (b) 2 x 22-µF Output Capacitor

If the output capacitor has a high DC bias effect, its effective capacitance can drop up to 50% or more. Different size capacitors have different DC bias effects and different parasitic properties.

The same technique of increasing the inductance and output capacitance also reduces the ripple in PWM mode. The ripple in PWM mode is usually lower than in power save mode.

4 Conclusion

This application report has presented methods to analyze control loop stability, optimize transient response, and minimize output voltage ripple for the TPS62097 device. The methods presented in this application report and in the references show that a wider variety of external components can be used to achieve the desired power supply performance when the default output filter is not sufficient for the application. Using components outside of the standard circuit has benefits and tradeoffs across all measures of performance, such as stability, transient response, output ripple, power save mode performance, efficiency, and so on. This application report discusses these tradeoffs and aids with the design of a TPS62097-based power supply.

References

1. *How to Measure the Control Loop of DCS-Control™ Devices* (SLVA465)
2. *Simplifying Stability Checks* (SLVA381).
3. *TPS62097, 2A High Efficiency Step Down Converter with iDCS-Control™, Forced PWM Mode and Selectable Switching Frequency* (SLVSCD6)
4. *DCS-Control™* Landing Page: http://www.ti.com/dcs-control

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