Application Report
SLVA708–September 2017

LNB Design Considerations on TPS65233 and TPS65235

Junjie Mai

ABSTRACT

The TPS65233 and TPS65235 are designed for analog and digital satellite receivers. They are monolithic voltage regulator with I^2C interface. This application report mainly introduces some design considerations in application which including soft start design consideration, I^2C address and tone mode setup, DisEqc2.x tone design consideration and surge protection design consideration.

Contents

1 Introduction 3
2 Soft Start Design Consideration 3
3 I^2C Address and Tone Mode Setup 10
4 DisEqc2.x Tone Design Consideration 12
5 Surge Protection Design Consideration 15
6 Summary 17
7 References 17

List of Figures

1 Startup with 13.4-V VLNB Output 4
2 Startup with 18.2-V VLNB Output 4
3 Startup with 13.4-V VLNB and Hiccup Triggered 5
4 Startup with 13.4-V VLNB and non Hiccup Triggered 5
5 Startup with 18.2-V VLNB and Hiccup Triggered 6
6 Startup with 18.2-V VLNB and non Hiccup Triggered 6
7 Startup with 13.4-V VLNB and Hiccup Triggered 7
8 Startup with 13.4-V VLNB and non Hiccup Triggered 7
9 Startup with 18.2-V VLNB Output 7
10 Startup with 13.4-V VLNB Output 8
11 Startup with 18.6-V VLNB Output 8
12 Startup with 18.6-V VLNB Output 8
13 Startup with 18.6-V VLNB Output 8
14 Voltage Transition for TPS65233 9
15 Voltage Transition for TPS65235 9
16 I^2C access when EN is “Low" 10
17 I^2C access when EN is “High" 10
18 Mode 5 with EXTM Stop at “Low” 11
19 Mode 5 with EXTM Stop at “High 11
20 44-KHz Tone Output 12
21 Application for DiSEqc2.x Support on TPS65235 13
22 GDR = 18.8 V for Transmit Data “0”, GDR = 13.4 V for Tone Receive 13
23 GDR = 18.8 V for Transmit Data “1”, GDR = 13.4 V for Tone Receive 13
24 Transmit Data “0” 13
25 Transmit Data “1” 13

26 GDR Output Controlled by TONE_TRANS Bit From “0” to “1” 13
27 GDR Output Controlled by TONE_TRANS Bit From “1” to “0” 13
28 Block for Surge Protection Design 15
29 TONE Output with D4 Added without R1 16
30 TONE Output with D4 and R1 Added 16
31 TONE Output with D4 and R1 Added 16
32 TONE Output with D4 and R1 Added 16

List of Tables

1 Tone Mode Setup for TPS65233 11
2 TPS65235 Tone Mode 12
3 22-KHz Tone Receive Mode Selection 12
4 TI LNB Regulators 17

Trademarks

1 Introduction

TPS65233 and TPS65235 are LNB (Low Noise Block) voltage regulators for digital and analog satellite receivers. It offers a complete solution with low component count, low power dissipation, together with simple design and I^2C standard interface.

2 Soft Start Design Consideration

2.1 Soft Start

Usually LNB regulator needs to support different types of LNB, some LNBs have smaller capacitive load, some have larger capacitive load up to serval hundreds of micro farad.

With this higher capacitive load on VLNB output, the startup current is higher and reachs the current limit set for the devices, this triggers the hiccup timer. If this over current situation keeps longer than hiccup ON time (8 ms maximum for TPS65235 and 4 ms for TPS65233), the device is in hiccup state which means off and startup again, this is not expected in application.

Equation 1 can be used to do the estimation for startup current.

$$I_{startup}\ (mA) = \frac{C_{load}\ (uF) \times V_{VLNB}(V)}{T_{ss}(ms)}$$

where

- $I_{startup}$ → Startup current
- T_{SS} → Soft start time
- V_{VLNB} → VLNB output voltage when startup
- C_{load} →Capacitive load on VLNB output

(1)

In TPS65233 or TPS65235 design, an external capacitor is added on TCAP pin to implement the soft start time control, Equation 2 is used to do the estimation for soft start time.

$$T_{ss}(ms) = \frac{C_{ss}\ (nF) \times V_{VLNB}(V)}{I_{ss}(uA)\ \times K}$$

where

- I_{SS} → Internal charging current for TCAP pin, about 10 µA
- C_{SS} → External capacitor on TCAP pin
- K → Internal ratio, 10 for TPS65233, 6 for TPS65235

(2)

Combine Equation 1 and Equation 2, Equation 3 to provide a startup current estimation.

$$I_{startup}\ (mA) = \frac{C_{load}\ (uF) \times I_{ss}(uA) \times K}{C_{ss}(nF)}$$

(3)

Based on this equation, for TPS65233 or TPS65235, since the I_{SS} and K is fixed, given C_{load} (capacitive load on VLNB output), the conclusions are as follows:

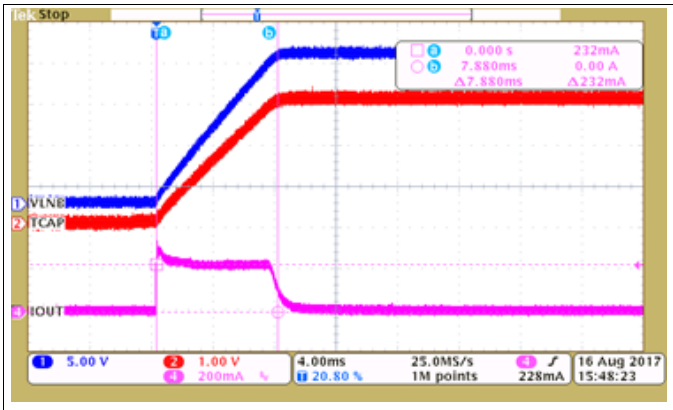
- The startup current is not related to VLNB startup voltage.
- The larger C_{SS} (capacitor on TCAP pin), the smaller startup current.

For TPS65233 and TPS65235, the I_{SS} is nearly same about 10 µA, while for K, it is different. For TPS6233, the K is 10, and for TPS65235, the K is 6.

2.2 TPS65235 Soft Start Test Result

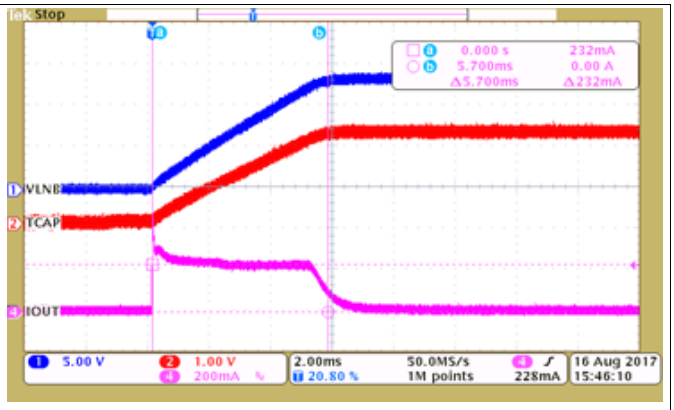
2.2.1 Normal Startup

The startup current for TPS65235 is in Figure 1 and Figure 2. With 100 µF ±20% capacitive load on VLNB output, the C_{SS} is 22 nF. Based on Equation 3, the startup current is not related to VLNB startup voltage, either with 13.4-V VLNB output or 18.2-V VLNB output, the startup current is same with 232 mA.



C_{SS} = 22 nF C_{load} = 100 µF

Figure 1. Startup with 13.4-V VLNB Output



C_{SS} = 22 nF C_{load} = 100 µF

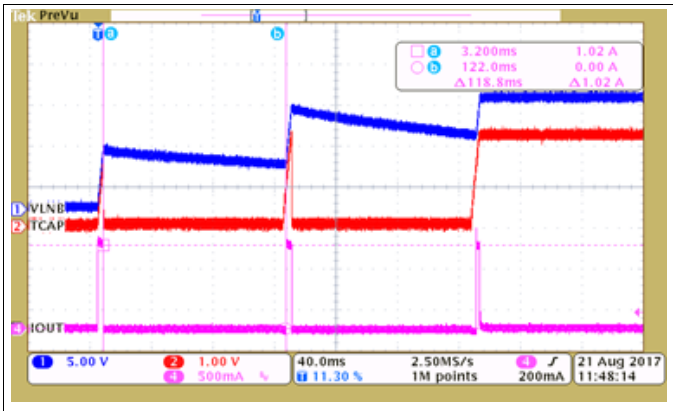
Figure 2. Startup with 18.2-V VLNB Output

2.2.2 Startup with Different HICCUP_ON Time

Keep the same C_{SS} with 22 nF, enlarge the capacitive load on VLNB output to 560 µF ±20%. With 13.4-V VLNB output startup, the waveform is in Figure 3.

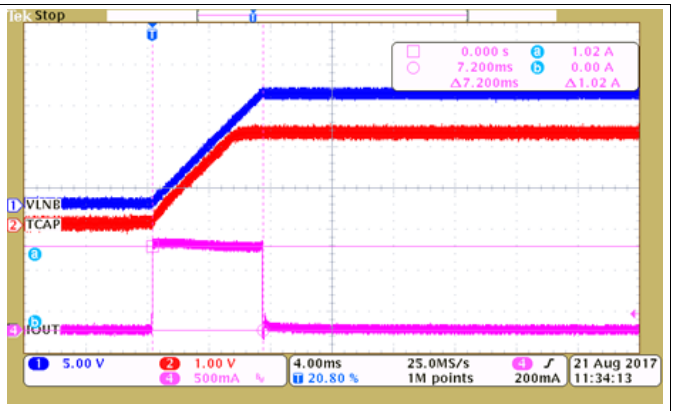
Based on the Equation 3, the startup current is 1.4 A, it is larger than the OCL setting 1 A in TPS65235. Triggering the OCL leads the hiccup timer starts to count and limits the VLNB output charging the capacitive load with 1 A current only.

For TPS65235, the hiccup ON/OFF time is about 4 ms / 128 ms and 8 ms / 256 ms selectable by I^2C register. As default, it is 4 ms / 128 ms setting.



C_{SS} = 22 nF C_{load} = 560 µF Hiccup_ON = 4ms

Figure 3. Startup with 13.4-V VLNB and Hiccup Triggered



C_{SS} = 22 nF C_{load} = 560 µF Hiccup_ON = 8ms

Figure 4. Startup with 13.4-V VLNB and non Hiccup Triggered

With 1-A charging on 560 µF C_{load}. It takes about 7.2 ms for 13.4-V VLNB output to startup, which is less than hiccup ON time 8 ms, the startup can be finished without hiccup trigger in Figure 4.

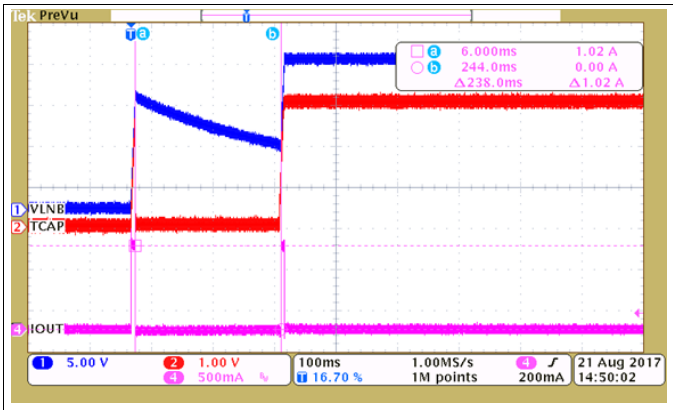
Due to the current is limited to be 1 A for charging the capacitive load on VLNB, the VLNB output voltage ramping is lower than TCAP voltage ramping in Figure 4.

Setting the hiccup ON/OFF time to be 8 ms / 256 ms, it can be implemented by pull EN to low when power up, then control the VLNB output through the I^2C register. For the detail, refer to 7.3.10 in SLVSD80.

2.2.3 Startup with Different C_{SS} on TCAP Pin

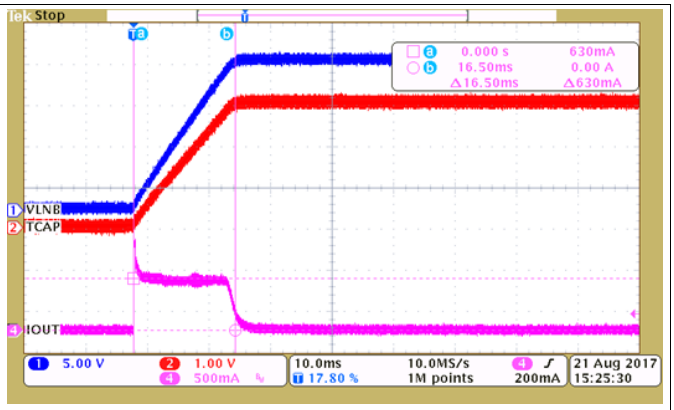
With same setting, when startup with 18.2-V VLNB output voltage, OCL 1-A charging on about 560-µF capacitive load, It takes about 10 ms for 18.2-V VLNB output startup. Which means even put the hiccup ON time to be 8 ms, it still cannot startup without hiccup trigger in Figure 5.

Based on Equation 3, the C_{SS} on TCAP pin should be enlarged to make sure the startup current to be less than OCL value. Replace C_{SS} with 47-nF capacitor, and the startup waveform is in Figure 6. The startup current is 630 mA, since the OCL is not triggered, the hiccup timer is not started, and the startup waveform is not related to the hiccup ON time.



C_{SS} = 22 nF C_{load} = 560 µF Hiccup_ON = 8 ms

Figure 5. Startup with 18.2-V VLNB and Hiccup Triggered

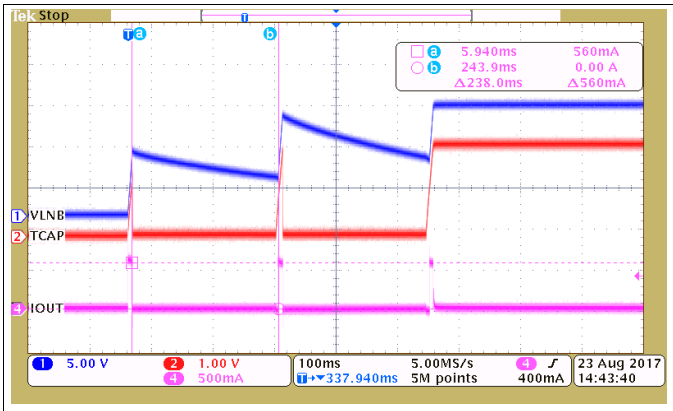


C_{SS} = 22 nF C_{load} = 560 µF Hiccup_ON = 4 or 8 ms

Figure 6. Startup with 18.2-V VLNB and non Hiccup Triggered

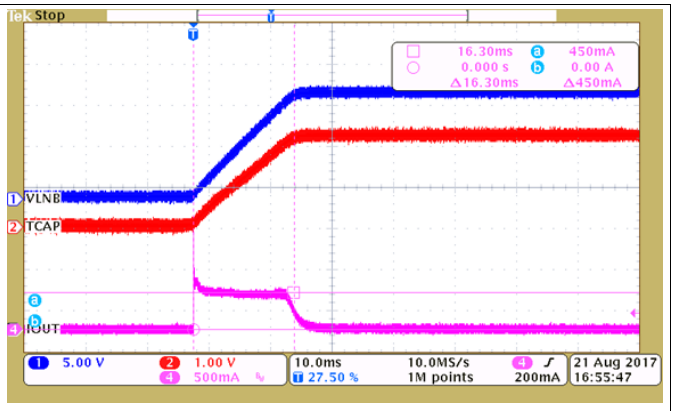
2.2.4 Startup with Different OCL Setting

With same setting, and the OCL lowered from 1 A to 560 mA with a 630 mA startup current, the over current and hiccup timer are triggered. Figure 7 shows a hiccup when started up with 13.4-V VLNB output and OCL 560 mA setting. To fix this, the 68 nF C_{SS} is used for to get a lower startup current of 450 mA in Figure 8 and Figure 9.



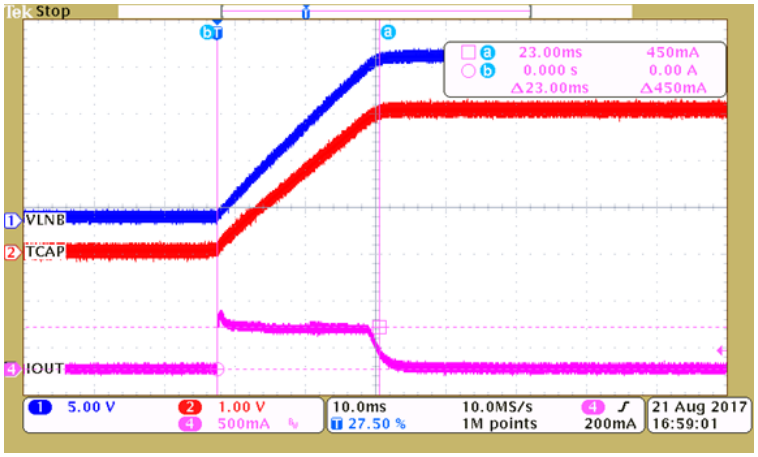
C_{SS} = 47 nF C_{load} = 560 µF OCL = 560 mA
Hiccup_ON = 8 ms

Figure 7. Startup with 13.4-V VLNB and Hiccup Triggered



C_{SS} = 68 nF C_{load} = 560 µF OCL = 560 mA
Hiccup_ON = 4 or 8 ms

Figure 8. Startup with 13.4-V VLNB and non Hiccup Triggered

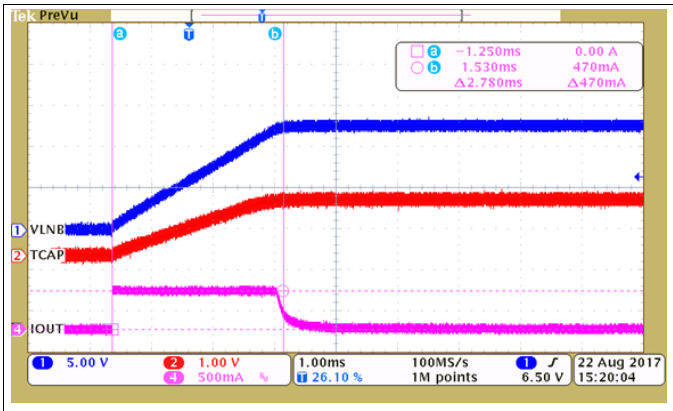


C_{SS} = 68 nF C_{load} = 560 µF OCL = 560 mA
Hiccup_ON = 4 or 8 ms

Figure 9. Startup with 18.2-V VLNB Output

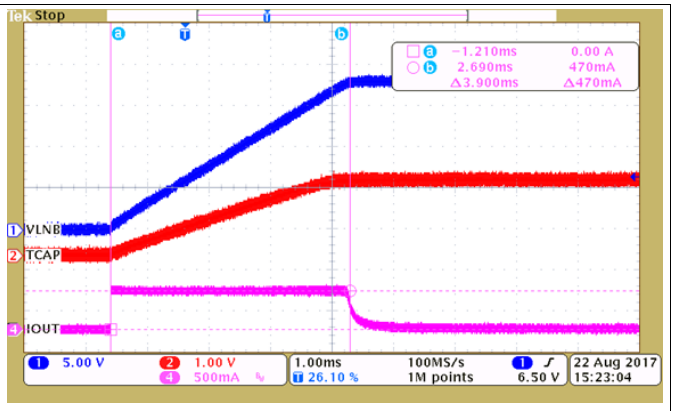
2.3 TPS65233 Soft Start Test Results

The startup current for TPS65233 is in Figure 10 and Figure 11, with 100 µF ±20% capacitive load on VLNB output, the C_{SS} is 22 nF. Either with 13.4-V VLNB output or 18.6-V VLNB output, the startup current is same with 470 mA. Based on the Equation 3, the K in the TPS65233 is 10 which is larger than TPS65235, with the same setting, the startup current is larger than TPS65235.



C_{SS} = 22 nF C_{load} = 100 µF OCL = 670 mA

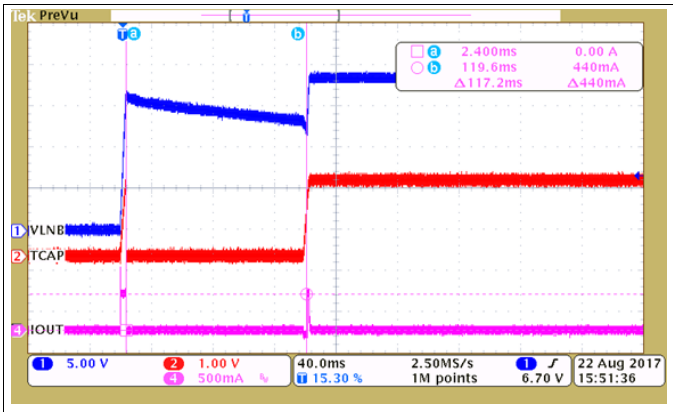
Figure 10. Startup with 13.4-V VLNB Output



C_{SS} = 22 nF C_{load} = 100 µF OCL = 670 mA

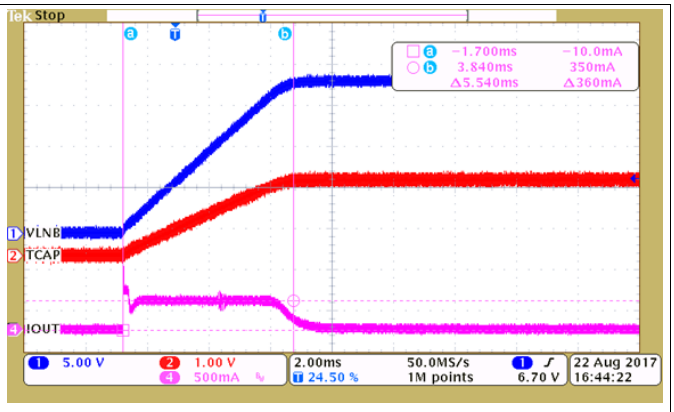
Figure 11. Startup with 18.6-V VLNB Output

For TPS65233, all the behaviors are same with the TPS65235, while the hiccup ON time is fixed about 4 ms. To support lower OCL setting or higher capacitive load on VLNB output, if hiccup happens when startup, the larger TCAP capacitor C_{SS} should be used to decrease the startup current lower than OCL value.



C_{SS} = 22 nF C_{load} = 100 µF OCL = 440 mA

Figure 12. Startup with 18.6-V VLNB Output



C_{SS} = 33 nF C_{load} = 100 µF OCL = 440 mA

Figure 13. Startup with 18.6-V VLNB Output

2.4 VLNB Output Voltage Transition

To support the vertical polarization and horizontal polarization control for LNB, the voltage transition frequently happens in the application.

Larger C_{SS} on the TCAP pin can avoid the hiccup happens when startup, while the VLNB output voltage transition time is also enlarged, Equation 4 can be used for estimation.

$$T_{ts}(ms) = \frac{Abs(V_{VLNB1}(V) - V_{VLNB2}(V))}{K} \times \frac{C_{ss}(nF)}{I_{ss}(uA)} \quad (4)$$

where

- T_{ts} → Transition time between V_{VLNB1} and V_{VLNB2}
- For TPS65233, from 13.4 V to 18.6 V transition, the transition time is about 1.1 ms with 22 nF C_{SS}.
- For TPS65235, from 13.4 V to 18.2 V transition, the transition time is about 2 ms with 22 nF C_{SS}.

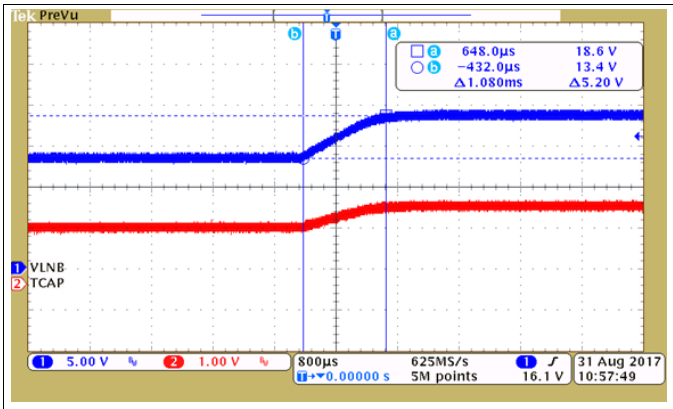


Figure 14. Voltage Transition for TPS65233

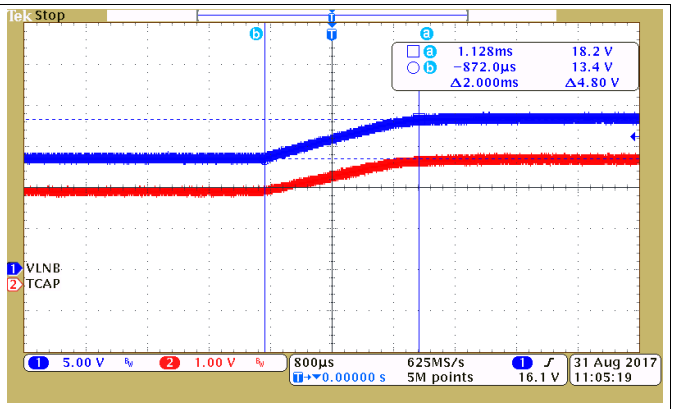


Figure 15. Voltage Transition for TPS65235

3 I²C Address and Tone Mode Setup

3.1 I²C Address Setup

The TPS65233 has two I²C address, which is 0x60H and 0x61H.

If 0x60H is used, the EN pin should be always pulled low and the VLNB output is controlled by I²C bit 3 in control register 1. Which means before the I²C configuration done, there is no VLNB output as the default bit 7 in control register 1 is “0” to disable the I²C control.

If 0x61H is used, the EN pin should always be pulled high, and the VLNB output is not controlled by I²C bit 3 in control register 1 when powered up. The VLNB output is enabled once VIN power up and the initial VLNB output voltage may not be what the application needs. So the VCTRL pin should be set to make sure the VLNB output voltage is expected by application

If two TPS65233 are used with I²C interface in one application, one EN pin should be always kept low and the other should be always kept high for correct I²C access.

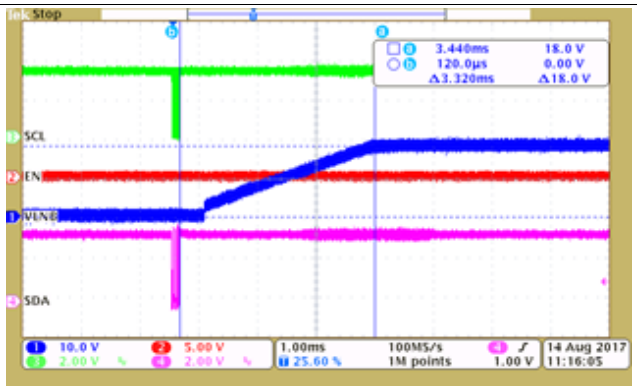


Figure 16. I²C access when EN is “Low"

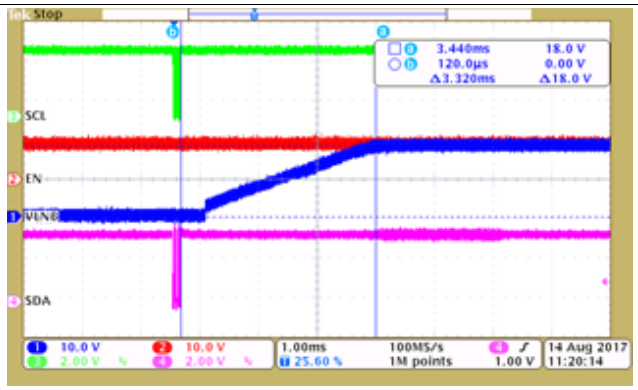


Figure 17. I²C access when EN is “High"

For TPS65235 I²C address setup, refer to SLVSD80.

3.2 Tone Mode Setup

3.2.1 TPS65233 Tone Mode Setup

There are totally 5 kinds of tone control mode in TPS65233, two modes are for non-I²C application mode 1 and mode 2, three modes are for I²C application mode 3, mode 4 and mode 5.

Table 1. Tone Mode Setup for TPS65233

Mode	Control Register 1					Note For EXTM Pin
	bit 7 (I2C_CON)	bit 6 (RSV)	bit 5 (TGATE)	bit 4 (TMODE)	bit3 (EN)	
Mode 1	0	0	0	0	1	22 kHz clock in burst mode
Mode 2	0	0	0	0	1	High or low DC voltage
Mode 3	1	0	X	0	1	Must have continuous 22 KHz on EXTM
Mode 4	1	0	X	1	1	No effect, can be grounded
Mode 5	1	0	1	0	1	22 kHz clock in burst mode, when no 22 KHz, must be kept as “High”

NOTE: For mode 3 and mode 4, bit5 = 1 tone on; bit5 = 0 tone off

For mode 5, as the note in Table 1, when the tone stops, the EXTM signal should be kept “High”, then the bit3 and bit4 in control register 2 can be used to control the tone level of the VLNB output. Otherwise, if it is kept as “Low”, bit3 and bit4 in control register 2 are useless, the tone level is always above the DC output in Figure 18 , and this is usually not expected in this design. In Figure 19, EXTM stops the tone and stays in “High”, the tone level can be set in the middle of VLNB output.

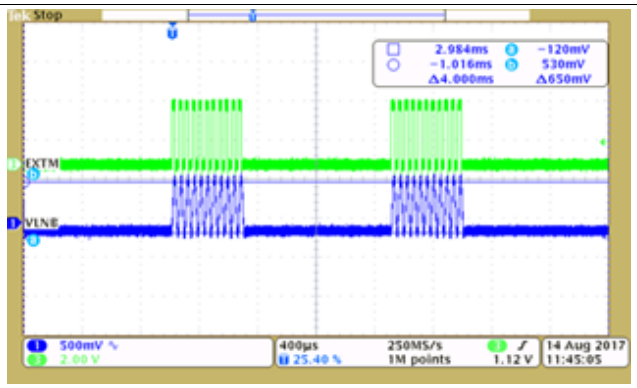


Figure 18. Mode 5 with EXTM Stop at “Low”

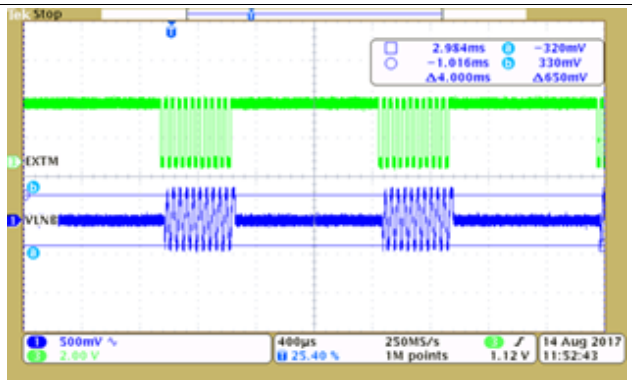


Figure 19. Mode 5 with EXTM Stop at “High

If the application cannot put the EXTM stops at “High”, then use TPS65235.

For other tone mode introduction, refer to the TPS65233-1 datasheet SLVSD66 for detail clarification.

3.2.2 TPS65235 44-KHz Tone Mode Setup

The TPS65235 also supports the 44-KHz tone output. Compared with 22-KHz tone output mode, the 44-KHz tone output only has an external tone mode. To support the 44-KHz external tone mode, the bit0 (EXTM TONE) in control register 1 should be “1”.

Table 2. TPS65235 Tone Mode

Output Tone Frequency	External Tone Mode	Internal Tone Mode	EXTM TONE
22 KHz	√	√	"0"
44 KHz	√	×	"1"

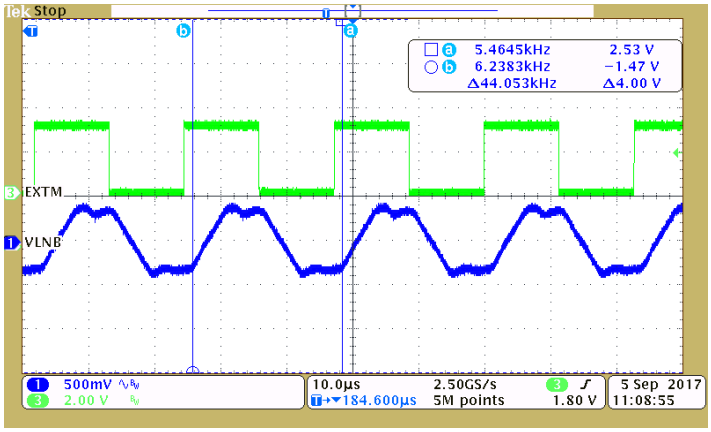


Figure 20. 44-KHz Tone Output

4 DisEqc2.x Tone Design Consideration

The TPS65235 supports DisEqc2.x tone signal detection. There are two I^2C bits in Control Register 2 TONE_AUTO and TONE_TRANS for tone detection mode selection. When the tone transmits from the TPS65235, the Bypass FET should be turn on and pass the tone signal output. When receiving the tone signal from satellite, the Bypass FET should be turn off for DisEqC 2.x tone receiving. Turning on or off the Bypass FET is controlled by the GDR pin from the TPS65235.

Table 3. 22-KHz Tone Receive Mode Selection

TONE_AUTO	TONE_TRANS	Bypass FET
0	0	OFF
0	1	ON
1	X	Auto Detect

When TONE_AUTO is set to “0”, the MCU software should control the TONE_TRANS bit through I^2C interface. For example, when it needs to send the tone output, the MCU software puts the TONE_TRANS to be “1”; otherwise, the MCU software keeps TONE_TRANS as “0” for receiving the tone from satellite.

When TONE_AUTO is set to “1”, the TPS65235 does the same thing as MCU software. When the EXTM is high or has the 22-KHz tone input, which means TPS65235 outputs the 22-KHz tone, then TPS65235 controls the GDR output with VCP voltage value (higher than VLNB output about 5.4-V) to close the external Bypass FET for tone transmit. Otherwise, the TPS65235 controls the GDR output with VLNB voltage value to open the Bypass FET for tone receiving from satellite.

Figure 21 shows the DisEqc 2.x application for TPS65235. The RC Network is for tone detection input, and the recommended value should be followed.

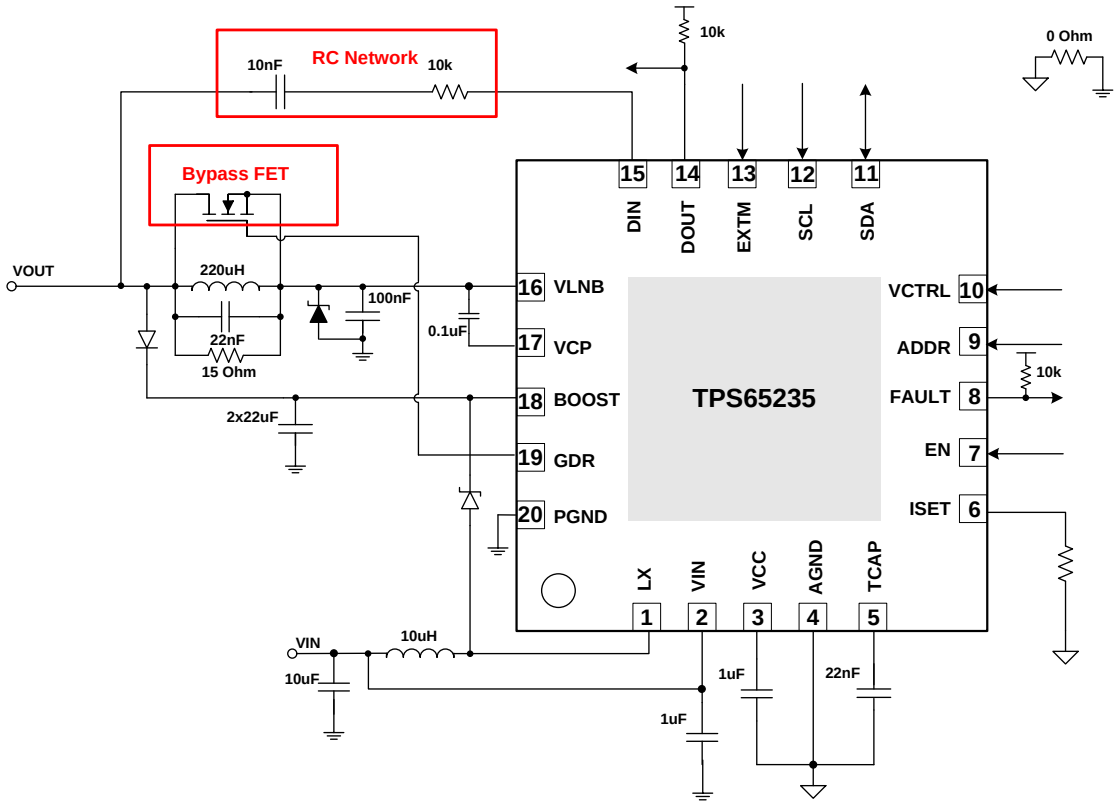
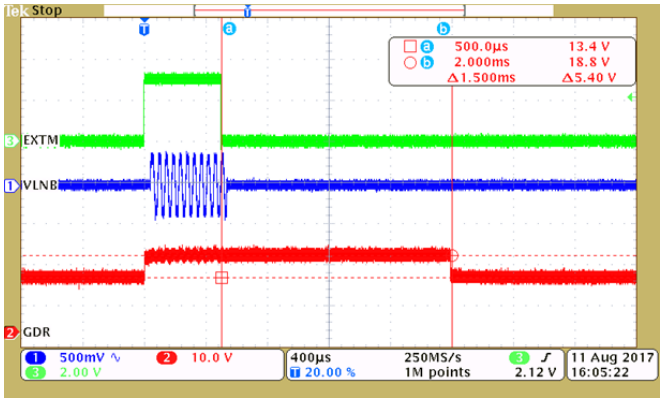
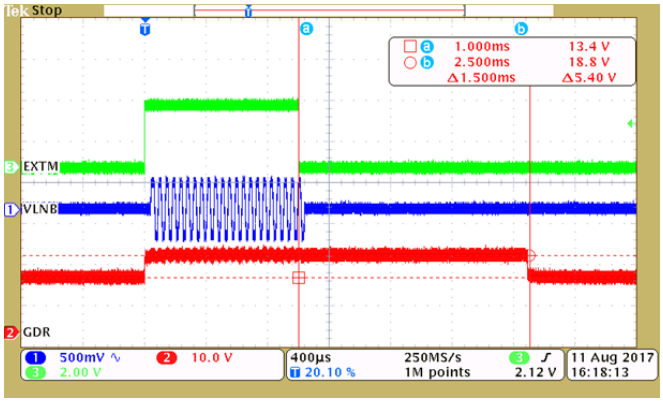


Figure 21. Application for DiSEqc2.x Support on TPS65235



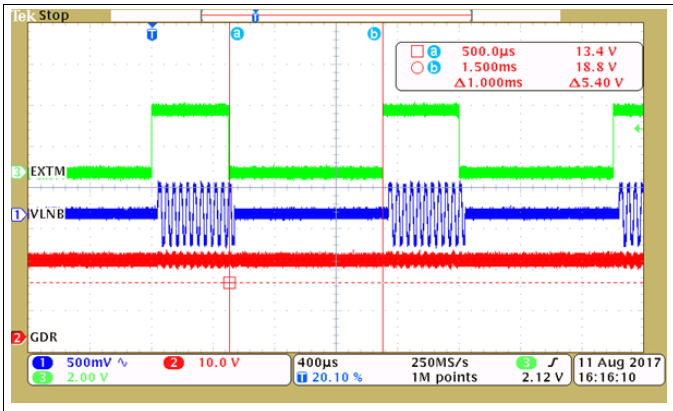
V_{VLNB} = 13.4 V TONE_AUTO = 1

Figure 22. GDR = 18.8 V for Transmit Data "0", GDR = 13.4 V for Tone Receive



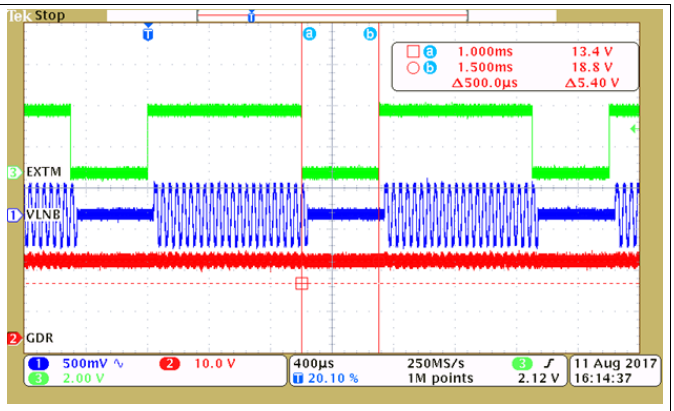
V_{VLNB} = 13.4 V TONE_AUTO = 1

Figure 23. GDR = 18.8 V for Transmit Data "1", GDR = 13.4 V for Tone Receive



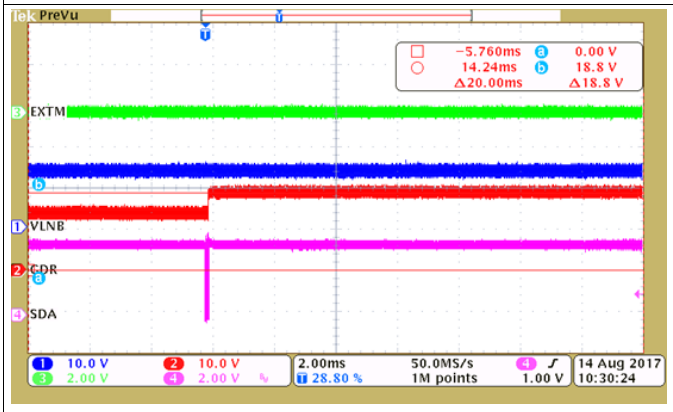
V_{VLNB} = 13.4 V TONE_AUTO = 1

Figure 24. Transmit Data “0”



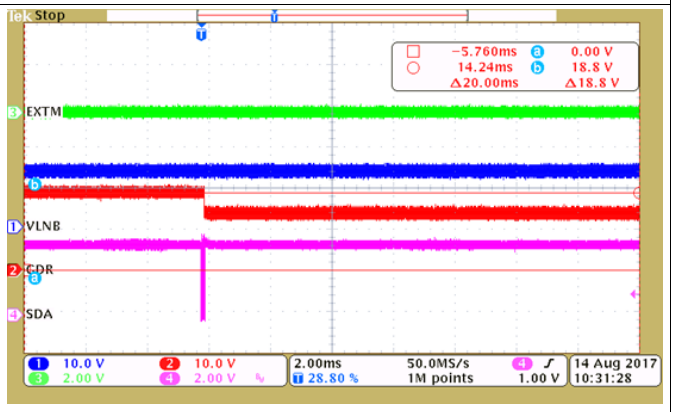
V_{VLNB} = 13.4 V TONE_AUTO = 1

Figure 25. Transmit Data “1”



V_{VLNB} = 13.4 V TONE_AUTO = 0

Figure 26. GDR Output Controlled by TONE_TRANS Bit From “0” to “1”



V_{VLNB} = 13.4 V TONE_AUTO = 0

Figure 27. GDR Output Controlled by TONE_TRANS Bit From “1” to “0”

As the default status of TONE_AUTO is “0”, the TPS65235 cannot implement the tone detection function in non-I^2C working condition.

To be noted, the TPS65235 does not do anything related to DisEqC protocol.

For TPS65233, it also can support the DisEqC2.x application by adding the external circuit for tone receiving detection and to control Bypass FET. This application report does not clarify the detail due to it is more related to the customer design.

5 Surge Protection Design Consideration

For surge design consideration, except D0 and D2, usually a schottky diode is serialized in the path of VLNB output, refer to D4 in Figure 28. This external schottky diode D4 is to block the surge current into the device, and the external dummy load R1 is to provide the discharge path for C1 to make sure the correct tone output.

Without the D4, the C1 discharge through internal M1 to implement the tone falling edge. With D4 added, the new discharge path will be C1 to R1.The value of C1 and R1 will influence the falling edge of the tone output.

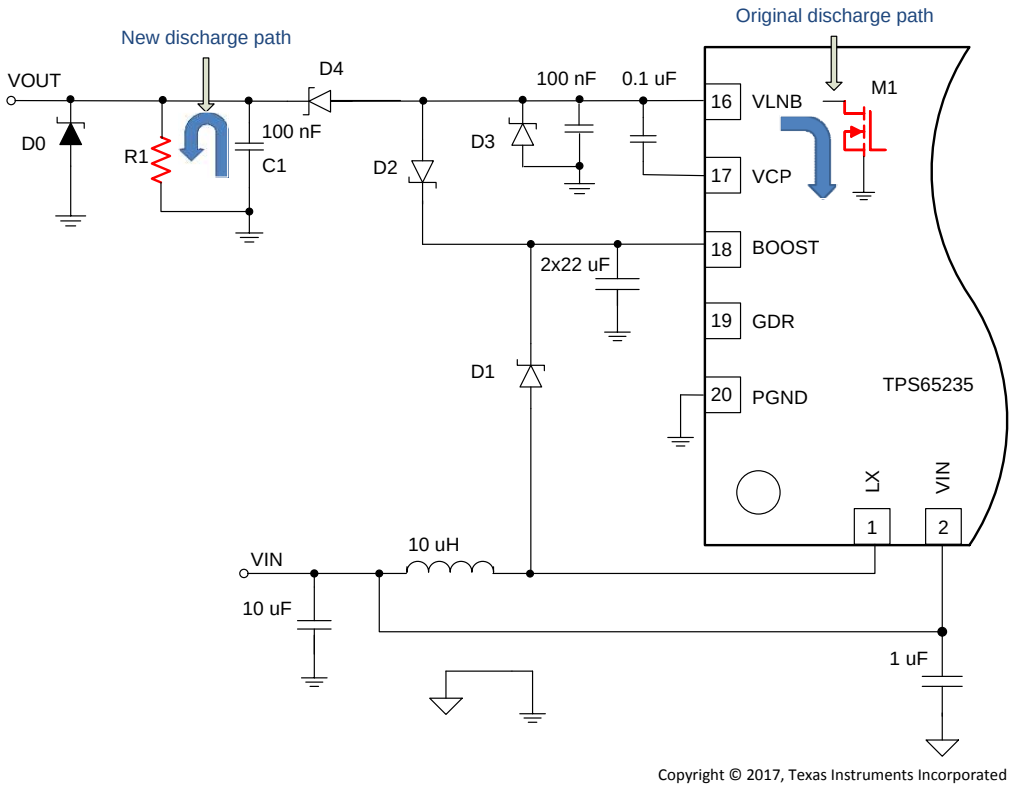
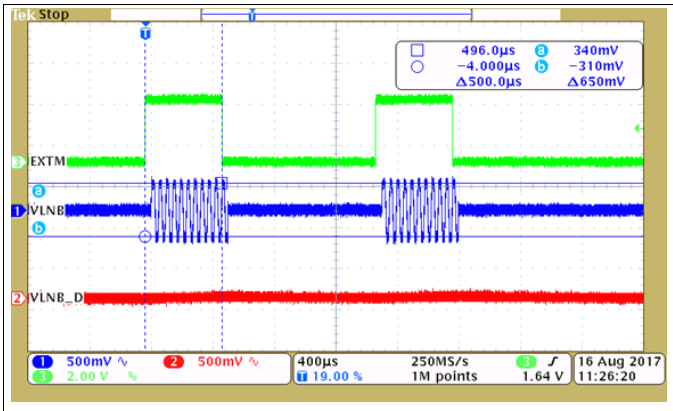
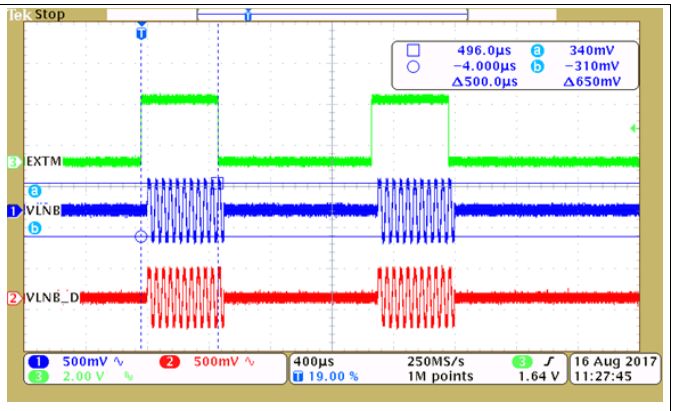


Figure 28. Block for Surge Protection Design



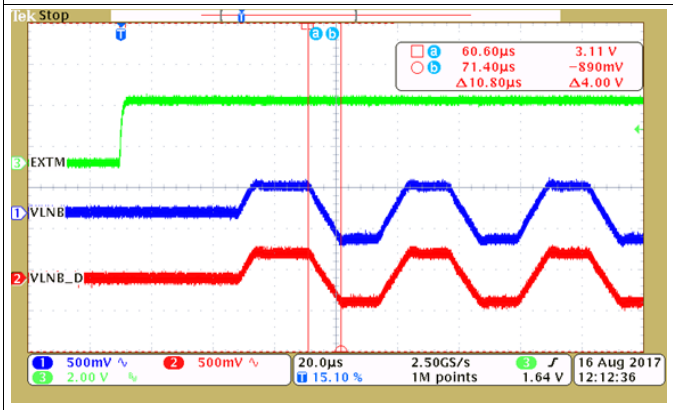
C1 = 100 nF R1 = NA

Figure 29. TONE Output with D4 Added without R1



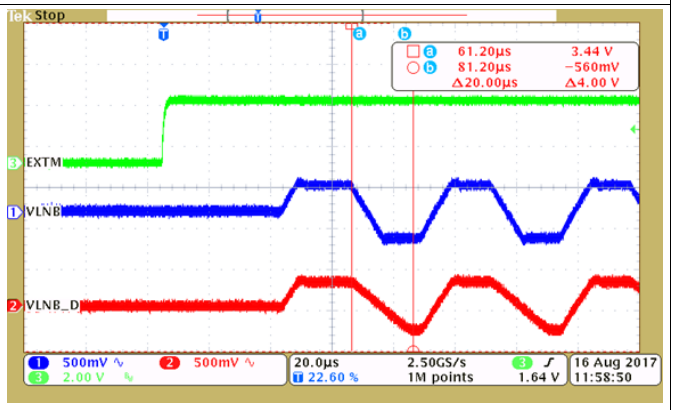
C1 = 100 nF R1 = 1.5 K

Figure 30. TONE Output with D4 and R1 Added



C1 = 100 nF R1 = 1.5 K

Figure 31. TONE Output with D4 and R1 Added



C1 = 100 nF R1 = 5 K

Figure 32. TONE Output with D4 and R1 Added

The smaller R1, the more power loss, but the larger R1 cannot provide enough discharge current for C1 to discharge in time, to meet the tone spec requirement for falling edge. To choose the suitable R1, use Equation 5.

$$R1(k\Omega) < \frac{V_{VLNB\_min}\,(V) \times T_{tone\_falling}\ \ (us)}{C1(nF) \times T_{tone\_amp}\,(V)}$$

where

- V_{VLNB_min} → Minimum VLNB DC output in application
- $T_{tone\_falling}$ → Tone falling edge requirement, about 10 µs
- T_{tone_amp} → Tone amplitude in application, 650 mV for TPS65233, 650 mV / 750 mV for TPS65235 (5)

6 Summary

This application report introduces some design considerations on the TPS65233 and TPS65235. TI has more LNB regulator products. The TPS65233-1 has higher switching frequency up to 1-MHz compared with TPS65233. The TPS65235-1 has the anti-audible noise feature. The TPS65235-2 is based on TPS65235-1 which has the highest VLNB voltage output up to 20.3-V typical.

Table 4. TI LNB Regulators

Features / Part Number	TPS65233	TPS65233-1	TPS65235	TPS65235-1	TPS65235-2
Switching frequency	500 KHz	1 MHz	500 KHz / 1 MHz	500 KHz / 1 MHz	500 KHz / 1 MHz
22-KHz tone output support?	Y	Y	Y	Y	Y
44-KHz tone output support?	N	N	Y	Y	Y
Tone detection for DisEqC2.x?	N	N	Y	Y	Y
Tone amplitude 650 mV /750 mV selectable?	N	N	Y	Y	Y
Anti-audible noise feature?	N	N	N	Y	Y
VLNB output range	13 V - 19.8 V	13 V - 19.8 V	11 V - 20 V	11 V - 20 V	11 V - 20 V

7 References

- Datasheet: *TPS65233 LNB Voltage Regulator With I²C Interface, SLVSC22*
- Datasheet: *TPS65233-1 LNB Voltage Regulator With I²C Interface, SLVSD66*
- Datasheet: *TPS65235 LNB Voltage Regulator With I²C Interface, SLVSD80*
- Datasheet: *TPS65235-1 LNB Voltage Regulator With I²C Interface, SLVSDP1*
- User Guide: *TPS65233 EVM User's Guide , SLVU941*
- User Guide: *Evaluation Module for the TPS65235 LNB Voltage Regulator With I²C Interface for DiSEqC2.x Application, SLVUAO1*

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265